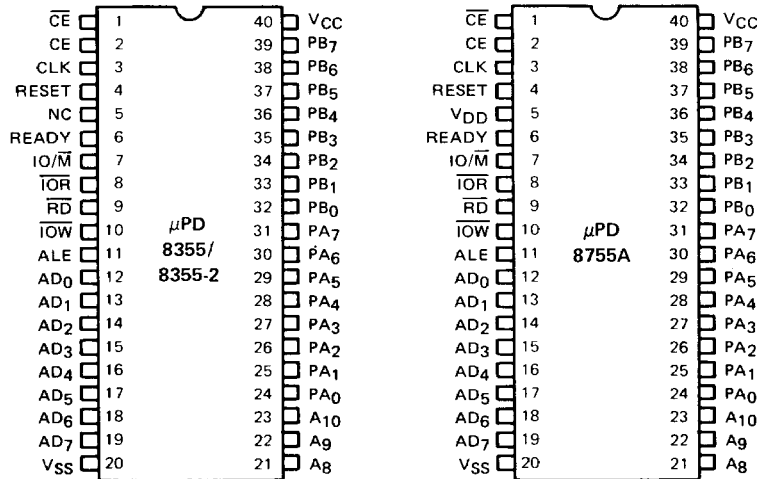


**16,384-BIT ROM WITH I/O PORTS**  
**\*16,384-BIT EPROM WITH I/O PORTS**

**DESCRIPTION** The μPD8355 and the μPD8755A are μPD8085A Family components. The μPD8355 contains 2048 x 8 bits of mask ROM and the μPD8755A contains 2048 x 8 bits of mask EPROM for program development. Both components also contain two general purpose 8-bit I/O ports. They are housed in 40 pin packages, are designed to directly interface to the μPD8085A, and are pin-for-pin compatible with each other.

- FEATURES**
- 2048 X 8 Bits Mask ROM (μPD8355 and μPD8355-2)
  - 2048 X 8 Bits Mask EPROM (μPD8755A)
  - 2 Programmable I/O Ports
  - Single Power Supplies: +5V
  - Directly Interfaces to the μPD8085A
  - Pin for Pin Compatible
  - μPD8755A: UV Erasable and Electrically Programmable
  - μPD8335 and μPD8355-2 Available in Plastic Package
  - μPD8755A Available in Ceramic Package

**PIN CONFIGURATIONS**

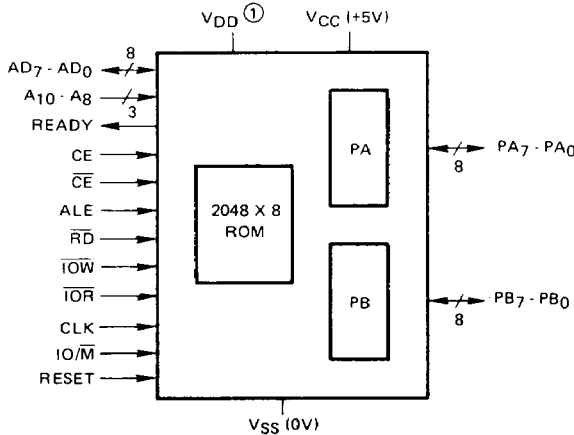


www.DataSheet4U.com NC: Not Connected

# μPD8355/8755A

The μPD8355 and μPD8755A contain 16,384 bits of mask ROM and EPROM respectively, organized as 2048 X 8. The 2048 word memory location may be selected anywhere within the 64K memory space by using the upper 5 bits of address from the μPD8085A as a chip select.

The two general purpose I/O ports may be programmed input or output at any time. Upon power up, they will be reset to the input mode.



Note: ① V<sub>DD</sub> applies to μPD8755A only.

Operating Temperature (μPD8355)	0°C to +70°C
(μPD8755A)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin (μPD8355)	-0.5 to +7V ①
(μPD8755A)	-0.5 to +7V ①
Power Dissipation	1.5W

Note: ① With Respect to Ground

T<sub>a</sub> = 25°C

\*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T<sub>a</sub> = 0°C to +70°C; V<sub>CC</sub> = 5V ± 5%

PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input Low Voltage	V <sub>IL</sub>	-0.5	0.8	V	V <sub>CC</sub> = 5.0V ①
Input High Voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> +0.5	V	V <sub>CC</sub> = 5.0V ①
Output Low Voltage	V <sub>OL</sub>		0.45	V	I <sub>OL</sub> = 2 mA
Output High Voltage	V <sub>OH</sub>	2.4		V	I <sub>OH</sub> = -400 μA
Input Leakage	I <sub>IL</sub>		10	μA	V <sub>IN</sub> = V <sub>CC</sub> to 0V
Output Leakage Current	I <sub>LO</sub>		±10	μA	0.45V < V <sub>OUT</sub> < V <sub>CC</sub>
V <sub>CC</sub> Supply Current	I <sub>CC</sub>		180/125	mA	μPD8355/8355-2

Note: ① These conditions apply to μPD8355/μPD8355-2 only.

## FUNCTIONAL DESCRIPTION

## BLOCK DIAGRAM

## ABSOLUTE MAXIMUM RATINGS\*

## DC CHARACTERISTICS

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1,2	$\overline{CE}$ , CE	Chip Enables	Enable Chip activity for memory or I/O
3	CLK	Clock Input	Used to Synchronize Ready
4	Reset	Reset Input	Resets PA and PB to all inputs
5 ①	NC	Not Connected	
5 ②	V <sub>DD</sub>	Programming Voltage	Used as a programming voltage, tied to +5V normally
6	Ready	Ready Output	A tri-state output which is active during data direction register loading
7	I/O $\overline{M}$	I/O or Memory Indicator	An input signal which is used to indicate I/O or memory activity
8	IOR	I/O Read	I/O Read Strobe In
9	$\overline{RD}$	Memory Read	Memory Read Strobe In
10	$\overline{IOW}$	I/O Write	I/O Write Strobe In
11	ALE	Address Low Enable	Indicates information on Address/Data lines is valid
12-19	AD <sub>0</sub> -AD <sub>7</sub>	Low Address/Data Bus	Multiplexed Low Address and Data Bus
20	V <sub>SS</sub>	Ground	Ground Reference
21-23	A <sub>8</sub> -A <sub>10</sub>	High Address	High Address inputs for ROM reading
24-31	PA <sub>0</sub> -PA <sub>7</sub>	Port A	General Purpose I/O Port
32-39	PB <sub>0</sub> -PB <sub>7</sub>	Port B	General Purpose I/O Port
40	V <sub>CC</sub>	5V Input	Power Supply

Notes: ① μPD8355  
 ② μPD8755A

I/O PORTS

I/O port activity is controlled by performing I/O reads and writes to selected I/O port numbers. Any activity to and from the μPD8355 requires the chip enables to be active. This can be accomplished with no external decoding for multiple devices by utilizing the upper address lines for chip selects. ① Port activity is controlled by the following I/O addresses:

AD <sub>1</sub>	AD <sub>0</sub>	PORT SELECTED	FUNCTION
0	0	A	Read or Write PA
0	1	B	Read or Write PB
1	0	A	Write PA Data Direction
1	1	B	Write PB Data Direction

Since the data direction registers for PA and PB are each 8-bits, any pin on PA or PB may be programmed as input or output (0 = in, 1 = out).

Note: ① During ALE time the data/address lines are duplicated on A<sub>15</sub>-A<sub>8</sub>.

# μPD8355/8755A

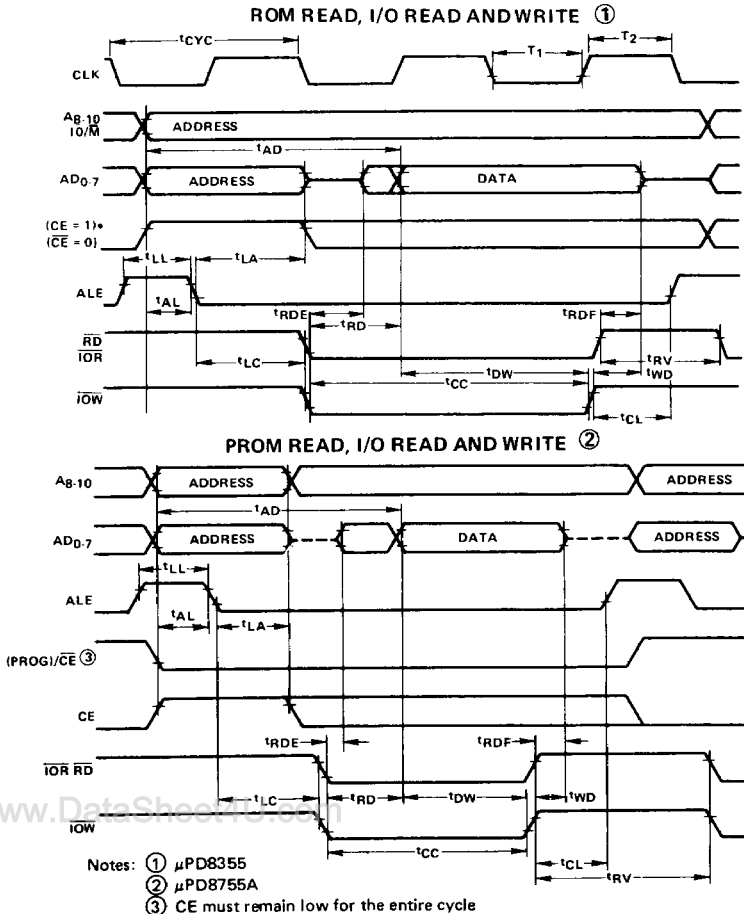
T<sub>a</sub> = 0°C to 70°C, V<sub>CC</sub> = 5V ± 5%

## AC CHARACTERISTICS

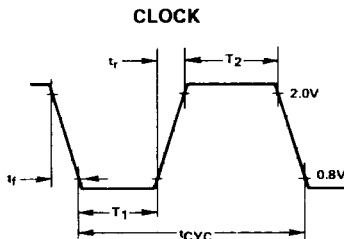
Symbol	Parameter	8355		8355-2		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
t <sub>CYC</sub>	Clock Cycle Time	320		200		ns	C <sub>LOAD</sub> = 150 pF
T <sub>1</sub>	CLK Pulse Width	80		40		ns	
T <sub>2</sub>	CLK Pulse Width	120		70		ns	
t <sub>r</sub> , t <sub>f</sub>	CLK Rise and Fall Time		30		30	ns	
t <sub>AL</sub>	Address to Latch Set Up Time	50		30		ns	150 pF Load
t <sub>LA</sub>	Address Hold Time after Latch	80		30		ns	
t <sub>LC</sub>	Latch to READ/WRITE Control	100		40		ns	
t <sub>RD</sub>	Valid Data Out Delay from READ Control		170		140	ns	
t <sub>AD</sub>	Address Stable to Data Out Valid		400		330	ns	
t <sub>LL</sub>	Latch Enable Width	100		70		ns	
t <sub>RDF</sub>	Data Bus Float after READ	0	100	0	85	ns	
t <sub>CL</sub>	READ/WRITE Control to Latch Enable	20		10		ns	
t <sub>CC</sub>	READ/WRITE Control Width	250		200		ns	
t <sub>DW</sub>	Data in to Write Set Up Time	150		150		ns	
t <sub>WD</sub>	Data in Hold Time After WRITE	10		10		ns	
t <sub>WP</sub>	WRITE to Port Output		400		400	ns	
t <sub>PR</sub>	Port Input Set Up Time	50		50		ns	
t <sub>PH</sub>	Port Input Hold Time	50		50		ns	
t <sub>RVH</sub>	READY HOLD Time	0	160	0	160	ns	
t <sub>ARY</sub>	ADDRESS (CE) to READY		160		160	ns	
t <sub>RV</sub>	Recovery Time Between Controls	300		200		ns	
t <sub>RDE</sub>	READ Control to Data Bus Enable	10		10		ns	

Notes: 30 ns for μPD8755A  
C<sub>LOAD</sub> = 150 pF

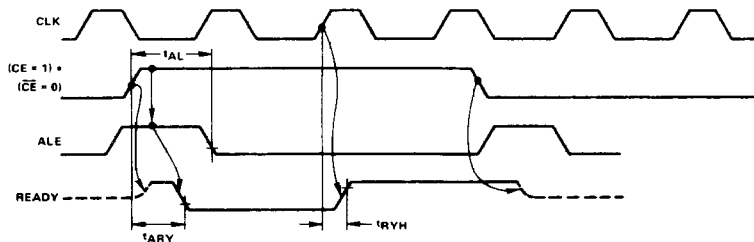
## TIMING WAVEFORMS



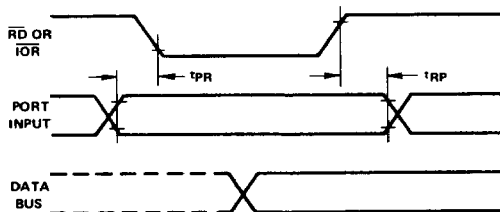
TIMING WAVEFORMS  
(CONT.)



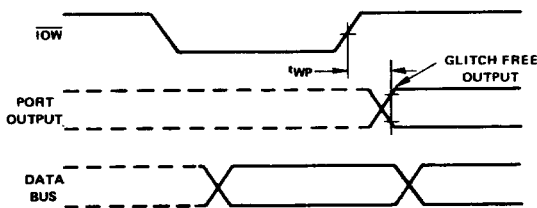
WAIT STATE TIMING (READY = 0)



INPUT MODE: I/O PORT



OUTPUT MODE:



EPROM PROGRAMMING  
μPD8755A

Erasure of the μPD8755A occurs when exposed to ultraviolet light sources of wavelengths less than 4000 Å. It is recommended, if the device is exposed to room fluorescent lighting or direct sunlight, that opaque labels be placed over the window to prevent exposure. To erase, expose the device to ultraviolet light at 2537 Å at a minimum of 15 W-sec/cm<sup>2</sup> (intensity X expose time). After erasure, all bits are in the logic 1 state. Logic 0's must be selectively programmed into the desired locations. It is recommended that NEC's PROM programmer be used for this application.

# $\mu$ PD8355/8755A

## Package Outlines

For information, see Package Outline Section 7.

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Plastic,  $\mu$ PD8355HC/8755AC

Ceramic,  $\mu$ PD8355D

Ceramic,  $\mu$ PD8355HD

Ceramic,  $\mu$ PD8755AD

Cerdip,  $\mu$ PD8755AD, has quartz window