MAR 29 1992

PaceMips™ PR3400 CPU 32-BIT RISC PROCESSOR WITH FLOATING POINT ACCELERATOR

FEATURES

- CPU and FPA in a monolithic VLSI package
- 32-BIT RISC Processor (PaceMips PR3000A) that contains thirty-two general purpose 32-bit registers
- On-Chip Memory Management Unit provides fast address translation for virtual-to-physical memory mapping of the 4 GByte virtual address space
- On-Chip Cache Control for Separate External Instruction and Data Caches of up to 256KBytes each
- Five stage pipeline provides peak execution rate of 1.0 clock cycles per instruction
- Produced with PACE III Technology™
- Single 1xClock input
  - Built-in delay line
- Floating Point Accelerator (PaceMips PR3010A):
  - Contains sixteen 64-bit floating point registers to support single and double precision arithmetic.
  - Fully conforms to ANSI/IEEE Standard 754-1985 "IEEE Standard for Binary Floating Point Arithmetic"
- System performance at 40 MHz:
  - 34 VAX MIPS
  - 11.36 MFLOPS Single-Precision LINPACK
  - 6.56 MFLOPS Double-Precision LINPACK
- Available in 175-pin Ceramic PGA package and 160-pin Metal Quad Flat Pack
- Military product compliant to MIL-STD-883C, Class B

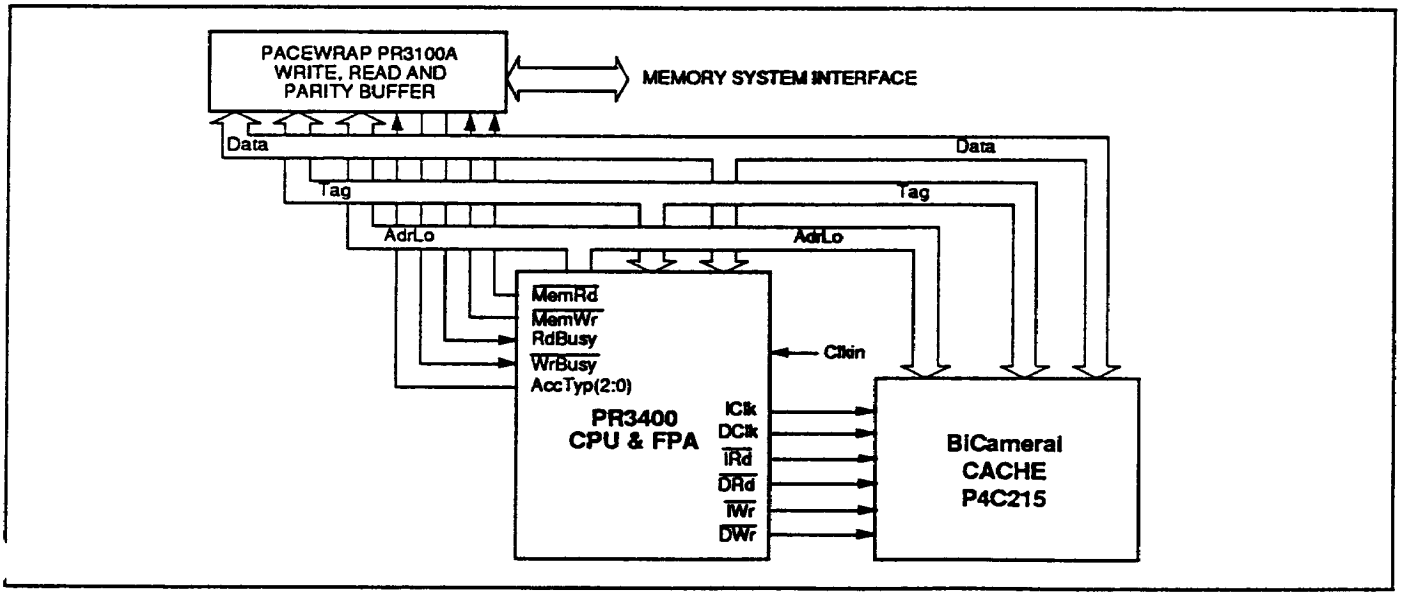
DESCRIPTION

The PaceMips PR3400 is an integrated advanced 32-bit RISC processor including a floating point accelerator designed for applications requiring maximum balanced performance and minimum board space. The PR3400 with its additional capability remains software compatible with the PR3000A processor. When used with the PACEWRAP™ PR3100A single-chip write, read, and parity buffer and Performance Semiconductor BiCameral cache memories, a single-board PaceMips RISC computer becomes a reality at frequencies of 25, 33 and 40 MHz.

The PaceMips PR3400 is manufactured using PACE III Technology which is Performance Advanced CMOS Engineered to use 0.6 micron effective channel lengths resulting in 250 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology is supported by a Class 1 environment volume production facility.

* For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply.

SYSTEM APPLICATION



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1.0 PR3400 PROCESSOR OVERVIEW

1.1 INTRODUCTION

Designed for systems which have limited available board area, the PR3400 provides the maximum performance achievable with the PR3000A RISC microprocessor. It contains both the PR3000A processor and its tightly coupled floating point coprocessor on a single die.

By reducing printed circuit board trace lengths and capacitance on the most critical high-speed signals which service the cache, this packaging provides the PR3000A and PR3010A an environment that is ideal for high-speed operation. The result is a microprocessor system excellent for use in systems from embedded control to workstations.

1.2 CPU & FPA INTERCONNECTION

The PR3400 contains the PR3000A and PR3010A integrated on a single die. This means that the signals which provide communication between the CPU and the FPA are connected internally on the chip. The connection scheme used is typical of most PR3000A system applications. Table 1.1 describes the connection of the two devices.

Because of the constraints imposed by a monolithic device, the PR3400 does not supply any signals unique to the FPA. There are actually very few of these signals and their absence should not affect most systems applications. Table 1.2 lists these signals and their internal connections.

1.3 Built-In Delay Line and Programmable Interrupts

The PR3400 now provides two new features which make the task of system design even easier: (1) on-chip clock generation unit and (2) a programmable FPA/CPU interrupt connection. The built-in clock generation scheme eliminates the need for an external delay line and replaces the external 2X clock oscillator with a 1X oscillator. The output clock $\overline{\text{SysOut}}$ is synchronized with the 1X input clock that is supplied externally. The internal synchonization mechanism takes 6000 cycles to lock. This means that for both warm and cold resets, $\overline{\text{Reset}}$ must be held low for at least 6000 cycles.

Since the four 2X clocks are generated on-chip, from the external 1X clock, phase differences between the four clocks are fixed at a given frequency and the values of T_{Sys}, T_{Smp} and T_{Rd} are shown in Table 1.4. T_{Sys}, T_{Smp} and T_{Rd} are specified with respect to the internal Clk2XPhi and their values are expressed in terms of the input clock period, T_{CkP}. These phase delays, T_{Sys}, T_{Smp} and T_{Rd}, are positioned to maximize performance for a given set of SRAM parameters.

The new monolithic PR3400 supports all interrupts (5:0). Programming is performed at reset and stays fixed until the next reset. Table 1.3 lists the options. Note that $\overline{\text{PhaseDelayOn}}$ is asserted on $\overline{\text{Int}}$ (4) in the W cycle and then $\overline{\text{Int}}$ (4) is used to select the $\overline{\text{FpInt}}$ connection to the CPU in the X, Y and Z cycles.

1.4 PR3400 OPERATION

The operation of the PR3400 is identical to the operation of the PR3000A CPU and PR3010A FPU (connected as described in Section 1.2). For detailed operational and timing information, please consult the PR3000A and PR3010A Interface Specifications.

Table 1.1 FPA & CPU Connections

Connection		Connection	
FPA	CPU	FPA	CPU
Data (31:0)	Data (31:0)	$\overline{\text{Exception}}$	$\overline{\text{Exception}}$
DataP (3:0)	DataP (3:0)	$\overline{\text{FpSync}}$	$\overline{\text{CpSync}}$
$\overline{\text{FpInt}}$	See Table 1.3	$\overline{\text{Reset}}$	$\overline{\text{Reset}}$
FpBusy	CpBusy (output)	$\overline{\text{Run}}$	$\overline{\text{Run}}$
FpCond	CpCond(1) (output)		

Table 1.2 FPA Internal Connections

Signal	Connection
$\overline{\text{FpSysOut}}$	$\overline{\text{FpSysIn}}$
$\overline{\text{PllOn}}$	$\overline{\text{PhaseDelayOn}}$
$\overline{\text{FpPresent}}$	Gnd

Table 1.3 Mode Select on $\overline{\text{Int}}$ (4) During Reset

W Cycle	X Cycle	Y Cycle	Z Cycle	$\overline{\text{FPInt}}$ Connected to CPU Interrupt
$\overline{\text{PhaseDelayOn}}$	0	0	0	5
$\overline{\text{PhaseDelayOn}}$	0	0	1	4
$\overline{\text{PhaseDelayOn}}$	0	1	0	3
$\overline{\text{PhaseDelayOn}}$	0	1	1	2
$\overline{\text{PhaseDelayOn}}$	1	0	0	1
$\overline{\text{PhaseDelayOn}}$	1	0	1	0
$\overline{\text{PhaseDelayOn}}$	1	1	0	NC
$\overline{\text{PhaseDelayOn}}$	1	1	1	NC

Table 1.4 Phase Delays for 2x Clocks

T_{Rd}[2]	= 10%	of T_{CkP}[1]
T_{Smp}[2]	= 12.5%	of T_{CkP}[1]
T_{Sys}[2]	= 25%	of T_{CkP}[1]
$T_{Sys} - T_{Smp}$[2]	= 12.5%	of T_{CkP}[1]
$T_{Sys} - T_{Rd}$[2]	= 15%	of T_{CkP}[1]

Notes: 1. T_{CkP} is the input clock period.
2. The tolerance on each clock delay is ± 4%.
e.g., T_{Smp} = (12.5 ±0.5)%.

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2.0 SIGNAL DESCRIPTION

Data(31:0)	I/O	A 32-bit bus used for all instruction and data transmission among the processor, caches, memory interface, and coprocessors including the FPA.
DataP(3:0)	I/O	A 4-bit bus containing even parity over the data bus.
Tag(31:12)	I/O	A 20-bit bus used for transferring cache tags and high addresses between the processor, caches, and memory interface.
TagV	I/O	The tag validity indicator.
TagP(2:0)	I/O	A 3-bit bus containing even parity over the catenation of TagV and Tag (31:12).
AdrLo(15:0)	O	A 18-bit bus containing byte addresses used for transferring low addresses from the processor to the caches and memory interface.
AdrLo(17:16)	I/O	AdrLo (17:16) can also function as CpCond (3:2) input pins based on the reset configuration.
$\overline{\text{IRd1}}$	O	Read enable for the instruction cache.
$\overline{\text{IWr1}}$	O	Write enable for the instruction cache.
$\overline{\text{IRd2}}$	O	An identical copy of $\overline{\text{IRd1}}$ used to split the load.
$\overline{\text{IWr2}}$	O	An identical copy of $\overline{\text{IWr1}}$ used to split the load.
IClk	O	The instruction cache address latch clock. This clock runs continuously.
$\overline{\text{DRd1}}$	O	The read enable for the data cache.
$\overline{\text{DWr1}}$	O	The write enable for the data cache.
$\overline{\text{DRd2}}$	O	An identical copy of $\overline{\text{DRd1}}$ used to split the load.
$\overline{\text{DWr2}}$	O	An identical copy of $\overline{\text{DWr1}}$ used to split the load.
DClk	O	The data cache address latch clock. This clock runs continuously.
$\overline{\text{XEn}}$	O	The read enable for the Read Buffer.
AccTyp(2:0)	O	A 3-bit bus used to indicate the size of data being transferred on the data bus, whether or not a data transfer is occuring, and the purpose of the transfer.
$\overline{\text{MemWr}}$	O	Signals the occurrence of a main memory write.
$\overline{\text{MemRd}}$	O	Signals the occurrence of a main memory read.
$\overline{\text{BusError}}$	I	Signals the occurrence of a bus error during a main memory read or write.
$\overline{\text{Run}}$	O	Indicates whether the processor is in the run or stall state.
$\overline{\text{Exception}}$	O	Indicates that the instructions about to commit state should be aborted and other exception related information.
$\overline{\text{SysOut}}$	O	A reflection of the internal processor clock used to generate the system clock.
RdBusy	I	The main memory read stall termination signal. In most system designs RdBusy is normally asserted and is deasserted only to indicate the successful completion of a memory read. RdBusy is sampled by the processor only during memory read stalls.
$\overline{\text{WrBusy}}$	I	The main memory write stall initiation/termination signal.
CpBusy	O	Coprocessor busy stall initiation/termination signal. FpBusy of FPA is connected internally. Output of PR3400.
CpCond(0)	I	A 1-bit bus used to transfer conditional branch status from the coprocessors to the main processor.
CpCond(1)	O	The Co-processor 1 (FPA) condition signal FpCond is connected internally. Output of PR3400.
$\overline{\text{Int(5:0)}}$	I	A 6-bit bus used by the memory interface and coprocessors to signal maskable interrupts to the processor.
$\overline{\text{Reset}}$	I	Synchronous initialization input used to force execution starting from the reset memory address. $\overline{\text{Reset}}$ must be deasserted synchronously but asserted asynchronously. The deassertion of $\overline{\text{Reset}}$ must be synchronized by the leading edge of $\overline{\text{SysOut}}$. $\overline{\text{Reset}}$ must be asserted for at least 6000 cycles to allow for clock synchronization.
Clkin	I	The 1x input clock used to generate Clk2xSys, Clk2xSmp, Clk2xRd and Clk2xPhi.
$\overline{\text{CPSync}}$	O	A clock that is identical to $\overline{\text{SysOut}}$ and used by coprocessors for timing synchronization with the CPU.

Note: CpBusy, CpCond (1) are output pins from PR3400.

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3.0 ELECTRICAL SPECIFICATIONS, COMMERCIAL TEMPERATURE RANGE (T = 0° TO 70°C, V = 5V±5%)

3.1 MAXIMUM RATINGS [3]

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		-0.5	+7.0	V
V_{IN}	Input Voltage[1,2]		-0.5	+7.0	V

Notes:
1. V_{IN} Min. = -3.0V for pulse width less than 15ns.
2. $V_{IN} \leq V_{CC} + 0.5$
2. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

3.2 RECOMMENDED OPERATING CONDITIONS [1,2 & 3]

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 5%

Notes:
1. The case temperature must be limited by using adequate air flow and/or an appropriate heat sink or other thermal management design.
2. The maximum operating junction temperature should be limited to 125°C.
3. For optimum performance and improved reliability, it is recommended that the operating junction temperature should be kept below 85°C.

3.3 CAPACITIVE LOAD DERATING FACTOR

Sym.	Parameter	Conditions	25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	
C_{LD}	Load Derate		0.5	1	0.5	1	0.5	1	ns/25pF

3.4 DC ELECTRICAL CHARACTERISTICS

Sym.	Parameter	Conditions	25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = -4mA	3.5		3.5		3.5		V
V_{OHC}	Output HIGH Voltage[3]	V_{CC} = Min. I_{OH} = -4mA	4.0		4.0		4.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 4mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2	V_{CC}+0.5	2	V_{CC}+0.5	2	V_{CC}+0.5	V
V_{IL}	Input LOW Voltage[1]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
V_{IHS}	Input HIGH Voltage[2]		3.0	V_{CC}+0.5	3.0	V_{CC}+0.5	3.0	V_{CC}+0.5	V
V_{ILS}	Input LOW Voltage[2]		-0.5	0.5	-0.5	0.5	-0.5	0.5	V
C_{IN}	Input Capacitance			10		10		10	pF
C_{OUT}	Output Capacitance			10		10		10	pF
I_{CC}	Operating Current	V_{CC} = Max.		800		1000		1200	mA
C_{Ld}	Load Capacitance			25		25		25	pF
I_{OH}	Output HIGH Current[4]			–8		–8		–8	mA

Notes:
1. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively are permissible for pulse widths up to 15ns.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{\text{Reset}}$.
3. V_{OHC} applies to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.
4. I_{OH} for AdrLo (17:0) only.

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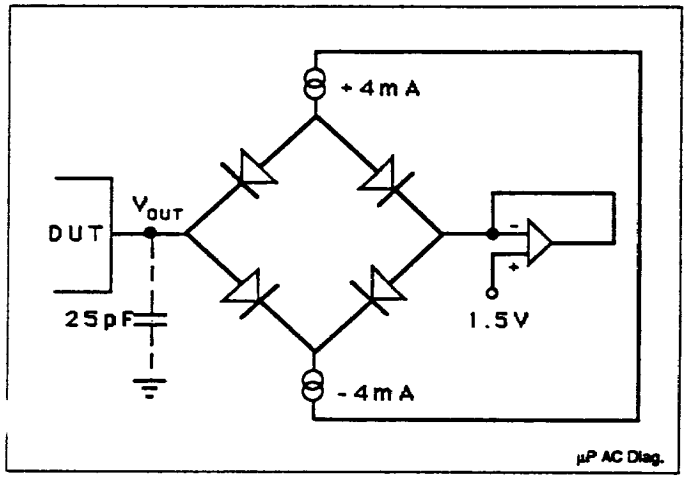
3.5 AC ELECTRICAL CHARACTERISTICS, COMMERCIAL TEMPERATURE RANGE[1&2] (T = 0° TO 70°C, V = 5V±5%)

Sym.	Parameter	Conditions	25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	
$T_{ClkHigh}$	Input Clock High	Transitions≤5.0ns	13		10		8		ns
T_{ClkLow}	Input Clock Low	Transitions≤5.0ns	13		10		8		ns
T_{ClkP}	Input Clock Period		40	200	30	150	25	100	ns
T_{DEn}	Data Enable	Run	-0.5	-1.5		-1		-1	ns
T_{DDis}	Data Disable	Run	0	-0.5		-0.5		-0.5	ns
T_{DVal}	Data Valid	Run	1	2		2		1.5	ns
T_{WrDly}	Write Delay	Run	0	3		2		1.5	ns
T_{DS}	Data Setup	Run	6		5		3		ns
T_{DH}	Data Hold	Run	-2.5		-1.5		-0.5		ns
T_{AcTy}	Access Type (1:0)	Run	1	5		4		3	ns
T_{AT2}	Access Type (2)	Run	1	12		8.5		7	ns
T_{MWr}	Memory Write	Run	1	18	0	8.5	0	7	ns
T_{Exc}	Exception	Run	1	5		3.5		3	ns
T_{AVal}	Address Valid	Run				2		1.0	ns
T_{IntS}	Int Setup	Run	6		5		3		ns
T_{IntH}	Int Hold	Run			-1.5		-0.5		ns
T_{SAVal}	Address Valid	Stall		20		15		12.5	ns
T_{SAcTY}	Access Type	Stall		18		9.5		8	ns
T_{MRdI}	Memory Read Initiate	Stall	1	18	1	9.5	0.5	8	ns
T_{MRdT}	Mem. Read Terminate	Stall	1	5		3.5		3	ns
T_{Sd}	Run Terminate	Stall	3	11	2	8	0	7	ns
T_{Run}	Run Initiate	Stall	1	4		3		2.5	ns
T_{SMWr}	Memory Write	Stall	3	18	1	9.5	1	8	ns
T_{SExc}	Exception Valid	Stall	3	15		9		7.0	ns

Notes: 1. All output times are given assuming 25pF of capacitive load.
2. All timings referenced to 1.5V.

Figure 3.5.1 Output Loading for AC Testing



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4.0 ELECTRICAL SPECIFICATIONS, MILITARY TEMPERATURE RANGE (T_A=-55°C TO 125°C, V=5V±10%)

4.1 MAXIMUM RATINGS[3]

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		-0.5	+7.0	V
V_{IN}	Input Voltage[1,2]		-0.5	+7.0	V

Notes:
1. V_{IN} Min. = -3.0V for pulse width less than 15ns.
2. $V_{IN} \leq V_{CC}$ +0.5
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

4.2 RECOMMENDED OPERATING CONDITIONS[1, 2 & 3]

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%

Notes:
1. The case temperature must be limited by using adequate air flow and/or an appropriate heat sink or other thermal management design.
2. The maximum operating junction temperature should be limited to 125°C.
3. For optimum performance and improved reliability, it is recommended that the operating junction temperature should be kept below 85°C.

4.3 CAPACITIVE LOAD DERATING FACTOR

Sym.	Parameter	Conditions	25MHz		33MHz		Units
			Min	Max	Min	Max	
C_{LD}	Load Derate		0.5	1	0.5	1	ns/25pF

4.4 DC ELECTRICAL CHARACTERISTICS

Sym.	Parameter	Conditions	25MHz		33MHz		Units
			Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = -4mA	3.5		3.5		V
V_{OHC}	Output HIGH Voltage[3]	V_{CC} = Min. I_{OH} = -4mA	4.0		4.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 4mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2	V_{CC}+0.5	2	V_{CC}+0.5	V
V_{IL}	Input LOW Voltage[1]		-0.5	0.8	-0.5	0.8	V
V_{IHS}	Input HIGH Voltage[2]		3.0	V_{CC}+0.5	3.0	V_{CC}+0.5	V
V_{ILS}	Input LOW Voltage[2]		-0.5	0.5	-0.5	0.5	V
C_{IN}	Input Capacitance			10		10	pF
C_{OUT}	Output Capacitance			10		10	pF
I_{CC}	Operating Current	V_{CC} = Max.		1000		1200	mA
C_{Ld}	Load Capacitance			25		25	pF
I_{OH}	Output HIGH Current[4]			–8		–8	mA

Notes:
1. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively are permissible for pulse widths up to 15ns.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{\text{Reset}}$.
3. V_{OHC} applies to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.
4. I_{OH} for AdrLo (17:0) only.

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4.5 AC ELECTRICAL CHARACTERISTICS, MILITARY TEMPERATURE RANGE[1&2] (T = –55°C TO 125°C, V = 5V±10%)

Sym.	Parameter	Conditions	25MHz		33MHz		Units
			Min	Max	Min	Max	
T_{CkHigh}	Input Clock High	Transitions≤5.0ns	13		10		ns
T_{CkLow}	Input Clock Low	Transitions≤5.0ns	13		10		ns
T_{CkP}	Input Clock Period		40	200	30	150	ns
T_{DEn}	Data Enable	Run	-0.5	-1.5		-1	ns
T_{DDis}	Data Disable	Run	0	-0.5		-0.5	ns
T_{DVal}	Data Valid	Run	1	2		2	ns
T_{WrDly}	Write Delay	Run	0	3		2	ns
T_{DS}	Data Setup	Run	6		5		ns
T_{DH}	Data Hold	Run	-2.5		-1.5		ns
T_{AcTy}	Access Type (1:0)	Run	1	5		4	ns
T_{AT2}	Access Type (2)	Run	1	12		8.5	ns
T_{MWr}	Memory Write	Run	1	18	0	8.5	ns
T_{Exc}	Exception	Run	1	5		3.5	ns
T_{AVal}	Address Valid	Run				2	ns
T_{IntS}	Int Setup	Run	6		5		ns
T_{IntH}	Int Hold	Run			-1.5		ns
T_{SAVal}	Address Valid	Stall		20		15	ns
T_{SAcTY}	Access Type	Stall		18		9.5	ns
T_{MRdI}	Memory Read Initiate	Stall	1	18	1	9.5	ns
T_{MRdT}	Mem. Read Terminate	Stall	1	5		3.5	ns
T_{Sd}	Run Terminate	Stall	3	11	2	8	ns
T_{Run}	Run Initiate	Stall	1	4		3	ns
T_{SMWr}	Memory Write	Stall	3	18	1	9.5	ns
T_{SExc}	Exception Valid	Stall	3	15		9	ns

Notes: 1. All output times are given assuming 25pF of capacitive load.
2. All timings referenced to 1.5V.

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5.0 MECHANICAL DATA —PIN ASSIGNMENTS and PACKAGE DIMENSIONS

5.1 175-pin Ceramic Pin Grid Array

Table 5.1 Pinout—175-pin Ceramic Pin Grid Array, Cavity Down

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
AccTyp 0	P15	Data(19)	N3	Tag(17)	D14	Gnd	C12
AccTyp 1	M14	Data(20)	P2	Tag(18)	C15	Gnd	C7
AccTyp 2	L13	Data(21)	R2	Tag(19)	D15	Gnd	M4
AdrLo(0)	C1	Data(22)	P4	Tag(20)	E14	Gnd	M6
AdrLo(1)	E3	Data(23)	P1	Tag(21)	F14	Gnd	M8
AdrLo(2)	D2	Data(24)	N5	Tag(22)	G14	Gnd	N9
AdrLo(3)	B1	Data(25)	R3	Tag(23)	F15	Vcc	H13
AdrLo(4)	C2	Data(26)	P5	Tag(24)	H15	Vcc	A15
AdrLo(5)	C4	Data(27)	P6	Tag(25)	H14	Vcc	A5
AdrLo(6)	A2	Data(28)	R5	Tag(26)	J15	Vcc	C3
AdrLo(7)	B3	Data(29)	R7	Tag(27)	K15	Vcc	E15
AdrLo(8)	C5	Data(30)	P8	Tag(28)	J13	Vcc	F1
AdrLo(9)	B4	Data(31)	R4	Tag(29)	J14	Vcc	L1
AdrLo(10)	A3	Data P0	E1	Tag(30)	L15	Vcc	M15
AdrLo(11)	A4	Data P1	J2	Tag(31)	L14	Vcc	N7
AdrLo(12)	B5	Data P2	M3	TagP(0)	C14	Vcc	N8
AdrLo(13)	B7	Data P3	N6	TagP(1)	G15	Vcc	R1
AdrLo(14)	A6	DClk	P11	TagP(2)	K14	Vcc	R12
AdrLo(15)	A7	$\overline{\text{DRd1}}$	N11	TagV	N15	Vcc	R15
AdrLo(16)	A9	$\overline{\text{DRd2}}$	B2	$\overline{\text{Wrbusy}}$	A13	Vcc	D11
AdrLo(17)	A10	$\overline{\text{DWr1}}$	R14	$\overline{\text{XEn}}$	P7	Vcc	D5
$\overline{\text{BusError}}$	B12	$\overline{\text{DWr2}}$	B13	ClkIn	P9	Vcc	D7
CpBusy	B11	$\overline{\text{Exception}}$	R8	Gnd	D3	Vcc	D9
CpCond 0	A8	IClk	R13	Gnd	F13	Vcc	E12
CpCond 1	B8	$\overline{\text{Int 0}}$	C9	Gnd	G13	Vcc	E4
$\overline{\text{CpSync}}$	P14	$\overline{\text{Int 1}}$	B9	Gnd	G3	Vcc	G12
Data(0)	E2	$\overline{\text{Int 2}}$	A11	Gnd	K13	Vcc	G4
Data(1)	D1	$\overline{\text{Int 3}}$	B10	Gnd	K3	Vcc	J12
Data(2)	F3	$\overline{\text{Int 4}}$	C10	Gnd	M13	Vcc	J4
Data(3)	G2	$\overline{\text{Int 5}}$	A12	Gnd	N10	Vcc	L12
Data(4)	G1	$\overline{\text{IRd1}}$	P12	Gnd	N4	Vcc	L4
Data(5)	H2	$\overline{\text{IRd2}}$	B6	Gnd	R6	Vcc	M11
Data(6)	H1	$\overline{\text{IWr1}}$	P13	Gnd	D4	Vcc	M5
Data(7)	F2	$\overline{\text{IWr2}}$	P3	Gnd	D10	Vcc	M7
Data(8)	H3	$\overline{\text{MemRd}}$	N13	Gnd	D12	Vcc	M9
Data(9)	J3	$\overline{\text{MemWr}}$	N12	Gnd	D6	NC	P10
Data(10)	J1	RdBusy	C11	Gnd	D8	NC	R9
Data(11)	K2	$\overline{\text{Reset}}$	A14	Gnd	F12	NC	R10
Data(12)	L2	$\overline{\text{Run}}$	N14	Gnd	F4	NC	C6
Data(13)	M1	$\overline{\text{SysOut}}$	R11	Gnd	H12	NC	C8
Data(14)	N1	Tag(12)	B14	Gnd	H4		
Data(15)	K1	Tag(13)	C13	Gnd	K12		
Data(16)	M2	Tag(14)	D13	Gnd	K4		
Data(17)	L3	Tag(15)	B15	Gnd	M10		
Data(18)	N2	Tag(16)	E13	Gnd	M12		

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Figure 5.1 PaceMips PR3400 — 175-pin Ceramic Pin Grid Array, Cavity Down

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	Vcc	Data 21	Data 25	Data 31	Data 28	Gnd	Data 29	Exception	NC	NC	SysOut	Vcc	IClk	DWr1	Vcc
P	Data 23	Data 20	IWr2	Data 22	Data 26	Data 27	XEn	Data 30	ClkIn	NC	DClk	IRd1	IWr1	Cp Sync	Acc Typ0
N	Data 14	Data 18	Data 19	Gnd	Data 24	Data P3	Vcc	Vcc	Gnd	Gnd	DRd1	Mem Wr	Mem Rd	Run	Tag V
M	Data 13	Data 16	Data P2	Gnd	Vcc	Gnd	Vcc	Gnd	Vcc	Gnd	Vcc	Gnd	Gnd	Acc Typ1	Vcc
L	Vcc	Data 12	Data 17	Vcc								Vcc	Acc Typ2	Tag 31	Tag 30
K	Data 15	Data 11	Gnd	Gnd								Gnd	Gnd	Tag P2	Tag 27
J	Data 10	Data P1	Data 9	Vcc								Vcc	Tag 28	Tag 29	Tag 26
H	Data 6	Data 5	Data 8	Gnd				**175-pin PGA (Bottom View)**				Gnd	Vcc	Tag 25	Tag 24
G	Data 4	Data 3	Gnd	Vcc								Vcc	Gnd	Tag 22	Tag P1
F	Vcc	Data 7	Data 2	Gnd								Gnd	Gnd	Tag 21	Tag 23
E	Data P0	Data 0	AdrLo 1	Vcc								Vcc	Tag 16	Tag 20	Vcc
D	Data 1	AdrLo 2	Gnd	Gnd	Vcc	Gnd	Vcc	Gnd	Vcc	Gnd	Vcc	Gnd	Tag 14	Tag 17	Tag 19
C	AdrLo 0	AdrLo 4	Vcc	AdrLo 5	AdrLo 8	NC	GND	NC	Int 0	Int 4	Rd Busy	Gnd	Tag 13	Tag P0	Tag 18
B	AdrLo 3	DRd2	AdrLo 7	AdrLo 9	AdrLo 12	IRd2	AdrLo 13	Cp Cond 1	Int 1	Int 3	CpBusy	Bus Error	DWr2	Tag 12	Tag 15
A		AdrLo 6	AdrLo 10	AdrLo 11	Vcc	AdrLo 14	AdrLo 15	Cp Cond 0	AdrLo 16	AdrLo 17	Int 2	Int 5	Wr Busy	Reset	Vcc

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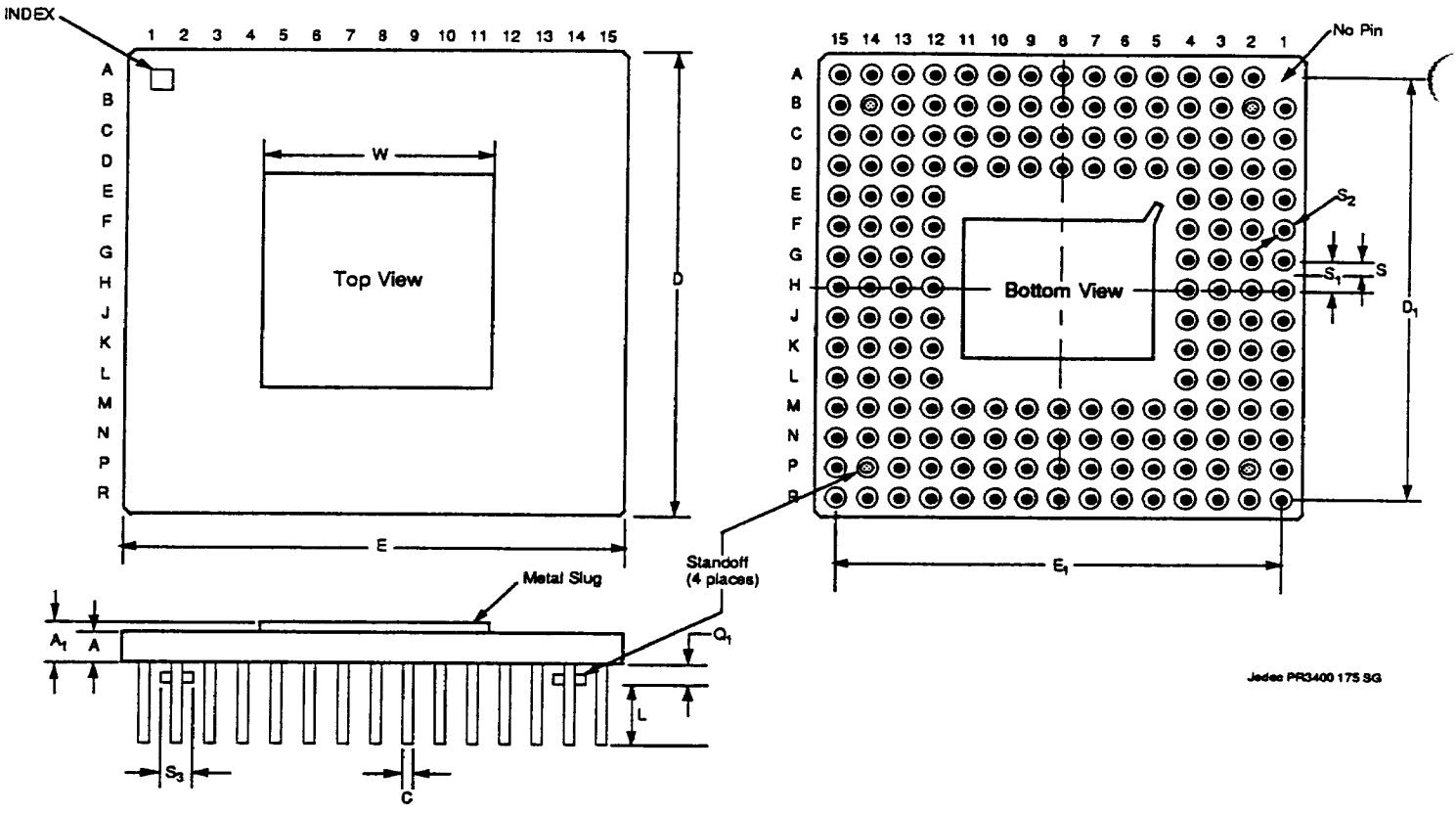
Figure 5.2 PR3400 Dimensions — 175-pin Ceramic Pin Grid Array, Cavity Down



Symbol	Min.		Max.	
	in.	mm.	in.	mm.
A	0.085	2,16	0.105	2,67
A_1	0.104	2,64	0.124	3,15
C	0.016	0,4	0.020	0,5
D/E	1.559	39,59	1.591	40,9
D_1/E_1	1.388	35,36	1.414	35,76
L	0.120	3,05	0.140	3,55
M*	15	15	15	15
N**	175	175	175	175
Q_1	0.040	1,00	0.060	1,52
S	0.050	1,27	0.050	1,27
S_1	0.100 BSC	2,54 BSC	0.100 BSC	2,54 BSC
S_2	0.065	1,65	0.075	1,90
S_3	0.045	1,14	0.055	1,40
W	0.990	25,15	1.010	25,65

* Typical number of pins per row
** Total number of pins per package
BSC = Basic Spacing between Centers

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5.3 160 -Lead Metal Quad Flat Pack

Table 5.3 Pinout —160-lead Metal Quad Flat Pack, Gull Wing, Cavity Down, EIAJ Standard

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
Data(0)	127	Tag(12)	79	AdrLo(0)	126	Gnd10	71
Data(1)	128	Tag(13)	78	AdrLo(1)	125	Gnd11	73
Data(2)	129	Tag(14)	76	AdrLo(2)	124	Gnd12	75
Data(3)	133	Tag(15)	74	AdrLo(3)	123	Gnd13	77
Data(4)	135	Tag(16)	70	AdrLo(4)	122	Gnd14	81
Data(5)	137	Tag(17)	69	AdrLo(5)	119	Gnd15	82
Data(6)	139	Tag(18)	68	AdrLo(6)	118	Gnd16	101
Data(7)	131	Tag(19)	67	AdrLo(7)	117	Gnd17	110
Data(8)	140	Tag(20)	66	AdrLo(8)	116	Gnd18	112
Data(9)	141	Tag(21)	64	AdrLo(9)	115	Gnd19	114
Data(10)	142	Tag(22)	63	AdrLo(10)	113	Gnd20	121
Data(11)	145	Tag(23)	62	AdrLo(11)	111	Gnd21	130
Data(12)	147	Tag(24)	59	AdrLo(12)	109	Gnd22	136
Data(13)	149	Tag(25)	58	AdrLo(13)	106	Gnd23	138
Data(14)	150	Tag(26)	56	AdrLo(14)	104	Gnd24	151
Data(15)	143	Tag(27)	54	AdrLo(15)	102	Gnd25	160
Data(16)	152	Tag(28)	53	$\overline{\text{Exception}}$	19		
Data(17)	153	Tag(29)	52	$\overline{\text{XEn}}$	13		
Data(18)	154	Tag(30)	51	$\overline{\text{Run}}$	43		
Data(19)	157	Tag(31)	48	Vcc1	8		
Data(20)	158	TagP(0)	72	Vcc2	10		
Data(21)	1	TagP(1)	61	Vcc3	12		
Data(22)	2	TagP(2)	50	Vcc4	22		
Data(23)	155	TagV	47	Vcc5	41		
Data(24)	3	$\overline{\text{Int}}$(0)	93	Vcc6	49		
Data(25)	4	$\overline{\text{Int}}$(1)	92	Vcc7	65		
Data(26)	5	$\overline{\text{Int}}$(2)	91	Vcc8	80		
Data(27)	9	$\overline{\text{Int}}$(3)	90	Vcc9	94		
Data(28)	11	$\overline{\text{Int}}$(4)	89	Vcc10	96		
Data(29)	15	$\overline{\text{Int}}$(5)	88	Vcc11	98		
Data(30)	17	CpCond(0)	100	Vcc12	103		
Data(31)	6	CpCond(1)	99	Vcc13	105		
DataP(0)	132	AdrLo(16)	97	Vcc14	107		
DataP(1)	144	AdrLo(17)	95	Vcc15	108		
DataP(2)	156	AccTyp(0)	44	Vcc16	120		
DataP(3)	7	AccTyp(1)	45	Vcc17	134		
1xClk	23	AccTyp(2)	46	Vcc18	146		
N.C.	21	$\overline{\text{MemWr}}$	38	Vcc19	148		
N.C.	24	$\overline{\text{MemRd}}$	39	Vcc20	159		
N.C.	20	$\overline{\text{DWr2}}$	36	Gnd1	14		
$\overline{\text{RdBusy}}$	85	$\overline{\text{IRd1}}$	31	Gnd2	16		
$\overline{\text{WrBusy}}$	86	$\overline{\text{IWr1}}$	35	Gnd3	18		
$\overline{\text{CpBusy}}$	87	$\overline{\text{DRd1}}$	33	Gnd4	27		
$\overline{\text{BusError}}$	84	$\overline{\text{DWr1}}$	37	Gnd5	29		
$\overline{\text{Reset}}$	83	IClk	28	Gnd6	42		
$\overline{\text{SysOut}}$	25	DClk	26	Gnd7	55		
$\overline{\text{CpSync}}$	40	$\overline{\text{IWr2}}$	34	Gnd8	57		
$\overline{\text{DRd2}}$	32	$\overline{\text{IRd2}}$	30	Gnd9	60		

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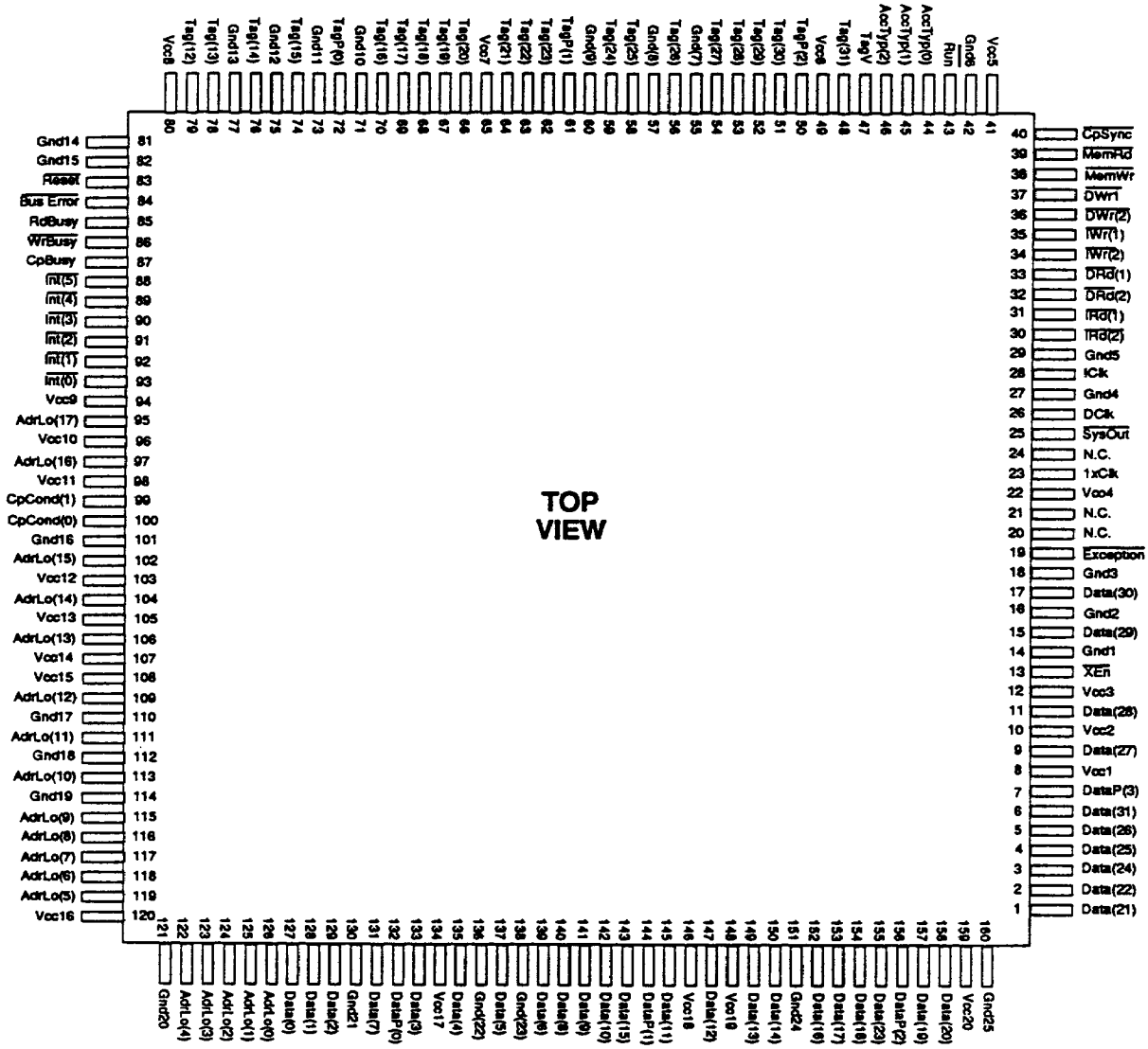
Figure 5.4 PR3400 Pin Diagram–160-Lead Metal Quad Flat Pack, Gull Wing, Cavity Down, EIAJ Standard



PR3400 160 Pinout

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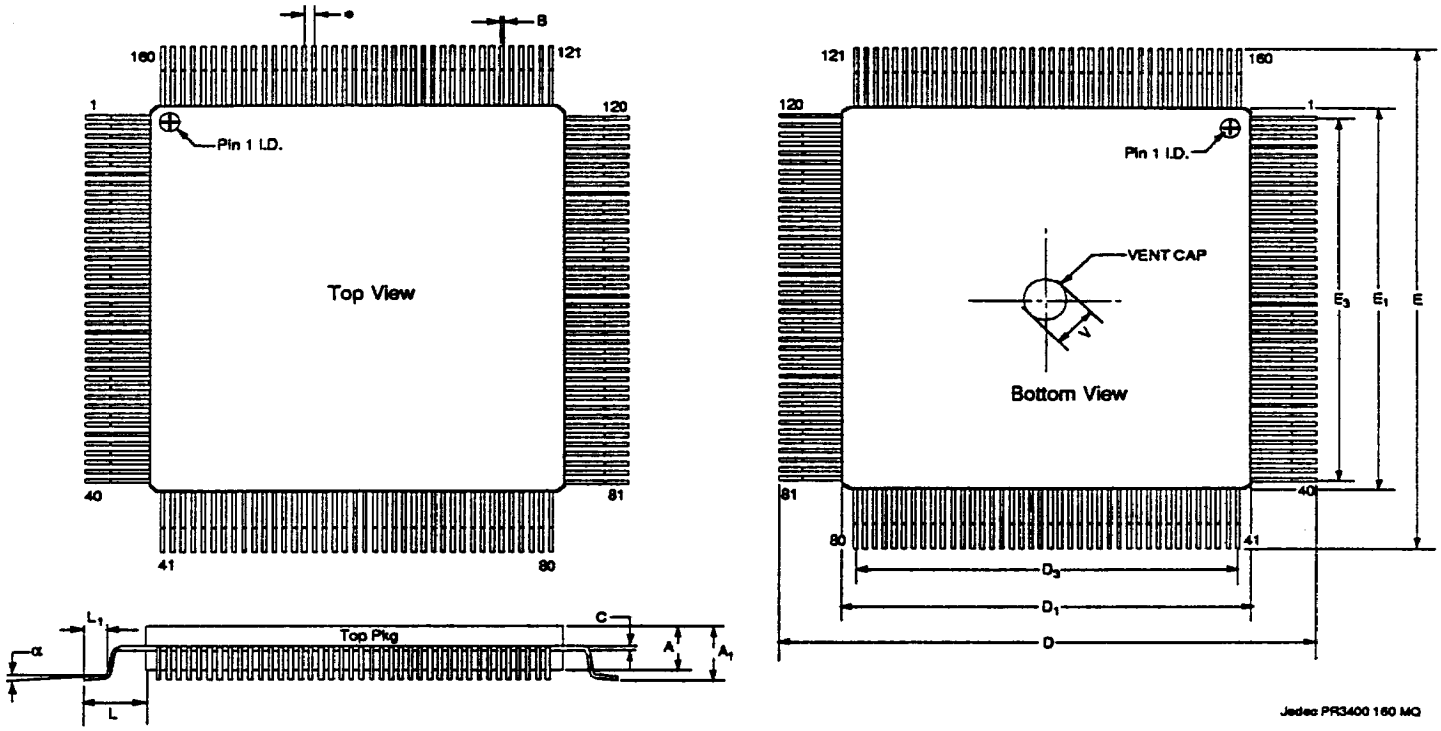
Figure 5.5 PR3400 Dimensions — 160-pin Metal Quad Flat Pack, Cavity Down



Symbol	Min.		Max.	
	in.	mm.	in.	mm.
A	0.125	3,15	0.135	3,45
A_1	0.135	3,50	0.150	3,85
C	0.004	0,10	0.008	0,20
B	0.010	0,25	0.012	0,30
D/E	1.240	31,50	1,260	32,0
D_1/E_1	1.085	27,55	1.100	27,75
D_3/E_3	1.000	25,4	1.000	25,4
e	0.025 BSC	0,64 BSC	0.25 BSC	0,64 BSC
L	0.040	1,00	0.080	2,00
L_1	0.025	0,65	0.040	0,95
V	0.120	3,10	0.125	3,20
α	0°–5°	0°–5°	0°–5°	0°–5°

BSC = Basic Spacing between Centers

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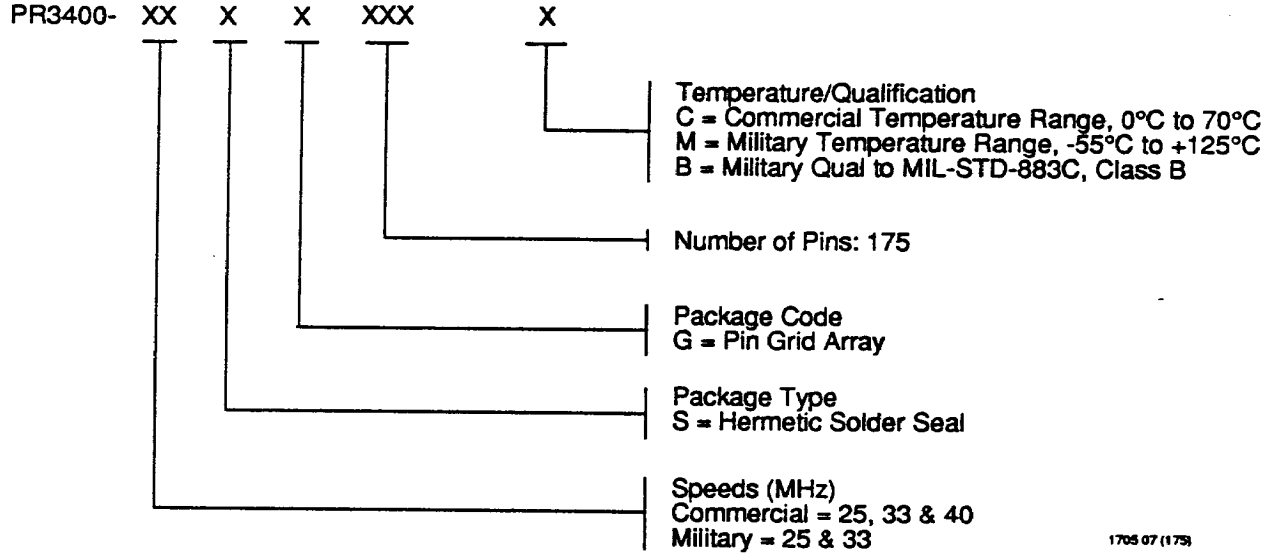
6.0 MOUNTING

A variety of sockets allow low insertion force or zero insertion force mountings, and a choice of terminals such as soldertail, surface mounts or wire wrap. Several sockets are available from the following sample list of socket manufacturers. Contact the manufacturer directly for the latest socket specifications.

- AMP Incorporated
  P.O.Box 3608
  Harrisburg, PA 17105-3608
  (800) 522-6752
- Burndy Corporation
  Richards Avenue
  Norwalk, CT 06856
  (203) 838-4444
- Yamaichi Electronics Inc.
  1425 Koll Circle, Suite 106
  San Jose, CA 95112
  (408) 452-0797
- Textool/3M Test
  and Interconnect Products Department
  3M Austin Center
  P.O.Box 2963
  Austin, TX 78769-2963
  (800) 225-5373

7.0 ORDERING INFORMATION



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