HI-8030, 31

High Voltage Display Driver with Independent Counter/Timer

General Description

The HI-8030 and HI-8031 devices are configured to drive either conventional twisted nematic or high voltage dichroic LCD's. The HI-8030 drives 3-digit, 7-segment displays with three independent general purpose annunciators. The HI-8031 drives 4-digit, 7-segment displays with four annunciators.

In addition, these devices include a multi-function counter/timer that can be used in conjunction with the display driver or independently for other unrelated system tasks. The HI-8030 has a 12-bit counter/timer, and the HI-8031 has a 16-bit counter/timer. The counter/timer is under software control and can be programmed to count in five different modes: hex, decimal, minutes/seconds, hours/minutes and seconds/hundredths of seconds.

The HI-8030 and HI-8031 simplify the task of implementing a cost-effective 7-segment display for microprocessor systems, since they latch data and perform character decoding. Two output decoder font options are available for each device. One will decode 4-bit binary data into a 7-segment hexadecimal output. The other option will provide the Code B output format 0-9, Dash, E, H, L, P, Blank.

Features

- Drives up to 35V Displays
- 12-Bit or 16-Bit Independently Programmable Counter/Timer
- 3- or 4-Digit 7-Segment Direct Drive Outputs
- Three or Four General Purpose Annunciator Outputs
- Hexadecimal or Code B Fonts Available
- Five Software-Controllable Counting Formats
- On-Chip Backplane Driver with Oscillator Circuitry
- Cascadable for Larger Displays and More Counter Stages
- Easily Interfaced with Most Microprocessors
- Operation up to 10MHz
- Leading Zero Blanking
- Schmitt Triggered Clock Input
- CMOS Circuitry: Wide Supply Voltage Range, Low Power Operation, High Noise Immunity, Wide Temperature Range
- TTL or CMOS Compatible
- Can Be Used as Stand-Alone Counter/Display
- Also Drives Vacuum Fluorescent Displays (up to 2mA/seg.)

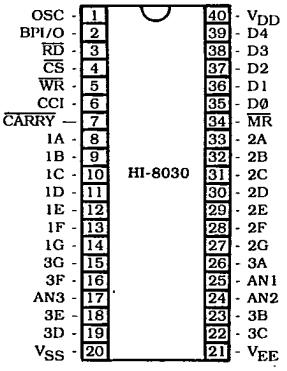
Ordering Information

HI-8030

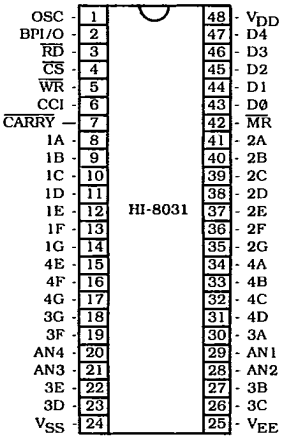
C	Commercial Grade
M	MIL-STD-883C, Class B, Method 5004 Equivalent
1	Decodes HEX
2	Decodes Code B
P	Plastic DIP
C	Ceramic Side Brazed DIP
D	CerDIP — (40-Pin Package Only)
L	Ceramic Leadless Chip Carrier
0	3-Digit, 40-Pin
1	4-Digit, 48-Pin

NOTE: Several other optional packaging and pinout configurations are available on special order for larger volume applications.

Pin Configuration

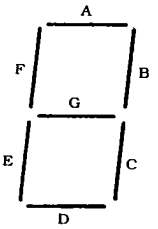


(Top View)



(Top View)

Segment Assignment



HOLT INC.
INTEGRATED CIRCUITS

Absolute Maximum Ratings (Voltages Referenced to V_{SS} = OV)

Supply Voltage V_{DD} ..... −.3V to +13V V_{EE} ..... +.3V to −36V	Power Dissipation ..... 250mW @ 70°C
Voltage at Any Input ..... −.3V to V_{DD} +.3V	Operating Temperature Range: Plastic ..... −40°C to +85°C Ceramic ..... −55°C to +125°C
DC Current Drain per Input Pin 10mA	Storage Temperature Range: Plastic ..... −40°C to +125°C Ceramic ..... −65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Total Clock Cycle Time

t_{CT}	Total Clock Cycle Time	$t_{CL} + t_{CH}$	
		HI-8030	HI-8031
t_{CRY}	CARRY Pulse Width		
	Hex Mode	t_{CT} x 2,048	t_{CT} x 32,768
	Decimal Mode	t_{CT} x 200	t_{CT} x 2,000
	Min/Sec	t_{CT} x 120	t_{CT} x 600
	Hr/Min	t_{CT} x 120	t_{CT} x 120
	Sec/ 1/100 Sec	t_{CT} x 200	t_{CT} x 1,000

DC Electrical Characteristics

V_{DD} = 5V, V_{EE} = -30V, V_{SS} = 0V, TA = 25°C (Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DD}	Logic Supply Voltage		3	—	12	V
V_{EE}	Display Supply Voltage	$3V \leqslant V_{DD} \leqslant 12V$	V_{DD} - 35	—	0	V
I_{DD}	Logic Supply Current	CMOS Input Levels No Load f_c = ØHz	—	—	350	μA
I_{EE}	Display Driver Current	No load, f_{BP} = 100Hz	—	—	-200	μA
I_{DOH}	Output High Display Current	$V_{DOH} = V_{DD} - 2V$	1.5	2	—	mA
I_{DOL}	Output Low Display Current	$V_{DOL} = V_{EE} + 2V$	1.5	2	—	mA
V_{IH}	High Level Input Voltage (Except CCI)	V_{DD} = 5V	2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage (Except CCI)	V_{DD} = 5V	0	—	1.3	V
V_{IH}	CCI High Level Input Voltage	$3V \leqslant V_{DD} \leqslant 12V$	50% V_{DD}	55% V_{DD}	60% V_{DD}	V
V_{IL}	CCI Low Level Input Voltage	$3V \leqslant V_{DD} \leqslant 12V$	40% V_{DD}	45% V_{DD}	50% V_{DD}	V
I_{OL}	Logic Output Low Current	V_{OUT} = .8V	1.6	—	—	mA
I_{OH}	Logic Output High Current	V_{OUT} = 2.4V	400	—	—	μA
Vo Avg.	DC Bias (average) Any Segment Output to Backplane	$f_{BP} \leqslant 100Hz$	—	—	20	mV
I_L	Input Leakage Current		—	—	5	μA
C_I	Input Capacitance		—	—	5	pF

Input/Output Designation

Pin Number		Pin Name	Symbol	Function
8030	8031			
1	1	Oscillator	OSC	Controls backplane frequency when attached to an RC circuit. Disables backplane output (BPI/O) and allows synchronizing backplane input when tied to V_{DD}
2	2	Backplane input/output	BPI/O	Provides backplane drive when OSC is oscillating and allows backplane synchronization of cascaded devices when OSC is tied to V_{DD}.
3	3	Read	RD	Active low, selects data Read operation.
4	4	Chip Select	CS	Active low, enables either a Read or Write operation. Enables 3-state Data I/O lines.
5	5	Write	WR	Active low, selects data or instruction Write operation.
6	6	Counter Clock Input	CCI	Increments counter/timer on each Ø to 1 transition when enabled. Schmitt triggered.
7	7	Carry Out	CARRY	Goes low when digit 4 (or 3) MSB goes to 1 or when this digit reaches its maximum count, and stays low until digit 4 (or 3) MSB changes to Ø or its minimum count.
8-14	8-14	Digit 1 output	1A-1G	Digit 1 seven segment outputs.
—	15-17 31-34	Digit 4 Output	4A-4G	Digit 4 seven segment outputs.
15, 16 18, 19 22, 23 26	18, 19 22, 23 26, 27 30	Digit 3 Output	3A-3G	Digit 3 seven segment outputs.
—	20	Annunciator 4	AN4	Annunciator 4 output.
17, 24 25	21, 28 29	Annunciator 1, 2 & 3	AN1-AN3	Annunciators 1, 2 & 3 outputs.
20	24	Ground	V_{SS}	Negative logic voltage reference, common display voltage reference input.
21	25	Display Power	V_{EE}	Negative display supply input.
27-33	35-41	Digit 2 Output	2A-2G	Digit 2 seven segment outputs.
34	42	Master Reset	MR	Active low input, same function as software Master Reset.
35-39	43-47	Data Input/Output	DØ-D4	3-state data input or output and instruction code input.

Instruction Set

D4-D0	RD/WR Operation	# Cycles	Symbol	Name	Function
00000	WR	1	RSTC	Reset Counter	Resets all counter stages to zero.
00001	WR	1	RSTD	Reset Display	Resets all digit display registers to Ø.
00010	WR	1	MR	Master Reset	Resets all counter registers, digit display registers, annunciator register, sets data address to CR1 and forces PM1. Sets all conditions true indicated by *.
00011	WR	1	RSTA	Reset annunciators	Resets annunciator register to all Ø's.
00100	WR	1	CCD	Counter Clock Disable	Disables clock input to Counter/Timer.
00101	WR	1	*CCE	Counter Clock Enable	Enables clock input to Counter/Timer.
00110	WR	1	*UBLK	Unblank Display	Unblanks display.

Instruction Set, Cont.

D4-D0	RD/WR Operation	# Cycles	Symbol	Name	Function
00111	WR	1	BLK	Blank Display	Blanks display.
01000	WR	1	LZBD	Leading Zero Blank Disable	Allows display of leading zeroes.
01001	WR	1	*LZBE	Leading Zero Blank Enable	Prevents display of leading zeroes.
01010	WR/ RD-WR	2	ANR	Annunciator Register	Sets data pointer for either a Read or Write operation to the Annunciator Register.
01011	WR	1	CHEX	Count Hex Mode	Allows Counter to count in Hex format, 0000-FFFF.
01100	WR	1	CMS	Count Min/Sec	Allows Counter to count in minutes/seconds format 0000-5959.
01101	WR	1	*CDEC	Count Decimal Mode	Allows Counter to count in decimal format, 0000-9999.
01110	WR	1	CHS	Count Seconds/ Hundredths of Seconds	Allows Counter to count in seconds and hundreds of seconds format, 0000-5999.
01111	WR	1	CHM	Count Hours/ Minutes	Allows Counter to count in hours/minutes format, 0000-1259.
10000	WR	—	—	—	No Function
10001	WR	—	—	—	No Function
10010	WR	—	—	—	No Function
10011	WR	—	—	—	No Function
10100	WR	1	VDR	View Display Registers	Enables the contents of the Digit Display Registers to be displayed.
10101	WR	1	*VCR	View Counter Registers	Enables the contents of the Counter Registers to be displayed.
10110	WR	1	INC	Increment Counter	Increases counter by one count.
10111	WR	1	XFER	Transfer Count to Display	Transfers the contents of the Counter Registers to Digit Display Registers.
11000	WR/ RD-WR	2	DR1	Display Register One	Sets data pointer for either a Read or Write operation to Digit Display Register One.
11001	WR/ RD-WR	2	DR2	Display Register Two	Sets data pointer for either a Read or Write operation to Digit Display Register Two.
11010	WR/ RD-WR	2	DR3	Display Register Three	Sets data pointer for either a Read or Write operation to Digit Display Register Three.
11011	WR/ RD-WR	2	DR4	Display Register Four	Sets data pointer for either a Read or Write operation to Digit Display Register Four.
11100	WR/ RD-WR	2	CR1	Counter Register One	Sets data pointer for either a Read or Write operation to Counter Register One.
11101	WR/ RD-WR	2	CR2	Counter Register Two	Sets data pointer for either a Read or Write operation to Counter Register Two.
11110	WR/ RD-WR	2	CR3	Counter Register Three	Sets data pointer for either a Read or Write operation to Counter Register Three.
11111	WR/ RD-WR	2	CR4	Counter Register Four	Sets data pointer for either a Read or Write operation to Counter Register Four.

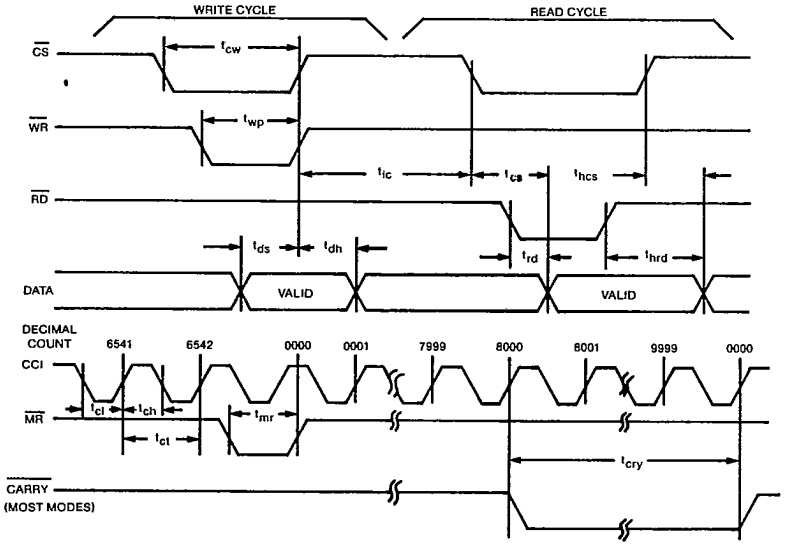
NOTES:
*True on Master Reset or Power Up.
WR/RD-WR indicates a Write cycle followed by a Read or Write cycle.

AC Electrical Characteristics

V_{DD} = 5V, V_{EE} = -30V, V_{SS} = 0V, TA = 25° C (Unless Otherwise Noted)

Symbol	Parameter	Min.	Max.	Units
t_{WP}	Write Pulse Width	250	—	nS
t_{CW}	Chip Select to End of Write	250	—	nS
t_{DS}	Data Setup Time	200	—	nS
t_{DH}	Data Hold Time	50	—	nS
t_{RD}	Read Time to Data Valid	—	200	nS
t_{CS}	Chip Select Access Time	—	200	nS
t_{HCS}	Output Hold from Chip Select	—	100	nS
t_{HRD}	Output Hold from Read	—	100	nS
t_{IC}	Inter-cycle Time	2	—	μS
t_R, t_F	Clock Rise, Fall Time	—	1	μS
t_{CH}	Clock Pulse Width High	50	—	nS
t_{CL}	Clock Pulse Width Low	50	—	nS
t_{MR}	Master Reset Pulse Width	200	—	nS

Timing Characteristics



Functional Description

Programming Sequence

The HI-8030 devices use a two-step Read/Write format for loading or retrieving data and a single step format for writing control instructions. To write a control instruction, a Write cycle is executed with the appropriate code. If data is to be written into the display or counter, the desired pointer instruction is first loaded using a normal Write cycle. The code word is recognized as requiring a data I/O function, and the data address is internally set for the destination of the data. The next immediate Write cycle will load the data on D_0 - D_3 into the location indicated by the address that was set by the pointer instruction.

A Read operation is performed in the same manner. First the pointer instruction is written; then a Read cycle is used to obtain data from this location. Each Read cycle need not be preceeded by a pointer instruction, unless the location is changed.

Master Reset

A low logic level on MR input performs the same function as a software Master Reset instruction. A Master Reset is automatically performed on a power up.

The internal control characteristics are set on power up or Master Reset so that the device can be used as a stand-alone counter with direct display output without any need for an external programming input. The Counter Clock input is enabled. The display output is unblanked. Leading zeroes are blanked. The Counter is set to count in the decimal format, and the contents of the counter registers are transparent to the display outputs.

Backplane Oscillator

The on-chip oscillator is designed to be very stable over a broad temperature range. The frequency variation over temperature is dependent on the temperature stability of the external capacitor and resistor. The actual backplane frequency in this case is derived from the formula:

$$f_{BP} = \frac{.357}{R_1 C_1}$$

A combination of C_X = .0033 F and R_X = 1 Meg. Ohm will produce the commonly used backplane frequency of approximately 100Hz.

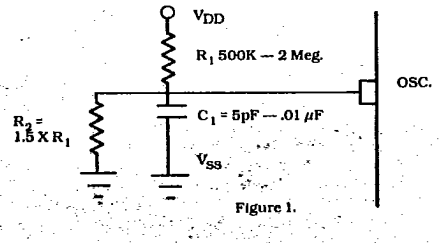


Figure 1.

Cascading Displays

The backplane output can be disabled by connecting the oscillator input to V_{DD}. This allows the segment outputs to be synchronized directly to a signal input at the Backplane (BP) Pin. Several slave devices may be cascaded to the active backplane output of one device or may be derived from an external source.

Cascading Counters

Several counter stages can be cascaded together by connecting the CARRY output from one stage to the Counter Clock Input (CCI) of the next stage. CARRY will go low when the MSB of the most significant digit changes to 1 or when this digit reaches its maximum count. For example, if the counter is programmed to count in Hex, the CARRY will go low when the most significant digit changed from 7 to 8. The CARRY output will go high again when it changed from F to Ø. This principle is also true of any other programmed count format.

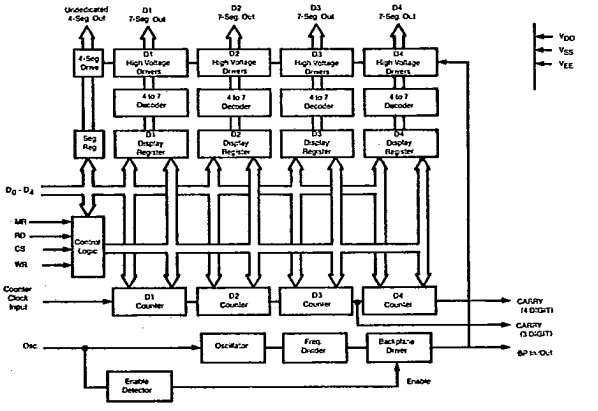
Timer Operation

The counter registers can be used as a programmable counter. This can be easily done by subtracting the desired number of counts from the count at which CARRY goes low, and loading this number into the counter register.

Leading Zero Blanking

When cascading devices, the count status of each device will need to be monitored by the system μP control in order to ensure proper leading zero blanking. When any counter "rolls over" the leading zero blank status of that device will not change. The leading zero blank should be disabled on lower magnitude devices which have "rolled over" so that the low order zeroes will not be blanked. High order devices will display their low order Ø even with leading zero blanking activated. In this case the high order devices must be given a Display Blank instruction to read properly.

Block Diagram



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