19-0795; Rev 0; 4/07

EVALUATION KIT AVAILABLE

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

General Description

The MAX109, 2.2Gsps, 8-bit, analog-to-digital converter (ADC) enables the accurate digitizing of analog signals with frequencies up to 2.5GHz. Fabricated on an advanced SiGe process, the MAX109 integrates a high-performance track/hold (T/H) amplifier, a quantizer, and a 1:4 demultiplexer on a single monolithic die. The MAX109 also features adjustable offset, full-scale voltage (via REFIN), and sampling instance allowing multiple ADCs to be interleaved in time.

The innovative design of the internal T/H amplifier, which has a wide 2.8GHz full-power bandwidth, enables a flat-frequency response through the second Nyquist region. This results in excellent ENOB performance of 6.9 bits. A fully differential comparator design and decoding circuitry reduce out-of-sequence code errors (thermometer bubbles or sparkle codes) and provide excellent metastability performance (10^{14} clock cycles). This design guarantees no missing codes.

The analog input is designed for both differential and single-ended use with a $500mV_{P-P}$ input-voltage range. The output data is in standard LVDS format, and is demultiplexed by an internal 1:4 demultiplexer. The LVDS outputs operate from a supply-voltage range of 3V to 3.6V for compatibility with single 3V-reference systems. Control inputs are provided for interleaving additional MAX109 devices to increase the effective system-sampling rate.

The MAX109 is offered in a 256-pin Super Ball-Grid Array (SBGA) package and is specified over the extended industrial temperature range (-40°C to +85°C).

Applications

Radar Warning Receivers (RWR)

Light Detection and Ranging (LIDAR)

Digital RF/IF Signal Processing

Electronic Warfare (EW) Systems

High-Speed Data-Acquisition Systems

Digital Oscilloscopes

High-Energy Physics Instrumentation

ATE Systems

Features

- **Ultra-High-Speed, 8-Bit, 2.2Gsps ADC**
- **2.8GHz Full-Power Analog Input Bandwidth**
- **Excellent Signal-to-Noise Performance**
  - **44.6dB SNR at f_{IN} = 300MHz**
  - **44dB SNR at f_{IN} = 1600MHz**
- **Superior Dynamic Range at High-IF**
  - **61.7dBc SFDR at f_{IN} = 300MHz**
  - **50.3dBc SFDR at f_{IN} = 1600MHz**
  - **-60dBc IM3 at f_{IN1} = 1590MHz and f_{IN2} = 1610MHz**
- **$500mV_{P-P}$ Differential Analog Inputs**
- **6.8W Typical Power Including the Demultiplexer**
- **Adjustable Range for Offset, Full-Scale, and Sampling Instance**
- **50Ω Differential Analog Inputs**
- **1:4 Demultiplexed LVDS Outputs**
- **Interfaces Directly to Common FPGAs with DDR and QDR Modes**

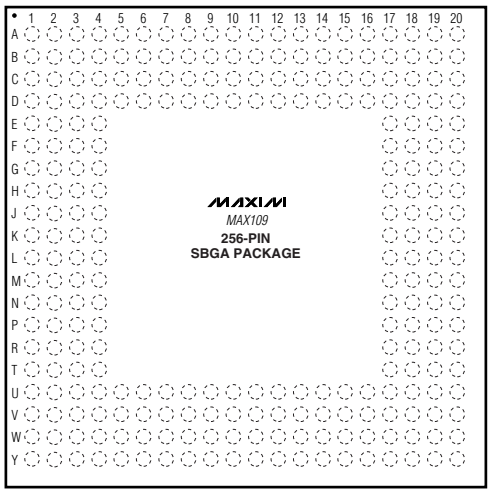
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX109EHF-D	-40°C to +85°C	256 SBGA	H256-1

D = Dry pack.

Pin Configuration

TOP VIEW



256-PIN SUPER BALL-GRID ARRAY

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

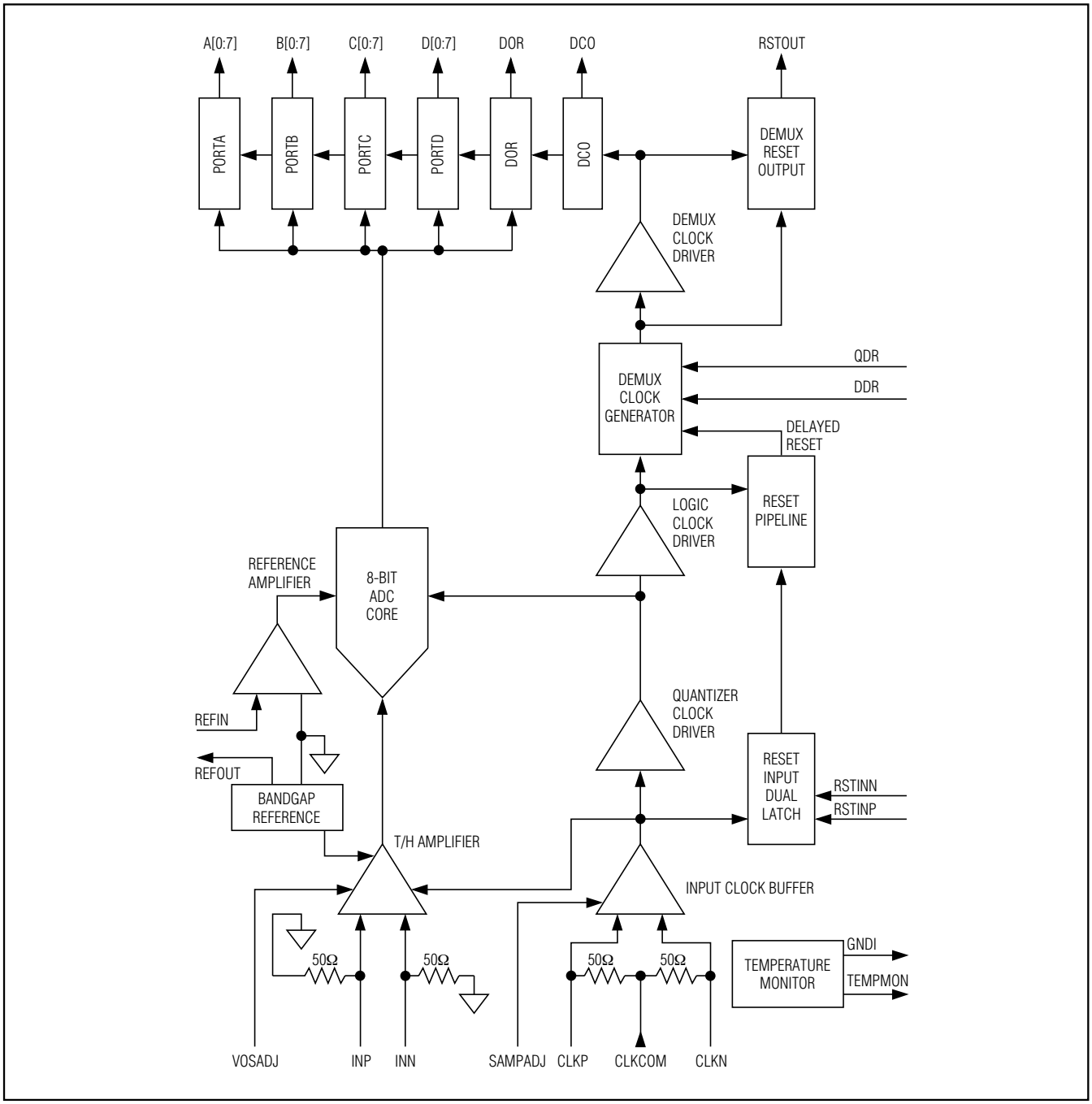


Figure 1. Functional Diagram of the MAX109

ABSOLUTE MAXIMUM RATINGS

$V_{CC}A$ to GNDA ..... -0.3V to +6V
$V_{CC}D$ to GNDD ..... -0.3V to +6V
$V_{CC}I$ to GNDI ..... -0.3V to +6V
$V_{CC}O$ to GNDO ..... -0.3V to +3.9V
V_{EE} to GNDI ..... -6V to +0.3V
Between Grounds (GNDA, GNDI, GNDO, GNDD, GNDR) ..... -0.3V to +0.3V
$V_{CC}A$ to $V_{CC}D$ ..... -0.3V to +0.3V
$V_{CC}A$ to $V_{CC}I$ ..... -0.3V to +0.3V
Differential Voltage between INP and INN ..... ±1V
INP, INN to GNDI ..... ±1V
Differential Voltage between CLKP and CLKN..... ±3V
CLKP, CLKN, CLKCOM to GNDI ..... -3V to +1V
Digital LVDS Outputs to GNDO ..... -0.3V to ($V_{CC}O$ - 0.3V)
REFIN, REFOUT to GNDR .....-0.3V to ($V_{CC}I$ + 0.3V)
REFOUT Current .....-100µA to +5mA
RSTINP, RSTINN to GNDA .....-0.3V to ($V_{CC}O$ + 0.3V)
RSTOUTP, RSTOUTN to GNDO .....-0.3V to ($V_{CC}O$ + 0.3V)
VOSADJ, SAMPADJ, TEMPMON to GNDI.....-0.3V to ($V_{CC}I$ + 0.3V)
PRN, DDR, QDR to GNDD.....-0.3V to ($V_{CC}D$ + 0.3V)
DELGATE0, DELGATE1 to GNDA .....-0.3V to ($V_{CC}A$ + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
256-Ball SBGA (derate 74.1mW/°C above +70°C for a multilayer board) 5925.9mW
Operating Temperature Range
MAX109EHF .....-40°C to +85°C
Thermal Resistance θ_{JA} (Note 1) .....3°C/W
Operating Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C

Note 1: Thermal resistance is based on a 5in x 5in multilayer board. The data sheet assumes a thermal environment of 3°C/W. Thermal resistance may be different depending on airflow and heatsink cooling capabilities.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDO = GNDD = GNDR = 0V, VOSADJ = SAMPADJ = open, digital output pins differential R_L = 100Ω. Specifications ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution	RES		8			Bits
Integral Nonlinearity (Note 2)	INL	(Note 8)	-0.8	±0.25	+0.8	LSB
Differential Nonlinearity (Note 2)	DNL	Guaranteed no missing codes, T_A = +25°C (Note 8)	-0.8	±0.25	+0.8	LSB
Transfer Curve Offset (Note 2)	V_{OS}	VOSADJ control input open (Note 8)	-5.5	0	+5.5	LSB
ANALOG INPUTS (INN, INP)						
Common-Mode Input-Voltage Range	V_{CM}	Signal and offset with respect to GNDI		±1		V
Common-Mode Rejection Ratio (Note 3)	CMRR			50		dB
Full-Scale Input Range (Note 2)	V_{FS}	V_{REFIN} = 2.5V	470	500	535	mV_{P-P}
Input Resistance	R_{IN}		45	50	55	Ω
Input Resistance Temperature Coefficient	TC_R			150		ppm/°C
VOS ADJUST CONTROL INPUT (VOSADJ)						
Input Resistance (Note 4)	R_{VOSADJ}		25	50	75	kΩ
Input Offset Voltage	V_{OS}	VOSADJ = 0V		-20		mV
		VOSADJ = 2.5V		20		mV
SAMPLE ADJUST CONTROL INPUT (SAMPADJ)						
Input Resistance	$R_{SAMPADJ}$		25	50	75	kΩ
Aperture Time Adjust Range	t_{AD}	SAMPADJ = 0 to 2.5V		30		ps

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDO = GNDD = GNDR = 0V, VOSADJ = SAMPADJ = open, digital output pins differential R_L = 100Ω. Specifications ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT AND OUTPUT (REFIN, REFOUT)						
Reference Output Voltage	REFOUT		2.460	2.500	2.525	V
Reference Output Load Regulation	ΔREFOUT	0 < I_{SOURCE} < 2.5mA		< 7.5		mV
Reference Input Voltage	REFIN			2.500 ±0.25		V
Reference Input Resistance	R_{REFIN}		4	5		kΩ
CLOCK INPUTS (CLKP, CLKN)						
Clock Input Amplitude		Peak-to-peak differential (Figure 13b)		200 to 2000		mV
Clock Input Common-Mode Range		Signal and offset referenced to CLKCOM		-2 to +2		V
Clock Input Resistance	R_{CLK}	CLKP and CLKN to CLKCOM	45	50	55	Ω
Input Resistance Temperature Coefficient	TC_R			150		ppm/°C
CMOS CONTROL INPUTS (DDR, QDR, PRN, DELGATE0, DELGATE1)						
High-Level Input Voltage	V_{IH}	Threshold voltage = 1.2V	1.4		3.3	V
Low-Level Input Voltage	V_{IL}	Threshold voltage = 1.2V			0.8	V
High-Level Input Current	I_{IH}	V_{IH} = 3.3V			50	µA
Low-Level Input Current	I_{IL}	V_{IL} = 0V	-50			µA
LVDS INPUTS (RSTINP, RSTINN)						
Differential Input High Voltage			0.2			V
Differential Input Low Voltage					-0.2	V
Minimum Common-Mode Input Voltage				1		V
Maximum Common-Mode Input Voltage				$V_{CC}O$ - 0.15		V
TEMPERATURE MEASUREMENT OUTPUT (TEMPMON)						
Temperature Measurement Accuracy		T (°C) = [($V_{TEMPMON}$ - V_{GNDI}) x 1303.5] - 371		±7		°C
Output Resistance		Measured between TEMPMON and GNDI		0.725		kΩ
LVDS OUTPUTS (PortA, PortB, PortC, PortD, DORP, DORN, DCOP, DCON, RSTOUTP, RSTOUTN) (Note 9)						
Differential Output Voltage	V_{OD}	R_{LOAD} = 100Ω	250		400	mV
Output Offset Voltage	V_{OS}	R_{LOAD} = 100Ω	1.10		1.28	V

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDO = GNDD = GNDR = 0V, VOSADJ = SAMPADJ = open, digital output pins differential R_L = 100Ω. Specifications ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Current	$IV_{CC}A$			556	744	mA
Positive Input Supply Current	$IV_{CC}I$			125	168	mA
Negative Input Supply Current	$IIV_{EE}I$			181	240	mA
Digital Supply Current	$IV_{CC}D$			291	408	mA
Output Supply Current	$IV_{CC}O$			222	300	mA
Power Dissipation	P_{DISS}			6.50	8.79	W
Positive Power-Supply Rejection Ratio	PSRRP	(Note 5)		50		dB
Negative Power-Supply Rejection Ratio	PSRRN	V_{EE} = -5.25V to -4.75V		50		dB

AC ELECTRICAL CHARACTERISTICS

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDD = GNDO = GNDR = 0V, f_{CLK} = 2.2Gsps, analog input amplitude at -1dBFS differential, clock input amplitude 400mV_{P-P} differential, digital output pins differential R_L = 100Ω. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Analog Input Full-Power Bandwidth (Note 6)	BW_{-3dB}			2.8		GHz
Gain Flatness	GF	1100MHz to 2200MHz		±0.3		dB
DYNAMIC SPECIFICATIONS						
Signal-to-Noise Ratio	SNR_{300}	f_{IN} = 300MHz, f_{CLK} = 2.2Gsps		44.6		dB
	SNR_{1000}	f_{IN} = 1000MHz, f_{CLK} = 2.2Gsps (Note 8)	43.6	44.5		
	SNR_{1600}	f_{IN} = 1600MHz, f_{CLK} = 2.2Gsps (Note 8)	42.2	44.0		
	SNR_{2500}	f_{IN} = 2500MHz, f_{CLK} = 2.2Gsps		42.9		
	SNR_{500}	f_{IN} = 500MHz, f_{CLK} = 2.5Gsps		44.4		
	SNR_{1600}	f_{IN} = 1600MHz, f_{CLK} = 2.5Gsps		44.0		
Total Harmonic Distortion (Note 7)	THD_{300}	f_{IN} = 300MHz, f_{CLK} = 2.2Gsps		-55.6		dBc
	THD_{1000}	f_{IN} = 1000MHz, f_{CLK} = 2.2Gsps (Note 8)		-48.5	-42.5	
	THD_{1600}	f_{IN} = 1600MHz, f_{CLK} = 2.2Gsps (Note 8)		-46.6	-39.6	
	THD_{2500}	f_{IN} = 2500MHz, f_{CLK} = 2.2Gsps		-43.7		
	THD_{500}	f_{IN} = 500MHz, f_{CLK} = 2.5Gsps		-49.0		
	THD_{1600}	f_{IN} = 1600MHz, f_{CLK} = 2.5Gsps		-43.1		

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDD = GNDO = GNDR = 0V, f_{CLK} = 2.2Gsps, analog input amplitude at -1dBFS differential, clock input amplitude 400mV_{P-P} differential, digital output pins differential R_L = 100Ω. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spurious Free Dynamic Range	$SFDR_{300}$	f_{IN} = 300MHz, f_{CLK} = 2.2Gsps		61.7		dBc
	$SFDR_{1000}$	f_{IN} = 1000MHz, f_{CLK} = 2.2Gsps (Note 8)	44.4	51.1		
	$SFDR_{1600}$	f_{IN} = 1600MHz, f_{CLK} = 2.2Gsps (Note 8)	43.7	50.3		
	$SFDR_{2500}$	f_{IN} = 2500MHz, f_{CLK} = 2.2Gsps		45.0		
	$SFDR_{500}$	f_{IN} = 500MHz, f_{CLK} = 2.5Gsps		53.7		
	$SFDR_{1600}$	f_{IN} = 1600MHz, f_{CLK} = 2.5Gsps		44.6		
Signal-to-Noise-Plus-Distortion Ratio	$SINAD_{300}$	f_{IN} = 300MHz, f_{CLK} = 2.2Gsps		44.1		dB
	$SINAD_{1000}$	f_{IN} = 1000MHz, f_{CLK} = 2.2Gsps (Note 8)	40.4	43.1		
	$SINAD_{1600}$	f_{IN} = 1600MHz, f_{CLK} = 2.2Gsps (Note 8)	37.9	42.1		
	$SINAD_{2500}$	f_{IN} = 2500MHz, f_{CLK} = 2.2Gsps		40.1		
	$SINAD_{500}$	f_{IN} = 500MHz, f_{CLK} = 2.5Gsps		43.1		
	$SINAD_{1600}$	f_{IN} = 1600MHz, f_{CLK} = 2.5Gsps		40.5		
Third-Order Intermodulation	IM3	f_{IN1} = 1590MHz, f_{IN2} = 1610MHz at -7dBFS		-60		dBc
Metastability Probability				10^{-14}		
TIMING CHARACTERISTICS						
Maximum Sample Rate	$f_{CLK(MAX)}$		2.2			Gsps
Clock Pulse-Width Low	t_{PWL}	t_{CLK} = t_{PWL} + t_{PWH} (Note 8)	180			ps
Clock Pulse-Width High	t_{PWH}	t_{CLK} = t_{PWL} + t_{PWH} (Note 8)	180			ps
Aperture Delay	t_{AD}			200		ps
Aperture Jitter	t_{AJ}			0.2		ps
Reset Input Data Setup Time	t_{SU}	(Note 8)	300			ps
Reset Input Data Hold Time	t_{HD}	(Note 8)	250			ps
CLK-to-DCO Propagation Delay	t_{PD1}	DCO = f_{CLK} / 4, CLK fall to DCO rise time		1.6		ns
	t_{PD1DDR}	DCO = f_{CLK} / 8, DDR mode, CLK fall to DCO rise time		1.6		
	t_{PD1QDR}	DCO = f_{CLK} / 16, QDR mode, CLK fall to DCO rise time		1.6		
DCO-to-Data Propagation Delay	t_{PD2}	DCO = f_{CLK} / 4, DCO rise to data transition (Note 8)	-520		+520	ps
	t_{PD2DDR}	DCO = f_{CLK} / 8, DDR mode, DCO rise to data transition (Note 8)	-520 + $2t_{CLK}$	$2t_{CLK}$	520 + $2t_{CLK}$	
	t_{PD2QDR}	DCO = f_{CLK} / 16, QDR mode, DCO rise to data transition (Note 8)	-520 + $2t_{CLK}$	$2t_{CLK}$	520 + $2t_{CLK}$	
DCO Duty Cycle		Clock mode independent		45 to 55		%

AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDD = GNDO = GNDR = 0V, f_{CLK} = 2.2Gsps, analog input amplitude at -1dBFS differential, clock input amplitude 400mV_{P-P} differential, digital output pins differential R_L = 100Ω. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS Output Rise Time	t_{RDATA}	20% to 80%, C_L < 2pF		500		ps
LVDS Output Fall Time	t_{FDATA}	20% to 80%, C_L < 2pF		500		ps
LVDS Differential Skew	t_{SKEW1}	Any two LVDS output signals, except DCO		<100		ps
PortD Data Pipeline Delay	t_{PDD}			7.5		Clock Cycles
PortC Data Pipeline Delay	t_{PDC}			8.5		Clock Cycles
PortB Data Pipeline Delay	t_{PDB}			9.5		Clock Cycles
PortA Data Pipeline Delay	t_{PDA}			10.5		Clock Cycles

Note 2: Static linearity and offset parameters are computed from a *best-fit* straight line through the code transition points. The full-scale range (FSR) is defined as 255 x slope of the line where the slope of the line is determined by the end-point code transitions. When the analog input voltage exceeds positive FSR, the output code is 11111111; when the analog input voltage is beyond the negative FSR, the output code is 00000000.

Note 3: Common-mode rejection ratio is defined as the ratio of the change in the transfer-curve offset voltage to the change in the common-mode voltage, expressed in dB.

Note 4: The offset-adjust control input is tied to an internal 1.25V reference level through a resistor.

Note 5: Measured with the positive supplies tied to the same potential, $V_{CC}A$ = $V_{CC}D$ = $V_{CC}I$. V_{CC} varies from 4.75V to 5.25V.

Note 6: To achieve 2.8GHz full-power bandwidth, careful board layout techniques are required.

Note 7: The total harmonic distortion (THD) is computed from the second through the 15th harmonics.

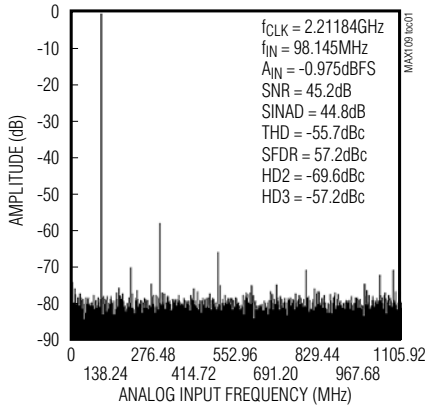
Note 8: Guaranteed by design and characterization.

Note 9: RSTOUTP/RSTOUTN are tested for functionality.

Typical Operating Characteristics

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDD = GNDO = GNDR = 0V, f_{CLK} = 2.21184Gsps, analog input amplitude at -1dBFS differential, clock input amplitude 10dBm differential, digital output pins differential R_L = 100Ω. Typical values are at T_J = +105°C, unless otherwise noted.)

FFT PLOT (16,384-POINT DATA RECORD)



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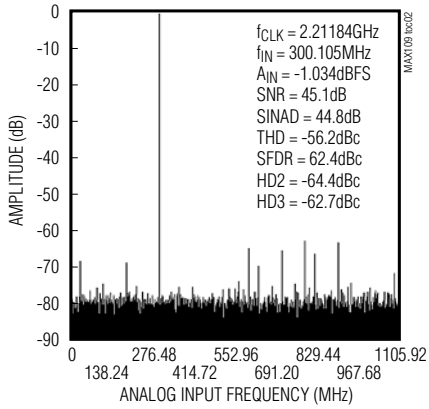

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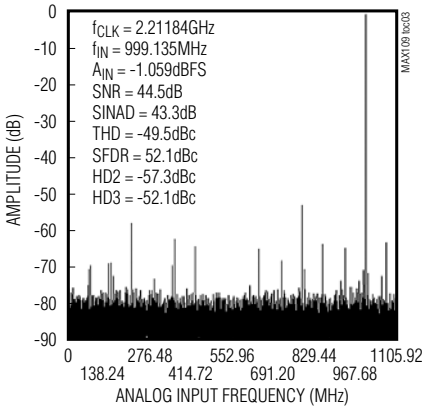

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

Typical Operating Characteristics (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDD = GNDO = GNDR = 0V, f_{CLK} = 2.21184Gsps, analog input amplitude at -1dBFS differential, clock input amplitude 10dBm differential, digital output pins differential R_L = 100Ω. Typical values are at T_J = +105°C, unless otherwise noted.)

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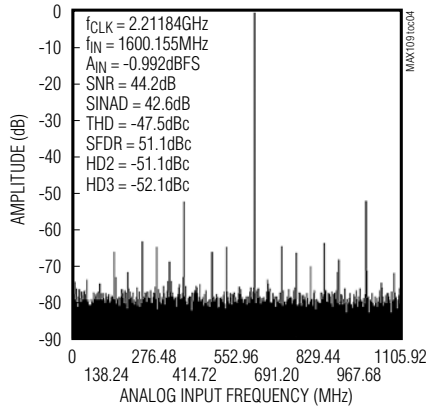
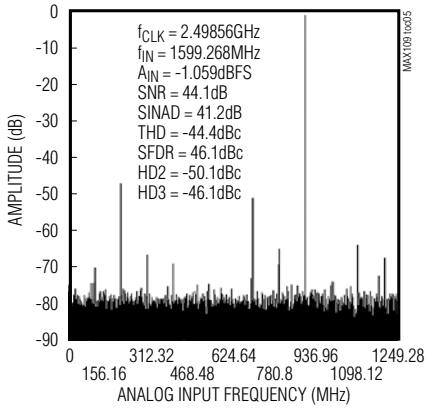
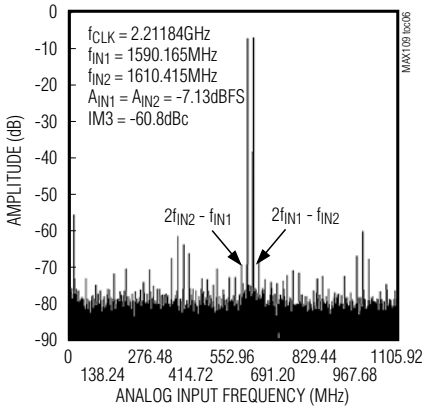


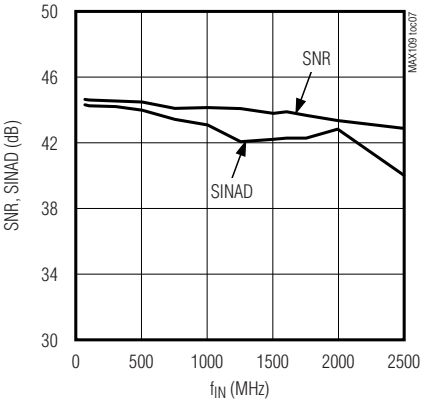
FFT PLOT (16,384-POINT DATA RECORD)



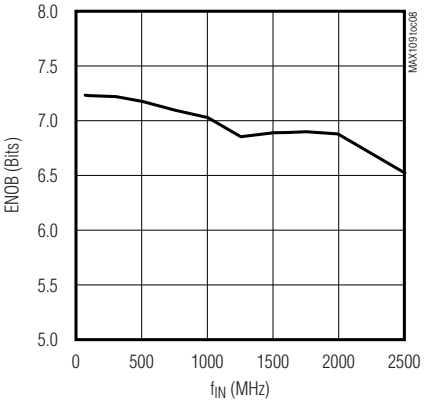
TTIMD PLOT (16,384-POINT DATA RECORD)



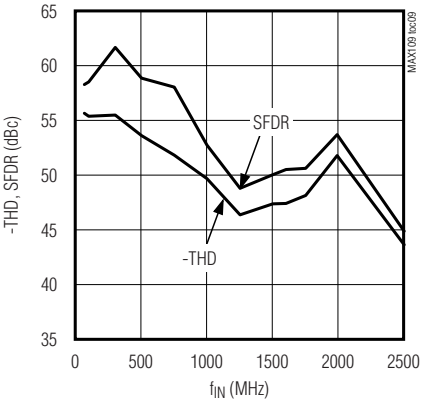
SNR, SINAD vs. ANALOG INPUT FREQUENCY (f_{CLK} = 2.21184Gsps, A_{IN} = -1dBFS)



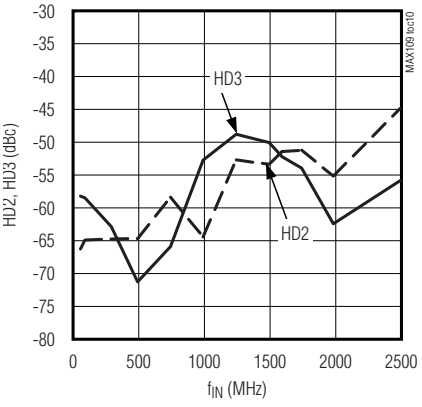
ENOB vs. ANALOG INPUT FREQUENCY (f_{CLK} = 2.21184Gsps, A_{IN} = -1dBFS)



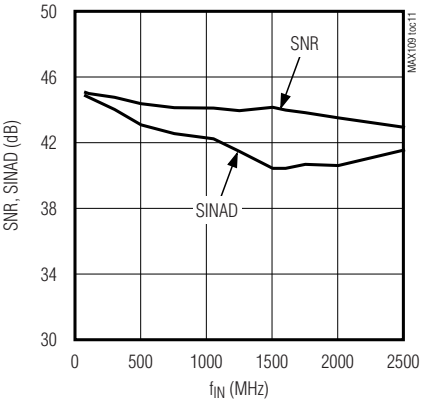
-THD, SFDR vs. ANALOG INPUT FREQUENCY (f_{CLK} = 2.21184Gsps, A_{IN} = -1dBFS)



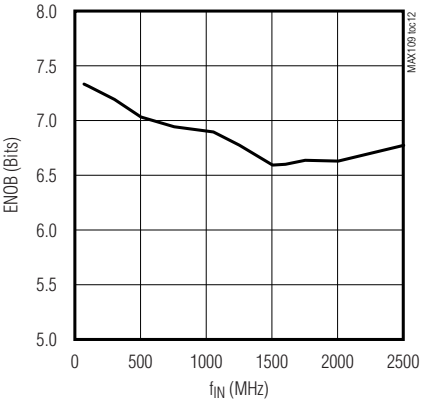
HD2, HD3 vs. ANALOG INPUT FREQUENCY (f_{CLK} = 2.21184Gsps, A_{IN} = -1dBFS)



SNR, SINAD vs. ANALOG INPUT FREQUENCY (f_{CLK} = 2.49856Gsps, A_{IN} = -1dBFS)



ENOB vs. ANALOG INPUT FREQUENCY (f_{CLK} = 2.49856Gsps, A_{IN} = -1dBFS)

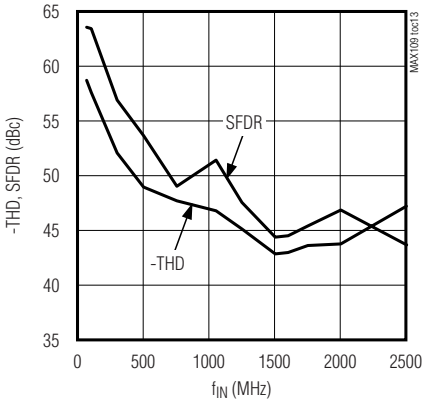


8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

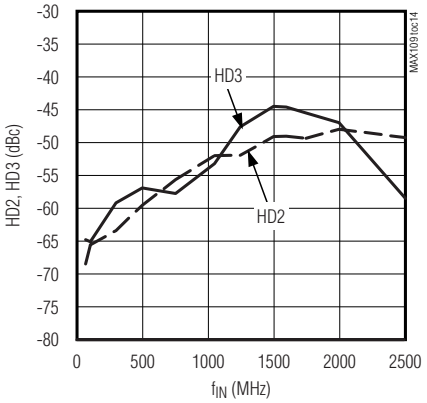
Typical Operating Characteristics (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDD = GNDO = GNDR = 0V, f_{CLK} = 2.21184Gsps, analog input amplitude at -1dBFS differential, clock input amplitude 10dBm differential, digital output pins differential R_L = 100Ω. Typical values are at T_J = +105°C, unless otherwise noted.)

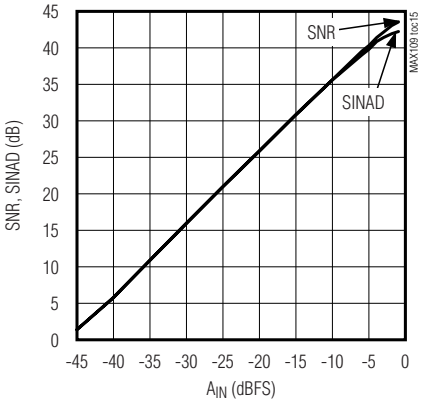
-THD, SFDR vs. ANALOG INPUT FREQUENCY (f_{CLK} = 2.49856Gsps, A_{IN} = -1dBFS)



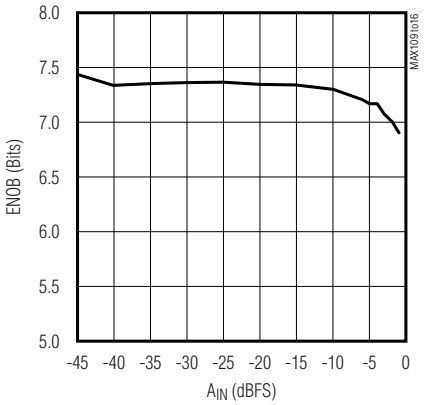
HD2, HD3 vs. ANALOG INPUT FREQUENCY (f_{CLK} = 2.49865Gsps, A_{IN} = -1dBFS)



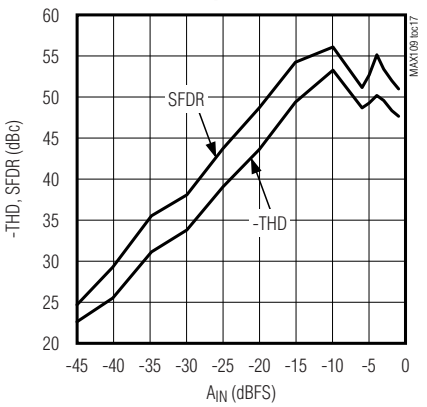
SNR, SINAD vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 2.21184Gsps, f_{IN} = 1600.1550MHz)



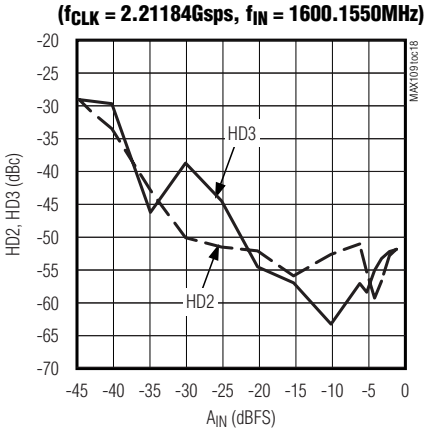
ENOB vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 2.21184Gsps, f_{IN} = 1600.1550MHz)



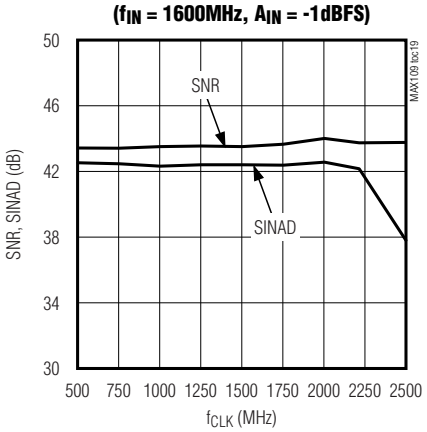
-THD, SFDR vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 2.21184Gsps, f_{IN} = 1600.1550MHz)



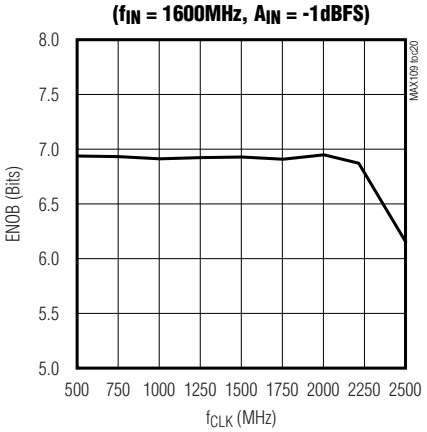
HD2, HD3 vs. ANALOG INPUT AMPLITUDE (f_{CLK} = 2.21184Gsps, f_{IN} = 1600.1550MHz)



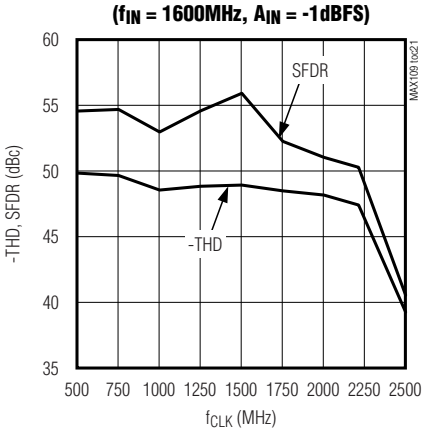
SNR, SINAD vs. CLOCK SPEED (f_{IN} = 1600MHz, A_{IN} = -1dBFS)



ENOB vs. CLOCK SPEED (f_{IN} = 1600MHz, A_{IN} = -1dBFS)



-THD, SFDR vs. CLOCK SPEED (f_{IN} = 1600MHz, A_{IN} = -1dBFS)

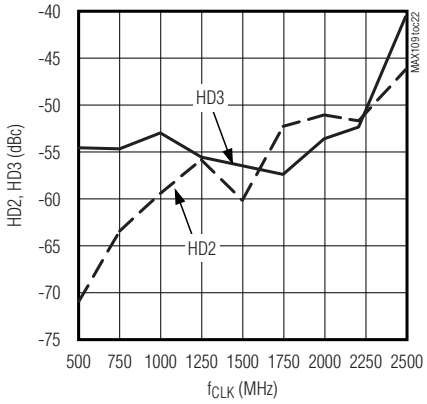


8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

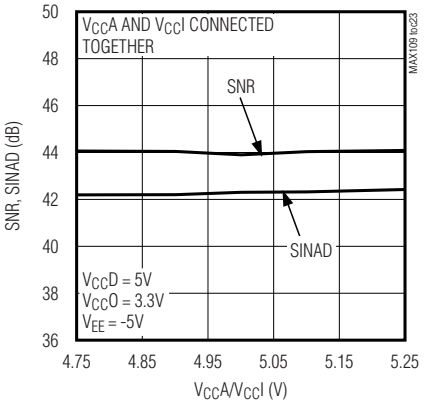
Typical Operating Characteristics (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDD = GNDO = GNDR = 0V, f_{CLK} = 2.21184Gsps, analog input amplitude at -1dBFS differential, clock input amplitude 10dBm differential, digital output pins differential R_L = 100Ω. Typical values are at T_J = +105°C, unless otherwise noted.)

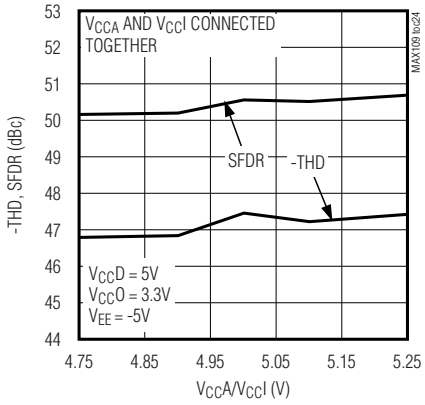
HD2, HD3 vs. CLOCK SPEED (f_{IN} = 1600MHz, A_{IN} = -1dBFS)



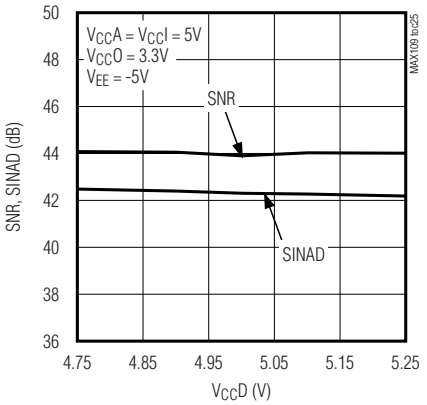
SNR, SINAD vs. $V_{CC}A/V_{CC}I$ (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



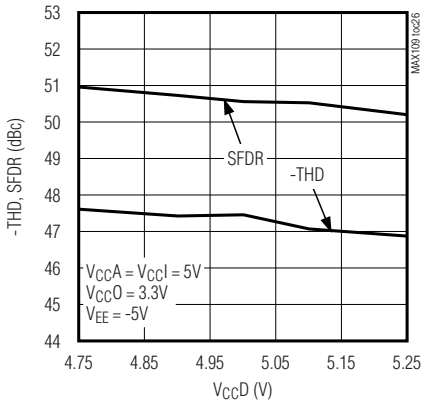
-THD, SFDR vs. $V_{CC}A/V_{CC}I$ (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



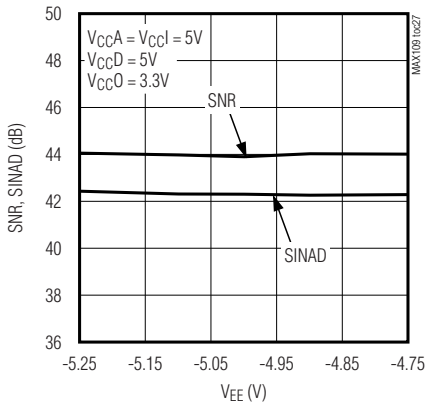
SNR, SINAD vs. $V_{CC}D$ (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



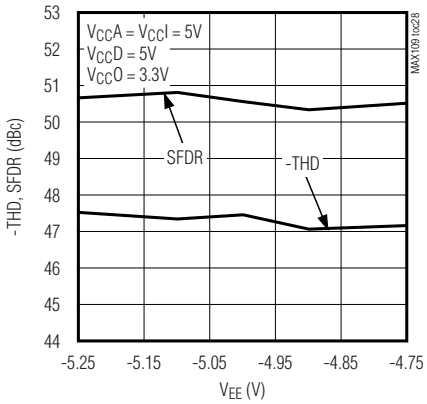
-THD, SFDR vs. $V_{CC}D$ (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



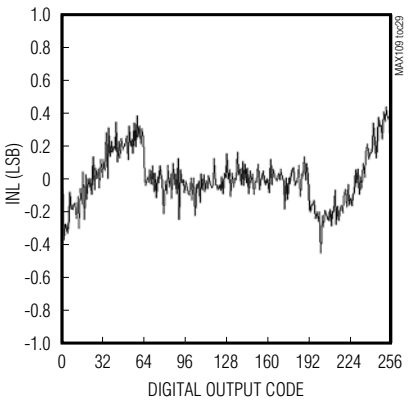
SNR, SINAD vs. V_{EE} (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



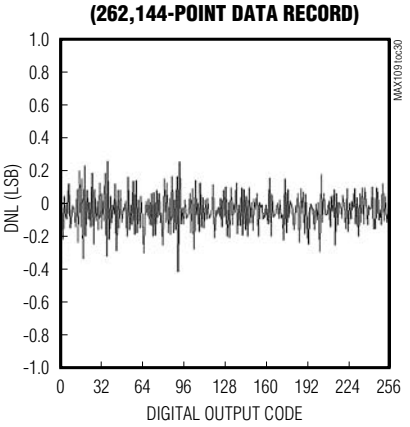
-THD, SFDR vs. V_{EE} (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE (262,144-POINT DATA RECORD)



DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE (262,144-POINT DATA RECORD)

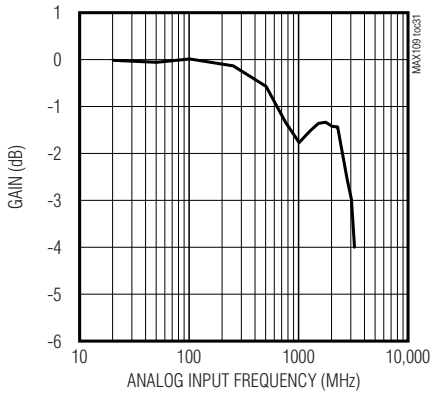


8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

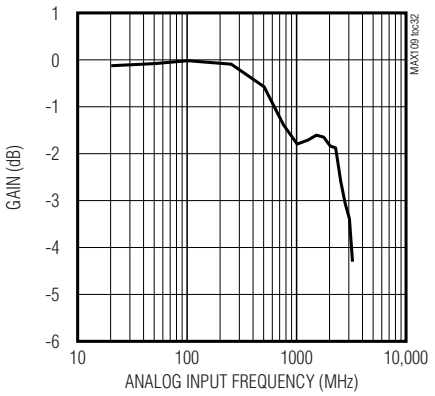
Typical Operating Characteristics (continued)

($V_{CC}A$ = $V_{CC}I$ = $V_{CC}D$ = 5V, $V_{CC}O$ = 3.3V, V_{EE} = -5V, GNDA = GNDI = GNDD = GNDO = GNDR = 0V, f_{CLK} = 2.21184Gsps, analog input amplitude at -1dBFS differential, clock input amplitude 10dBm differential, digital output pins differential R_L = 100Ω. Typical values are at T_J = +105°C, unless otherwise noted.)

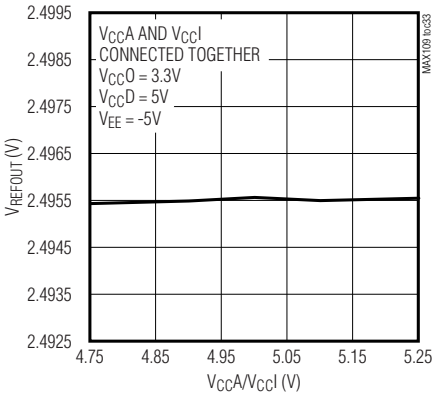
FULL-POWER INPUT BANDWIDTH vs. ANALOG INPUT FREQUENCY (A_{IN} = -1dBFS)



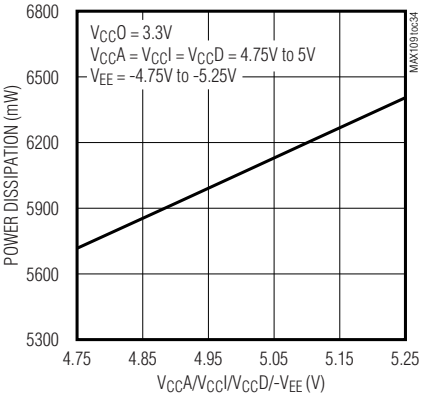
SMALL-SIGNAL INPUT BANDWIDTH vs. ANALOG INPUT FREQUENCY (A_{IN} = -20dBFS)



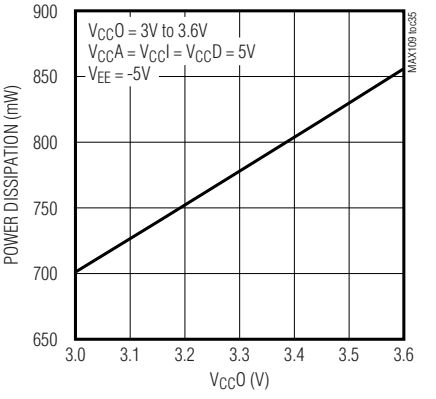
REFERENCE VOLTAGE vs. $V_{CC}A$/$V_{CC}I$



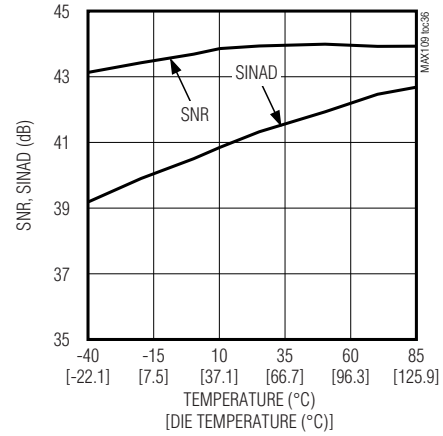
ANALOG/DIGITAL POWER DISSIPATION vs. $V_{CC}A$/$V_{CC}I$/$V_{CC}D$/-V_{EE} (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



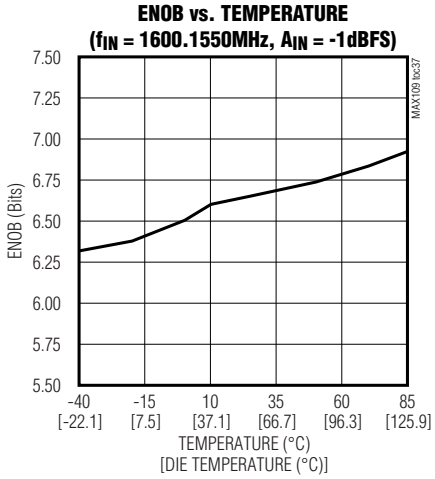
OUTPUT DRIVER POWER DISSIPATION vs. $V_{CC}O$ (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



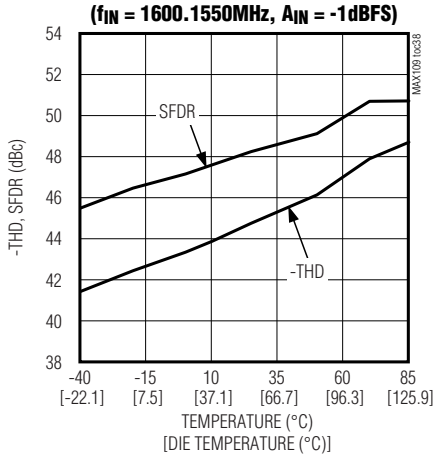
SNR, SINAD vs. TEMPERATURE (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



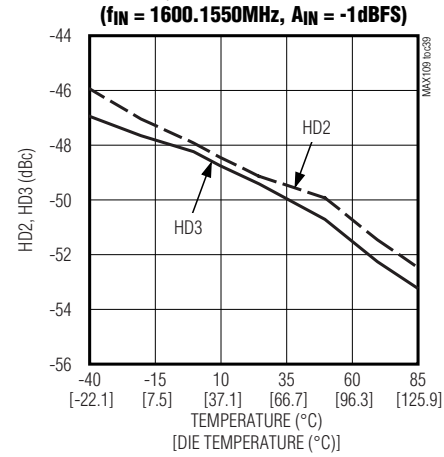
ENOB vs. TEMPERATURE (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



-THD, SFDR vs. TEMPERATURE (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



HD2, HD3 vs. TEMPERATURE (f_{IN} = 1600.1550MHz, A_{IN} = -1dBFS)



8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

Pin Description

PIN	NAME	FUNCTION
A1, A2, B1, B2, C1–C5, D5, L1–L4, U5, V1–V4, W1, W2, Y1, Y2	$V_{CC}O$	LVDS Output Power Supply. Accepts an input-voltage range of 3.3V ±10%.
A3, A4, B3, B4, D1–D4, K1–K4, U1–U4, W3, W4, Y3, Y4	GNDO	LVDS Output Ground. Ground connection for LVDS output drivers.
A9, B9, C10, D10, U10, V10, W10, Y10	$V_{CC}D$	Digital Logic Power Supply. Accepts an input-voltage range of 5V ±5%.
A10, B10, C11, D11, U11, V11, W11, Y11	GNDD	Digital Ground. Ground connection for digital logic circuitry.
A11, A19, B11, B18, C12, C18, D12, D18, E17, U17, V17, W17, Y17, U12, V12, W12, Y12	$V_{CC}A$	Analog Supply Voltage for Comparator Array. Accepts an input-voltage range of 5V ±5%.
A12, A18, B12, B13, B17, C13, C17, D13, D17, U13, U16, V13, V16, W13, W16, Y13, Y16	GNDA	Analog Ground. Ground connection for comparator array.
H17–H20, P17–P20, U15, V15, W15, Y15	$V_{CC}I$	Analog Supply Voltage. Analog power supply (positive rail) for T/H amplifier. Accepts an input-voltage range of 5V ±5%.
E18, F17–F20, J17, J18, J19, N17, N18, N19, T17–T20, U18	V_{EE}	Negative Power Supply. Analog power supply (negative rail) for the T/H amplifier. Accepts an input-voltage range of -5V ±5%.
D19, D20, E19, E20, G17–G20, J20, K17, K18, K19, L17–L20, M17, M18, M19, N20, R17–R20, U14, U19, U20, V14, V19, V20, W14, Y14	GNDI	Analog Ground. Ground connection for the T/H amplifier.

Pin Description (continued)

PIN	NAME	FUNCTION
A14	CLKP	True/Positive Sampling Clock Input. Positive terminal for differential input configuration.
A16	CLKN	Complementary/Negative Sampling Clock Input. Negative terminal for differential input configuration.
A13, A15, A17, B14, B15, B16, C14, C15, C16, D14, D15, D16	CLKCOM	50Ω Clock Termination Return
B20	SAMPADJ	Sampling Point Adjustment Input. Allows the user to adjust the sampling event by applying a voltage between 0 to 2.5V to this input.
B19	DELGATE1	Timing Delay Adjustment. Coarse (MSB) adjustment for the timing between T/H amplifier and quantizer.
C19	DELGATE0	Timing Delay Adjustment. Coarse (LSB) adjustment for the timing between T/H amplifier and quantizer.
Y20	REFIN	Reference Voltage Input. For applications requiring improved gain performance and reference-voltage adjustability, allows the user to utilize the REFIN input by applying a more accurate and adjustable reference source. This input accepts an input-voltage range of 2.5V ±10%.
Y19	REFOUT	Internal Reference Output. Connect to REFIN, if using the internal 2.5V bandgap reference.
V18, W18, Y18	GNDR	Bandgap Reference Ground. Ground connection for the internal bandgap reference and its related circuitry.
M20	INP	True/Positive Analog Input Terminal. For single-ended signals, apply signal to INP and reverse-terminate INN to GNDI with a 50Ω resistor.
K20	INN	Complementary/Negative Analog Input Terminal. For singled-ended signals, reverse-terminate INN to GNDI with a 50Ω resistor and apply the signal directly to INP.
W20	VOSADJ	Analog Voltage Input to Adjust the Converter Offset. This input accepts an input-voltage range of 0 to 2.5V allowing the offset to be adjusted at roughly ±10 LSB.
M4	DORP	True/Positive LVDS Data-Overrange Output Bit. This output flags over- and under-range conditions of the data converter.
M3	DORN	Complementary/Negative LVDS Data-Overrange Output Bit. This output flags over- and under-range conditions on the data converter.
M2	DCOP	True/Positive LVDS Data Clock Output. Synchronize user-supplied data-capture board or data-acquisition system to this clock.
M1	DCON	Complementary/Negative LVDS Data Clock Output. Synchronize user-supplied data-capture board or data-acquisition system to this clock.

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

Pin Description (continued)

PIN	NAME	FUNCTION
Y5	QDR	Quad Data Rate Input (CMOS). Connect to GNDD for the default data rate to be applied. Connect to $V_{CC}D$ to achieve four times the specified data rate.
W5	DDR	Double Data Rate Input (CMOS). Connect to GNDD for the standard data rate to be applied. Connect to $V_{CC}D$ to achieve two times the specified data rate.
V5	PRN	Pseudorandom Number Generator Enable Input (CMOS). When enabled, pseudorandom patterns appear on all four LVDS output ports (PortA, PortB, PortC, and PortD).
D9	RSTINP	True/Positive Reset Input
C9	RSTINN	Complementary/Negative Reset Input
B5	RSTOUTP	True/Positive LVDS Reset Output
A5	RSTOUTN	Complementary LVDS Reset Output
B8	D7P	True/Positive Output Bit D7P, PortD, Bit 7
A8	D7N	Complementary/Negative Output Bit D7N, PortD, Bit 7
B6	D6P	True/Positive Output Bit D6P, PortD, Bit 6
A6	D6N	Complementary/Negative Output Bit D6N, PortD, Bit 6
F2	D5P	True/Positive Output Bit D5P, PortD, Bit 5
F1	D5N	Complementary/Negative Output Bit D5N, PortD, Bit 5
H2	D4P	True/Positive Output Bit D4P, PortD, Bit 4
H1	D4N	Complementary/Negative Output Bit D4N, PortD, Bit 4
N2	D3P	True/Positive Output Bit D3P, PortD, Bit 3
N1	D3N	Complementary/Negative Output Bit D3N, PortD, Bit 3
R2	D2P	True/Positive Output Bit D2P, PortD, Bit 2
R1	D2N	Complementary/Negative Output Bit D2N, PortD, Bit 2
W6	D1P	True/Positive Output Bit D1P, PortD, Bit 1
Y6	D1N	Complementary/Negative Output Bit D1N, PortD, Bit 1
W8	D0P	True/Positive Output Bit D0P, PortD, Bit 0
Y8	D0N	Complementary/Negative Output Bit, D0N, PortD, Bit 0
D8	C7P	True/Positive Output Bit C7P, PortC, Bit 7
C8	C7N	Complementary/Negative Output Bit C7N, PortC, Bit 7
D6	C6P	True/Positive Output Bit C6P, PortC, Bit 6
C6	C6N	Complementary/Negative Output Bit C6N, PortC, Bit 6
F4	C5P	True/Positive Output Bit C5P, PortC, Bit 5
F3	C5N	Complementary/Negative Output Bit C5N, PortC, Bit 5
H4	C4P	True/Positive Output Bit C4P, PortC, Bit 4
H3	C4N	Complementary/Negative Output Bit C4N, PortC, Bit 4
N4	C3P	True/Positive Output Bit C3P, PortC, Bit 3
N3	C3N	Complementary/Negative Output Bit C3N, PortC, Bit 3
R4	C2P	True/Positive Output Bit C2P, PortC, Bit 2

Pin Description (continued)

PIN	NAME	FUNCTION
R3	C2N	Complementary/Negative Output Bit C2N, PortC, Bit 2
U6	C1P	True/Positive Output Bit C1P, PortC, Bit 1
V6	C1N	Complementary/Negative Output Bit C1N, PortC, Bit 1
U8	C0P	True/Positive Output Bit C0P, PortC, Bit 0
V8	C0N	Complementary/Negative Output Bit C0N, PortC, Bit 0
B7	B7P	True/Positive Output Bit B7P, PortB, Bit 7
A7	B7N	Complementary/Negative Output Bit B7N, PortB, Bit 7
E2	B6P	True/Positive Output Bit B6P, PortB, Bit, 6
E1	B6N	Complementary/Negative Output Bit B6N, PortB, Bit 6
G2	B5P	True/Positive Output Bit B5P, PortB, Bit 5
G1	B5N	Complementary/Negative Output Bit B5N, PortB, Bit 5
J2	B4P	True/Positive Output Bit B4P, PortB, Bit 4
J1	B4N	Complementary/Negative Output Bit B4N, PortB, Bit 4
P2	B3P	True/Positive Output Bit B3P, PortB, Bit 3
P1	B3N	Complementary/Negative Output Bit B3N, PortB, Bit 3
T2	B2P	True/Positive Output Bit B2P, PortB, Bit 2
T1	B2N	Complementary/Negative Output Bit B2N, PortB, Bit 2
W7	B1P	True/Positive Output Bit B1P, PortB, Bit 1
Y7	B1N	Complementary/Negative Output Bit B1N, PortB, Bit 1
W9	B0P	True/Positive Output Bit B0P, PortB, Bit 0
Y9	B0N	Complementary/Negative Output Bit B0N, PortB, Bit 0
D7	A7P	True/Positive Output Bit A7P, PortA, Bit 7
C7	A7N	Complementary/Negative Output Bit A7N, PortA, Bit 7
E4	A6P	True/Positive Output Bit A6P, PortA, Bit 6
E3	A6N	Complementary/Negative Output Bit A6N, PortA, Bit 6
G4	A5P	True/Positive Output Bit A5P, PortA, Bit 5
G3	A5N	Complementary/Negative Output Bit A5N, PortA, Bit 5
J4	A4P	True/Positive Output Bit A4P, PortA, Bit 4
J3	A4N	Complementary/Negative Output Bit A4N, PortA, Bit 4
P4	A3P	True/Positive Output Bit A3P, PortA, Bit 3
P3	A3N	Complementary/Negative Output Bit A3N, PortA, Bit 3
T4	A2P	True/Positive Output Bit A2P, PortA, Bit 2
T3	A2N	Complementary/Negative Output Bit A2N, PortA, Bit 2

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

Pin Description (continued)

PIN	NAME	FUNCTION
U7	A1P	True/Positive Output Bit A1P, PortA, Bit 1
V7	A1N	Complementary/Negative Output Bit A1N, PortA, Bit 1
U9	A0P	True/Positive Output Bit A0P, PortA, Bit 0
V9	A0N	Complementary/Negative Output Bit A0N, PortA, Bit 0
W19	TEMPMON	Temperature Monitor Output. Resulting output voltage corresponds to die temperature.
A20, C20	T.P.	Test Point. **Do not connect.**

Detailed Description

The MAX109 is an 8-bit, 2.2Gsps flash analog-to-digital converter (ADC) with an on-chip T/H amplifier and 1:4 demultiplexed high-speed LVDS outputs. The ADC (Figure 1) employs a fully differential 8-bit quantizer and a unique encoding scheme to limit metastable states and ensures no error exceeds a maximum of 1 LSB.

An integrated 1:4 output demultiplexer simplifies interfacing to the part by reducing the output data rate to one-quarter the sampling clock rate. This demultiplexer circuit has integrated reset capabilities that allow multiple MAX109 converters to be time-interleaved to achieve higher effective sampling rates.

When clocked at 2.2Gsps, the MAX109 provides a typical effective number of bits (ENOB) of 6.9 bits at an analog input frequency of 1600MHz. The MAX109 analog input is designed for both differential and single-ended use with a 500mV$_{P-P}$ full-scale input range. In addition, this fast ADC features an on-chip 2.5V precision bandgap reference. In order to improve the MAX109 gain error further, an external reference may be used (see the *Internal Reference* section).

Principle of Operation

The architecture of the MAX109 provides the fastest multibit conversion of all common integrated ADC designs. The key to its architecture is an innovative, high-performance comparator design. The MAX109 quantizer and its encoding logic translate the comparator outputs into a parallel 8-bit output code and pass the binary code on to the 1:4 demultiplexer. Four separate ports (PortA, PortB, PortC, and PortD) output true LVDS data at speeds of up to 550Msps per port (depending on how the demultiplexer section is set on the MAX109).

The ideal transfer function appears in Figure 2.

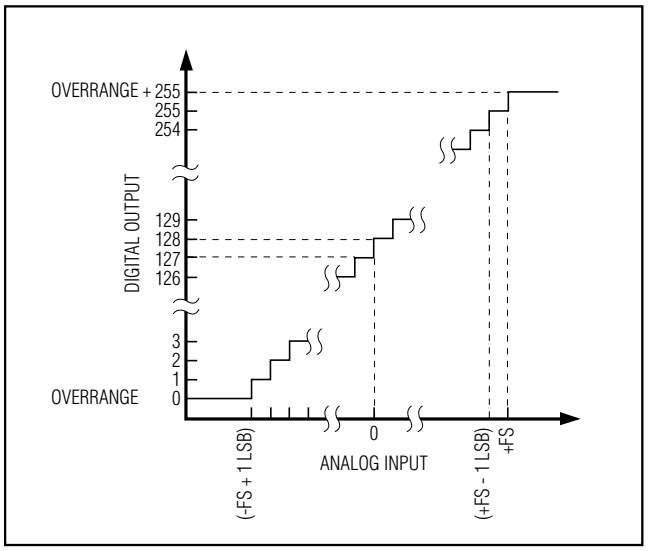


Figure 2. Ideal Transfer Function

On-Chip Track/Hold Amplifier

As with all ADCs, if the input waveform is changing rapidly during conversion, ENOB and signal-to-noise ratio (SNR) specifications will degrade. The MAX109's on-chip, wide-bandwidth (2.8GHz) T/H amplifier reduces this effect and increases the ENOB performance significantly, allowing precise capture of fast-changing analog data at high conversion rates.

The T/H amplifier accepts and buffers both DC- and AC-coupled analog input signals and allows a full-scale signal input range of 500mV$_{P-P}$. The T/H amplifier's differential 50Ω input termination simplifies interfacing to the MAX109 with controlled impedance lines. Figure 3 shows a simplified diagram of the T/H amplifier stage internal to the MAX109.

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

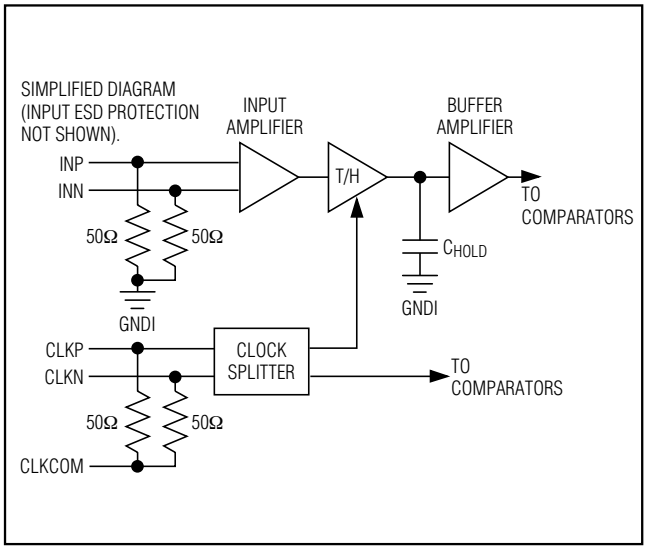


Figure 3. Internal Structure of the 3.2GHz T/H Amplifier

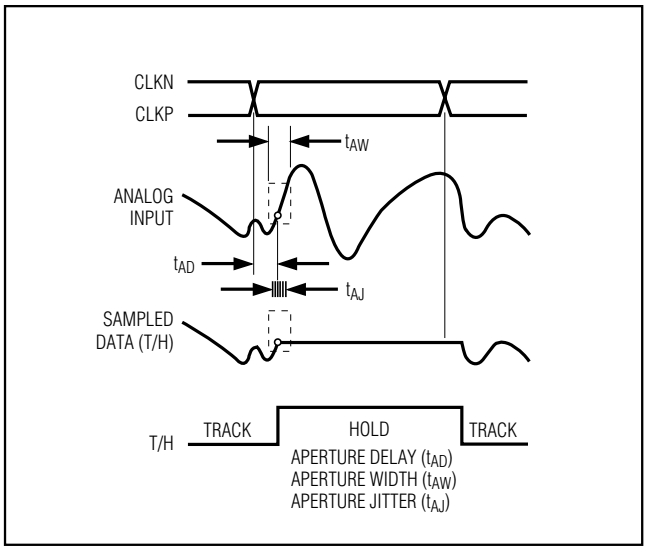


Figure 4. T/H Aperture Timing

Aperture width, delay, and jitter are parameters that affect the dynamic performance of high-speed converters. Aperture jitter, in particular, directly influences SNR and limits the maximum slew rate (dV/dt) that can be digitized without contributing significant errors. The MAX109's innovative T/H amplifier design limits aperture jitter typically to 0.2ps.

Aperture Width, Aperture Jitter, and Aperture Delay

Aperture width (t_{AW}) is the time the T/H circuit requires to disconnect the hold capacitor from the input circuit (e.g., to turn off the sampling bridge and put the T/H unit in hold mode). Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples. Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample event is occurring (Figure 4).

Clock System

The MAX109 clock signals are terminated with 50Ω to the CLKCOM pin. The clock system provides clock signals, T/H amplifier, quantizer, and all back-end digital blocks. The MAX109 also produces a digitized output clock for synchronization with external FPGA or data-capture devices. Note that there is a 1.6ns delay between the clock input (CLKP/CLKN) and its digitized output representation (DCOP/DCON).

Sampling Point Adjustment (SAMPADJ)

The proper sampling point can be adjusted by utilizing SAMPADJ as the control line. SAMPADJ accepts an input-voltage range of 0 to 2.5V, correlating with up to 32ps timing adjustment. The nominal open-circuit voltage corresponds to the minimum sampling delay. With an input resistance $R_{SAMPADJ}$ of typically 50kΩ, this pin can be adjusted externally with a 10kΩ potentiometer connected between REFOUT and GNDI to adjust for the proper sampling point.

T/H Amplifier to Quantizer Capture Point Adjustment (DELGATE0, DELGATE1)

Another important feature of the MAX109, is the selection of the proper quantizer capture point between the T/H amplifier and the ADC core. Depending on the selected sampling speed for the application, two control lines can be utilized to set the proper capture point between these two circuits. DELGATE0 (LSB) and DELGATE1 (MSB) set the *coarse* timing of the proper capture point. Using these control lines allow the user to adjust the time after which the quantizer latches *held* data from the T/H amplifier between 25ps and 50ps (Table 1). This timing feature enables the MAX109 T/H amplifier to settle its output properly before the quantizer captures and digitizes the data, thereby achieving the best dynamic performance for any application.

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

Table 1. Timing Adjustments for T/H Amplifier and Quantizer

DELGATE1	DELGATE0	TIME DELAY BETWEEN T/H AND QUANTIZER	RECOMMENDED FOR CLOCK SPEEDS OF
0	1	25ps	f_{CLK} = 2.2Gsps to 2.5Gsps
1	0	50ps	f_{CLK} = 1.75Gsps to 2.2Gsps

Internal Reference

The MAX109 features an on-chip 2.5V precision bandgap reference used to generate the full-scale range for the data converter. Connecting REFIN with REFOUT applies the reference output to the positive input of the reference buffer. The buffer's negative input is internally connected to GNDR. It is recommended that GNDR be connected to GNDI on the user's application board.

If required, REFOUT can source up to 2.5mA to supply other external devices. Additionally, an adjustable external reference can be used to adjust the ADC's full-scale range. To use an external reference supply, connect a high-precision bandgap reference to the REFIN pin and leave the REFOUT pin floating. REFIN has a typical input resistance R_{REFIN} of 5kΩ and accepts input voltages of 2.5V ±10%.

Digital LVDS Outputs

The MAX109 provides data in offset binary format to differential LVDS outputs on four output ports (PortA, PortB, PortC, and PortD). A simplified circuit schematic of the LVDS output cells is shown in Figure 5. All LVDS outputs are powered from the output driver supply $V_{CC}O$, which can be operated at 3.3V ±10%. The MAX109 LVDS outputs provide a differential output-voltage swing of 600mV_{P-P} with a common-mode voltage of approximately 1.2V, and must be differentially terminated at the far end of each transmission line pair (true and complementary) with 100Ω.

Data Out-of-Range Operation (DORP, DORN)

A single differential output pair (DORP, DORN) is provided to flag an out-of-range condition, if the applied signal is outside the allowable input range, where out-of-range is above positive full scale (+FS) or below negative full scale (-FS). The DORP/DORN transitions high/low whenever any of the four output ports (PortA, PortB, PortC, and PortD) display out-of-range data. DORP/DORN features the same latency as the ADC output data and is demultiplexed in a similar fashion, so that this out-of-range signal and the data samples are time-aligned.

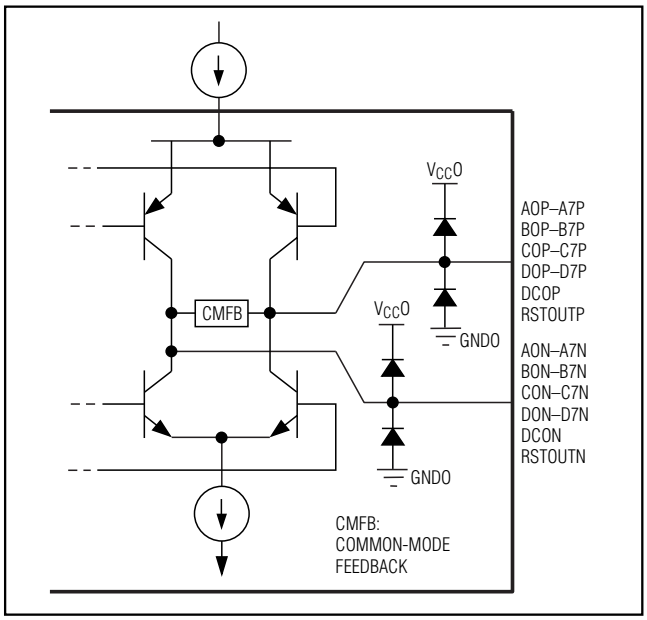


Figure 5. Simplified LVDS Output Circuitry

Table 2. Data Rate Selection for Demultiplexer Operation

DDR	QDR	DEMULTIPLEXER OPERATION	DCO SPEED
0	X	SDR mode, PortA, PortB, PortC, and PortD enabled, 550Msps per port	f_{CLK} / 4
1	0	DDR mode, PortA, PortB, PortC, and PortD enabled, 550Msps per port	f_{CLK} / 8
1	1	QDR mode, PortA, PortB, PortC, and PortD enabled, 550Msps per port	f_{CLK} / 16

X = Do not care.

Demultiplexer Operation

The MAX109's internal 1:4 demultiplexer spreads the ADC core's 8-bit data across 32 true LVDS outputs and allows for easy data capture in three different modes. Two TTL/CMOS-compatible inputs are utilized to create the different modes: SDR (standard data rate), DDR

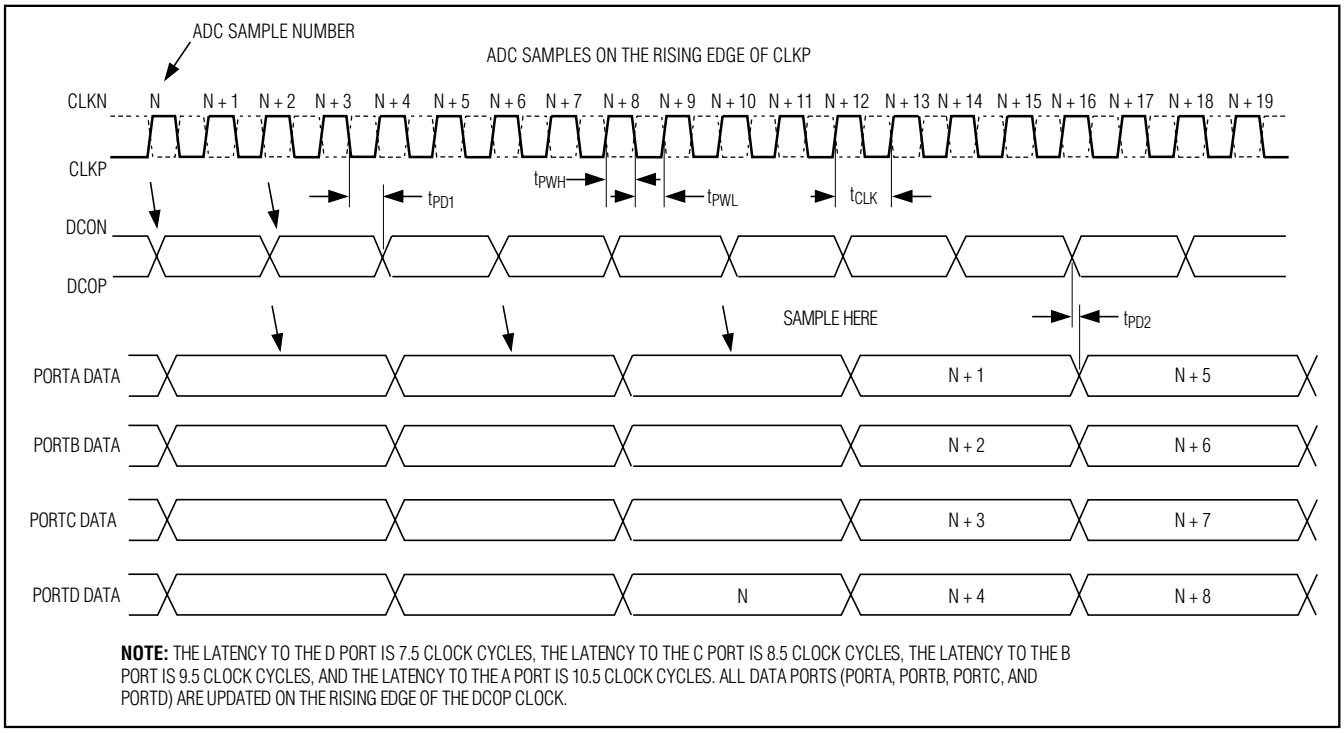


Figure 6. Timing Diagram for SDR Mode, f_{CLK} / 4 Mode

(double data rate), and QDR (quadruple data rate). Setting these two bits for different modes allows the user to update and process the outputs at one-quarter (SDR mode), one-eighth (DDR mode), or one-sixteenth (QDR mode) the sampling clock (Table 2), relaxing the need for an ultra-fast FPGA or data-capture interface.

Data is presented on all four ports of the converter-demultiplexer circuit outputs. Note that there is a data latency between the sampled data and each of the output ports. The data latency is 10.5 clock cycles for PortA, 9.5 clock cycles for PortB, 8.5 clock cycles for PortC, and 7.5 clock cycles for PortD. This holds true for all demultiplexer modes. Figures 6, 7, and 8 display the demultiplexer timing for f_{CLK} / 4, f_{CLK} / 8, and f_{CLK} / 16 modes.

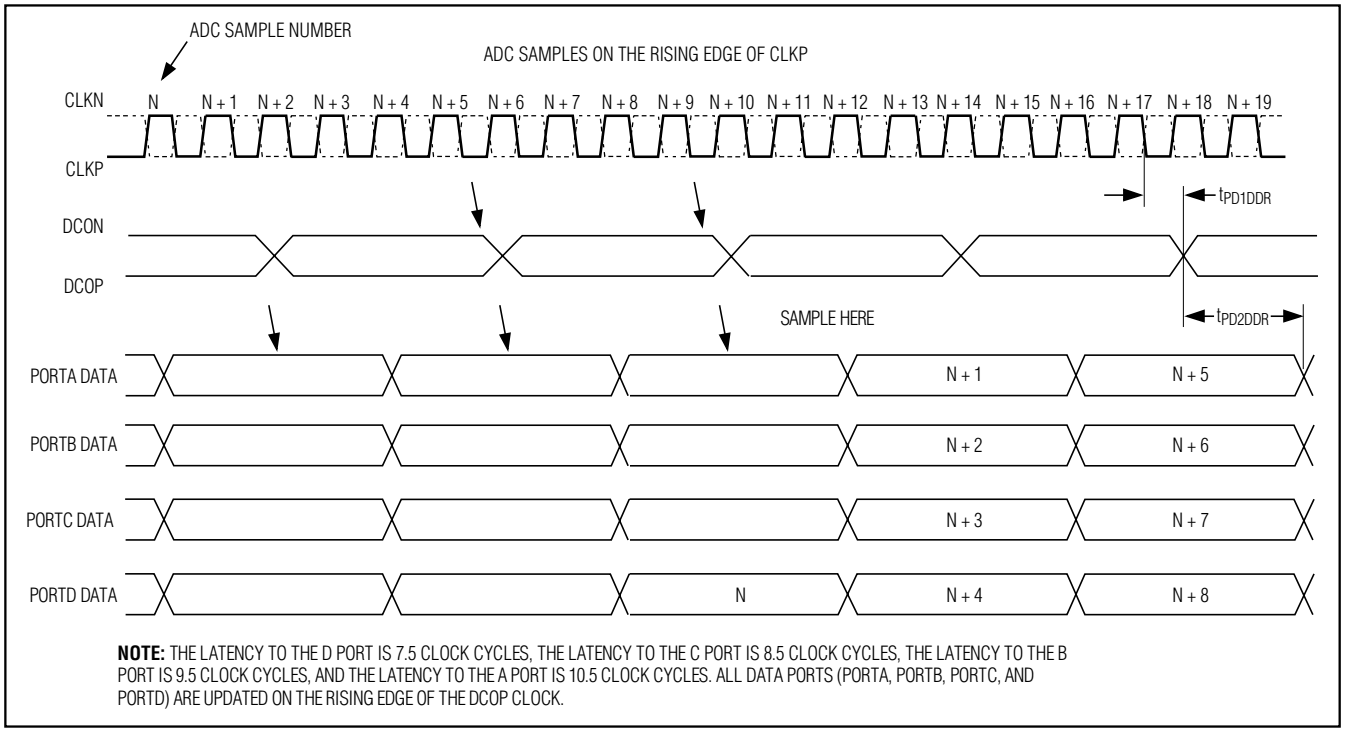
Pseudorandom Number (PRN) Generator

The MAX109 features a PRN generator that enables the user to test the demultiplexed digital outputs at full clock speed and with a known test pattern. The PRN generator is a combination of shift register and feedback logic with 255 states. When PRN is high, the inter-

Table 3. Pseudorandom Number Generator Patterns

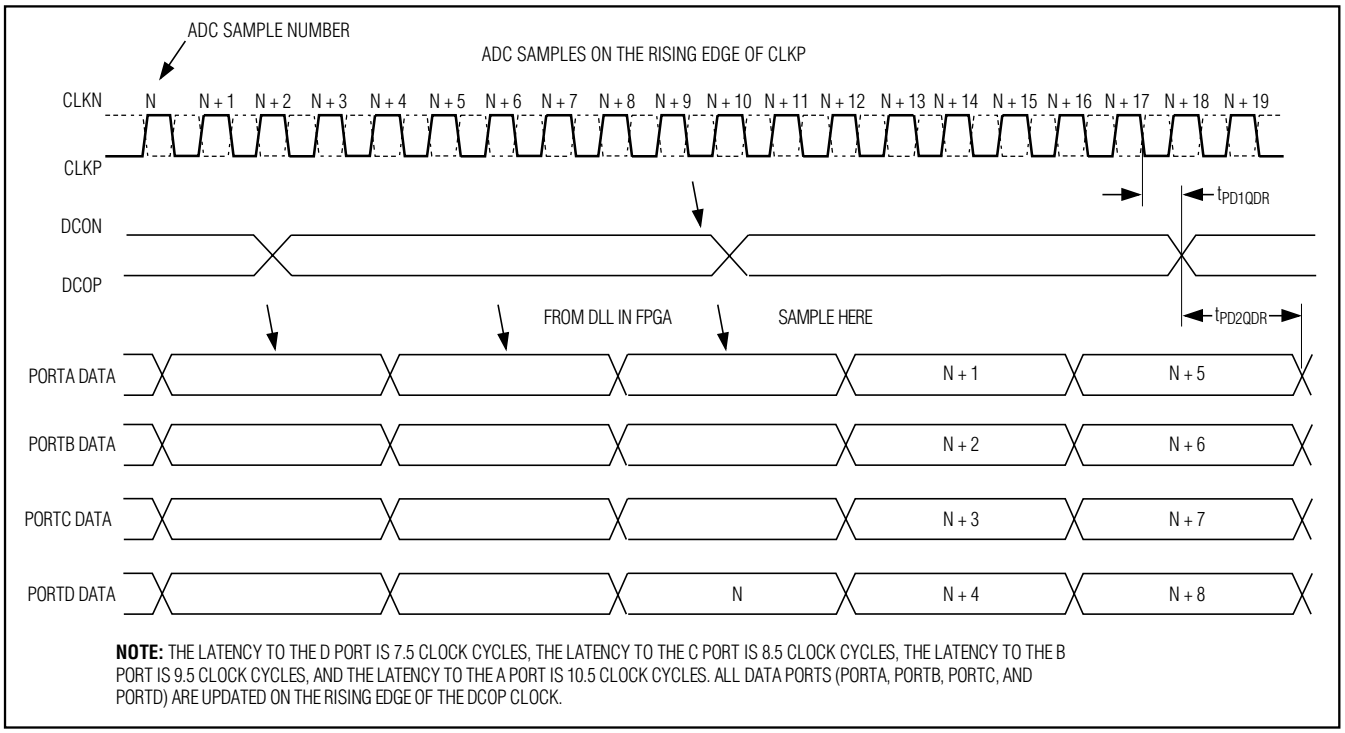
CODE	OUTPUT PRN PATTERN
1	00000001
2	00000010
3	00000100
4	00001000
5	00010001
6	00100011
7	01000111
8	10001110
9	00011100
10	00111000
—	—
—	—
250	00110100
251	01101000
252	11010000
253	10100000
254	01000000
255	10000000

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs



NOTE: THE LATENCY TO THE D PORT IS 7.5 CLOCK CYCLES, THE LATENCY TO THE C PORT IS 8.5 CLOCK CYCLES, THE LATENCY TO THE B PORT IS 9.5 CLOCK CYCLES, AND THE LATENCY TO THE A PORT IS 10.5 CLOCK CYCLES. ALL DATA PORTS (PORTA, PORTB, PORTC, AND PORTD) ARE UPDATED ON THE RISING EDGE OF THE DCOP CLOCK.

Figure 7. Timing Diagram for DDR Mode, f_{CLK} / 8 Mode



NOTE: THE LATENCY TO THE D PORT IS 7.5 CLOCK CYCLES, THE LATENCY TO THE C PORT IS 8.5 CLOCK CYCLES, THE LATENCY TO THE B PORT IS 9.5 CLOCK CYCLES, AND THE LATENCY TO THE A PORT IS 10.5 CLOCK CYCLES. ALL DATA PORTS (PORTA, PORTB, PORTC, AND PORTD) ARE UPDATED ON THE RISING EDGE OF THE DCOP CLOCK.

Figure 8. Timing Diagram for QDR Mode, f_{CLK} / 16 Mode

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

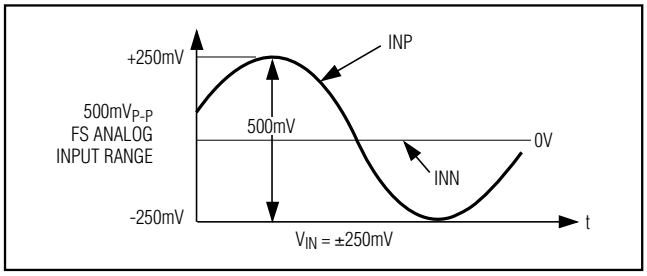


Figure 9. Single-Ended Analog Input Signal Swing

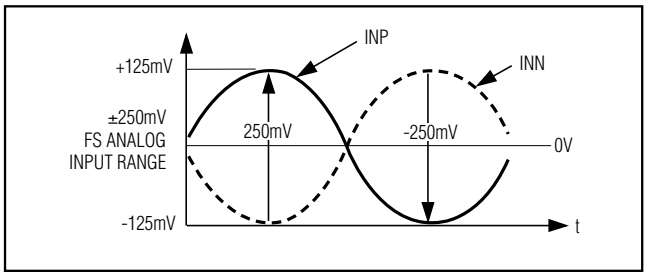


Figure 10. Differential Analog Input Signal Swing

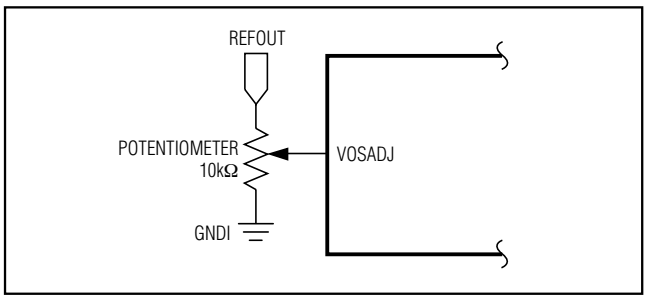


Figure 11. Offset Adjustment Circuit

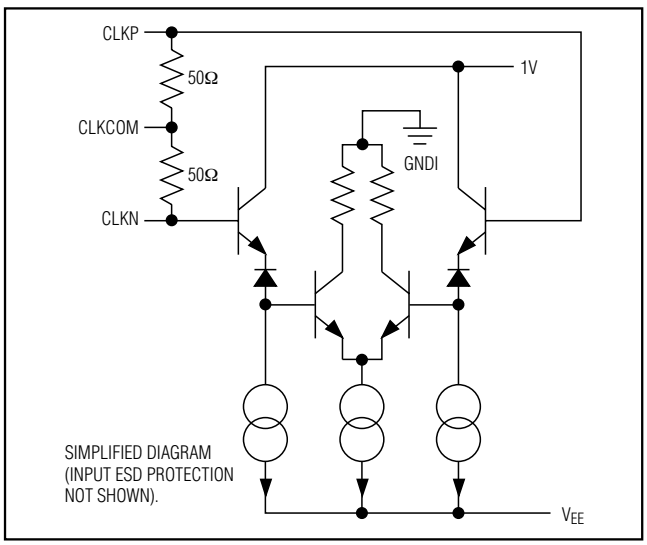


Figure 12. Clock Input Structure

nal shift register is enabled and multiplexed with the input of the 1:4 demultiplexer, replacing the quantizer 8-bit output. The test pattern consists of 8 bits. Table 3 depicts the composition of the first and last steps of the PRN pattern. The entire look-up table can be downloaded from the Maxim website at www.maxim-ic.com.

Applications Information

Single-Ended Analog Inputs

The MAX109 is designed to work at full speed for both single-ended and differential analog inputs; however, for optimum dynamic performance it is recommended that the inputs are driven differentially. Inputs INP and INN feature on-chip, laser-trimmed 50Ω termination resistors.

In a typical single-ended configuration, the analog input signal (Figure 9) enters the T/H amplifier stage at the in-phase input (INP), while the inverted phase input (INN) is reverse-terminated to GNDI with an external 50Ω resistor. Single-ended operation allows for an input amplitude of $500mV_{P-P}$. Table 4 shows a selection of input voltages and their corresponding output codes for single-ended operation.

Differential Analog Inputs

To obtain a full-scale digital output with differential input drive (Figure 10), $250mV_{P-P}$ must be applied between INP and INN (INP = 125mV and INN = -125mV). Mid-scale digital output codes (01111111 or 10000000) occur when there is no voltage difference between INP and INN. For a zero-scale digital output code, the in-phase INP input must see -125mV and the inverted input INN must see 125mV. A differential input drive is recommended for best performance. Table 5 represents a selection of differential input voltages and their corresponding output codes.

Offset Adjust

The MAX109 provides a control input (VOSADJ) to compensate for system offsets. The offset adjust input is a self-biased voltage-divider from the internal 2.5V precision reference. The nominal open-circuit voltage is one-half the reference voltage. With an input resistance (R_{VOSADJ}) of typically 50kΩ, VOSADJ can be driven with an external 10kΩ potentiometer (Figure 11) connected between REFOUT and GNDI to correct for offset errors. For stabilizing purposes, decouple this output with a 0.01µF capacitor to GNDI. VOSADJ allows for a typical offset adjustment of ±10 LSB.

Clock Operation

The MAX109 clock inputs are designed for either single-ended or differential operation (Figure 12) with flexi-

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

Table 4. Digital Output Codes Corresponding to a DC-Coupled Single-Ended Analog Input

IN-PHASE/TRUE INPUT (INP)	INVERTED/COMPLEMENTARY INPUT (INN)	OUT-OF-RANGE BIT (DORP/DORN)	OUTPUT CODE
250mV	0	1	11111111 (full scale)
250mV - 1 LSB	0	0	11111111
0	0	0	10000000 toggles 01111111
-250mV + 1 LSB	0	0	00000001
-250mV	0	0	00000000 (zero scale)
<-250mV	0	1	00000000 (out of range)

Table 5. Digital Output Codes Corresponding to a DC-Coupled Differential Analog Input

IN-PHASE/TRUE INPUT (INP)	INVERTED/COMPLEMENTARY INPUT (INN)	OUT-OF-RANGE BIT (DORP/DORN)	OUTPUT CODE
125mV	-125mV	1	11111111 (full scale)
125mV - 0.5 LSB	-125mV + 0.5 LSB	0	11111111
0	0	0	10000000 toggles 01111111
-125mV + 0.5 LSB	125mV - 0.5 LSB	0	00000001
-125mV	125mV	0	00000000 (zero scale)
<-125mV	>+125mV	1	00000000 (out of range)

Table 6. Driving Options for DC-Coupled Clock

CLOCK DRIVE	CLKP	CLKN	CLKCOM	REFERENCE
Single-ended sine wave	-10dBm to +15dBm	Externally terminated to GNDI with 50Ω	GNDI	Figure 13a
Differential sine wave	-10dBm to +10dBm	-10dBm to +10dBm	GNDI	Figure 13b
Single-ended ECL	ECL drive	-1.3V	-2V	Figure 13c
Differential ECL	ECL drive	$\overline{\text{ECL}}$ drive	-2V	Figure 13d

Table 7. Demultiplexer and Reset Operations

SIGNAL/PIN NAME	TYPE	FUNCTIONAL DESCRIPTION
CLKP/CLKN	Sampling clock inputs	Master ADC timing signal. The ADC samples on the rising edge of CLKP.
DCOP/DCON	LVDS outputs	Data clock output (LVDS). Output data changes on the rising edge of DCOP.
RSTINP/RSTINN	LVDS inputs	Demultiplexer reset input signals. Resets the internal demultiplexer when asserted.
RSTOUTP/RSTOUTN	LVDS outputs	Reset outputs for synchronizing the resets of multiple external devices.

ble input drive requirements. Each clock input is terminated with an on-chip, laser-trimmed 50Ω resistor to CLKCOM (clock-termination return). The CLKCOM termination voltage can be connected anywhere between ground and -2V for compatibility with standard-ECL drive levels. The clock inputs are internally buffered with a preamplifier to ensure proper operation of the data converter, even with small-amplitude sine-wave sources. The MAX109 was designed for single-ended, low-phase noise sine-wave clock signals with as little as 100mV amplitude (-10dBm), thereby eliminating the need for an external ECL clock buffer and its added jitter.

Single-Ended Clock Inputs (Sine-Wave Drive)

Excellent performance is obtained by AC- or DC-coupling a low-phase-noise sine-wave source into a single clock input (Figure 13a, Table 6). For proper DC balance, the undriven clock input should be externally

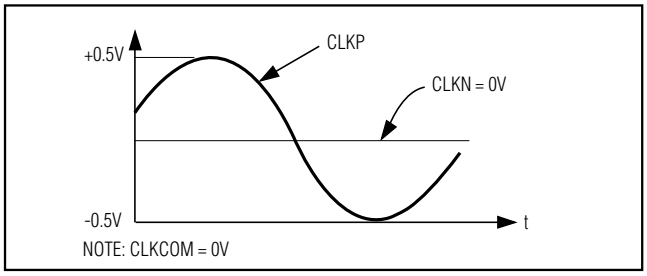


Figure 13a. Single-Ended Clock Input—Sine-Wave Drive

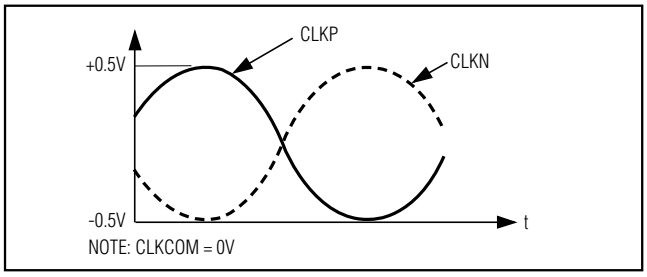


Figure 13b. Differential Clock Input—Sine-Wave Drive

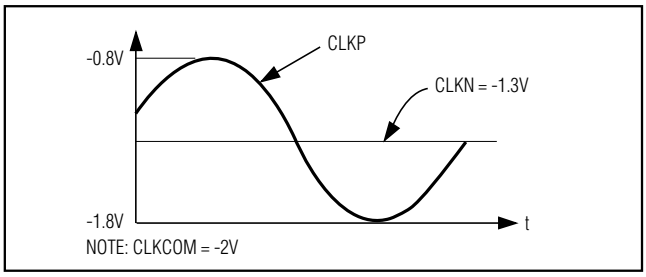


Figure 13c. Single-Ended Clock Input—ECL Drive

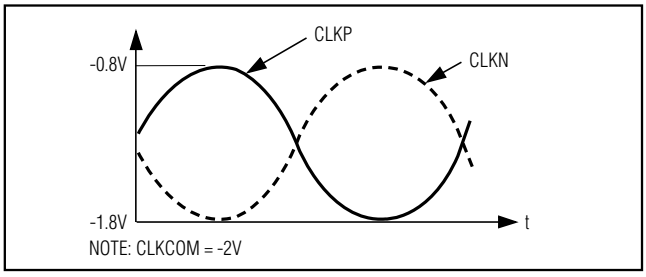


Figure 13d. Differential Clock Input—ECL Drive

50Ω reverse-terminated to GNDI. The dynamic performance of the data converter is essentially unaffected by clock-drive power levels from -10dBm to +10dBm. The MAX109 dynamic performance specifications are determined by a single-ended clock drive of 10dBm. To avoid saturation of the input amplifier stage, limit the clock power level to a maximum of 15dBm.

Differential Clock Inputs (Sine-Wave Drive)

The advantages of differential clock drive (Figure 13b, Table 6) can be obtained by using an appropriate balun transformer to convert single-ended sine-wave sources into differential drives. The precision on-chip, laser-trimmed 50Ω clock-termination resistors ensure excellent amplitude matching. See the *Single-Ended Clock Inputs (Sine-Wave Drive)* section for proper input amplitude requirements.

Single-Ended Clock Inputs (ECL Drive)

Configure the MAX109 for single-ended ECL clock drive by connecting the clock inputs as shown in Figure 13c and Table 6. A well-bypassed V_{BB} supply (-1.3V) is essential to avoid coupling noise into the undriven clock input, which would degrade dynamic performance.

Differential Clock Inputs (ECL Drive)

Drive the MAX109 from a standard differential ECL clock source (Figure 13d, Table 6) by setting the clock termination voltage at CLKCOM to -2V. Bypass the clock termination return (CLKCOM) as close to the ADC as possible with a 0.01µF capacitor connected to GNDI.

Demultiplexer Reset Operation

The MAX109 features an internal 1:4 demultiplexer that reduces the data rate of the output digital data to one-quarter the sample clock rate. A reset for the demultiplexer is necessary when interleaving multiple MAX109 converters and/or synchronizing external demultiplexers. The simplified block diagram of Figure 1 shows that the demultiplexer reset signal path consists of four main circuit blocks. From input to output, they are the reset input dual latch, the reset pipeline, the demultiplexer clock generator, and the reset output. The signals associated with the demultiplexer-reset operation and the control of this section are listed in Table 7.

Reset Input Dual Latch

The reset input dual-latch circuit block accepts LVDS reset inputs. For applications that do not require a synchronizing reset, the reset inputs may be left open. Figure 14 shows a simplified schematic of the reset input structure. To latch the reset input data properly, the setup time (t_{SU}) and the data-hold time (t_{HD}) must be met with respect to the rising edge of the sample clock. The timing diagram of Figure 15 shows the timing relationship of the reset input and sampling clock.

Reset Pipeline

The next section in the reset signal path is the reset pipeline. This block adds clock cycles of latency to the

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

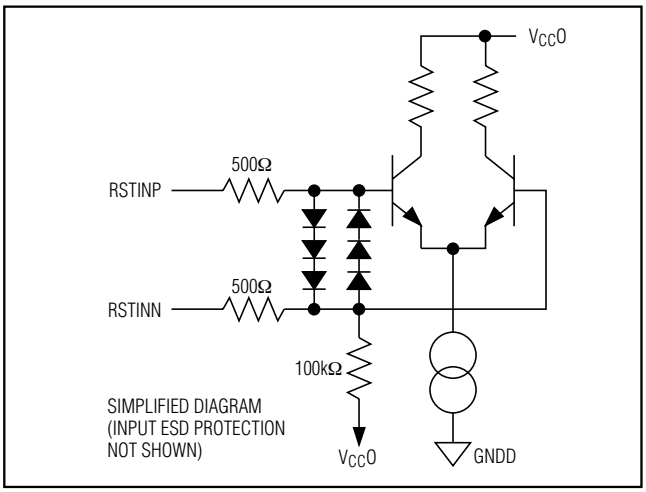


Figure 14. Reset Circuitry—Input Structure

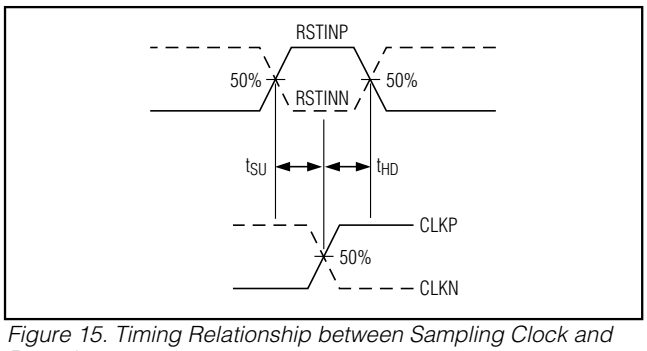


Figure 15. Timing Relationship between Sampling Clock and Reset Input

reset signal to match the latency of the converted analog data through the ADC. In this way, when reset data arrives at the RSTOUTP/RSTOUTN LVDS output it will be time-aligned with the analog data present in data ports PortA, PortB, PortC, and PortD at the time the reset input was deasserted.

Demultiplexer Clock Generator

The demultiplexer clock generator creates the clocks required for the different modes of demultiplexer operation. DDR and QDR control the demultiplexed mode selection, as described in Table 2. The timing diagrams in Figures 6, 7, and 8 show the output timing and data alignment for SDR, DDR, and QDR modes, respectively. The phase relationship between the sampling clock at the CLKP/CLKN inputs and the DCO clock at the DCOP/DCON outputs is random at device power-up. Reset all MAX109 devices to a known DCO phase after initial power-up for applications such as interleaving, where two or more MAX109 devices are used to achieve higher effective sampling rates. This synchronization is necessary to set the order of output samples between the devices. Resetting the converters accomplishes this synchronization. The reset signal is used to force the internal counter in the demultiplexer clock-generator block to a known phase state.

Reset Output

Finally, the reset signal is presented in true LVDS format to the last block of the reset signal path. RSTOUT outputs the time-aligned reset signal, used for resetting additional external demultiplexers in applications that need further output data-rate reduction. Many demultiplexer devices require their reset signal to be asserted for several clock cycles while they are clocked. To accomplish this, the MAX109 DCO clock will continue to toggle while RSTOUT is asserted. When a single MAX109 device is used, no synchronizing reset is required because the order of the samples in the output ports remains unchanged, regardless of the phase of the DCO clock. In all modes, RSTOUT is delayed by 7.5 clock cycles, starting with the first rising edge of CLKP following the falling edge of the RSTINP signal. With the next reset cycle PortD data shows the expected and proper data on the output, while the remaining three ports (PortA, PortB, and PortC) keep their previous data, which may or may not be *swallowed*, depending on the power-up state of the demultiplexer clock generator. With the next cycle, the right data is presented for all four ports in the proper order. The aforementioned reset output and data-reset operation is valid for SDR, DDR, and QDR modes.

Die Temperature Measurement

The die temperature of the MAX109 can be determined by monitoring the voltage $V_{TEMPMON}$ between the TEMPMON output and GNDI. The corresponding voltage is proportional to the actual die temperature of the converter and can be calculated as follows:

$$T_{DIE}\ (°C) = [(V_{TEMPMON} - V_{GNDI}) \times 1303.5] - 371$$

The MAX109 exhibits a typical TEMPMON voltage of 0.35V, resulting in an overall die temperature of +90°C. The converter's die temperature can be lowered considerably by *cooling* the MAX109 with a properly sized heatsink. Adding airflow across the part with a small fan can further lower the die temperature, making the system more thermally manageable and stable.

Thermal Management

Depending on the application environment for the SBGA-packaged MAX109, the user can apply an external heatsink with integrated fan to the package after board assembly. Existing open-tooled heatsinks with

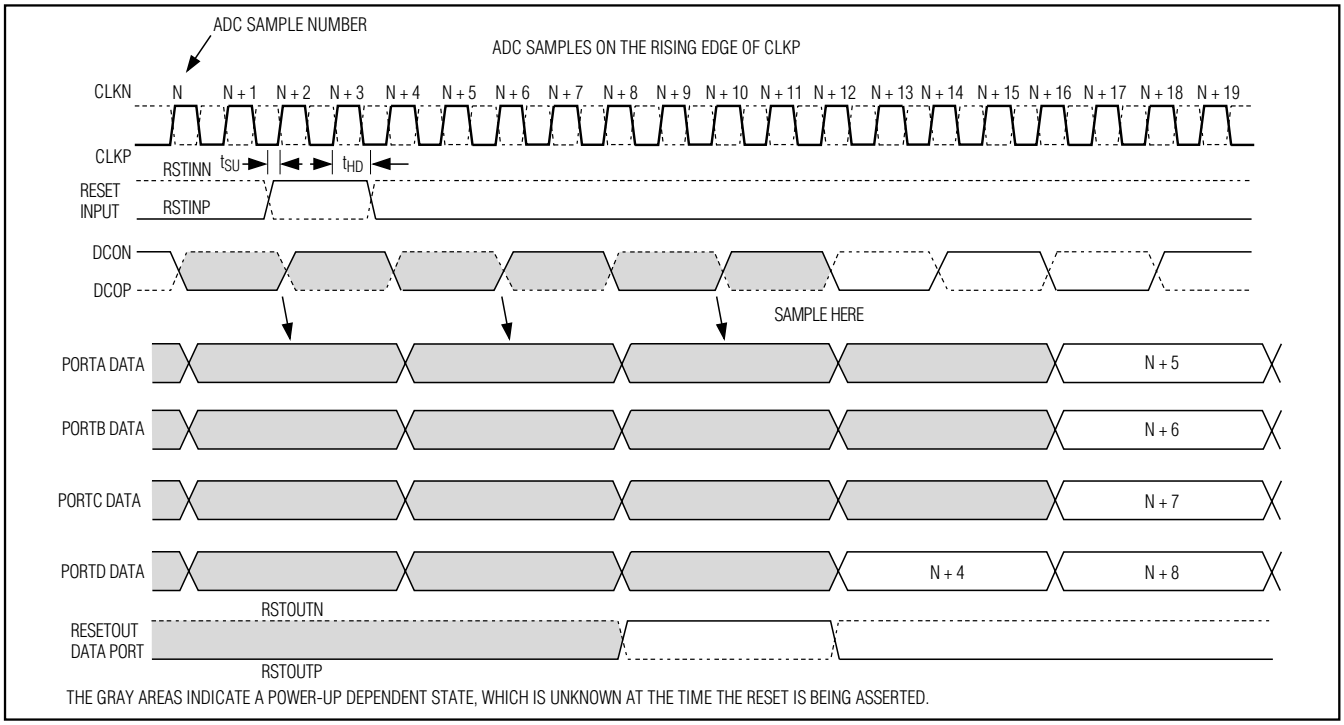


Figure 16. Reset Output Timing in Demultiplexed SDR Mode

integrated fans are available from Co-Fan USA (e.g., the 30-1101-02 model, which is used on the evaluation kit of the MAX109). This particular heatsink with integrated fan is available with pre-applied adhesive for easy package mounting.

Bypassing/Layout/Power Supply

Grounding and power-supply decoupling strongly influence the MAX109's performance. At a 2.2GHz clock frequency and 8-bit resolution, unwanted digital crosstalk may couple through the input, reference, power supply, and ground connections and adversely influence the dynamic performance of the ADC. Therefore, closely follow the grounding and power-supply decoupling guidelines (Figure 17). Maxim strongly recommends using a multilayer printed circuit board (PCB) with separate ground and power-supply planes. Since the MAX109 has separate analog and digital ground connections (GNDA, GNDI, GNDR, and GNDD, respectively), the PCB should feature separate analog and digital ground sections connected at only one point (star ground at the power supply). Digital signals should run above the digital ground plane, and analog signals should run above the analog ground plane. Keep digital signals far away from the sensitive analog inputs, reference inputs, and clock inputs. High-speed signals, including clocks, analog inputs, and digital outputs, should be routed on 50Ω microstrip lines, such as those employed on the MAX109 evaluation kit.

The MAX109 has separate analog and digital power-supply inputs:

- V_{EE} (-5V) is the analog and substrate supply
- $V_{CC}I$ (5V) to power the T/H amplifier, clock distribution, bandgap reference, and reference amplifier
- $V_{CC}A$ (5V) to supply the ADC's comparator array
- $V_{CC}O$ (3.3V) to establish power for all LVDS-based circuit sections
- $V_{CC}D$ (5V) to supply all logic circuits of the data converter

The MAX109 V_{EE} supply contacts must not be left open while the part is being powered up. To avoid this condition, add a high-speed Schottky diode (such as a Motorola 1N5817) between V_{EE} and GNDI. This diode prevents the device substrate from forward biasing, which could cause latchup. All supplies should be decoupled with large tantalum or electrolytic capacitors at the point they enter the PCB. For best performance, bypass all power supplies to the appropriate grounds with a 330µF and 33µF tantalum capacitor to filter power-supply noise, in parallel with 0.1µF capacitors and high-quality 0.01µF ceramic chip capacitors. Each power

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

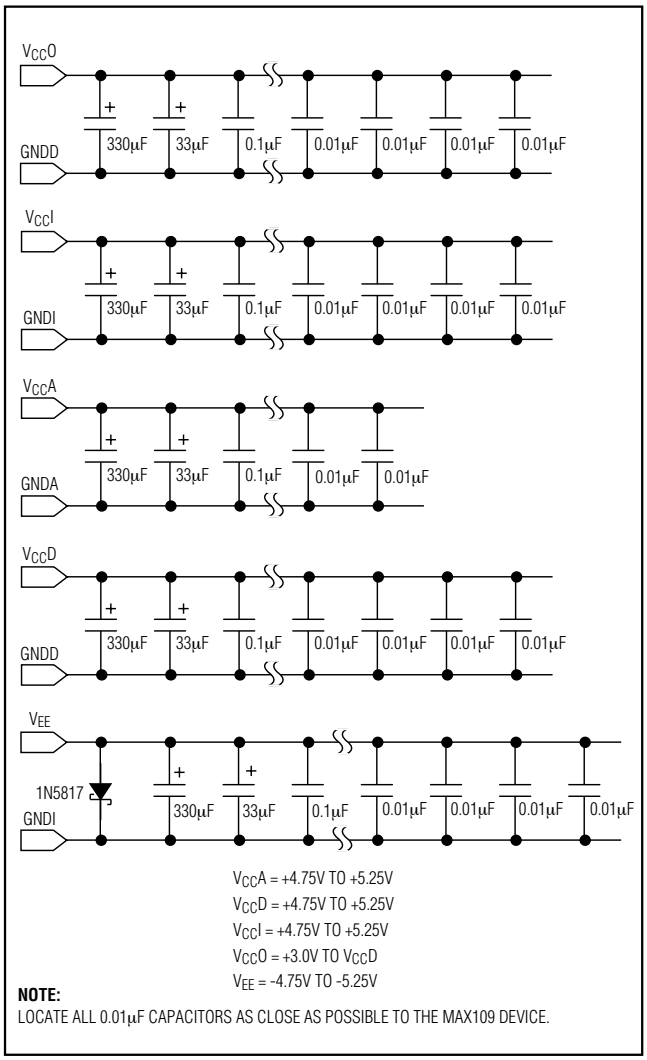


Figure 17. MAX109 Decoupling and Bypassing Recommendations

supply for the chip should have its own 0.01µF capacitor, which should be placed as close as possible to the MAX109 for optimum high-frequency noise filtering.

Static/DC Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. For the MAX109, this straight line is between the endpoints of the transfer function, once offset and gain errors have been nullified. INL deviations are measured at every step of the transfer function and the worst-case deviation is reported in the *Electrical Characteristics* table.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. For the MAX109, DNL deviations are measured at every step of the transfer function and the worst-case deviation is reported in the *Electrical Characteristics* table.

Offset Error

Offset error is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. Ideally, the mid-scale MAX109 transition occurs at 0.5 LSB above mid scale. The offset error is the amount of deviation between the measured mid-scale transition point and the ideal mid-scale transition point.

Bit Error Rates

Errors resulting from metastable states may occur when the analog input voltage (at the time the sample is taken) falls close to the decision point of any one of the input comparators. Here, the magnitude of the error depends on the location of the comparator in the comparator network. If it is the comparator for the MSB, the error will reach full scale. The MAX109's unique encoding scheme solves this problem by limiting the magnitude of these errors to 1 LSB.

Dynamic/AC Parameter Definitions

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR[max] = 6.02 \times N + 1.76$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first 15 harmonics (HD2 through HD16), and the DC offset:

$$SNR = 20 \times \log (SIGNAL_{RMS} / NOISE_{RMS})$$

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus

distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB is calculated from a curve fit referenced to the theoretical full-scale range.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 15 harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + ... + V_{16}^2}}{V_1} \right)$$

where V1 is the fundamental amplitude, and V_2 through V_{16} are the amplitudes of the 2nd- through 16th-order harmonics (HD2 through HD16).

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Third-Order Intermodulation (IM3)

IM3 is the total power of the third-order intermodulation product to the Nyquist frequency relative to the total input power of the two input tones, $f_{IN}1$ and $f_{IN}2$. The individual input tone levels are at -7dBFS. The third-order intermodulation products are located at 2 x f_{IN1}-f_{IN2}, 2 x f_{IN2}-f_{IN1}, 2 x f_{IN1}+f_{IN2}, and 2 x f_{IN2}+f_{IN1}.

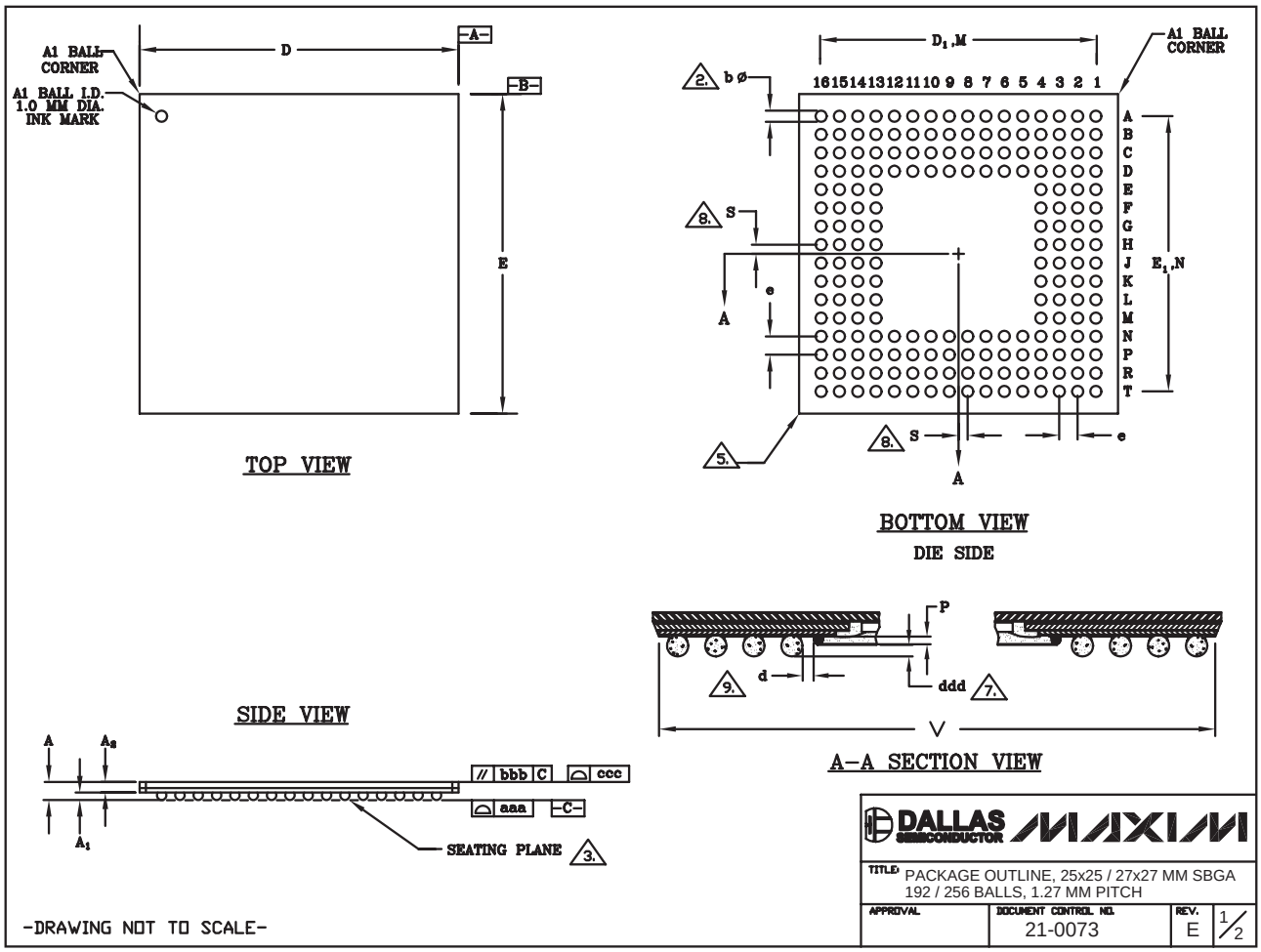
Full-Power Bandwidth

A large -1dBFS analog input signal is applied to an ADC and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as full-power input bandwidth frequency.

8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION 'b' IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-.
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. THE 192 BALL 25 X 25 MM SBGA HAS 3 ROWS OF BALLS. THE 256 BALL 27 X 27 MM SBGA HAS 4 ROWS OF BALLS. NUMBER OF BALLS SHOWN ARE FOR REFERENCE ONLY.
5. SHAPE AT CORNER.

SINGLE FORM

6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. HEIGHT FROM BALL SEATING PLANE TO PLANE OF ENCAPSULANT.
8. 'S' IS MEASURED WITH RESPECT TO -A- AND -B- AND DEFINES THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW 'S'=.000; WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW THE VALUE 'S'=e/2. 'S' MAY BE EITHER .000 OR e/2 FOR EACH VARIATION.
9. THE DIMENSION FROM THE OUTER EDGE OF THE RESIN DAM TO THE EDGE OF THE INNERMOST ROW OF SOLDER BALL PADS IS TO BE A MINIMUM OF 0.50mm.
10. 'SUPER BGA' IS A REGISTERED TRADEMARK OF AMKOR TECHNOLOGIES.
11. MEETS JEDEC MS034.

STANDARD BODY SIZE DIMENSION TABLE

	25.0 X 25.0MM PACKAGE			27.0 X 27.0MM PACKAGE			BODY SIZE
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	NOTE
A	1.41	1.54	1.67	1.41	1.54	1.67	OVERALL THICKNESS
A1	0.56	0.63	0.70	0.56	0.63	0.70	BALL HEIGHT
A2	0.85	0.91	0.97	0.85	0.91	0.97	BODY THICKNESS
D	24.90	25.00	25.10	26.90	27.00	27.10	BODY SIZE
D1	22.76	22.86	22.96	24.03	24.13	24.23	BALL FOOTPRINT
E	24.90	25.00	25.10	26.90	27.00	27.10	BODY SIZE
E1	22.76	22.86	22.96	24.03	24.13	24.23	BALL FOOTPRINT
M,N	19 x 19			20 x 20			BALL MATRIX
	192			256			# OF BALLS
b	0.60	0.75	0.90	0.60	0.75	0.90	BALL DIAMETER
d	0.6			0.6			MIN DISTANCE ENCAP TO BALLS
e	1.27			1.27			BALL PITCH
aaa			0.15			0.15	COPLANARITY
bbb			0.15			0.15	PARALLEL
ccc			0.20			0.20	TOP FLATNESS
ddd (8)	0.15	0.33	0.50	0.15	0.33	0.50	SEATING PLANE CLEARANCE
P	0.20	0.30	0.35	0.20	0.30	0.35	ENCAPSULATION HEIGHT
S	0.00 REF.			0.635 REF.			SOLDER BALL PLACEMENT
V	24.2	—	24.9	26.2	—	26.9	V - GROOVE BOTTOM SIZE

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 25x25 / 27x27 MM SBGA 192 / 256 BALLS, 1.27 MM PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0073	E	2/2

-DRAWING NOT TO SCALE-

Note: The MAX109 is packaged in a 27mm x 27mm, 256 SBGA package.