



80960HA/HD/HT 32-Bit High-Performance Superscalar Processor

Data Sheet

Advance Information

Product Features

- 32-Bit Parallel Architecture
 - Load/Store Architecture
 - Sixteen 32-Bit Global Registers
 - Sixteen 32-Bit Local Registers
 - 1.28 Gbyte Internal Bandwidth (80 MHz)
 - On-Chip Register Cache
- Processor Core Clock
 - 80960HA is 1x Bus Clock
 - 80960HD is 2x Bus Clock
 - 80960HT is 3x Bus Clock
- Binary Compatible with Other 80960 Processors
- Issue Up To 150 Million Instructions per Second
- High-Performance On-Chip Storage
 - 16 Kbyte Four-Way Set-Associative Instruction Cache
 - 8 Kbyte Four-Way Set-Associative Data Cache
 - 2 Kbyte General Purpose RAM
 - Separate 128-Bit Internal Paths For Instructions/Data
- 3.3 V Supply Voltage
 - 5 V Tolerant Inputs
 - TTL Compatible Outputs
- Guarded Memory Unit
 - Provides Memory Protection
 - User/Supervisor Read/Write/Execute
- 32-Bit Demultiplexed Burst Bus
 - Per-Byte Parity Generation/Checking
 - Address Pipelining Option
 - Fully Programmable Wait State Generator
 - Supports 8-, 16- or 32-Bit Bus Widths
 - 160 Mbyte/s External Bandwidth (40 MHz)
- High-Speed Interrupt Controller
 - Up to 240 External Interrupts
 - 31 Fully Programmable Priorities
 - Separate, Non-maskable Interrupt Pin
- Dual On-Chip 32-Bit Timers
 - Auto Reload Capability and One-Shot
 - CLKIN Prescaling, $\div 1, 2, 4$ or 8
 - JTAG Support - IEEE 1149.1 Compliant

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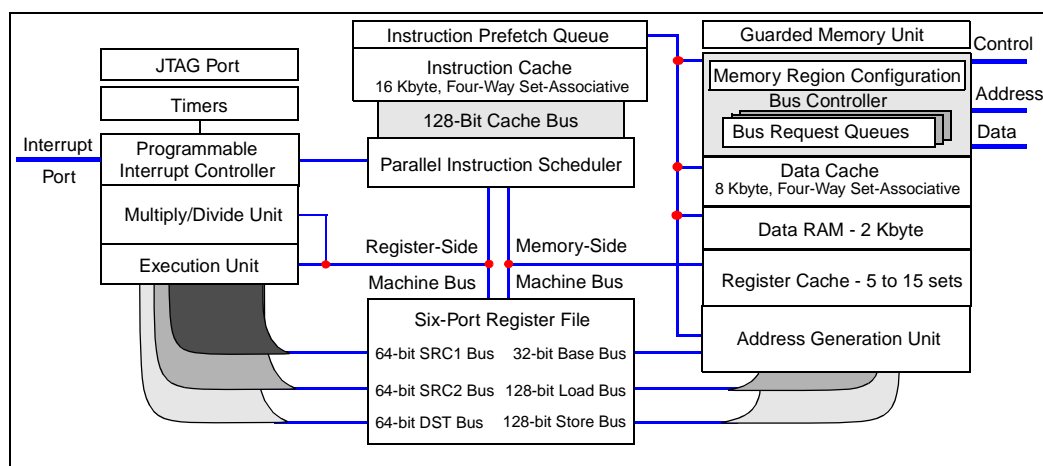
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1.0 About This Document

This document describes the parametric performance of Intel’s 80960Hx embedded superscalar microprocessors. Detailed descriptions for functional topics — other than parametric performance — are published in the *i960[®] Hx Microprocessor User’s Guide (272484)*.

In this document, “80960Hx” and “i960 Hx processor” refer to the products described in [Table 1](#). Throughout this document, information that is specific to each is clearly indicated.

Figure 1. 80960Hx Block Diagram



2.0 Intel’s 80960Hx Processor

Intel’s 80960Hx processor provides new performance levels while maintaining backward compatibility (pin¹ and software) with the i960 CA/CF processor. This newest member of the family of i960 32-bit, RISC-style, embedded processors allows customers to create scalable designs that meet multiple price and performance points. This is accomplished by providing processors that can run at the bus speed or faster using Intel’s clock multiplying technology ([Table 1](#)). The 80960Hx core is capable of issuing 150 million instructions per second, using a sophisticated instruction scheduler that allows the processor to sustain a throughput of two instructions every core clock, with a peak performance of three instructions per clock. The 80960Hx-series comprises three processors, which differ in the ratio of core clock speed to external bus speed.

Table 1. 80960Hx Product Description

| Product | Core | Voltage | Operating Frequency (bus/core) |
|---------|------|--------------------|--------------------------------|
| 80960HA | 1x | 3.3 V [*] | 25/25, 33/33, 40/40 |
| 80960HD | 2x | 3.3 V [*] | 16/32, 25/50, 33/66, 40/80 |
| 80960HT | 3x | 3.3 V [*] | 20/60, 25/75 |

^{*}Processor inputs are 5 V tolerant.

- The 80960Hx is not “drop-in” compatible in an 80960Cx-based system. Customers can design systems that accept either 80960Hx or Cx processors.

In addition to expanded clock frequency options, the 80960Hx provides essential enhancements for an emerging class of high-performance embedded applications. Features include a larger instruction cache, data cache, and data RAM than any other 80960 processor to date. It also boasts a 32-bit demultiplexed and pipelined burst bus, fast interrupt mechanism, guarded memory unit, wait state generator, dual programmable timers, ONCE and IEEE 1149.1-compliant boundary scan test and debug support, and new instructions.

2.1 The i960[®] Processor Family

The i960 processor family is a 32-bit RISC architecture created by Intel to serve the needs of embedded applications. The embedded market includes applications as diverse as industrial automation, avionics, image processing, graphics and communications.

Because all members of the i960 processor family share a common core architecture, i960 applications are code-compatible. Each new processor in the family adds its own special set of functions to the core to satisfy the needs of a specific application or range of applications in the embedded market.

2.2 Key 80960Hx Features

2.2.1 Execution Architecture

Independent instruction paths inside the processor allow the execution of multiple, out-of-sequence instructions per clock. Register and resource scoreboard interlocks maintain the logical integrity of sequential instructions that are being executed in parallel. To sustain execution of multiple instructions in each clock cycle, the processor decodes multiple instructions in parallel and simultaneously issues these instructions to parallel processing units. The various processing units are then able to independently access instruction operands in parallel from a common register set.

Local Register Cache integrated on-chip provides automatic register management on call/return instructions. Upon a call instruction, the processor allocates a set of local registers for the called procedure, then stores the registers for the previous procedure in the on-chip register cache. As additional procedures are called, the cache stores the associated registers such that the most recently called procedure is the first available by the next return (**ret**) instruction. The processor can store up to fifteen register sets, after which the oldest sets are stored (spilled) into external memory.

The 80960Hx supports the 80960 architecturally-defined branch prediction mechanism. This allows many branches to execute with no pipeline break. With the 80960Hx's efficient pipeline, a branch can take as few as zero clocks to execute. The maximum penalty for an incorrect prediction is two core clocks.

2.2.2 Pipelined, Burst Bus

A 32-bit high performance bus controller interfaces the 80960Hx core to the external memory and peripherals. The Bus Control Unit features a maximum transfer rate of 160 Mbytes per second (at a 40 MHz external bus clock frequency). A key advantage of this design is its versatility. The user can independently program the physical and logical attributes of system memory. Physical attributes include wait state profile, bus width, and parity. Logical attributes include cacheability and Big or Little Endian byte order. Internally programmable wait states and 16 separately configurable physical memory regions allow the processor to interface with a variety of memory

subsystems with minimum system complexity. To reduce the effect of wait states, the bus design is decoupled from the core. This lets the processor execute instructions while the bus performs memory accesses independently.

The Bus Controller's key features include:

- Demultiplexed, Burst Bus to support most efficient DRAM access modes
- Address Pipelining to reduce memory cost while maintaining performance
- 32-, 16- and 8-bit modes to facilitate I/O interfacing
- Full internal wait state generation to reduce system cost
- Little and Big Endian support
- Unaligned Access support implemented in hardware
- Three-deep request queue to decouple the bus from the core
- Independent physical and logical address space characteristics

2.2.3 On-Chip Caches and Data RAM

As shown in [Figure 1](#), the 80960Hx provides generous on-chip cache and storage features to decouple CPU execution from the external bus. The processor includes a 16 Kbyte instruction cache, an 8 Kbyte data cache and 2 Kbytes of Data RAM. The caches are organized as 4-way set associative. Stores that hit the data cache are written through to memory. The data cache performs write allocation on cache misses. A fifteen-set stack frame cache allows the processor to rapidly allocate and deallocate local registers. All of the on-chip RAM sustains a 4-word (128-bit) access every clock cycle.

2.2.4 Priority Interrupt Controller

The interrupt unit provides the mechanism for the low latency and high throughput interrupt service essential for embedded applications. A priority interrupt controller provides full programmability of 240 interrupt sources with a typical interrupt task switch (latency) time of 17 core clocks. The controller supports 31 priority levels. Interrupts are prioritized and signaled within 10 core clocks of the request. If the interrupt has a higher priority than the processor priority, the context switch to the interrupt routine would typically complete in another 7 bus clocks.

External agents post interrupts via the 8-bit external interrupt port. The Interrupt unit also handles the two internal sources from the Timers. Interrupts can be level- or edge-triggered.

2.2.5 Guarded Memory Unit

The Guarded Memory Unit (GMU) provides memory protection without the address translation found in Memory Management Units. The GMU contains two memory protection schemes: one prevents illegal memory accesses, the other detects memory access violations. Both signal a fault to the processor. The programmable protection modes are: user read, write or execute; and supervisor read, write or execute.

2.2.6 Dual Programmable Timers

The processor provides two independent 32-bit timers, with four programmable clock rates. The user configures the timers via the Timer Unit registers. These registers are memory-mapped within the 80960Hx, addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the processor's interrupt controller.

2.2.7 Processor Self Test

When a system error is detected, the $\overline{\text{FAIL}}$ pin is asserted, a fail code message is driven onto the address bus, and the processor stops execution at the point of failure. The only way to resume normal operation is to perform a RESET operation. Because System Error generation can occur sometime after the bus confidence test and even after initialization during normal processor operation, the $\overline{\text{FAIL}}$ pin is HIGH (logic "1") before the detection of a System Error.

The processor uses only one read bus-transaction to signal the fail code message; the address of the bus transaction is the fail code itself. The fail code is of the form: **0xfeffffmm**; bits 6 to 0 contain a mask recording the possible failures. Bit 7, when set to 1, indicates that the mask contains failures from the internal Built-In Self-Test (BIST); when 0, the mask indicates other failures.

Ignore reserved bits 0 and 1. Also ignore bits 5 and 6 when bit 7 is clear (=0).

The mask is shown in [Table 2](#) and [Table 3](#).

Table 2. Fail Codes For BIST (bit 7 = 1)

| Bit | When Set: |
|-----|--|
| 6 | On-chip Data-RAM failure detected by BIST. |
| 5 | Internal Microcode ROM failure detected by BIST. |
| 4 | Instruction cache failure detected by BIST. |
| 3 | Data cache failure detected by BIST. |
| 2 | Local-register cache or processor core failure detected by BIST. |
| 1 | Reserved. Always zero. |
| 0 | Reserved. Always zero. |

Table 3. Remaining Fail Codes (bit 7 = 0)

| Bit | When Set: |
|-----|--|
| 6 | Reserved. Always one. |
| 5 | Reserved. Always one. |
| 4 | A data structure within the IMI is not aligned to a word boundary. |
| 3 | A System Error during normal operation has occurred. |
| 2 | The Bus Confidence test has failed. |
| 1 | Reserved. Always zero. |
| 0 | Reserved. Always zero. |

2.3 Instruction Set Summary

Table 4 summarizes the 80960Hx instruction set by logical groupings.

Table 4. 80960Hx Instruction Set

| Data Movement | Arithmetic | Logical | Bit / Bit Field / Byte |
|---|---|--|---|
| Load Store Move Load Address Conditional Select ⁽²⁾ | Add Subtract Multiply Divide Remainder Modulo Shift Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry Rotate Conditional Add ⁽²⁾ Conditional Subtract ⁽²⁾ | And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand | Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal Byte Swap ⁽²⁾ |
| Comparison | Branch | Call/Return | Fault |
| Compare Conditional Compare Compare and Increment Compare and Decrement Compare Byte ⁽²⁾ Compare Short ⁽²⁾ Test Condition Code Check Bit | Unconditional Branch Conditional Branch Compare and Branch | Call Call Extended Call System Return Branch and Link | Conditional Fault Synchronize Faults |
| Debug | Processor Mgmt | Atomic | Cache Control |
| Modify Trace Controls Mark Force Mark | Flush Local Registers Modify Arithmetic Controls Modify Process Controls Interrupt Enable/Disable ^(1,2) System Control ⁽¹⁾ | Atomic Add Atomic Modify | Instruction Cache Control ^(1,2) Data Cache Control ^(1,2) |

NOTES:

1. 80960Hx extensions to the 80960 core instruction set.
2. 80960Hx extensions to the 80960Cx instruction set.

3.0 Package Information

This section describes the pins, pinouts and thermal characteristics for the 80960Hx in the 168-pin ceramic Pin Grid Array (PGA) package, 208-pin PowerQuad2* (PQ4). For complete package specifications and information, see the Intel *Packaging Handbook* (Order# 240800).

The 80960HA/HD/HT is offered with eight speeds and two package types (Table 5). Both the 168-pin ceramic Pin Grid Array (PGA) and the 208-pin PowerQuad2* (PQ4) devices are specified for operation at $V_{CC} = 3.3 \text{ V} \pm 0.15 \text{ V}$ over a case temperature range of 0° to 85°C.

Table 5. 80960HA/HD/HT Package Types and Speeds

| Package/Name | Device | Core Speed (MHz) | Bus Speed (MHz) | Order # |
|----------------------------------|---------|------------------|-----------------|--------------------|
| 168L PGA | 80960HA | 25 | | A80960HA25 S L2GX |
| | | 33 | | A80960HA33 S L2GY |
| | | 40 | | A80960HA40 S L2GZ |
| | 80960HD | 32 | 16 | A80960HD32 S L2GG |
| | | 50 | 25 | A80960HD50 S L2GH |
| | | 66 | 33 | A80960HD66 S L2GJ |
| | | 80 | 40 | A80960HD80 S L2GK |
| | 80960HT | 60 | 20 | A80960HT60 |
| | | 75 | 25 | A80960HT75 S L2GP |
| 208L PQFP (also known as PQ4) | 80960HA | 25 | | FC80960HA25 S L2GU |
| | | 33 | | FC80960HA33 S L2GV |
| | | 40 | | FC80960HA40 S L2GW |
| | 80960HD | 32 | 16 | FC80960HD32 S L2GL |
| | | 50 | 25 | FC80960HD50 S L2GM |
| | | 66 | 33 | FC80960HD66 S L2GN |
| | | 80 | 40 | FC80960HD80 S L2LZ |
| | 80960HT | 60 | 20 | FC80960HT60 S L2G2 |
| | | 75 | 25 | FC80960HT75 S L2GT |

3.1 Pin Descriptions

This section defines the 80960Hx pins. Table 6 presents the legend for interpreting the pin descriptions in Table 7. All pins float while the processor is in the ONCE mode, except TDO, which can be driven active according to normal JTAG specifications.

Table 6. Pin Description Nomenclature

| Symbol | Description |
|--------|---|
| I | Input only pin. |
| O | Output only pin. |
| I/O | Pin can be input or output. |
| - | Pin must be connected as indicated for proper device functionality. |
| S(E) | Synchronous edge sensitive input. This input must meet the setup and hold times relative to CLKIN to ensure proper operation of the processor. |
| S(L) | Synchronous level sensitive input. This input must meet the setup and hold times relative to CLKIN to ensure proper operation of the processor. |
| A(E) | Asynchronous edge-sensitive input. |
| A(L) | Asynchronous level-sensitive input. |
| H(...) | While the processor bus is in the HOLD state (HOLDA asserted), the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Z) floats H(Q) continues to be a valid output |
| B(...) | While the processor is in the bus backoff state (BOFF asserted), the pin: B(1) is driven to V_{CC} B(0) is driven to V_{SS} B(Z) floats B(Q) continues to be a valid output |
| R(...) | While the processor's \overline{RESET} pin is asserted, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Z) floats R(Q) continues to be a valid output |

Table 7. 80960Hx Processor Family Pin Descriptions (Sheet 1 of 4)

| Name | Type | Description |
|--------------|--|---|
| A31:2 | O H(Z) B(Z) R(Z) | ADDRESS BUS carries the upper 30 bits of the physical address. A31 is the most significant address bit and A2 is the least significant. During a bus access, A31:2 identify all external addresses to word (4-byte) boundaries. The byte enable signals indicate the selected byte in each word. During burst accesses, A3 and A2 increment to indicate successive addresses. |
| D31:0 | I/O S(L) H(Z) B(Z) R(Z) | DATA BUS carries 32, 16, or 8-bit data quantities depending on bus width configuration. The least significant bit of the data is carried on D0 and the most significant on D31. The lower 8 data lines (D7:0) are used when the bus is configured for 8-bit data. When configured for 16-bit data, D15:0 are used. |
| DP3:0 | I/O S(L) H(Z) B(Z) R(Z) | DATA PARITY carries parity information for the data bus. Each parity bit is assigned a group of 8 data bus pins as follows: DP3 generates/checks parity for D31:24 DP2 generates/checks parity for D23:16 DP1 generates/checks parity for D15:8 DP0 generates/checks parity for D7:0 Parity information is generated for a processor write cycle and is checked for a processor read cycle. Parity checking and polarity are programmable. Parity generation/checking is only performed for the size of the data accessed. |
| PCHK | O H(Q) B(Q) R(1) | PARITY CHECK indicates the result of a parity check operation. An asserted PCHK indicates that the previous bus read access resulted in a parity check error. |
| BE3:0 | O H(Z) B(Z) R(1) | BYTE ENABLES select which of the four bytes addressed by A31:2 are active during a bus access. Byte enable encoding is dependent on the bus width of the memory region accessed: <i>32-bit bus:</i> BE3 enables D31:24 BE2 enables D23:16 BE1 enables D15:8 BE0 enables D7:0 <i>16-bit bus:</i> BE3 becomes Byte High Enable (enables D15:8) BE2 is not used (state is undefined) BE1 becomes Address Bit 1 (A1) BE0 becomes Byte Low Enable (enables D7:0) <i>8-bit bus:</i> BE3 is not used (state is undefined) BE2 is not used (state is undefined) BE1 Address Bit 1 (A1) BE0 Address Bit 0 (A0) |
| W/R | O H(Z) B(Z) R(0) | WRITE/READ is low for read accesses and high for write accesses. W/R becomes valid during the address phase of a bus cycle and remains valid until the end of the cycle for non-pipelined accesses. For pipelined accesses, W/R changes state when the next address is presented. 0= Read 1= Write |
| D/C | O H(Z) B(Z) R(0) | DATA/CODE indicates that a bus access is a data access or an instruction access. D/C has the same timing as W/R. 0 = Code 1 = Data |

Table 7. 80960Hx Processor Family Pin Descriptions (Sheet 2 of 4)

| Name | Type | Description |
|--------------|---------------------------|--|
| SUP | ○ H(Z) B(Z) R(1) | SUPERVISOR ACCESS indicates whether the current bus access originates from a request issued while in supervisor mode or user mode. SUP can be used by the memory subsystem to isolate supervisor code and data structures from non-supervisor access. 0 = Supervisor Mode 1 = User Mode |
| ADS | ○ H(Z) B(Z) R(1) | ADDRESS STROBE indicates a valid address and the start of a new bus access. ADS is asserted for the first clock of a bus access. |
| READY | I S(L) | READY , when enabled for a memory region, is asserted by the memory subsystem to indicate the completion of a data transfer. READY is used to indicate that read data on the bus is valid, or that a write transfer has completed. READY works in conjunction with the internal wait state generator to accommodate various memory speeds. READY is sampled after any programmed wait states: During each data cycle of a burst access During the data cycle of a non-burst access |
| BTERM | I S(L) | BURST TERMINATE , when enabled for a memory region, is asserted by the memory subsystem to terminate a burst access in progress. When BTERM is asserted, the current burst access is terminated and another address cycle occurs. |
| WAIT | ○ H(Z) B(Z) R(1) | WAIT indicates the status of the internal wait-state generator. WAIT is asserted when the internal wait state generator generates N _{WAD} , N _{RAD} , N _{WDD} and N _{RDD} wait states. WAIT can be used to derive a write data strobe. |
| BLAST | ○ H(Z) B(Z) R(1) | BURST LAST indicates the last transfer in a bus access. BLAST is asserted in the last data transfer of burst and non-burst accesses after the internal wait-state generator reaches zero. BLAST remains active as long as wait states are inserted via the READY pin. BLAST becomes inactive after the final data transfer in a bus cycle. |
| DT/R | ○ H(Z) B(Z) R(0) | DATA TRANSMIT/RECEIVE indicates direction for data transceivers. DT/R is used with DEN to provide control for data transceivers connected to the data bus. DT/R is driven low to indicate the processor expects data (a read cycle). DT/R is driven high when the processor is "transmitting" data (a store cycle). DT/R only changes state when DEN is high. 0 = Data Receive 1 = Data Transmit |
| DEN | ○ H(Z) B(Z) R(1) | DATA ENABLE indicates data transfer cycles during a bus access. DEN is asserted at the start of the first data cycle in a bus access and de-asserted at the end of the last data cycle. DEN remains asserted for an entire bus request, even when that request spans several bus accesses. For example, a lq _d instruction starting at an unaligned quad word boundary is one bus request spanning at least two bus accesses. DEN remains asserted throughout all the accesses (including ADS states) and de-asserts when the lq _d instruction request is satisfied. DEN is used with DT/R to provide control for data transceivers connected to the data bus. DEN remains asserted for sequential reads from pipelined memory regions. |
| LOCK | ○ H(Z) B(Z) R(1) | BUS LOCK indicates that an atomic read-modify-write operation is in progress. LOCK may be used by the memory subsystem to prevent external agents from accessing memory that is currently involved in an atomic operation (e.g., a semaphore). LOCK is asserted in the first clock of an atomic operation and de-asserted when BLAST is deasserted in the last bus cycle. |

Table 7. 80960Hx Processor Family Pin Descriptions (Sheet 3 of 4)

| Name | Type | Description | | | | | | | | | | | | | | | | | | | | |
|---|---------------------------|---|------------|----------|--|-------|---|-------|---|-------|--|-------|---|-------|---|-------|----------|-------|------------------------------|-------|----------|-------|
| HOLD | I S(L) | HOLD REQUEST signals that an external agent requests access to the processor's address, data, and control buses. When HOLD is asserted, the processor: Completes the current bus request. Asserts HOLDA and floats the address, data, and control buses. When HOLD is deasserted, the HOLDA pin is deasserted and the processor reassumes control of the address, data, and control pins. | | | | | | | | | | | | | | | | | | | | |
| HOLDA | O H(1) B(0) R(Q) | HOLD ACKNOWLEDGE indicates to an external master that the processor has relinquished control of the bus. The processor grants HOLD requests and enters the HOLDA state while the RESET pin is asserted. HOLDA is never granted while LOCK is asserted. | | | | | | | | | | | | | | | | | | | | |
| BOFF | I S(L) | BUS BACKOFF forces the processor to immediately relinquish control of the bus on the next clock cycle. When READY/BTERM is enabled and: When BOFF is asserted, the address, data, and control buses are floated on the next clock cycle and the current access is aborted. When BOFF is deasserted, the processor resumes by regenerating the aborted bus access. See Figure 16 on page 40 for BOFF timing requirements. | | | | | | | | | | | | | | | | | | | | |
| BREQ | O H(Q) B(Q) R(0) | BUS REQUEST indicates that a bus request is pending in the bus controller. BREQ does not indicate whether or not the processor is stalled. See BSTALL for processor stall status. BREQ can be used with BSTALL to indicate to an external bus arbiter the processor's bus ownership requirements. | | | | | | | | | | | | | | | | | | | | |
| BSTALL | O H(Q) B(Q) R(0) | BUS STALL indicates that the processor has stalled pending the result of a request in the bus controller. When BSTALL is asserted, the processor must regain bus ownership to continue processing (i.e., it can no longer execute strictly out of on-chip cache memory). | | | | | | | | | | | | | | | | | | | | |
| CT3:0 | O H(Z) B(Z) R(Z) | CYCLE TYPE indicates the type of bus cycle currently being started or processor state. CT3:0 encoding follows: <table style="margin-left: 20px;"> <thead> <tr> <th>Cycle Type</th> <th>ADSCT3:0</th> </tr> </thead> <tbody> <tr> <td>Program-initiated access using 8-bit bus</td> <td>00000</td> </tr> <tr> <td>Program-initiated access using 16-bit bus</td> <td>00001</td> </tr> <tr> <td>Program-initiated access using 32-bit bus</td> <td>00010</td> </tr> <tr> <td>Event-initiated access using 8-bit bus</td> <td>00100</td> </tr> <tr> <td>Event-initiated access using 16-bit bus</td> <td>00101</td> </tr> <tr> <td>Event-initiated access using 32-bit bus</td> <td>00110</td> </tr> <tr> <td>Reserved</td> <td>00X11</td> </tr> <tr> <td>Reserved for future products</td> <td>01XXX</td> </tr> <tr> <td>Reserved</td> <td>1XXXX</td> </tr> </tbody> </table> | Cycle Type | ADSCT3:0 | Program-initiated access using 8-bit bus | 00000 | Program-initiated access using 16-bit bus | 00001 | Program-initiated access using 32-bit bus | 00010 | Event-initiated access using 8-bit bus | 00100 | Event-initiated access using 16-bit bus | 00101 | Event-initiated access using 32-bit bus | 00110 | Reserved | 00X11 | Reserved for future products | 01XXX | Reserved | 1XXXX |
| Cycle Type | ADSCT3:0 | | | | | | | | | | | | | | | | | | | | | |
| Program-initiated access using 8-bit bus | 00000 | | | | | | | | | | | | | | | | | | | | | |
| Program-initiated access using 16-bit bus | 00001 | | | | | | | | | | | | | | | | | | | | | |
| Program-initiated access using 32-bit bus | 00010 | | | | | | | | | | | | | | | | | | | | | |
| Event-initiated access using 8-bit bus | 00100 | | | | | | | | | | | | | | | | | | | | | |
| Event-initiated access using 16-bit bus | 00101 | | | | | | | | | | | | | | | | | | | | | |
| Event-initiated access using 32-bit bus | 00110 | | | | | | | | | | | | | | | | | | | | | |
| Reserved | 00X11 | | | | | | | | | | | | | | | | | | | | | |
| Reserved for future products | 01XXX | | | | | | | | | | | | | | | | | | | | | |
| Reserved | 1XXXX | | | | | | | | | | | | | | | | | | | | | |
| XINT7:0 | I A(E) A(L) | EXTERNAL INTERRUPT pins are used to request interrupt service. These pins can be configured in three modes: <i>Dedicated Mode:</i> Each pin is assigned a dedicated interrupt level. Dedicated inputs can be programmed to be level (low or high) or edge (rising or falling) sensitive. <i>Expanded Mode:</i> All eight pins act as a vectored interrupt source. The interrupt pins are level sensitive in this mode. <i>Mixed Mode:</i> The XINT7:5 pins act as dedicated sources and the XINT4:0 pins act as the five most significant bits of a vectored source. The least significant bits of the vectored source are set to "010" internally. | | | | | | | | | | | | | | | | | | | | |
| NMI | I A(E) | NON-MASKABLE INTERRUPT causes a non-maskable interrupt event to occur. NMI is the highest priority interrupt source. NMI is falling edge triggered. | | | | | | | | | | | | | | | | | | | | |

Table 7. 80960Hx Processor Family Pin Descriptions (Sheet 4 of 4)

| Name | Type | Description |
|--------|---------------------------|--|
| CLKIN | I | CLOCK INPUT provides the time base for the 80960Hx. All internal circuitry is synchronized to CLKIN. All input and output timings are specified relative to CLKIN. For the 80960HD, the 2x internal clock is derived by multiplying the CLKIN frequency by 2. For the 80960HT, the 3x internal clock is derived by multiplying the CLKIN frequency by 3. |
| RESET | I A(L) | RESET forces the device into reset. RESET causes all external and internal signals to return to their reset state (if defined). The rising edge of RESET starts the processor boot sequence. |
| STEST | I S(L) | SELF TEST , when asserted during the rising edge of RESET , causes the processor to execute its built in self-test. |
| FAIL | O H(Q) B(Q) R(O) | FAIL indicates a failure of the processor's built-in self-test performed during initialization. FAIL is asserted immediately out of reset and toggles during self-test to indicate the status of individual tests. If self-test passes, FAIL is de-asserted and the processor branches to the user's initialization code. When self-test fails, the FAIL pin asserts and the processor ceases execution. |
| ONCE | I | ON-CIRCUIT EMULATION control: the processor samples this pin during reset. If it is asserted low at the end of reset, the processor enters ONCE mode. In ONCE mode, the processor stops all clocks and floats all output pins except the TDO pin. ONCE uses an internal pull-up resistor; see R_{PU} definition in Table 21 "80960Hx DC Characteristics" on page 32 . Pull this pin high when not in use. |
| TCK | I | TEST CLOCK provides the clocking function for IEEE 1149.1 Boundary Scan testing. |
| TDI | I | TEST DATA INPUT is the serial input pin for IEEE 1149.1 Boundary Scan testing. TDI uses an internal pull-up resistor; see R_{PU} definition in Table 21 "80960Hx DC Characteristics" on page 32 . |
| TDO | O | TEST DATA OUTPUT is the serial output pin for IEEE 1149.1 Boundary Scan testing. ONCE does not disable this pin. |
| TRST | I | TEST RESET asynchronously resets the Test Access Port (TAP) controller. TRST must be held low at least 10,000 clock cycles after power-up. One method is to provide TRST with a separate power-on-reset circuit. TRST includes an internal pull-up resistor; see R_{PU} definition in Table 21 "80960Hx DC Characteristics" on page 32 . Pull this pin low when not in use. |
| TMS | I | TEST MODE SELECT is sampled at the rising edge of TCK . TCK controls the sequence of TAP controller state changes for IEEE 1149.1 Boundary Scan testing. TMS uses an internal pull-up resistor; see R_{PU} definition in Table 21 "80960Hx DC Characteristics" on page 32 . |
| VCC5 | I | 5 V REFERENCE VOLTAGE input is the reference voltage for the 5 V-tolerant I/O buffers. Connect this signal to +5 V for use with inputs which exceed 3.3 V. When all inputs are from 3.3 V components, connect this signal to 3.3 V. |
| VCCPLL | I | PLL VOLTAGE is the +3.3 VDC analog input for the PLL. |
| VOLDET | O | VOLTAGE DETECT signal allows external system logic to distinguish between a 5 V 80960Cx processor and the 3.3 V 80960Hx processor. This signal is active low for a 3.3 V 80960Hx (it is high impedance for 5 V 80960Cx). This pin is available only on the PGA version. 0 = 80960Hx 1 = 80960Cx |

3.2 80960Hx Mechanical Data

3.2.1 80960Hx PGA Pinout

Figure 2 depicts the complete 80960Hx PGA pinout as viewed from the top side of the component (i.e., pins facing down). Figure 3 shows the complete 80960Hx PGA pinout as viewed from the pin-side of the package (i.e., pins facing up). Table 9 lists the 80960Hx pin names with package location. See Section 4.3, “Recommended Connections” on page 30 for specifications and recommended connections.

Figure 2. 80960Hx 168-Pin PGA Pinout — View from Top (Pins Facing Down)

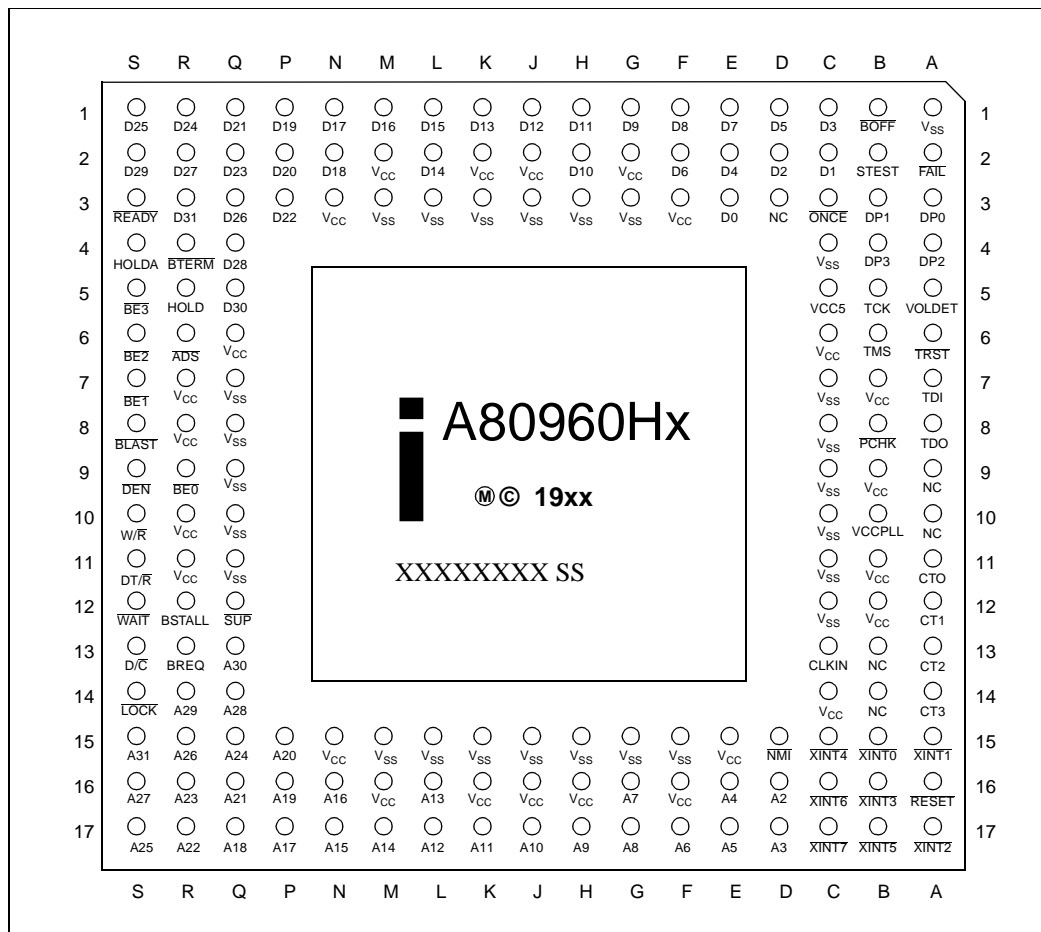


Figure 3. 80960Hx 168-Pin PGA Pinout — View from Bottom (Pins Facing Up)

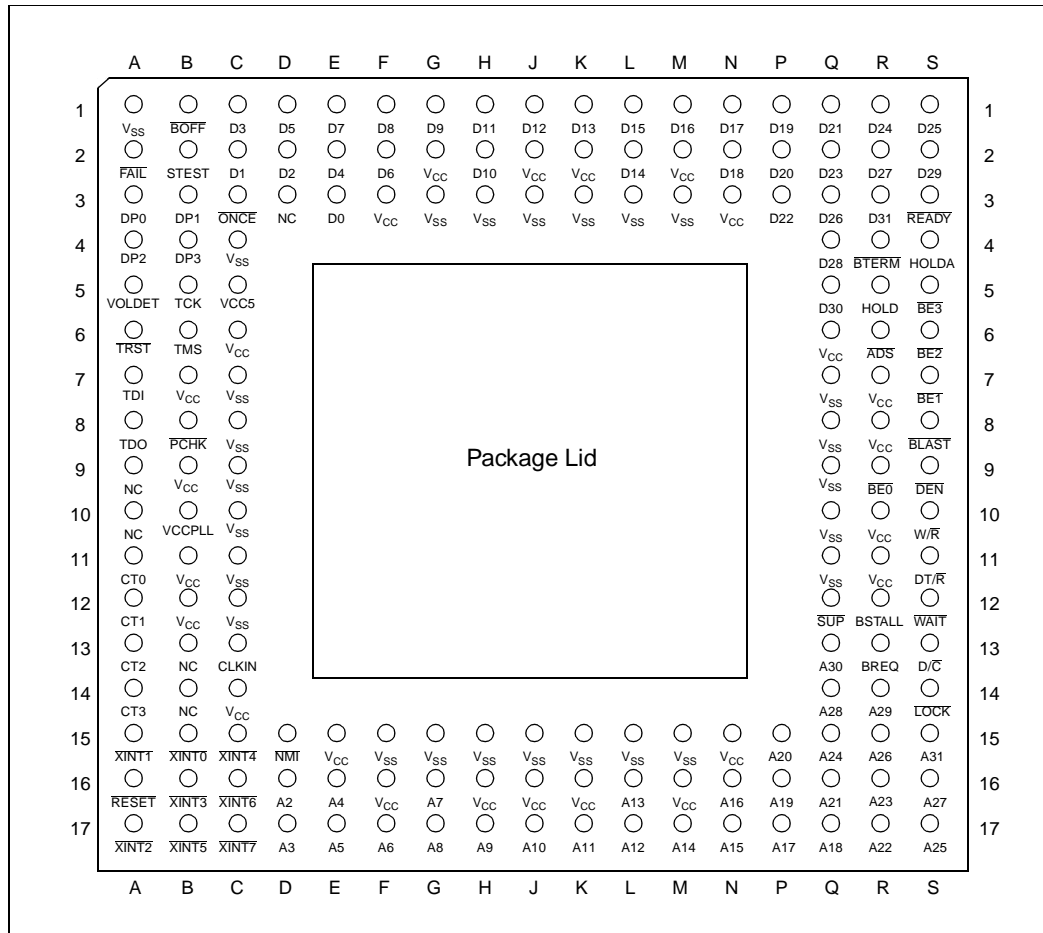


Table 8. 80960Hx 168-Pin PGA Pinout — Signal Name Order (Sheet 1 of 2)

| Signal Name | PGA Pin | Signal Name | PGA Pin | Signal Name | PGA Pin | Signal Name | PGA Pin |
|-------------|---------|-------------|---------|-------------|---------|-----------------|---------|
| A2 | D16 | ADS | R6 | D14 | L2 | LOCK | S14 |
| A3 | D17 | BE0 | R9 | D15 | L1 | NC | A9 |
| A4 | E16 | BE1 | S7 | D16 | M1 | NC | A10 |
| A5 | E17 | BE2 | S6 | D17 | N1 | NC | B13 |
| A6 | F17 | BE3 | S5 | D18 | N2 | NC | B14 |
| A7 | G16 | BLAST | S8 | D19 | P1 | NC | D3 |
| A8 | G17 | BOFF | B1 | D20 | P2 | NMI | D15 |
| A9 | H17 | BREQ | R13 | D21 | Q1 | ONCE | C3 |
| A10 | J17 | BSTALL | R12 | D22 | P3 | PCHK | B8 |
| A11 | K17 | BTERM | R4 | D23 | Q2 | READY | S3 |
| A12 | L17 | CLKIN | C13 | D24 | R1 | RESET | A16 |
| A13 | L16 | CT0 | A11 | D25 | S1 | STEST | B2 |
| A14 | M17 | CT1 | A12 | D26 | Q3 | SUP | Q12 |
| A15 | N17 | CT2 | A13 | D27 | R2 | TCK | B5 |
| A16 | N16 | CT3 | A14 | D28 | Q4 | TDI | A7 |
| A17 | P17 | D/C | S13 | D29 | S2 | TDO | A8 |
| A18 | Q17 | D0 | E3 | D30 | Q5 | TMS | B6 |
| A19 | P16 | D1 | C2 | D31 | R3 | TRST | A6 |
| A20 | P15 | D2 | D2 | DEN | S9 | V _{CC} | B7 |
| A21 | Q16 | D3 | C1 | DP0 | A3 | V _{CC} | B9 |
| A22 | R17 | D4 | E2 | DP1 | B3 | V _{CC} | B11 |
| A23 | R16 | D5 | D1 | DP2 | A4 | V _{CC} | B12 |
| A24 | Q15 | D6 | F2 | DP3 | B4 | V _{CC} | C6 |
| A25 | S17 | D7 | E1 | DT/R | S11 | V _{CC} | C14 |
| A26 | R15 | D8 | F1 | FAIL | A2 | V _{CC} | E15 |
| A27 | S16 | D9 | G1 | — | — | V _{CC} | F3 |
| A28 | Q14 | D10 | H2 | — | — | V _{CC} | F16 |
| A29 | R14 | D11 | H1 | — | — | V _{CC} | G2 |
| A30 | Q13 | D12 | J1 | HOLD | R5 | V _{CC} | H16 |
| A31 | S15 | D13 | K1 | HOLDA | S4 | V _{CC} | J2 |

Table 8. 80960Hx 168-Pin PGA Pinout — Signal Name Order (Sheet 2 of 2)

| Signal Name | PGA Pin | Signal Name | PGA Pin | Signal Name | PGA Pin | Signal Name | PGA Pin |
|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|---------|
| V _{CC} | J16 | VCCPLL | B10 | V _{SS} | H3 | V _{SS} | Q10 |
| V _{CC} | K2 | VOLDET | A5 | V _{SS} | H15 | V _{SS} | Q11 |
| V _{CC} | K16 | V _{SS} | A1 | V _{SS} | J3 | W/R | S10 |
| V _{CC} | M2 | V _{SS} | C4 | V _{SS} | J15 | WAIT | S12 |
| V _{CC} | M16 | V _{SS} | C7 | V _{SS} | K3 | XINT0 | B15 |
| V _{CC} | N3 | V _{SS} | C8 | V _{SS} | K15 | XINT1 | A15 |
| V _{CC} | N15 | V _{SS} | C9 | V _{SS} | L3 | XINT2 | A17 |
| V _{CC} | Q6 | V _{SS} | C10 | V _{SS} | L15 | XINT3 | B16 |
| V _{CC} | R7 | V _{SS} | C11 | V _{SS} | M3 | XINT4 | C15 |
| V _{CC} | R8 | V _{SS} | C12 | V _{SS} | M15 | XINT5 | B17 |
| V _{CC} | R10 | V _{SS} | F15 | V _{SS} | Q7 | XINT6 | C16 |
| V _{CC} | R11 | V _{SS} | G3 | V _{SS} | Q8 | XINT7 | C17 |
| VCC5 | C5 | V _{SS} | G15 | V _{SS} | Q9 | — | — |

Table 9. 80960Hx 168-Pin PGA Pinout — Pin Number Order (Sheet 1 of 2)

| PGA Pin | Signal Name | PGA Pin | Signal Name | PGA Pin | Signal Name | PGA Pin | Signal Name |
|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|
| A1 | V _{SS} | B14 | NC | E15 | V _{CC} | K15 | V _{SS} |
| A2 | FAIL | B15 | XINT0 | E16 | A4 | K16 | V _{CC} |
| A3 | DP0 | B16 | XINT3 | E17 | A5 | K17 | A11 |
| A4 | DP2 | B17 | XINT5 | F1 | D8 | L1 | D15 |
| A5 | VOLDET | C1 | D3 | F2 | D6 | L2 | D14 |
| A6 | TRST | C2 | D1 | F3 | V _{CC} | L3 | V _{SS} |
| A7 | TDI | C3 | ONCE | F15 | V _{SS} | L15 | V _{SS} |
| A8 | TDO | C4 | V _{SS} | F16 | V _{CC} | L16 | A13 |
| A9 | NC | C5 | VCC5 | F17 | A6 | L17 | A12 |
| A10 | NC | C6 | V _{CC} | G1 | D9 | M1 | D16 |
| A11 | CT0 | C7 | V _{SS} | G2 | V _{CC} | M2 | V _{CC} |
| A12 | CT1 | C8 | V _{SS} | G3 | V _{SS} | M3 | V _{SS} |
| A13 | CT2 | C9 | V _{SS} | G15 | V _{SS} | M15 | V _{SS} |
| A14 | CT3 | C10 | V _{SS} | G16 | A7 | M16 | V _{CC} |
| A15 | XINT1 | C11 | V _{SS} | G17 | A8 | M17 | A14 |
| A16 | RESET | C12 | V _{SS} | H1 | D11 | N1 | D17 |
| A17 | XINT2 | C13 | CLKIN | H2 | D10 | N2 | D18 |
| B1 | BOFF | C14 | V _{CC} | H3 | V _{SS} | N3 | V _{CC} |
| B2 | STEST | C15 | XINT4 | H15 | V _{SS} | N15 | V _{CC} |
| B3 | DP1 | C16 | XINT6 | H16 | V _{CC} | N16 | A16 |
| B4 | DP3 | C17 | XINT7 | H17 | A9 | N17 | A15 |
| B5 | TCK | D1 | D5 | J1 | D12 | P1 | D19 |
| B6 | TMS | D2 | D2 | J2 | V _{CC} | P2 | D20 |
| B7 | V _{CC} | D3 | NC | J3 | V _{SS} | P3 | D22 |
| B8 | PCHK | D15 | NMI | J15 | V _{SS} | P15 | A20 |
| B9 | V _{CC} | D16 | A2 | J16 | V _{CC} | P16 | A19 |
| B10 | VCCPLL | D17 | A3 | J17 | A10 | P17 | A17 |
| B11 | V _{CC} | E1 | D7 | K1 | D13 | Q1 | D21 |
| B12 | V _{CC} | E2 | D4 | K2 | V _{CC} | Q2 | D23 |
| B13 | NC | E3 | D0 | K3 | V _{SS} | Q3 | D26 |

Table 9. 80960Hx 168-Pin PGA Pinout — Pin Number Order (Sheet 2 of 2)

| PGA Pin | Signal Name | PGA Pin | Signal Name | PGA Pin | Signal Name | PGA Pin | Signal Name |
|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|
| Q4 | D28 | Q16 | A21 | R11 | V _{CC} | S6 | BE ₂ |
| Q5 | D30 | Q17 | A18 | R12 | BSTALL | S7 | BE ₁ |
| Q6 | V _{CC} | R1 | D24 | R13 | BREQ | S8 | BLAST |
| Q7 | V _{SS} | R2 | D27 | R14 | A29 | S9 | DN |
| Q8 | V _{SS} | R3 | D31 | R15 | A26 | S10 | W/R |
| Q9 | V _{SS} | R4 | BTERM | R16 | A23 | S11 | DT/R |
| Q10 | V _{SS} | R5 | HOLD | R17 | A22 | S12 | WAIT |
| Q11 | V _{SS} | R6 | ADS | S1 | D25 | S13 | D/C |
| Q12 | SUP | R7 | V _{CC} | S2 | D29 | S14 | LOCK |
| Q13 | A30 | R8 | V _{CC} | S3 | READY | S15 | A31 |
| Q14 | A28 | R9 | BE ₀ | S4 | HOLDA | S16 | A27 |
| Q15 | A24 | R10 | V _{CC} | S5 | BE ₃ | S17 | A25 |

3.2.2 80960Hx PQ4 Pinout

Figure 4. 80960Hx 208-Pin PQ4 Pinout

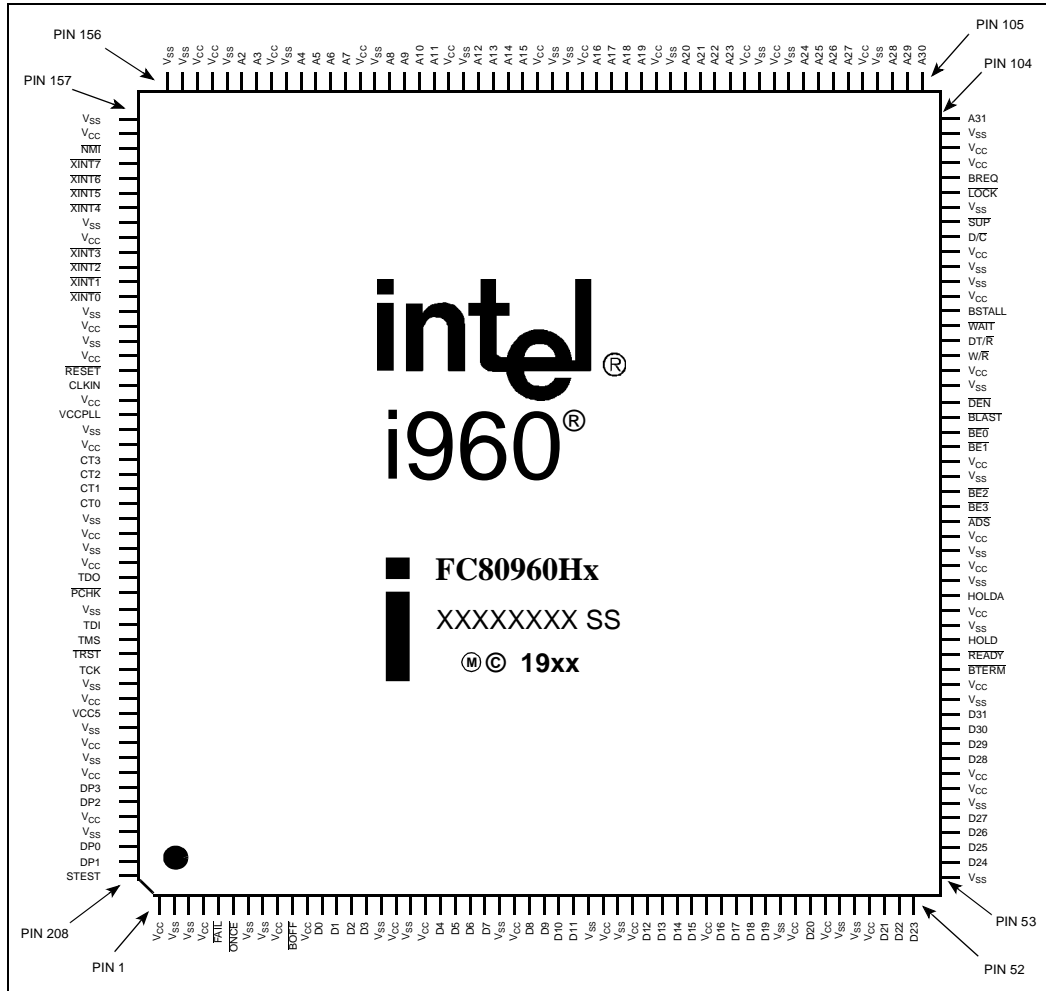


Table 10. 80960Hx PQ4 Pinout — Signal Name Order (Sheet 1 of 2)

| Signal Name | PQ4 Pin | Signal Name | PQ4 Pin | Signal Name | PQ4 Pin | Signal Name | PQ4 Pin |
|-------------|---------|-------------|---------|-------------|---------|-----------------|---------|
| A2 | 151 | BE0 | 83 | D16 | 39 | PCHK | 189 |
| A3 | 150 | BE1 | 82 | D17 | 40 | READY | 68 |
| A4 | 147 | BE2 | 79 | D18 | 41 | RESET | 174 |
| A5 | 146 | BE3 | 78 | D19 | 42 | STEST | 208 |
| A6 | 145 | BLAST | 84 | D20 | 45 | SUP | 97 |
| A7 | 144 | BOFF | 10 | D21 | 50 | TCK | 194 |
| A8 | 141 | BREQ | 100 | D22 | 51 | TDI | 191 |
| A9 | 140 | BSTALL | 91 | D23 | 52 | TDO | 188 |
| A10 | 139 | BTERM | 67 | D24 | 54 | TMS | 192 |
| A11 | 138 | CLKIN | 175 | D25 | 55 | TRST | 193 |
| A12 | 135 | CT0 | 183 | D26 | 56 | V _{CC} | 1 |
| A13 | 134 | CT1 | 182 | D27 | 57 | V _{CC} | 4 |
| A14 | 133 | CT2 | 181 | D28 | 61 | V _{CC} | 9 |
| A15 | 132 | CT3 | 180 | D29 | 62 | V _{CC} | 11 |
| A16 | 127 | D/C | 96 | D30 | 63 | V _{CC} | 17 |
| A17 | 126 | D0 | 12 | D31 | 64 | V _{CC} | 19 |
| A18 | 125 | D1 | 13 | DEN | 85 | V _{CC} | 25 |
| A19 | 124 | D2 | 14 | DP0 | 206 | V _{CC} | 31 |
| A20 | 121 | D3 | 15 | DP1 | 207 | V _{CC} | 33 |
| A21 | 120 | D4 | 20 | DP2 | 203 | V _{CC} | 38 |
| A22 | 119 | D5 | 21 | DP3 | 202 | V _{CC} | 44 |
| A23 | 118 | D6 | 22 | DT/R | 89 | V _{CC} | 46 |
| A24 | 113 | D7 | 23 | FAIL | 5 | V _{CC} | 49 |
| A25 | 112 | D8 | 26 | — | — | V _{CC} | 59 |
| A26 | 111 | D9 | 27 | — | — | V _{CC} | 60 |
| A27 | 110 | D10 | 28 | — | — | V _{CC} | 66 |
| A28 | 107 | D11 | 29 | HOLD | 69 | V _{CC} | 71 |
| A29 | 106 | D12 | 34 | HOLDA | 72 | V _{CC} | 74 |
| A30 | 105 | D13 | 35 | LOCK | 99 | V _{CC} | 76 |
| A31 | 104 | D14 | 36 | NMI | 159 | V _{CC} | 81 |
| ADS | 77 | D15 | 37 | ONCE | 6 | V _{CC} | 87 |

Table 10. 80960Hx PQ4 Pinout — Signal Name Order (Sheet 2 of 2)

| Signal Name | PQ4 Pin | Signal Name | PQ4 Pin | Signal Name | PQ4 Pin | Signal Name | PQ4 Pin |
|-----------------|---------|--------------------|---------|-----------------|---------|-----------------|---------|
| V _{CC} | 92 | V _{CC} | 187 | V _{SS} | 70 | V _{SS} | 164 |
| V _{CC} | 95 | V _{CC} | 196 | V _{SS} | 73 | V _{SS} | 170 |
| V _{CC} | 101 | V _{CC} | 199 | V _{SS} | 75 | V _{SS} | 172 |
| V _{CC} | 102 | V _{CC} | 201 | V _{SS} | 80 | V _{SS} | 178 |
| V _{CC} | 109 | V _{CC} | 204 | V _{SS} | 86 | V _{SS} | 184 |
| V _{CC} | 115 | V _{CC5} | 197 | V _{SS} | 93 | V _{SS} | 186 |
| V _{CC} | 117 | V _{CCPLL} | 177 | V _{SS} | 94 | V _{SS} | 190 |
| V _{CC} | 123 | V _{SS} | 2 | V _{SS} | 98 | V _{SS} | 195 |
| V _{CC} | 128 | V _{SS} | 3 | V _{SS} | 103 | V _{SS} | 198 |
| V _{CC} | 131 | V _{SS} | 7 | V _{SS} | 108 | V _{SS} | 200 |
| V _{CC} | 137 | V _{SS} | 8 | V _{SS} | 114 | V _{SS} | 205 |
| V _{CC} | 143 | V _{SS} | 16 | V _{SS} | 116 | W/R | 88 |
| V _{CC} | 149 | V _{SS} | 18 | V _{SS} | 122 | WAIT | 90 |
| V _{CC} | 153 | V _{SS} | 24 | V _{SS} | 129 | XINT0 | 169 |
| V _{CC} | 154 | V _{SS} | 30 | V _{SS} | 130 | XINT1 | 168 |
| V _{CC} | 158 | V _{SS} | 32 | V _{SS} | 136 | XINT2 | 167 |
| V _{CC} | 165 | V _{SS} | 43 | V _{SS} | 142 | XINT3 | 166 |
| V _{CC} | 171 | V _{SS} | 47 | V _{SS} | 148 | XINT4 | 163 |
| V _{CC} | 173 | V _{SS} | 48 | V _{SS} | 152 | XINT5 | 162 |
| V _{CC} | 176 | V _{SS} | 53 | V _{SS} | 155 | XINT6 | 161 |
| V _{CC} | 179 | V _{SS} | 58 | V _{SS} | 156 | XINT7 | 160 |
| V _{CC} | 185 | V _{SS} | 65 | V _{SS} | 157 | — | — |

Table 11. 80960Hx PQ4 Pinout — Pin Number Order (Sheet 1 of 2)

| PQ4 Pin | Signal Name | PQ4 Pin | Signal Name | PQ4 Pin | Signal Name | PQ4 Pin | Signal Name |
|---------|------------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 1 | V _{CC} | 31 | V _{CC} | 61 | D28 | 91 | BSTALL |
| 2 | V _{SS} | 32 | V _{SS} | 62 | D29 | 92 | V _{CC} |
| 3 | V _{SS} | 33 | V _{CC} | 63 | D30 | 93 | V _{SS} |
| 4 | V _{CC} | 34 | D12 | 64 | D31 | 94 | V _{SS} |
| 5 | F _{AIL} | 35 | D13 | 65 | V _{SS} | 95 | V _{CC} |
| 6 | ONCE | 36 | D14 | 66 | V _{CC} | 96 | D/ \bar{C} |
| 7 | V _{SS} | 37 | D15 | 67 | \bar{B} TERM | 97 | \bar{S} UP |
| 8 | V _{SS} | 38 | V _{CC} | 68 | READY | 98 | V _{SS} |
| 9 | V _{CC} | 39 | D16 | 69 | HOLD | 99 | \bar{L} OCK |
| 10 | \bar{B} OFF | 40 | D17 | 70 | V _{SS} | 100 | BREQ |
| 11 | V _{CC} | 41 | D18 | 71 | V _{CC} | 101 | V _{CC} |
| 12 | D0 | 42 | D19 | 72 | HOLDA | 102 | V _{CC} |
| 13 | D1 | 43 | V _{SS} | 73 | V _{SS} | 103 | V _{SS} |
| 14 | D2 | 44 | V _{CC} | 74 | V _{CC} | 104 | A31 |
| 15 | D3 | 45 | D20 | 75 | V _{SS} | 105 | A30 |
| 16 | V _{SS} | 46 | V _{CC} | 76 | V _{CC} | 106 | A29 |
| 17 | V _{CC} | 47 | V _{SS} | 77 | \bar{A} DS | 107 | A28 |
| 18 | V _{SS} | 48 | V _{SS} | 78 | \bar{B} E3 | 108 | V _{SS} |
| 19 | V _{CC} | 49 | V _{CC} | 79 | \bar{B} E2 | 109 | V _{CC} |
| 20 | D4 | 50 | D21 | 80 | V _{SS} | 110 | A27 |
| 21 | D5 | 51 | D22 | 81 | V _{CC} | 111 | A26 |
| 22 | D6 | 52 | D23 | 82 | \bar{B} E1 | 112 | A25 |
| 23 | D7 | 53 | V _{SS} | 83 | \bar{B} E0 | 113 | A24 |
| 24 | V _{SS} | 54 | D24 | 84 | \bar{B} LAST | 114 | V _{SS} |
| 25 | V _{CC} | 55 | D25 | 85 | \bar{D} EN | 115 | V _{CC} |
| 26 | D8 | 56 | D26 | 86 | V _{SS} | 116 | V _{SS} |
| 27 | D9 | 57 | D27 | 87 | V _{CC} | 117 | V _{CC} |
| 28 | D10 | 58 | V _{SS} | 88 | W/R | 118 | A23 |
| 29 | D11 | 59 | V _{CC} | 89 | DT/R | 119 | A22 |
| 30 | V _{SS} | 60 | V _{CC} | 90 | WAIT | 120 | A21 |

Table 11. 80960Hx PQ4 Pinout — Pin Number Order (Sheet 2 of 2)

| PQ4 Pin | Signal Name | PQ4 Pin | Signal Name | PQ4 Pin | Signal Name | PQ4 Pin | Signal Name |
|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 121 | A20 | 143 | V _{CC} | 165 | V _{CC} | 187 | V _{CC} |
| 122 | V _{SS} | 144 | A7 | 166 | XINT3 | 188 | TDO |
| 123 | V _{CC} | 145 | A6 | 167 | XINT2 | 189 | PCHK |
| 124 | A19 | 146 | A5 | 168 | XINT1 | 190 | V _{SS} |
| 125 | A18 | 147 | A4 | 169 | XINT0 | 191 | TDI |
| 126 | A17 | 148 | V _{SS} | 170 | V _{SS} | 192 | TMS |
| 127 | A16 | 149 | V _{CC} | 171 | V _{CC} | 193 | TRST |
| 128 | V _{CC} | 150 | A3 | 172 | V _{SS} | 194 | TCK |
| 129 | V _{SS} | 151 | A2 | 173 | V _{CC} | 195 | V _{SS} |
| 130 | V _{SS} | 152 | V _{SS} | 174 | RESET | 196 | V _{CC} |
| 131 | V _{CC} | 153 | V _{CC} | 175 | CLKIN | 197 | VCC5 |
| 132 | A15 | 154 | V _{CC} | 176 | V _{CC} | 198 | V _{SS} |
| 133 | A14 | 155 | V _{SS} | 177 | VCCPLL | 199 | V _{CC} |
| 134 | A13 | 156 | V _{SS} | 178 | V _{SS} | 200 | V _{SS} |
| 135 | A12 | 157 | V _{SS} | 179 | V _{CC} | 201 | V _{CC} |
| 136 | V _{SS} | 158 | V _{CC} | 180 | CT3 | 202 | DP3 |
| 137 | V _{CC} | 159 | NMI | 181 | CT2 | 203 | DP2 |
| 138 | A11 | 160 | XINT7 | 182 | CT1 | 204 | V _{CC} |
| 139 | A10 | 161 | XINT6 | 183 | CT0 | 205 | V _{SS} |
| 140 | A9 | 162 | XINT5 | 184 | V _{SS} | 206 | DP0 |
| 141 | A8 | 163 | XINT4 | 185 | V _{CC} | 207 | DP1 |
| 142 | V _{SS} | 164 | V _{SS} | 186 | V _{SS} | 208 | STEST |

3.3 Package Thermal Specifications

The 80960Hx is specified for operation when T_C (case temperature) is within the range of 0°C – 85°C . T_C may be measured in any environment to determine whether the 80960Hx is within the specified operating range. Measure the case temperature at the center of the top surface, opposite the pins. Refer to [Figure 5](#).

T_A (ambient temperature) is calculated from θ_{CA} (thermal resistance from case to ambient) using the equation:

$$T_A = T_C - P \cdot \theta_{CA}$$

[Table 12](#) shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies (f_{CLKIN}).

Note that T_A is greatly improved by attaching fins or a heatsink to the package. P (maximum power consumption) is calculated by using the typical I_{CC} as tabulated in [Section 4.6, “DC Specifications”](#) on [page 32](#) and V_{CC} of 3.3 V.

Figure 5. Measuring 80960Hx PGA Case Temperature

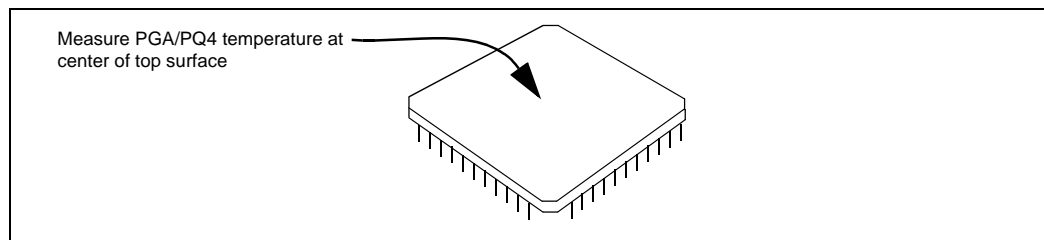


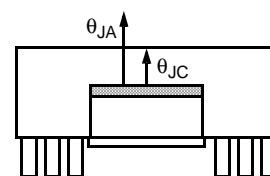
Table 12. Maximum T_A at Various Airflows in °C (PGA Package Only)

| | | Airflow-ft/min (m/sec) | | | | | | |
|-------------------------|------------------------------|------------------------|----------|---------------|---------------|---------------|---------------|----------------|
| | | f_{CLKIN} (MHz) | 0 (0) | 200 (1.01) | 400 (2.03) | 600 (3.04) | 800 (4.06) | 1000 (5.07) |
| Core 1X Bus Clock | T_A with Heatsink* | 25 | 69 | 74 | 78 | 79 | 80 | 80 |
| | | 33 | 63 | 70 | 75 | 77 | 79 | 79 |
| | | 40 | 59 | 67 | 73 | 75 | 77 | 77 |
| | T_A without Heatsink | 25 | 64 | 67 | 71 | 74 | 75 | 76 |
| | | 33 | 56 | 62 | 67 | 70 | 72 | 74 |
| | | 40 | 50 | 56 | 63 | 67 | 69 | 71 |
| Core 2X Bus Clock | T_A with Heatsink* | 16 | 68 | 73 | 77 | 79 | 80 | 80 |
| | | 25 | 58 | 66 | 73 | 75 | 77 | 77 |
| | | 33 | 49 | 60 | 69 | 71 | 74 | 74 |
| | T_A without Heatsink | 40 | 41 | 55 | 65 | 68 | 72 | 72 |
| | | 16 | 62 | 66 | 71 | 73 | 75 | 76 |
| | | 25 | 49 | 56 | 62 | 66 | 68 | 71 |
| Core 3X Bus Clock | T_A with Heatsink* | 33 | 38 | 46 | 55 | 60 | 63 | 66 |
| | | 40 | 27 | 38 | 48 | 55 | 58 | 62 |
| | | 20 | 53 | 63 | 71 | 73 | 76 | 76 |
| | T_A without Heatsink | 25 | 45 | 58 | 67 | 70 | 73 | 73 |
| | | 20 | 43 | 51 | 58 | 63 | 66 | 68 |
| | | 25 | 33 | 42 | 51 | 58 | 61 | 64 |

*0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 13. 80960Hx 168-Pin PGA Package Thermal Characteristics

| Thermal Resistance — °C/Watt | | | | | | |
|--|---------------------------|---------------|---------------|---------------|---------------|----------------|
| Parameter | Airflow — ft./min (m/sec) | | | | | |
| | 0 (0) | 200 (1.01) | 400 (2.03) | 600 (3.07) | 800 (4.06) | 1000 (5.07) |
| θ Junction-to-Case (Case measured as shown in Figure 5) | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 |
| θ Case-to-Ambient (No Heatsink) | 17 | 14 | 11 | 9 | 8 | 7 |
| θ Case-to-Ambient (With Heatsink)* | 13 | 9 | 6 | 5 | 4 | 4 |

**NOTES:**

1. This table applies to 80960Hx PGA plugged into socket or soldered directly to board.
 2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- *0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 14. Maximum T_A at Various Airflows in °C (PQ4 Package Only)

| | | f_{CLKIN} (MHz) | Airflow-ft/min (m/sec) | | | | | |
|-------------------------|------------------------------|----------------------|------------------------|---------------|---------------|---------------|---------------|----------------|
| | | | 0 (0) | 200 (1.01) | 400 (2.03) | 600 (3.04) | 800 (4.06) | 1000 (5.07) |
| Core 1X Bus Clock | T_A with Heatsink* | 25 | 71 | 76 | 79 | 79 | 80 | 80 |
| | | 33 | 67 | 74 | 77 | 77 | 79 | 79 |
| | | 40 | 63 | 71 | 75 | 75 | 77 | 77 |
| | T_A without Heatsink | 25 | 70 | 73 | 75 | 75 | 76 | 76 |
| | | 33 | 65 | 68 | 72 | 72 | 74 | 74 |
| | | 40 | 61 | 65 | 69 | 69 | 71 | 71 |
| Core 2X Bus Clock | T_A with Heatsink* | 16 | 71 | 76 | 79 | 79 | 80 | 80 |
| | | 25 | 62 | 71 | 75 | 75 | 77 | 77 |
| | | 33 | 55 | 66 | 71 | 71 | 74 | 74 |
| | T_A without Heatsink | 40 | 48 | 62 | 68 | 68 | 72 | 72 |
| | | 16 | 69 | 72 | 75 | 75 | 76 | 76 |
| | | 25 | 60 | 64 | 68 | 68 | 71 | 71 |
| Core 3X Bus Clock | T_A with Heatsink* | 33 | 52 | 57 | 63 | 63 | 66 | 66 |
| | | 40 | 42 | 51 | 58 | 58 | 62 | 62 |
| | | 20 | 58 | 68 | 73 | 73 | 76 | 76 |
| | T_A without Heatsink | 25 | 51 | 64 | 70 | 70 | 73 | 73 |
| | | 20 | 56 | 61 | 66 | 66 | 68 | 68 |
| | | 25 | 48 | 55 | 61 | 61 | 64 | 64 |

*0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 15. 80960Hx 208-Pin PQ4 Package Thermal Characteristics

| Thermal Resistance — °C/Watt | | | | | | | |
|---|---------------------------|---------------|---------------|---------------|---------------|----------------|--|
| Parameter | Airflow — ft./min (m/sec) | | | | | | |
| | 0 (0) | 200 (1.01) | 400 (2.03) | 600 (3.07) | 800 (4.06) | 1000 (5.07) | |
| θ Junction-to-Case (Case measured as shown in Figure 5) | 1 | 1 | 1 | 1 | 1 | 1 | |
| θ Case-to-Ambient (No Heatsink) | 12 | 10 | 8 | 8 | 7 | 7 | |
| θ Case-to-Ambient (With Heatsink)* | 11 | 7 | 5 | 5 | 4 | 4 | |

NOTES:

- This table applies to 80960Hx PQ4 plugged into socket or soldered directly to board.
 - $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- *0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

3.4 Heat Sink Adhesives

Intel recommends silicone-based adhesives to attach heat sinks to the PGA package. There is no particular recommendation concerning the PQ4 package.

3.5 PowerQuad4 Plastic Package

The 80960Hx family is available in an improved version of the common 208-lead SQFP plastic package called the PowerQuad4* (PQ4). The PQ4 package dimensions and lead pitch are identical to the SQFP package and the former PQ2 package, so the PQ4 fits into the same board footprint. The advantage of the PQ4 package is the superior thermal conductivity that allows the plastic version of the 80960Hx to operate with the same 0-85°C temperature specifications as the more expensive ceramic PGA package.

The PQ4 package integrates a copper heat sink within the package to dissipate heat effectively. See [Table 14](#) and [Table 15](#).

3.6 Stepping Register Information

The memory-mapped register at FF008710H contains the 80960Hx Device ID. The ID is identical to the ID obtained from a JTAG Query. [Figure 6](#) defines the current 80960Hx Device IDs. The value for device identification is compliant with the IEEE 1149.1 specification and Intel standards. [Table 16](#) describes the fields of the device ID.

Figure 6. 80960Hx Device Identification Register

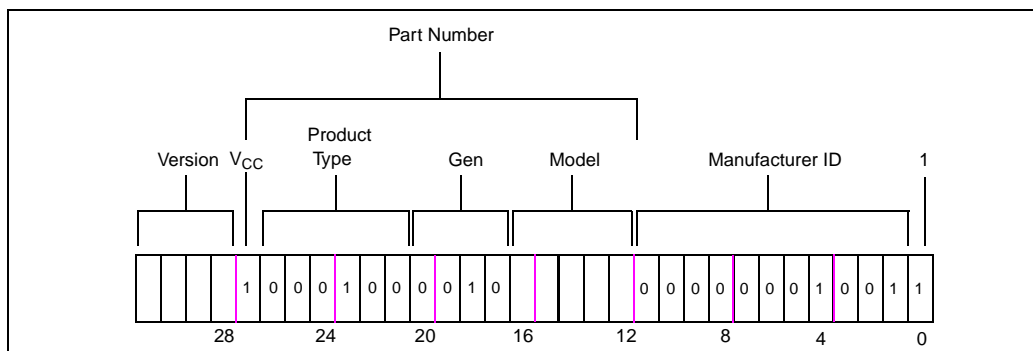


Table 16. Fields of 80960Hx Device ID

| Field | Value | Definition |
|-----------------|------------------------------------|--|
| Version | See Table 18 | Indicates major stepping changes. |
| V _{CC} | 1 = 3.3 V device | Indicates that a device is 3.3 V. |
| Product Type | 00 0100 (Indicates i960 CPU) | Designates type of product. |
| Generation Type | 0010 = H-series | Indicates the generation (or series) the product belongs to. |
| Model | See Table 17 | Indicates member within a series and specific model information. |
| Manufacturer ID | 000 0000 1001 (Indicates Intel) | Manufacturer ID assigned by IEEE. |

Table 17. 80960Hx Device ID Model Types

| Device | Version | V _{CC} | Product | Gen. | Model | Manufacturer ID | '1' |
|---------|-----------------|-----------------|---------|------|-------|-----------------|-----|
| 80960HA | See Table 18 | 1 | 000100 | 0010 | 00000 | 00000001001 | 1 |
| 80960HD | | 1 | 000100 | 0010 | 00001 | 00000001001 | 1 |
| 80960HT | | 1 | 000100 | 0010 | 00010 | 00000001001 | 1 |

Table 18. Device ID Version Numbers for Different Steppings

| Stepping | Version |
|----------|---------|
| A0 | 0000 |
| A1 | 0001 |
| A2 | 0001 |
| B0, B2 | 0010 |

This data sheet applies to the B2 stepping.

3.7 Sources for Accessories

The following is a list of suggested sources for 80960Hx accessories. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

Sockets

- 3M Textool Test and Interconnection Products
6801 River Place Blvd. MS 130-3N-29
Austin, TX 78726-9000
(800) 328-0411 FAX: (800) 932-9373
- Concept Mfg, Inc. (Decoupling Sockets)
400 Walnut St. Suite 609
Redwood City, CA 94063
(415) 365-1162 FAX: (415) 365-1164

Heatsinks/Fins

- Thermalloy, Inc.
2021 West Valley View Lane
Dallas, TX 75234-8993
(972) 243-4321 FAX: (972) 241-4656
- Wakefield Engineering, Inc.
60 Audubon Road
Wakefield, MA 01880
(617) 245-5900 FAX: (617) 246-0874
- Aavid Thermal Technologies, Inc.
One Kool Path
Laconia, NH 03247-0400
(603) 523-3400

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

| Parameter | Maximum Rating |
|---|------------------------|
| Storage Temperature | -65 °C to +150 °C |
| Case Temperature Under Bias | -65oC to +110oC |
| Supply Voltage with respect to V _{SS} | -0.5 V to + 4.6 V |
| Voltage on VCC5 with respect to V _{SS} | -0.5 V to + 6.5 V |
| Voltage on Other Pins with respect to V _{SS} | -0.5 V to VCC5 + 0.5 V |

Notice: This document contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications within this data sheet are subject to change without notice. Verify with your local Intel sales office that you have the latest data sheet before finalizing a design.

Warning: *Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.*

4.2 Operating Conditions

Table 19. Operating Conditions

| Symbol | Parameter | Min | Max | Units |
|---------------------------|---|------|------|-------|
| V _{CC} | Supply Voltage | 3.15 | 3.45 | V |
| VCC5 | Input Protection Bias | 3.15 | 5.5 | V |
| f _{CLKIN} 1xcore | Input Clock Frequency - 1x Core (80960HA) | 16 | 40 | MHz |
| f _{CLKIN} 2xcore | Input Clock Frequency - 2x Core (80960HD) | 16 | 40 | MHz |
| f _{CLKIN} 3xcore | Input Clock Frequency - 3x Core (80960HT) | 16 | 25 | MHz |
| T _C | Case Temp Under Bias (PGA and PQ4 Packages) | 0 | 85 | °C |

4.3 Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} (GND) pins. Every 80960Hx-based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane; every V_{SS} pin must be connected to the ground plane. Pins identified as “NC” —no connect pins—**must not** be connected in the system.

Liberal decoupling capacitance should be placed near the 80960Hx. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high-frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA packages offer the lowest possible inductance.

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, any unused interrupt (XINT7:0, NMI) input should be connected to V_{CC} through a pull-up resistor, as should \overline{BTERM} if not used. Pull-up resistors should be in the range of 20 K Ω for each pin tied high. If \overline{READY} or \overline{HOLD} are not used, the unused input should be connected to ground. **N.C. pins must always remain unconnected.**

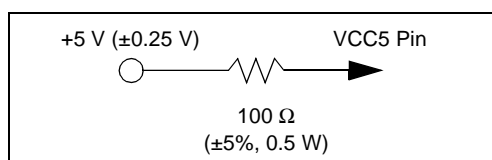
4.4 VCC5 Pin Requirements (V_{DIFF})

In mixed-voltage systems that drive 80960Hx processor inputs in excess of 3.3 V, the VCC5 pin must be connected to the system’s 5 V supply. To limit current flow into the VCC5 pin, there is a limit to the voltage differential between the VCC5 pin and the other V_{CC} pins. The voltage differential between the 80960Hx VCC5 pin and its 3.3 V V_{CC} pins should never exceed 2.25 V. This limit applies to power-up, power-down, and steady-state operation. Table 20 outlines this requirement.

Meeting this requirement ensures proper operation and guarantees that the current draw into the VCC5 pin does not exceed the I_{CC5} specification.

If the voltage difference requirements cannot be met due to system design limitations, an alternate solution may be employed. As shown in Figure 7, a minimum of 100 Ω series resistor may be used to limit the current into the VCC5 pin. This resistor ensures that current drawn by the VCC5 pin does not exceed the maximum rating for this pin.

Figure 7. VCC5 Current-Limiting Resistor



This resistor is not necessary in systems that can guarantee the V_{DIFF} specification.

In 3.3 V-only systems and systems that drive 80960Hx pins from 3.3 V logic, connect the VCC5 pin directly to the 3.3 V V_{CC} plane.

Table 20. V_{DIFF} Specification for Dual Power Supply Requirements (3.3 V, 5 V)

| Sym | Parameter | Min | Max | Units | Notes |
|------------|---------------------------|-----|------|-------|---|
| V_{DIFF} | VCC5- V_{CC} Difference | | 2.25 | V | VCC5 input should not exceed V_{CC} by more than 2.25 V during power-up and power-down, or during steady-state operation. |

4.5 VCCPLL Pin Requirements

If the voltage on the VCCPLL power supply pin exceeds the V_{CC} pin voltage by 0.5 V at any time, including the power up and power down sequences, excessive currents can permanently damage on-chip electrostatic discharge (ESD) protection diodes. The damage can accumulate over multiple episodes.

Pragmatically, this problem only occurs when the VCCPLL and V_{CC} pins are driven by separate power supplies or voltage regulators. Applications that use one power supply for VCCPLL and V_{CC} are not typically at risk. Verify that your application does not allow the VCCPLL voltage to exceed V_{CC} by 0.5 V.

The VCCPL low-pass filter recommended in the Developer's Manual does not promote this problem.

4.6 DC Specifications

Table 21. 80960Hx DC Characteristics (Sheet 1 of 2)

Per the conditions described in Section 4.3, "Recommended Connections" on page 30.

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|---|--|------------------------------|--|---|----------|--|
| V _{IL} | Input Low Voltage | -0.3 | | +0.8 | V | |
| V _{IH} | Input High Voltage | 2.0 | | VCC5 + 0.3 | V | |
| V _{OL} | Output Low Voltage All outputs except FAIL | | | 0.4 0.2 | V | I _{OL} = 3 mA I _{OL} = 100 μA |
| V _{OL} | Output Low Voltage FAIL pin | | | 0.4 | V | I _{OL} = 5 mA |
| V _{OH} | Output High Voltage | 2.4 V _{CC} - 0.2 | | | V V | I _{OH} = -3 mA I _{OH} = -100 μA |
| I _{LI} | Input Leakage Current Non-Test Inputs TDI, TMS, TRST and ONCE | -1 | | 1 -110 | μA μA | 0 ≤ V _{IN} ≤ V _{CC} V _{IN} = 0 V |
| I _{LO} | Output Leakage Current Non-Test Outputs TDO pin | | | 1 5 | μA μA | 0.45 ≤ V _{OUT} ≤ V _{CC} 0.45 ≤ V _{OUT} ≤ V _{CC} |
| I _{CC} Active (Power Supply) | 80960HA 25 33 40 80960HD 32 50 66 80 80960HT 60 75 | | | 579 765 927 631 985 1300 1578 1165 1455 | mA | (4,5) |
| I _{CC} Active (Thermal) | 80960HA 25 33 40 80960HD 32 50 66 80 80960HT 60 75 | | 392 518 628 413 645 851 1034 752 938 | | mA | (4,6) |
| I _{CC} Test (Reset Mode) | 80960HA 25 33 40 80960HD 32 50 66 80 80960HT 60 75 | | | 330 436 528 382 595 785 955 702 878 | mA | (7,8) |
| I _{CC} Test (ONCE mode) | | | | 25 | mA | (7) |

Table 21. 80960Hx DC Characteristics (Sheet 2 of 2)

 Per the conditions described in [Section 4.3, “Recommended Connections”](#) on page 30.

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|--|--|-----|-----|-------------------|------------------|------------------------------|
| I_{CC5} Current on the VCC5 Pin | 80960HA 80960HD 80960HT | | | 200 200 200 | μA | (9) |
| C_{IN} | Input Capacitance for: PQ4 PGA | | | 12 12 | pF pF | $F_C = 1 \text{ MHz}$ (10) |
| C_{OUT} | Output Capacitance of each output pin | | | 12 | pF | $F_C = 1 \text{ MHz}$ (3,10) |
| $C_{I/O}$ | I/O Pin Capacitance | | | 12 | pF | $F_C = 1 \text{ MHz}$ (10) |
| R_{PU} | Internal Pull-Up Resistance for $\overline{\text{ONCE}}$, TMS, TDI and TRST | 30 | 65 | 100 | $\text{k}\Omega$ | |

NOTES:

- I_{CC} Maximum is measured at worst case frequency, V_{CC} , and temperature, with device operating and outputs loaded to the test conditions described in [Section 4.7.1, “AC Test Conditions”](#) on page 37.
- I_{CC} Typical is not tested.
- Output Capacitance is the capacitive load of a floating output.
- Measured with device operating and outputs loaded to the test conditions in [Figure 8 “AC Test Load”](#) on page 37. Input signals rise to V_{CC} and fall to V_{SS} .
- I_{CC} Active (Power Supply) value is provided for selecting your system's power supply. It is measured using one of the worst case instruction mixes with $V_{CC} = 3.45 \text{ V}$. This parameter is characterized but not tested.
- I_{CC} Active (Thermal) value is provided for your system's thermal management. Typical I_{CC} is measured with $V_{CC} = 3.3 \text{ V}$ and temperature = 25°C . This parameter is characterized but not tested.
- I_{CC} Test (Power modes) refers to the I_{CC} values that are tested when the 80960HA/HD/HT is in Reset mode or $\overline{\text{ONCE}}$ mode with $V_{CC} = 3.45 \text{ V}$.
- Worst case is $V_{CC} = 3.45 \text{ V}$, 0°C .
- I_{CC5} is tested at $V_{CC} = 3.0 \text{ V}$, $V_{CC5} = 5.25 \text{ V}$.
- Pin capacitance is characterized, but not tested.

4.7 AC Specifications

Table 22. 80960Hx AC Characteristics (Sheet 1 of 2)

Per conditions in Section 4.2, "Operating Conditions" on page 29 and Section 4.7.1, "AC Test Conditions" on page 37.

| Symbol | Parameter | Min | Max | Units | Notes | |
|--------------------------------------|---|---------|------------|------------|-------|------|
| Input Clock (1,7) | | | | | | |
| T _F | CLKIN Frequency | 80960HA | 16 | 40 | MHz | |
| | | 80960HD | 16 | 40 | MHz | |
| | | 80960HT | 16 | 25 | MHz | |
| T | CLKIN Period | 80960HA | 25 | 62.5 | ns | |
| | | 80960HD | 25 | 62.5 | ns | |
| | | 80960HT | 40 | 62.5 | ns | |
| T _{CS} | CLKIN Period Stability | -250 | +250 | ps | (11) | |
| T _{CH} | CLKIN High Time | 8 | | ns | (11) | |
| T _{CL} | CLKIN Low Time | 80960HA | 8 | | ns | (11) |
| | | 80960HD | 8 | | ns | |
| | | 80960HT | 8 | | ns | |
| T _{CR} | CLKIN Rise Time | 0 | 4 | ns | (11) | |
| T _{CF} | CLKIN Fall Time | 0 | 4 | ns | (11) | |
| Synchronous Outputs (1,2,3,6) | | | | | | |
| T _{OV1} , T _{OH1} | Output Valid Delay and Output Hold for all outputs except DT/R, BLAST and BREQ for 3.3 V and 5 V inputs and I/Os. | 1.5 | 9.5 | ns | | |
| T _{OV2} , T _{OH2} | Output Valid Delay and Output Hold for DT/R | 80960HA | T/2 + 1.5 | T/2 + 9.5 | ns | |
| | | 80960HD | 3T/4 + 1.5 | 3T/4 + 9.5 | ns | |
| | | 80960HT | 5T/6 + 1.5 | 5T/6 + 9.5 | ns | |
| T _{OV3} , T _{OH3} | Output Valid Delay and Output Hold for BLAST | 1.5 | 9 | ns | | |
| T _{OV4} , T _{OH4} | Output Valid Delay and Output Hold for BREQ | 0.5 | 9 | ns | | |
| T _{OV5} , T _{OH5} | Output Valid Delay and Output Hold for A3:2 | 1.5 | 8.5 | | | |
| T _{OF} | Output Float for all outputs | 1.5 | 9 | ns | (11) | |
| Synchronous Inputs (1,7,8,9) | | | | | | |
| T _{IS1} | Input Setup for all inputs except READY, BTERM, HOLD, and BOFF | 2.5 | | ns | | |
| T _{IH1} | Input Hold for all inputs except READY, BTERM, HOLD, and BOFF | 2.5 | | ns | | |
| T _{IS2} | Input Setup for READY, BTERM, HOLD, and BOFF | 6 | | ns | | |

NOTE: See Table 23 "AC Characteristics Notes" on page 36 for all notes related to AC specifications.

Table 22. 80960Hx AC Characteristics (Sheet 2 of 2)

Per conditions in Section 4.2, "Operating Conditions" on page 29 and Section 4.7.1, "AC Test Conditions" on page 37.

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|-------------------------------|-------------------------------|----------------|--------|
| T _{IH2} | Input Hold for $\overline{\text{READY}}$, $\overline{\text{BTERM}}$, HOLD, and $\overline{\text{BOFF}}$ | 2.5 | | ns | |
| Relative Output Timings (1,2,3,6,10) | | | | | |
| T _{AVSH1} | A31:2 Valid to $\overline{\text{ADS}}$ Rising | T - 5 | T + 5 | ns | (10) |
| T _{AVSH2} | BE3:0, W/R, SUP, D/C Valid to $\overline{\text{ADS}}$ Rising | T - 5 | T + 5 | ns | (10) |
| T _{AVEL1} | A31:2 Valid to $\overline{\text{DEN}}$ Falling | T - 5 | T + 5 | ns | (10) |
| T _{AVEL2} | BE3:0, W/R, SUP Valid to $\overline{\text{DEN}}$ Falling | T - 5 | T + 5 | ns | (10) |
| T _{NLQV} | WAIT Falling to Output Data Valid | -5 | 5 | ns | (10) |
| T _{DVNH} | Output Data Valid to WAIT Rising | -5 + N*T | 5 + N*T | ns | (4,10) |
| T _{NLNH} | WAIT Falling to WAIT Rising | -4 + N*T | 4 + N*T | ns | (4,10) |
| T _{NHQX} | Output Data Hold after WAIT Rising | -5 + (N+1)*T | 5 + (N+1)*T | ns | (5,10) |
| T _{EHTV} | DT/R Hold after $\overline{\text{DEN}}$ High | T/2 - 5 | Infinite | ns | (10) |
| T _{TVEL} | DT/R Valid to $\overline{\text{DEN}}$ Falling | 80960HA 80960HD 80960HT | T/2 - 4 T/4 - 4 T/6 - 4 | ns ns ns | (10) |
| Relative Input Timings (1,7,10) | | | | | |
| T _{IS7} | $\overline{\text{XINT7:0}}$, NMI Input Setup | 6 | | ns | (9) |
| T _{IH7} | $\overline{\text{XINT7:0}}$, NMI Input Hold | 2.5 | | ns | (9) |
| T _{IS8} | RESET Input Setup | 3 | | ns | (8) |
| T _{IH8} | RESET Input Hold | T/4 + 1 | | ns | (8) |

NOTE: See Table 23 "AC Characteristics Notes" on page 36 for all notes related to AC specifications.

Table 23. AC Characteristics Notes

| | | | | | |
|--|--|--|--|--|--|
| NOTES: | | | | | |
| 1. See Section 4.8, “AC Timing Waveforms” on page 38 for waveforms and definitions. | | | | | |
| 2. See Figure 25 “Output Delay or Hold vs. Load Capacitance” on page 44 for capacitive derating information for output delays and hold times. | | | | | |
| 3. See Figure 22 “Rise and Fall Time Derating at 85°C and Minimum V _{CC} ” on page 43 for capacitive derating information for rise and fall times. | | | | | |
| 4. Where N is the number of N _{RAD} , N _{RDD} , N _{WAD} or N _{WDD} wait states that are programmed in the Bus Controller Region Table. WAIT never goes active when there are no wait states in an access. | | | | | |
| 5. N = Number of wait states inserted with READY. | | | | | |
| 6. These specifications are guaranteed by the processor. | | | | | |
| 7. These specifications must be met by the system for proper operation of the processor. | | | | | |
| 8. RESET is an asynchronous input that has no required setup and hold time for proper operation. However, to guarantee the device exits the reset mode synchronized to a particular clock edge, the rising edge of RESET must meet setup and hold times to the rising edge of the CLKIN. | | | | | |
| 9. The interrupt pins are synchronized internally by the 80960Hx. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every clock and must be active for at least two consecutive CLKIN rising edges when asserting them asynchronously. To guarantee recognition at a particular clock edge, the setup and hold times shown must be met. | | | | | |
| 10. Relative Output timings are not tested. | | | | | |
| 11. Not tested. | | | | | |
| 12. The processor minimizes changes to the bus signals when transitioning from a bus cycle to an idle bus for the following signals: A31:4, SUP, CT3:0, D/C, LOCK, W/R, BE3:0. | | | | | |

Table 24. 80960Hx Boundary Scan Test Signal Timings

| Symbol | Parameter | Min | Max | Units | Notes |
|---------------------|---|-----|----------|-------|-----------------------|
| T _{BSF} | TCK Frequency | 0 | 8 | MHz | |
| T _{BSC} | TCK Period | 125 | Infinite | ns | |
| T _{BSCH} | TCK High Time | 40 | | ns | Measured at 1.5 V (1) |
| T _{BSCL} | TCK Low Time | 40 | | ns | Measured at 1.5 V (1) |
| T _{BSCR} | TCK Rise Time | | 8 | ns | 0.8 V to 2.0 V (1) |
| T _{BSCF} | TCK Fall Time | | 8 | ns | 2.0 V to 0.8 V (1) |
| T _{BSIS1} | Input Setup to TCK — TDI, TMS | 8 | | ns | |
| T _{BSIH1} | Input Hold from TCK — TDI, TMS | 10 | | ns | |
| T _{BISOV1} | TDO Valid Delay | 3 | 30 | ns | |
| T _{BSOF1} | TDO Float Delay | | 36 | ns | (1) |
| T _{BISOV2} | All Outputs (Non-Test) Valid Delay | 3 | 30 | ns | Relative to TCK |
| T _{BSOF2} | All Outputs (Non-Test) Float Delay | | 36 | ns | Relative to TCK (1) |
| T _{BSIS2} | Input Setup to TCK - All Inputs (Non-Test) | 8 | | ns | |
| T _{BSIH2} | Input Hold from TCK - All Inputs (Non-Test) | 10 | | ns | |

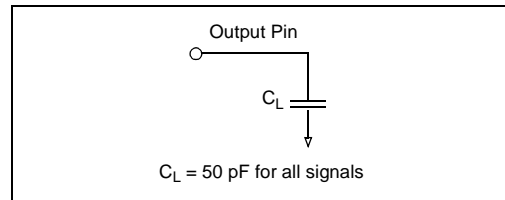
NOTE:

1. Not tested.

4.7.1 AC Test Conditions

AC values are derived using the 50 pF load shown in Figure 8. Figure 25 “Output Delay or Hold vs. Load Capacitance” on page 44, shows how timings vary with load capacitance. Input waveforms (except for CLKIN) are assumed to have a rise and fall time of ≤ 2 ns from 0.8 V to 2.0 V.

Figure 8. AC Test Load



4.8 AC Timing Waveforms

Figure 9. CLKIN Waveform

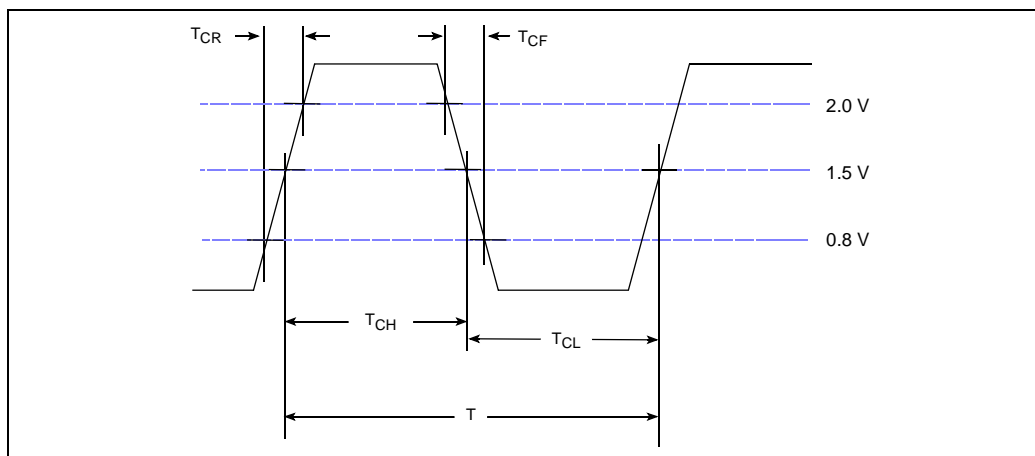


Figure 10. Output Delay Waveform

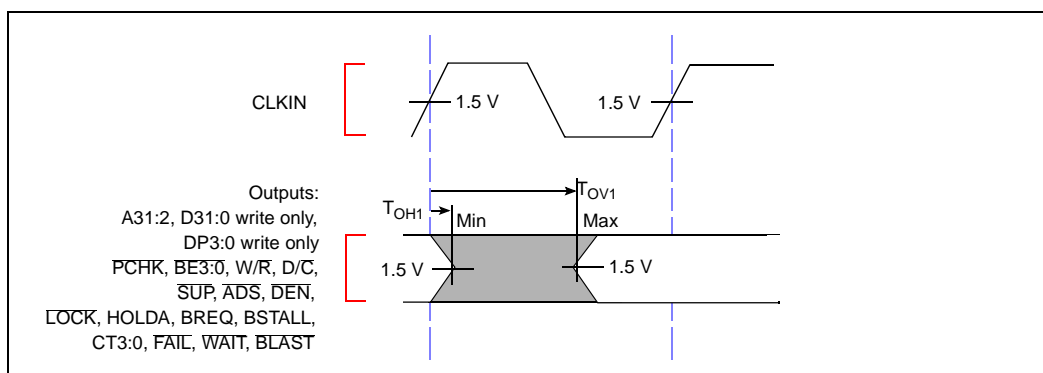


Figure 11. Output Delay Waveform

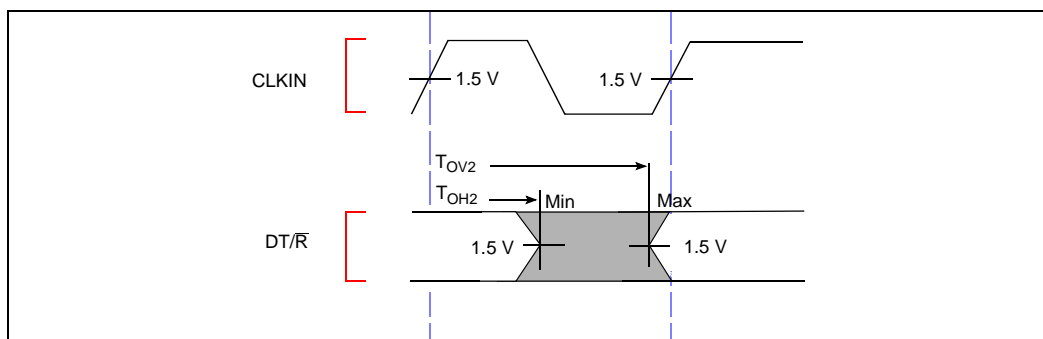


Figure 12. Output Float Waveform

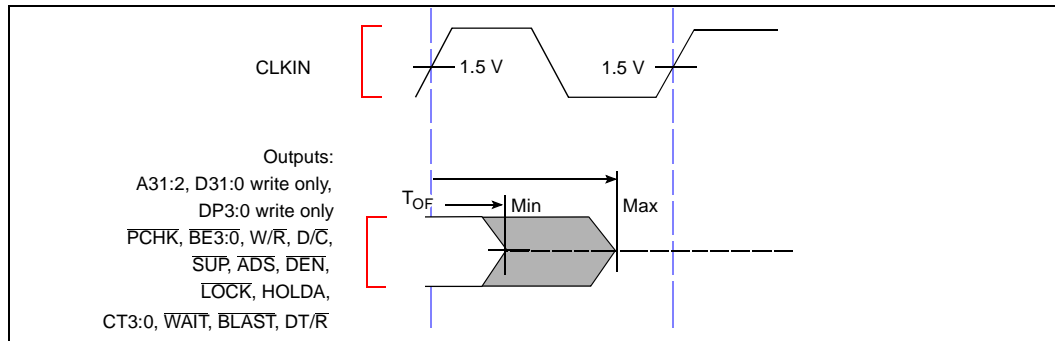


Figure 13. Input Setup and Hold Waveform

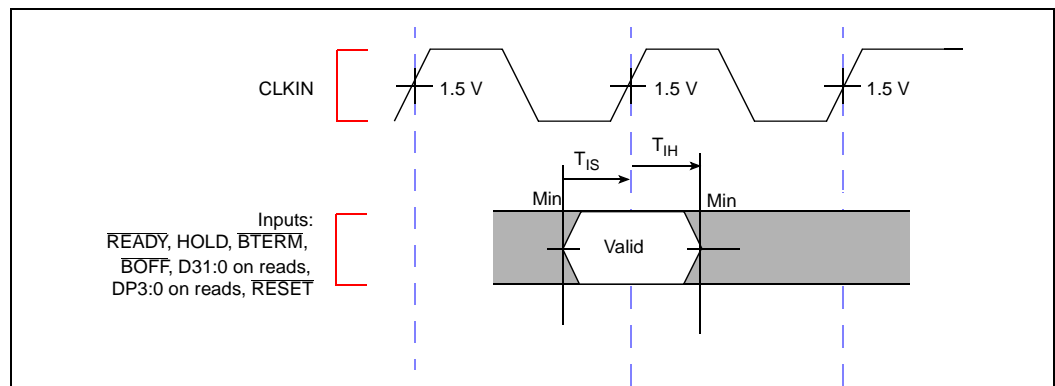


Figure 14. NMI, XINT7:0 Input Setup and Hold Waveform

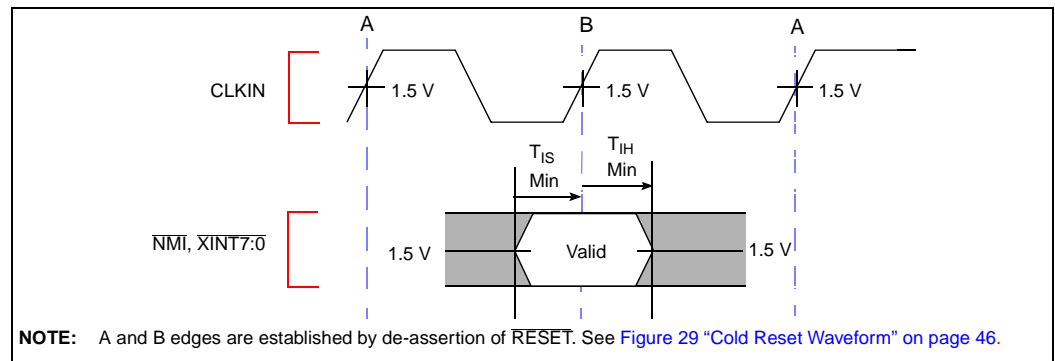


Figure 15. Hold Acknowledge Timings

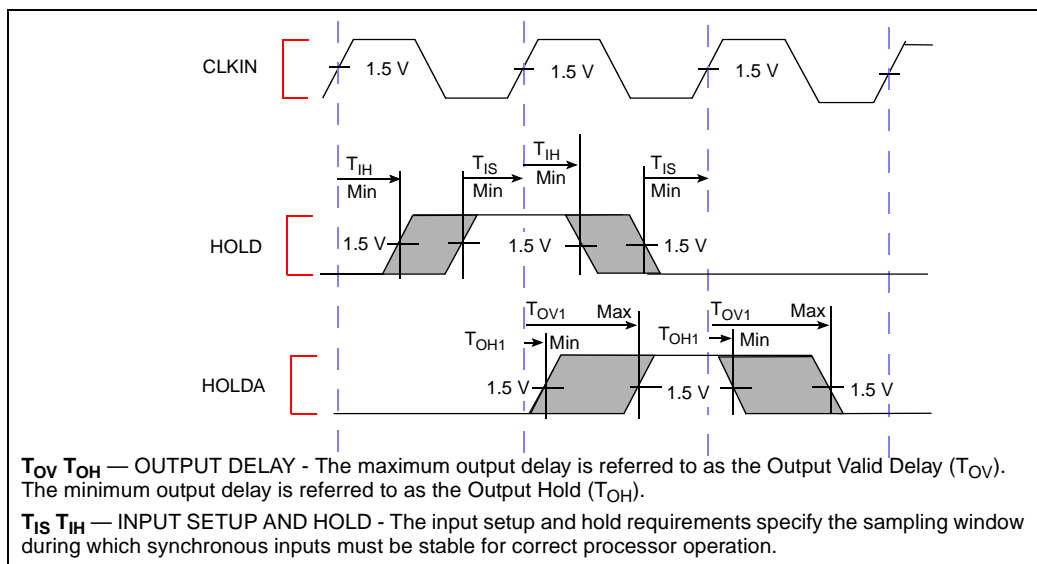
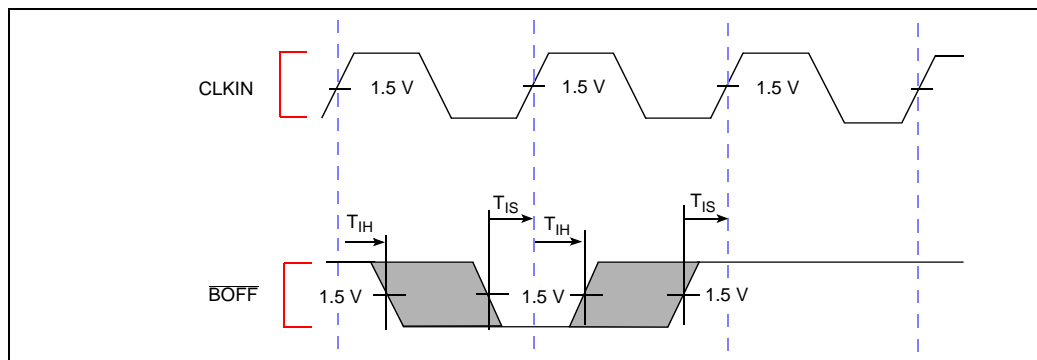
Figure 16. Bus Backoff (\overline{BOFF}) Timings

Figure 17. TCK Waveform

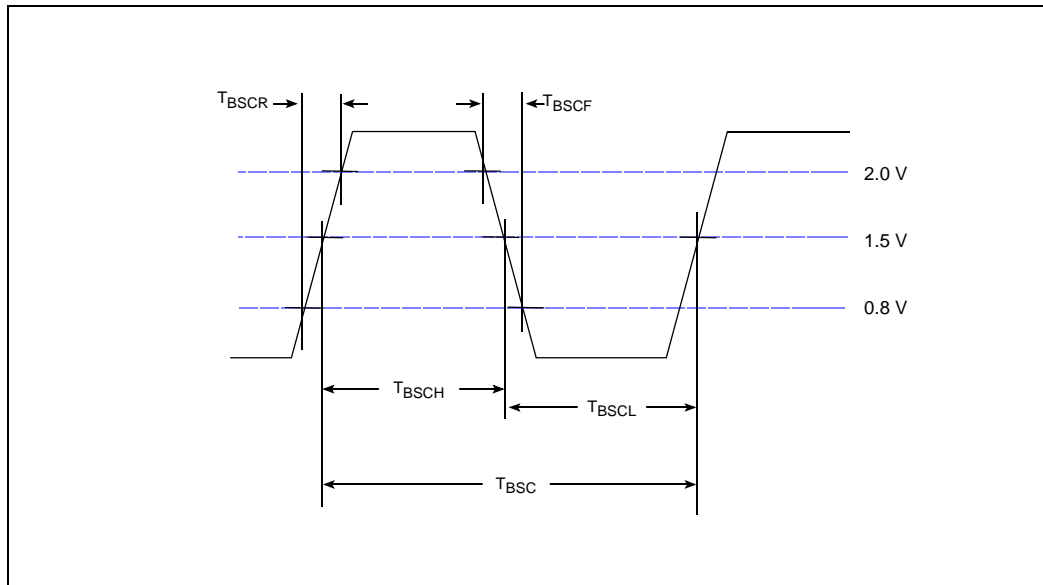


Figure 18. Input Setup and Hold Waveforms for T_{BSIS1} and T_{BSIH1}

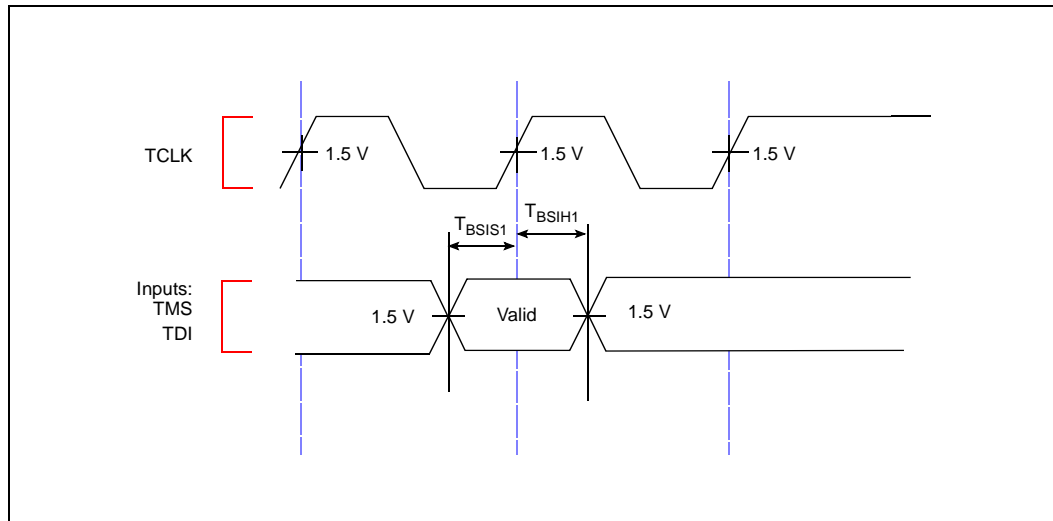


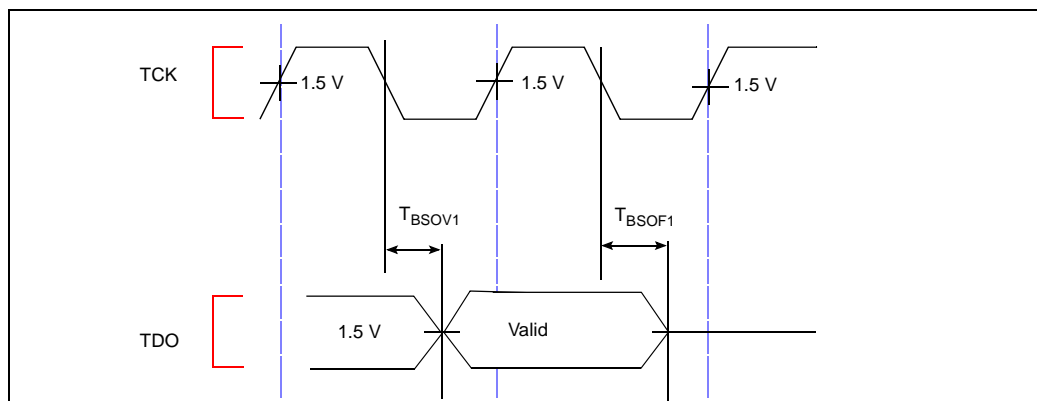
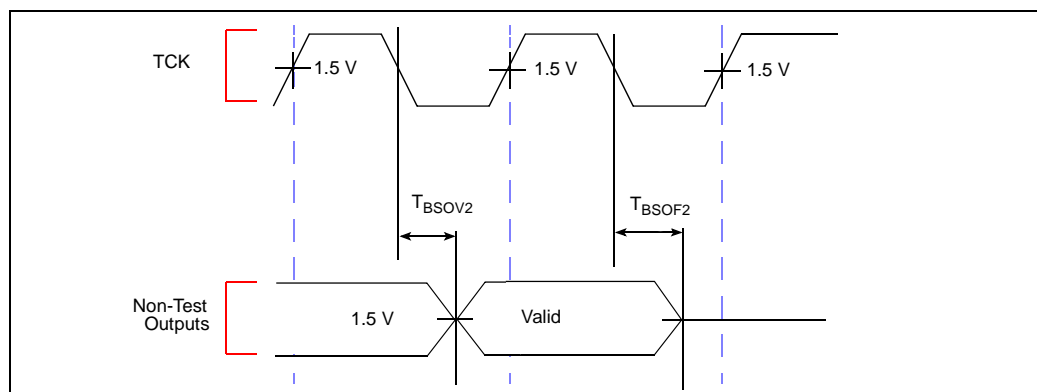
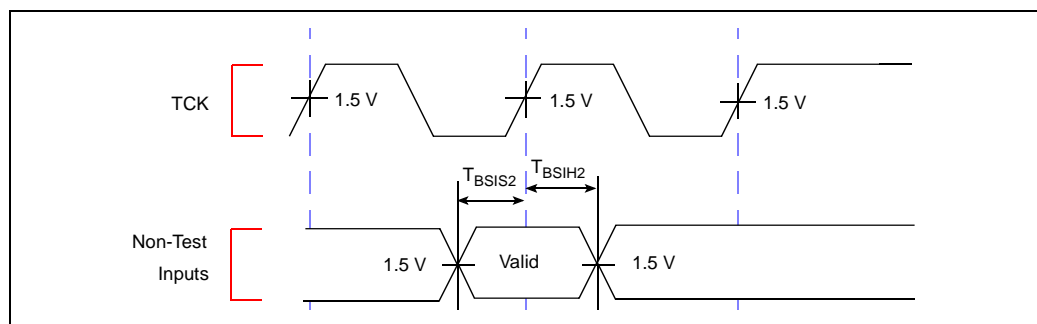
Figure 19. Output Delay and Output Float for T_{BSOV1} and T_{BSOF1} Figure 20. Output Delay and Output Float Waveform for T_{BSOV2} and T_{BSOF2} Figure 21. Input Setup and Hold Waveform for T_{BSIS2} and T_{BSIH2} 

Figure 22. Rise and Fall Time Derating at 85°C and Minimum V_{CC}

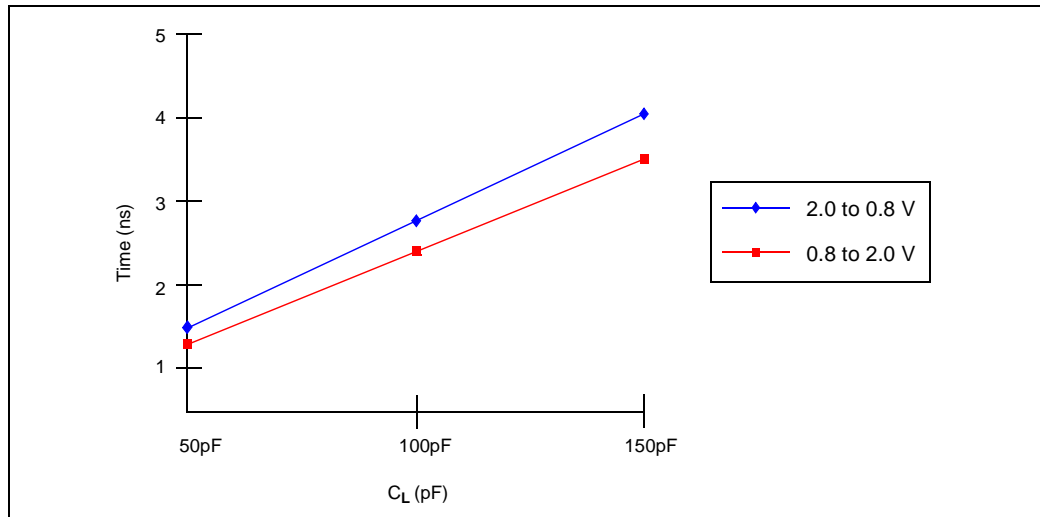


Figure 23. I_{CC} Active (Power Supply) vs. Frequency

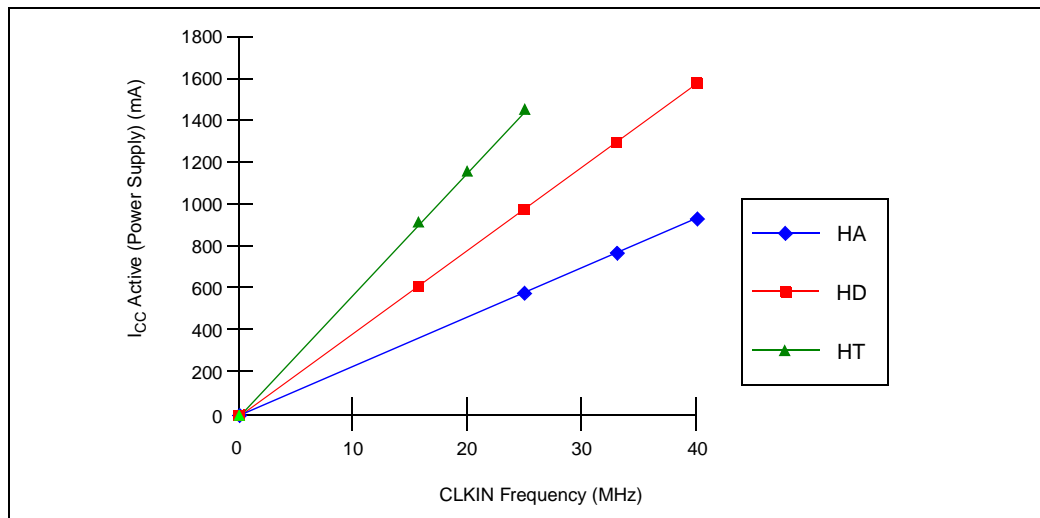


Figure 24. I_{CC} Active (Thermal) vs. Frequency

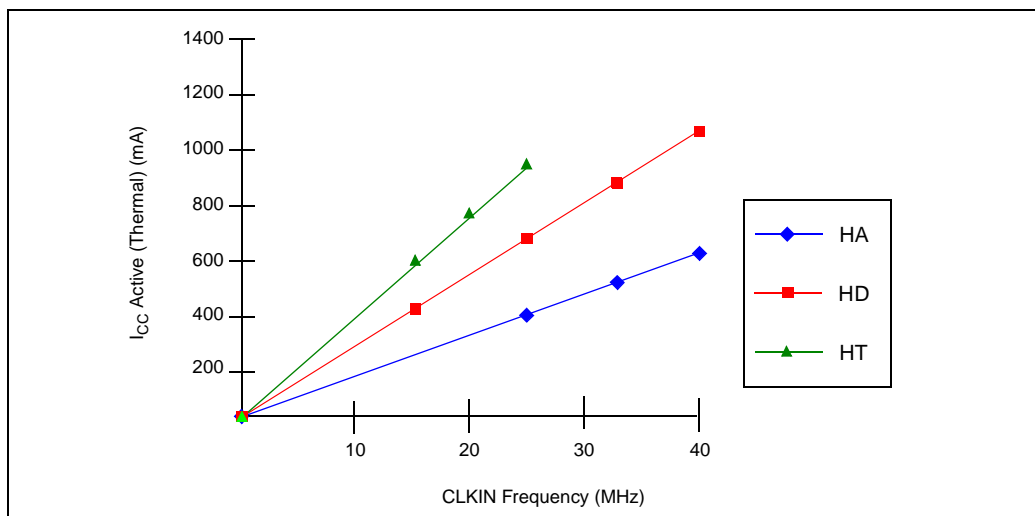


Figure 25. Output Delay or Hold vs. Load Capacitance

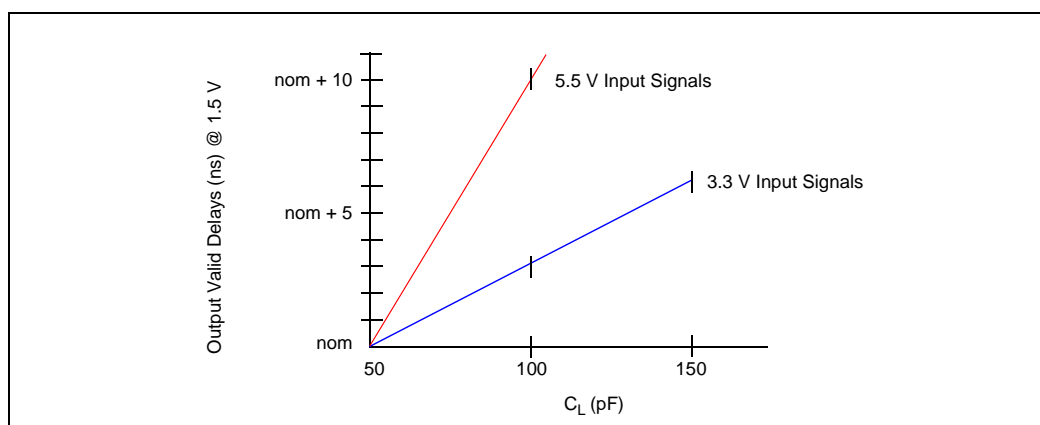


Figure 26. Output Delay vs. Temperature

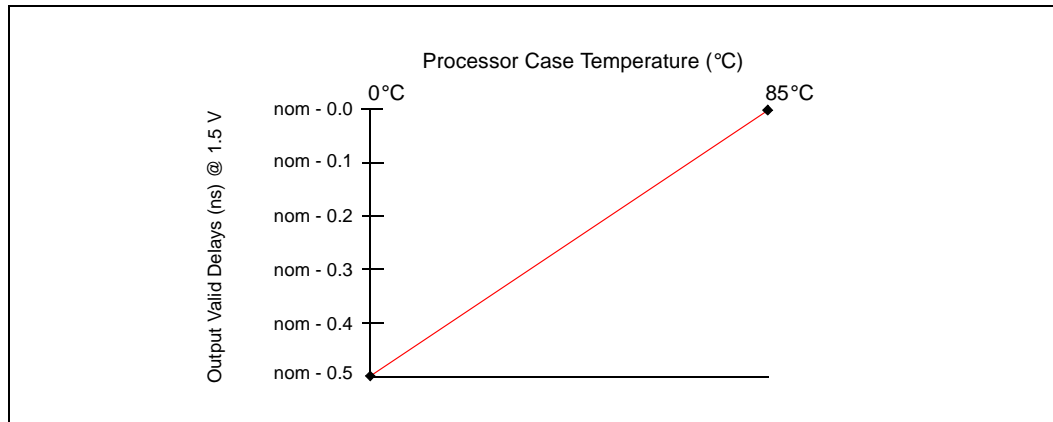


Figure 27. Output Hold Times vs. Temperature

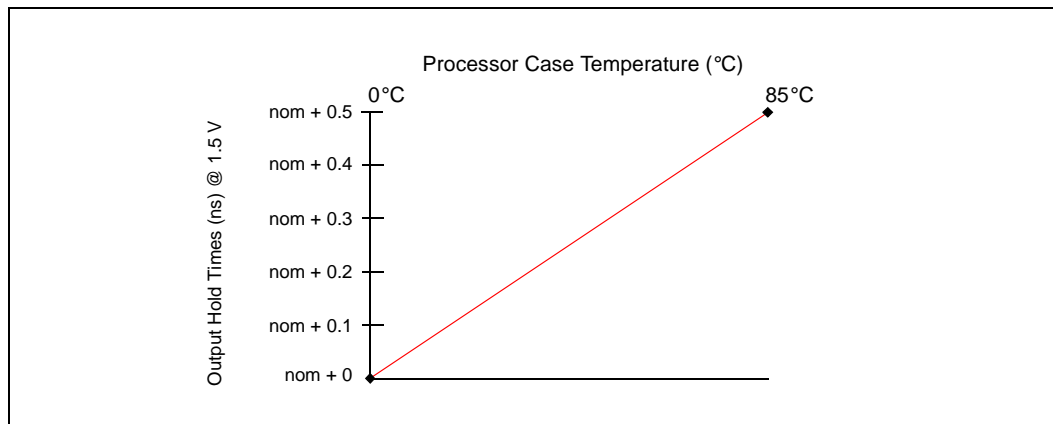
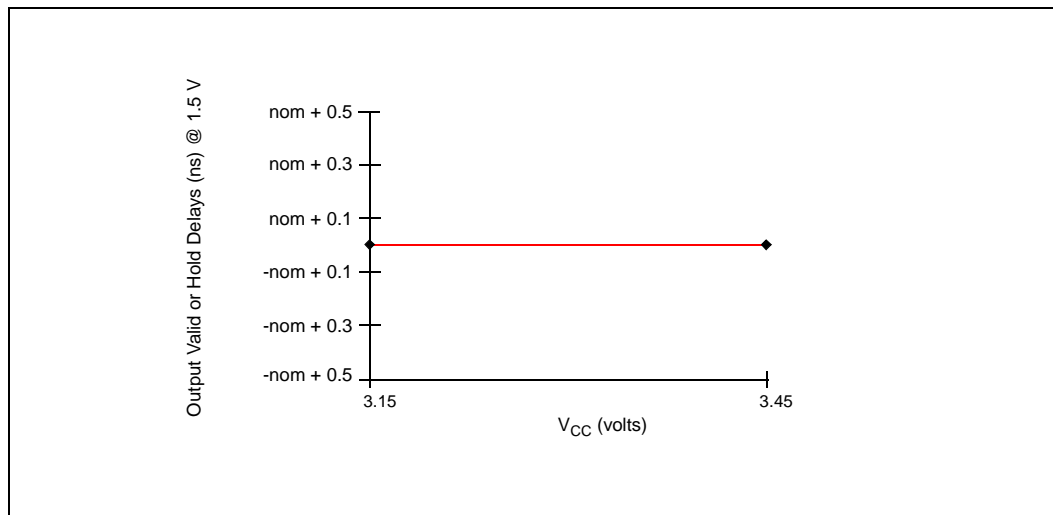


Figure 28. Output Delay vs. V_{CC}



5.0 Bus Waveforms

Figure 29. Cold Reset Waveform

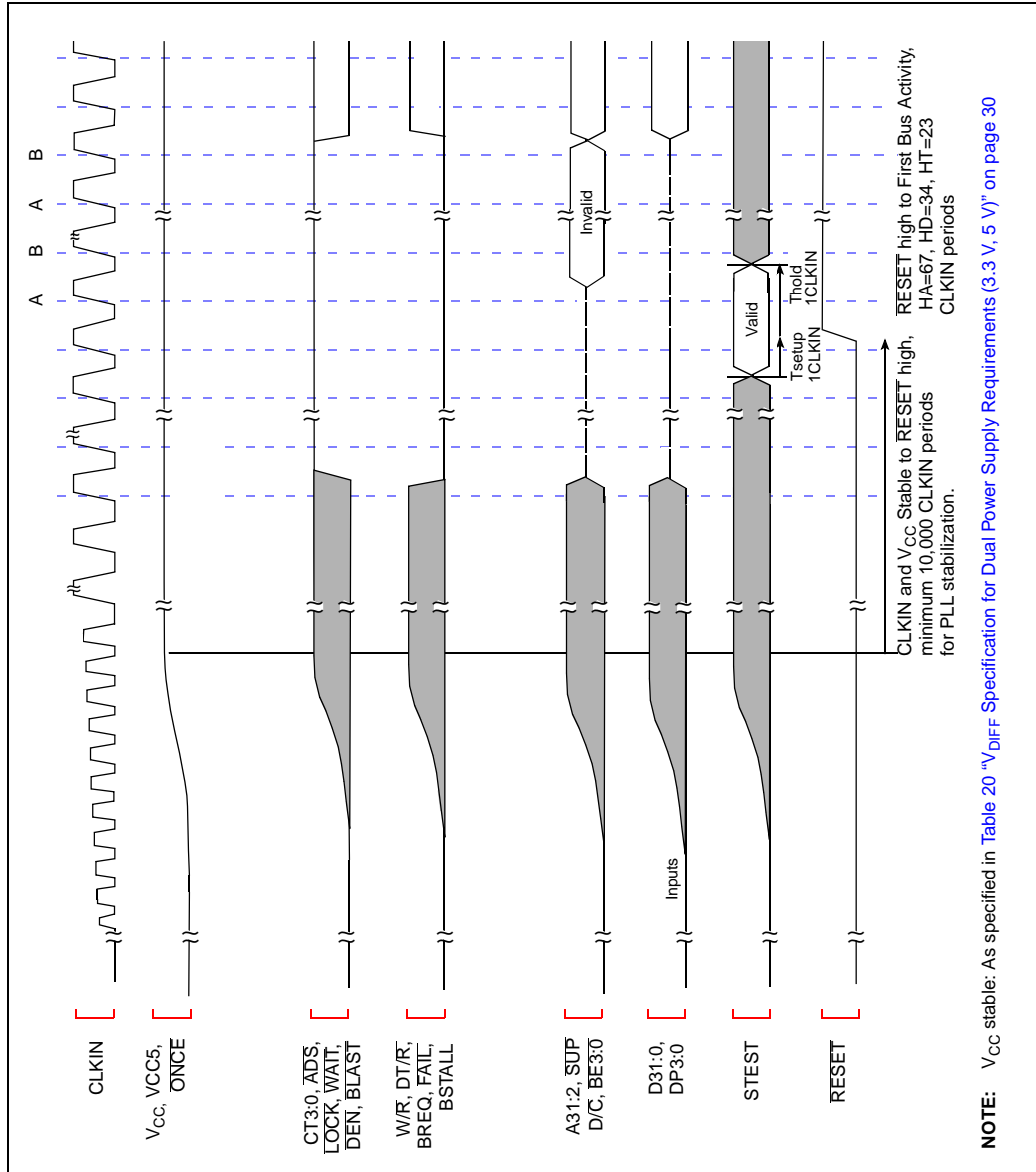


Figure 30. Warm Reset Waveform

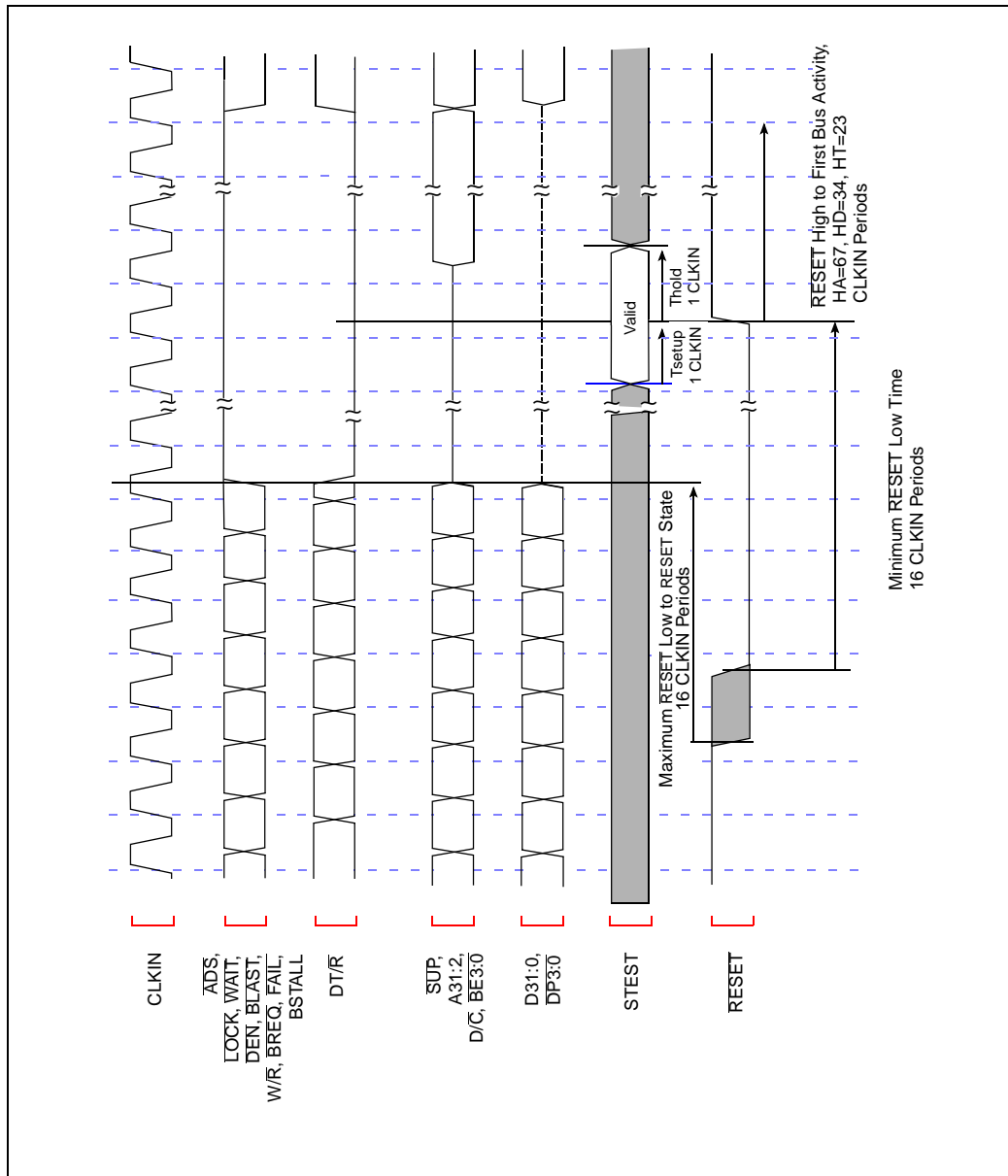


Figure 31. Entering ONCE Mode

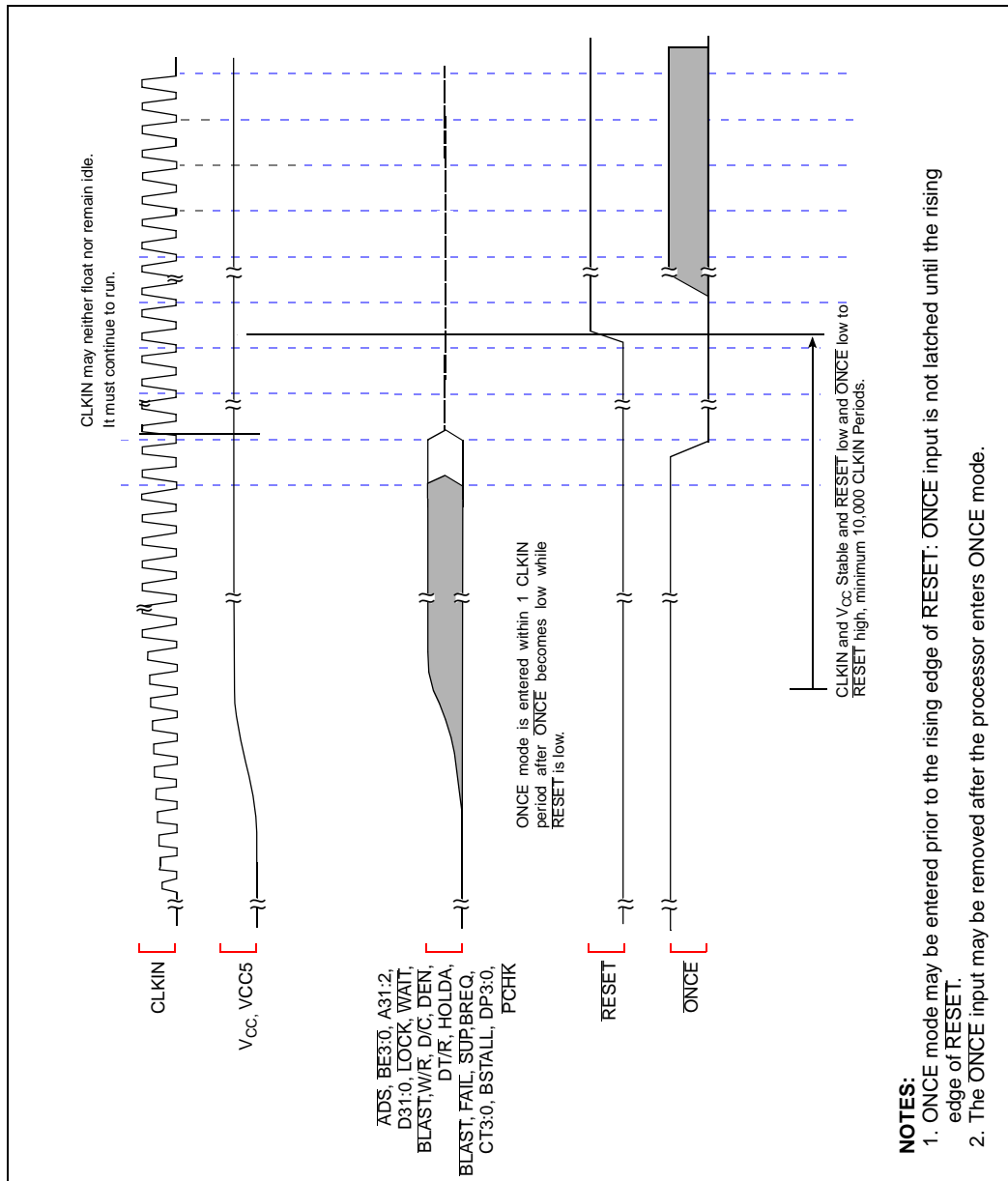


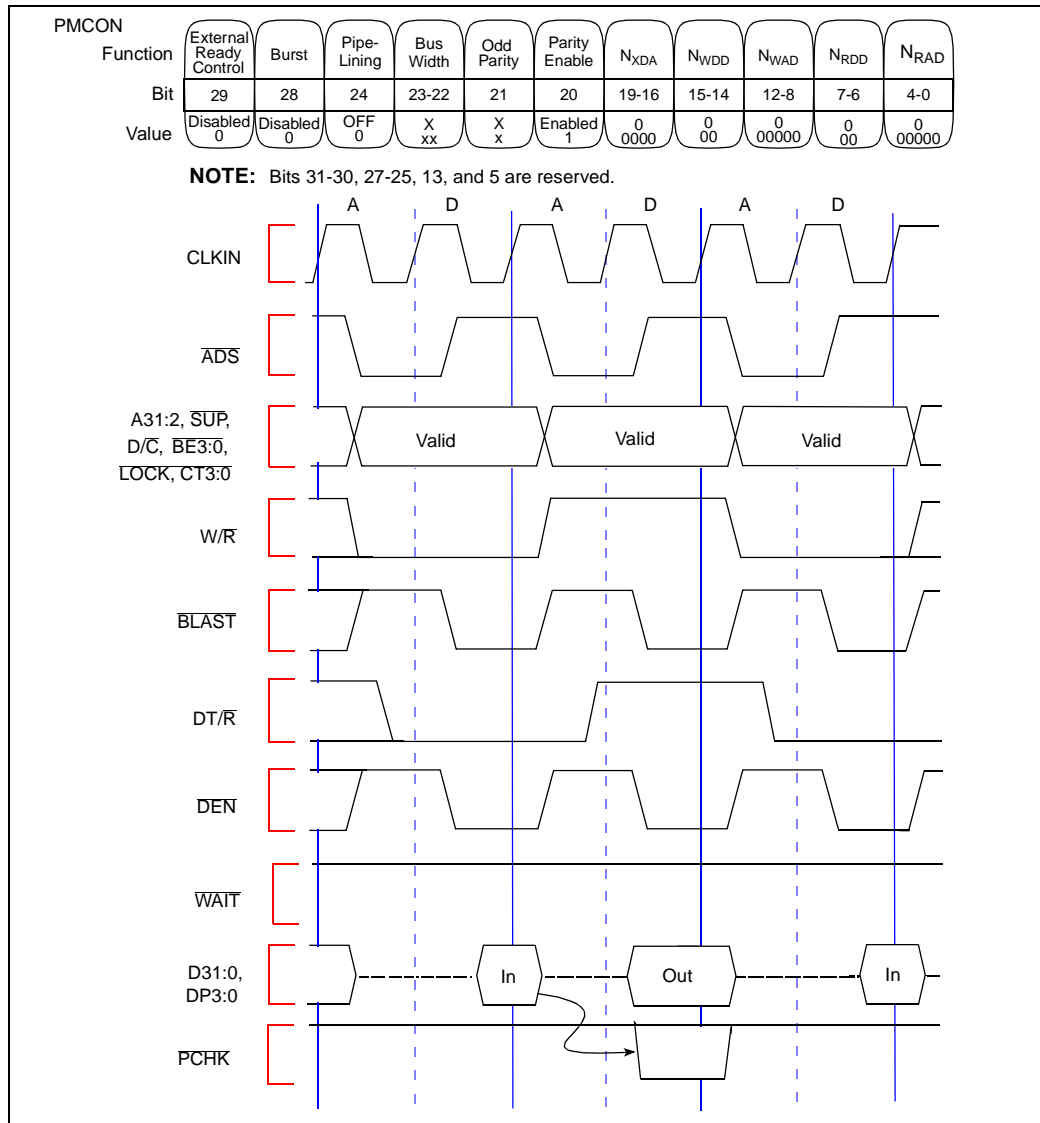
Figure 32. Non-Burst, Non-Pipelined Requests without Wait States


Figure 33. Non-Burst, Non-Pipelined Read Request with Wait States

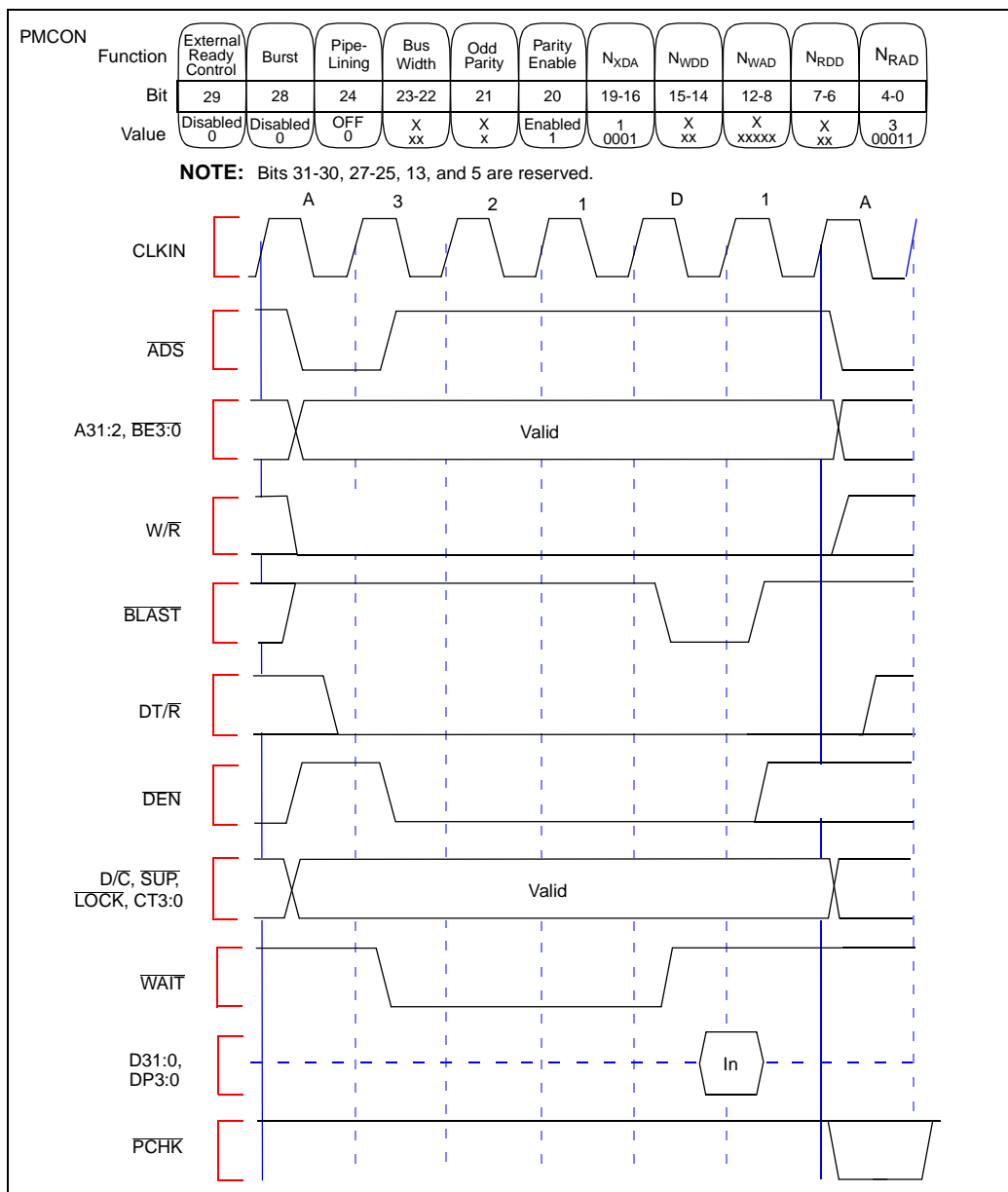


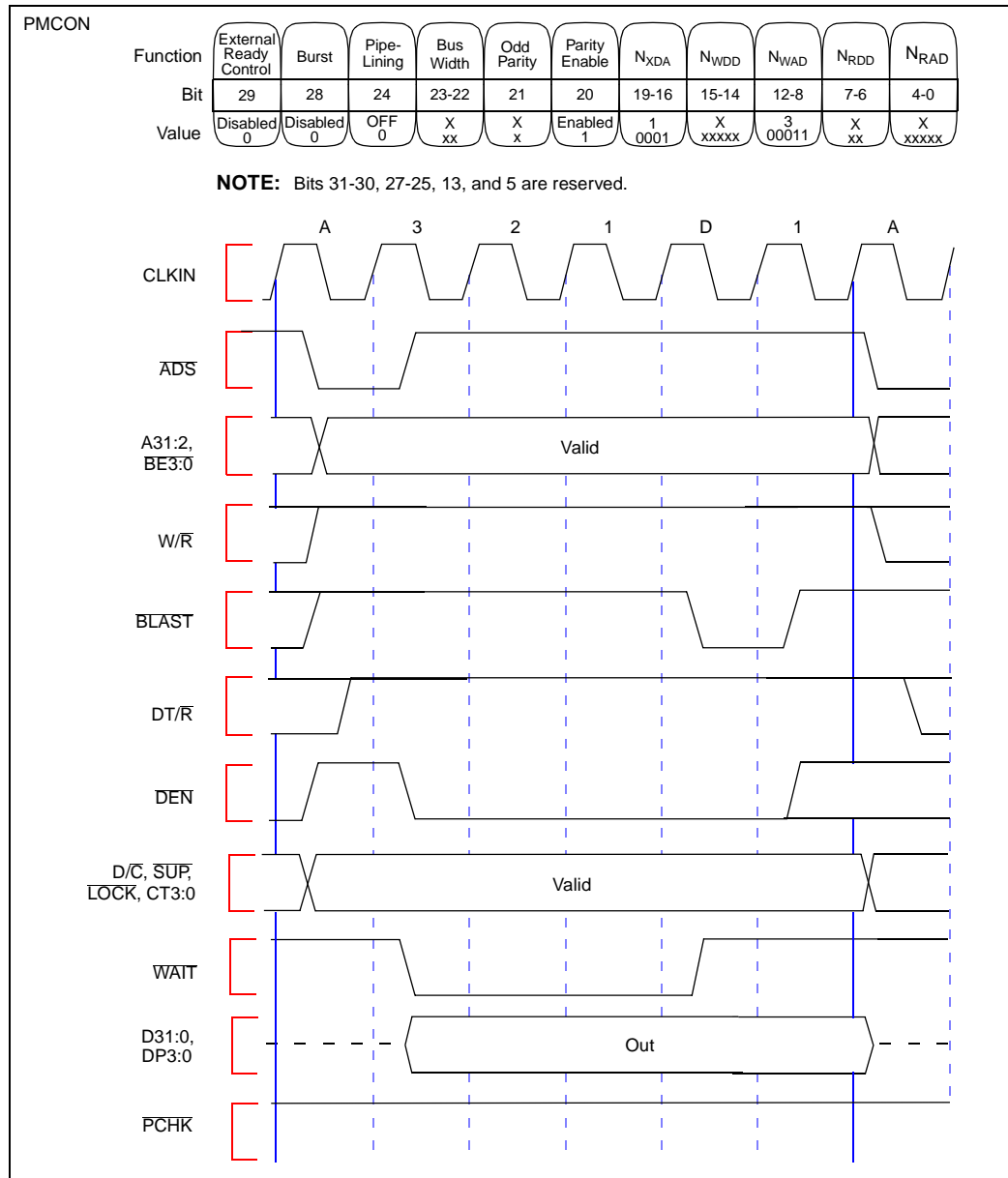
Figure 34. Non-Burst, Non-Pipelined Write Request with Wait States


Figure 35. Burst, Non-Pipelined Read Request without Wait States, 32-Bit Bus

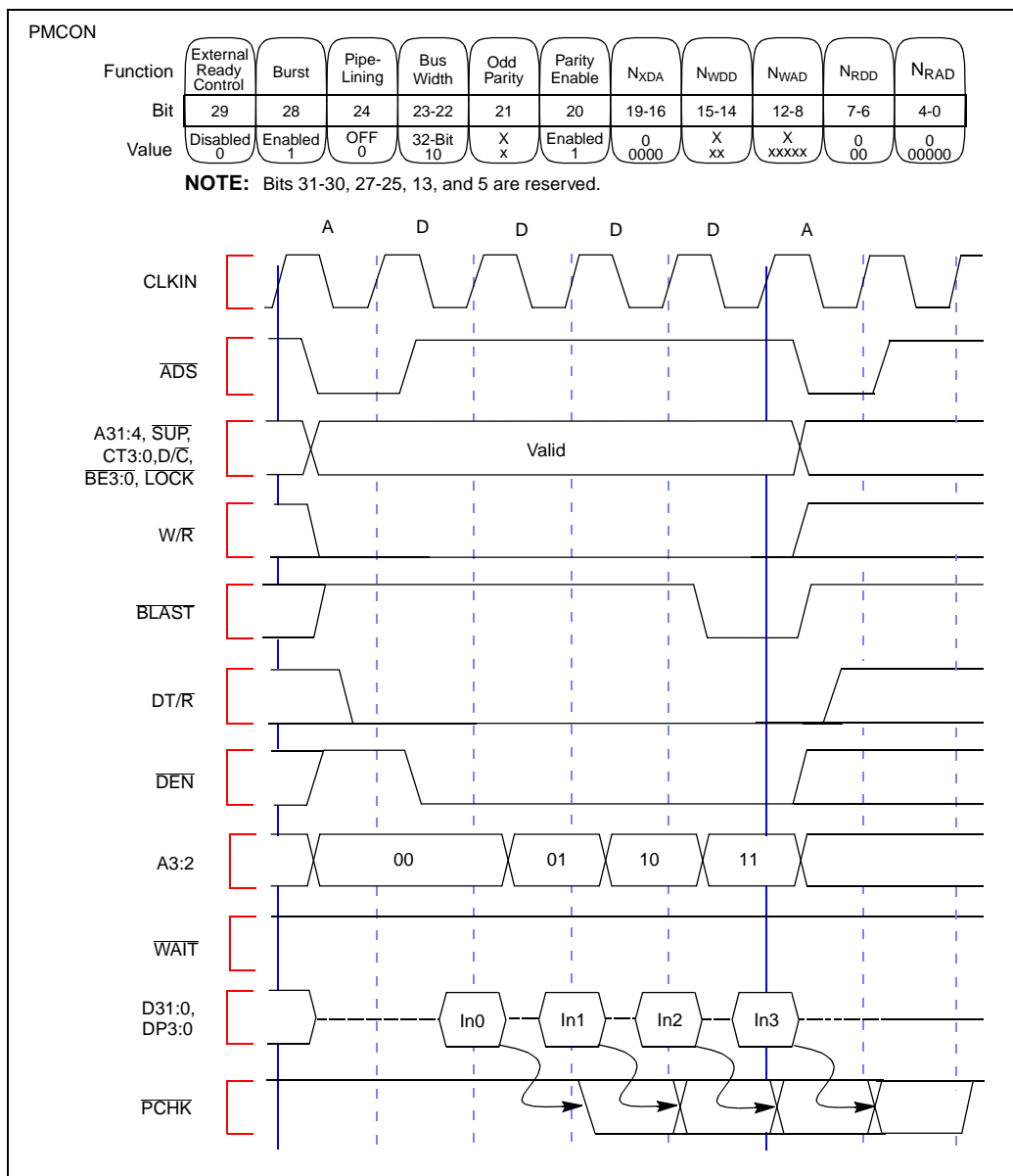


Figure 36. Burst, Non-Pipelined Read Request with Wait States, 32-Bit Bus

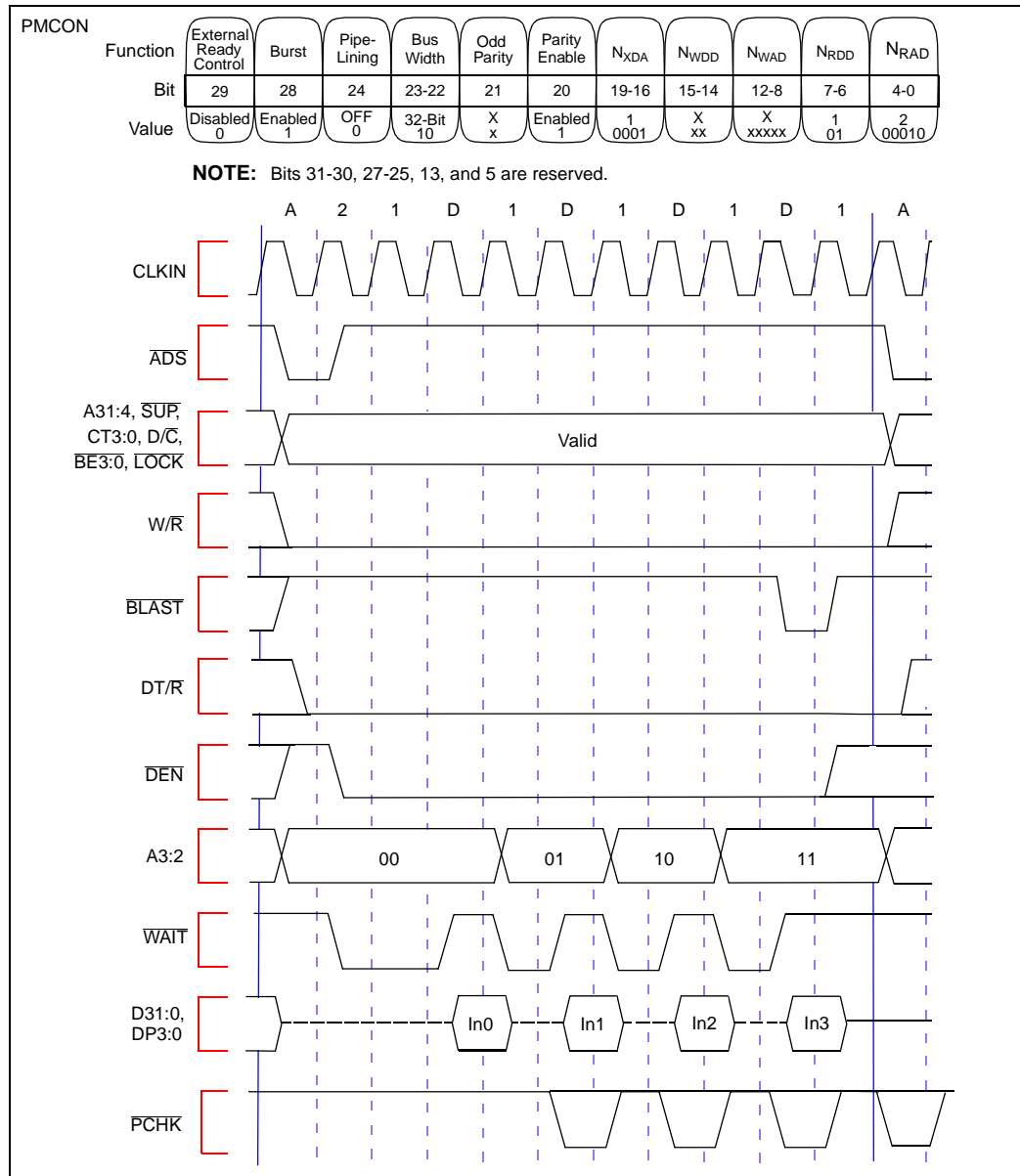


Figure 37. Burst, Non-Pipelined Write Request without Wait States, 32-Bit Bus

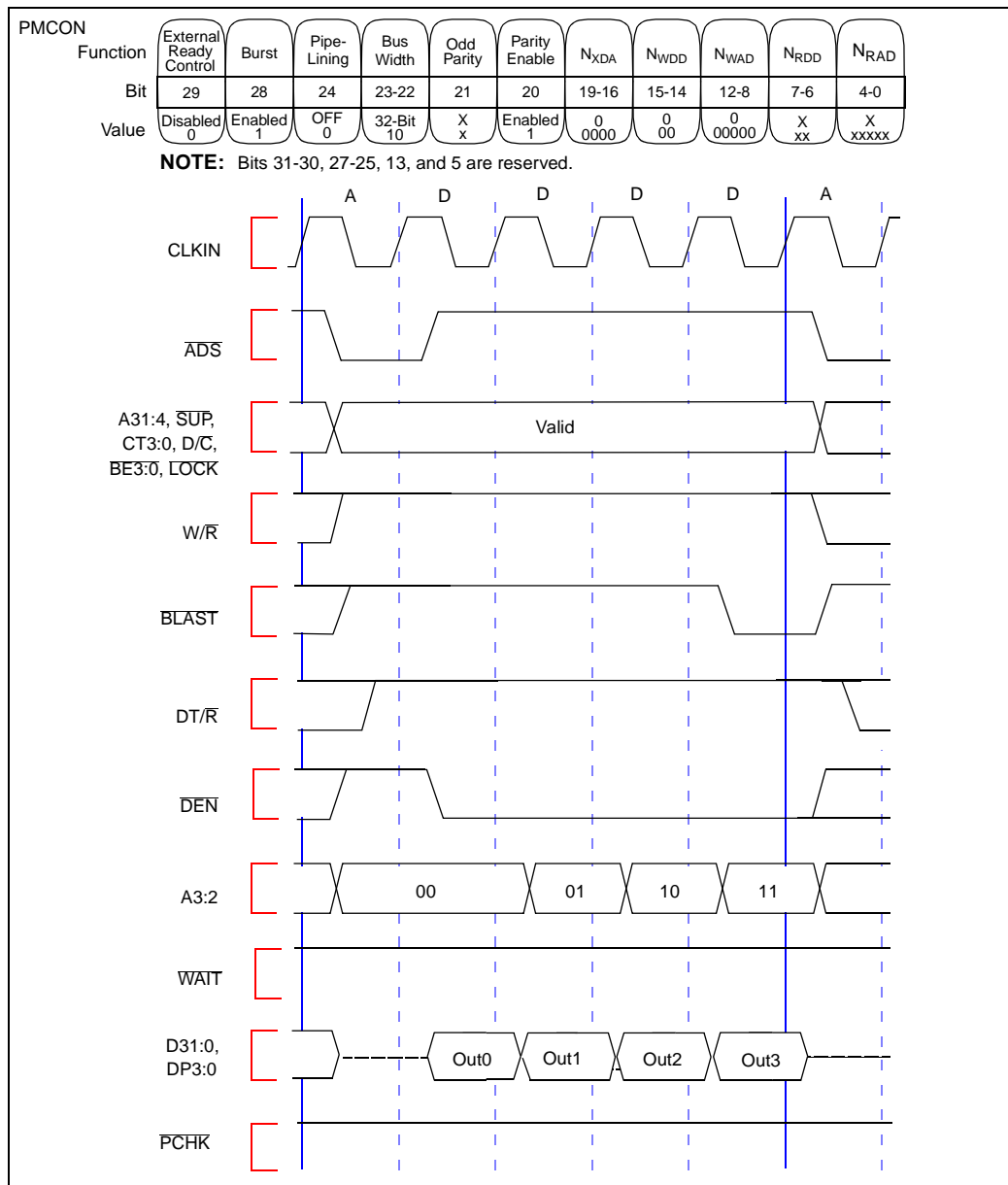


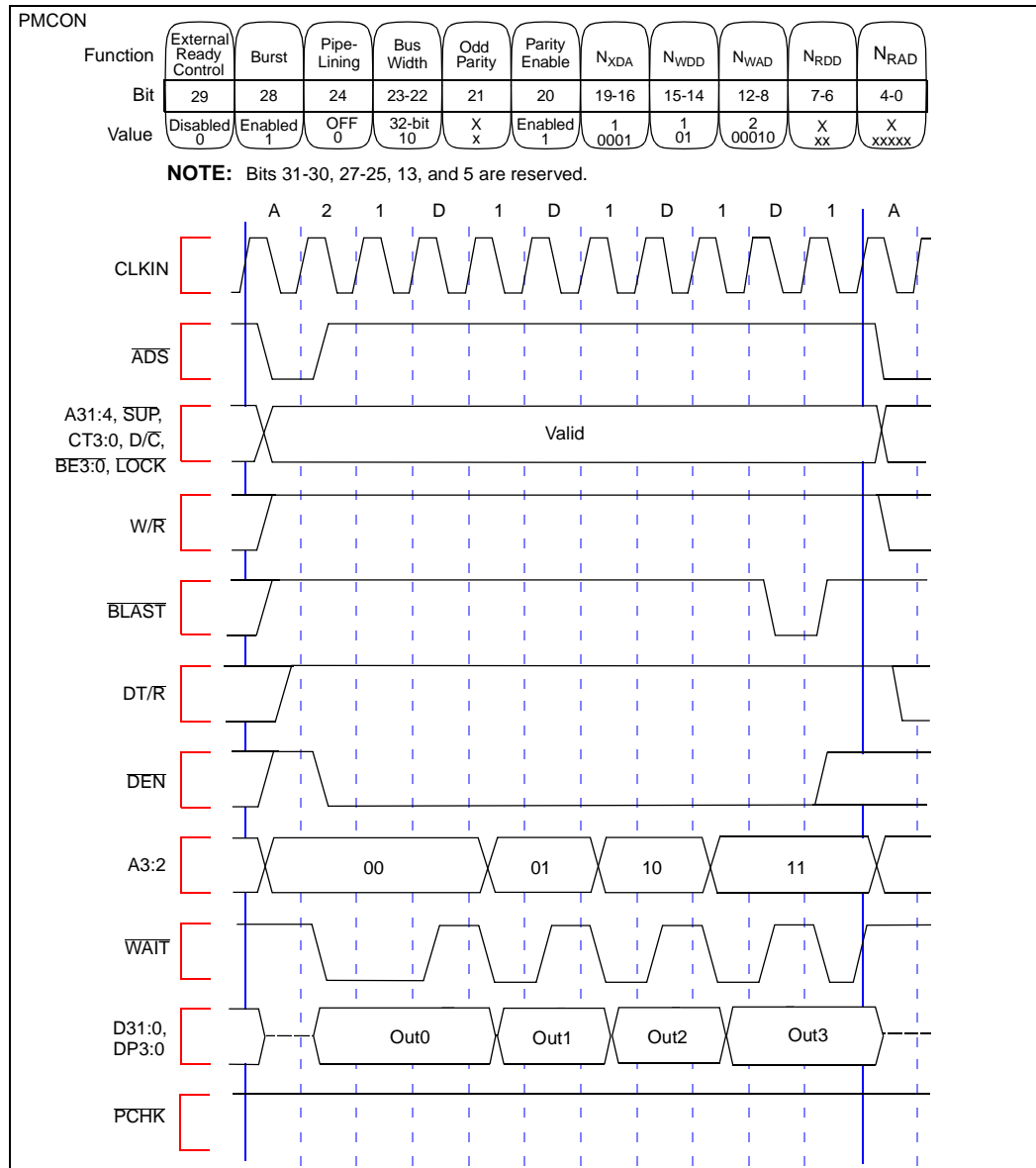
Figure 38. Burst, Non-Pipelined Write Request with Wait States, 32-Bit Bus


Figure 39. Burst, Non-Pipelined Read Request with Wait States, 16-Bit Bus

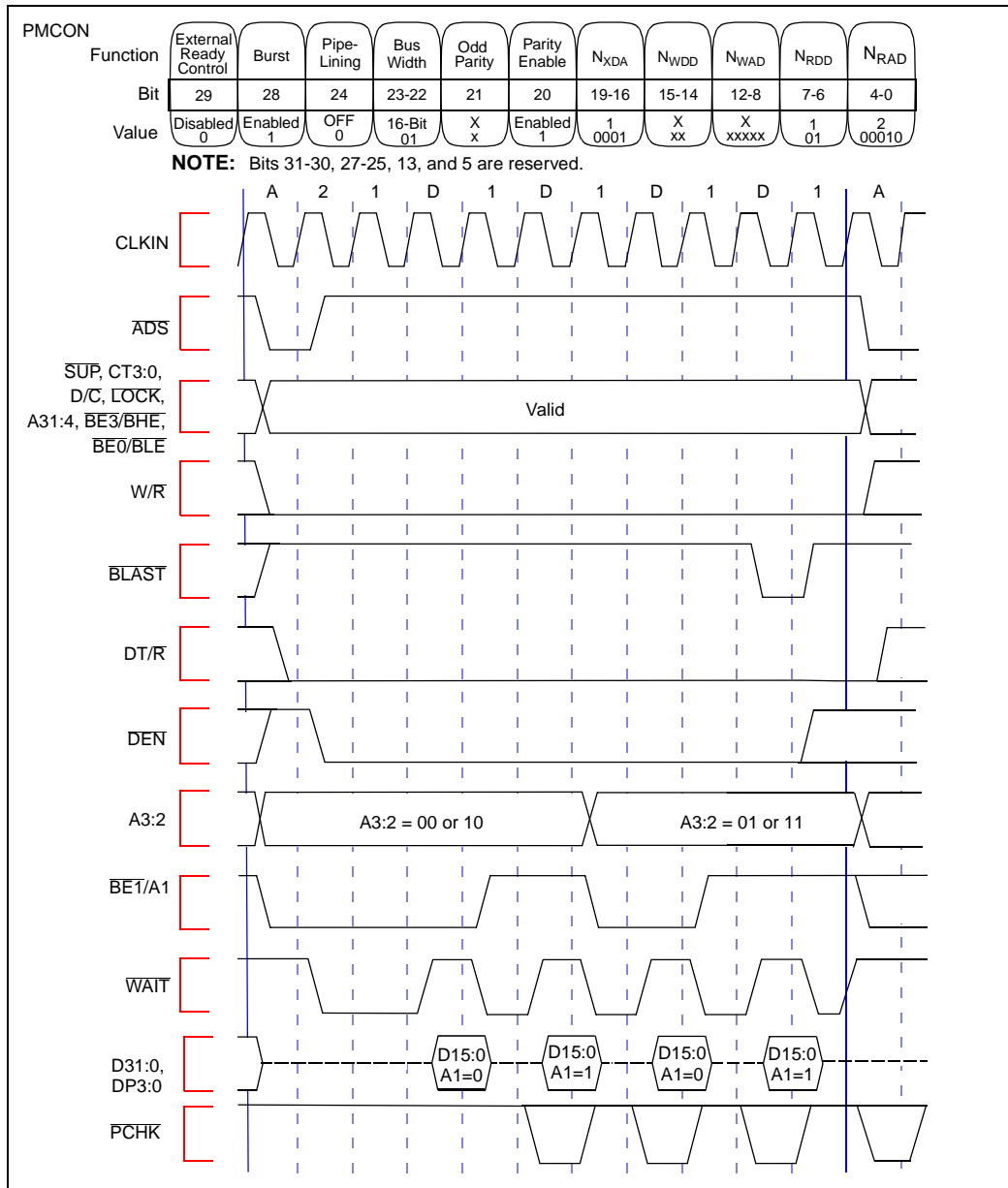


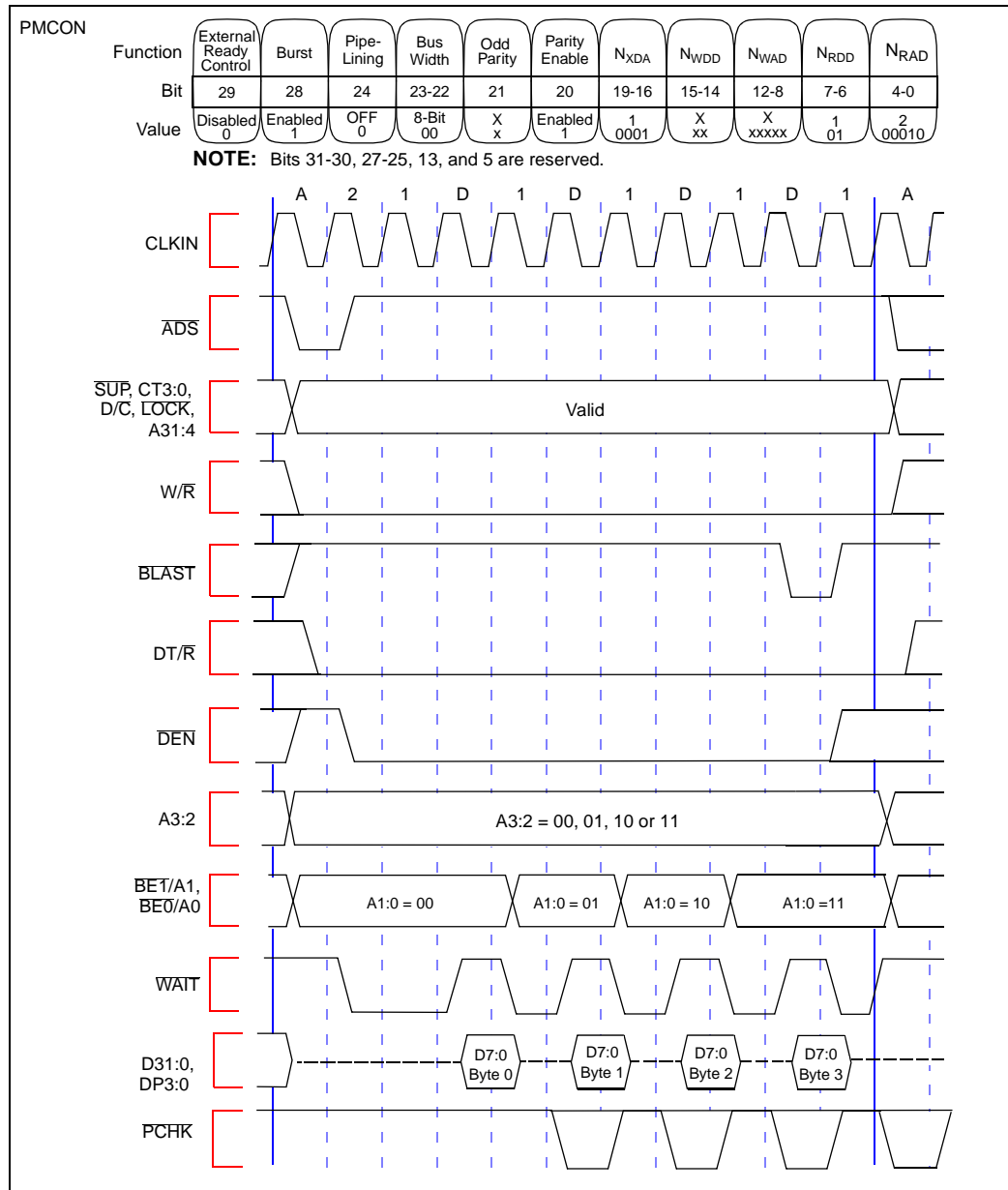
Figure 40. Burst, Non-Pipelined Read Request with Wait States, 8-Bit Bus


Figure 41. Non-Burst, Pipelined Read Request without Wait States, 32-Bit Bus

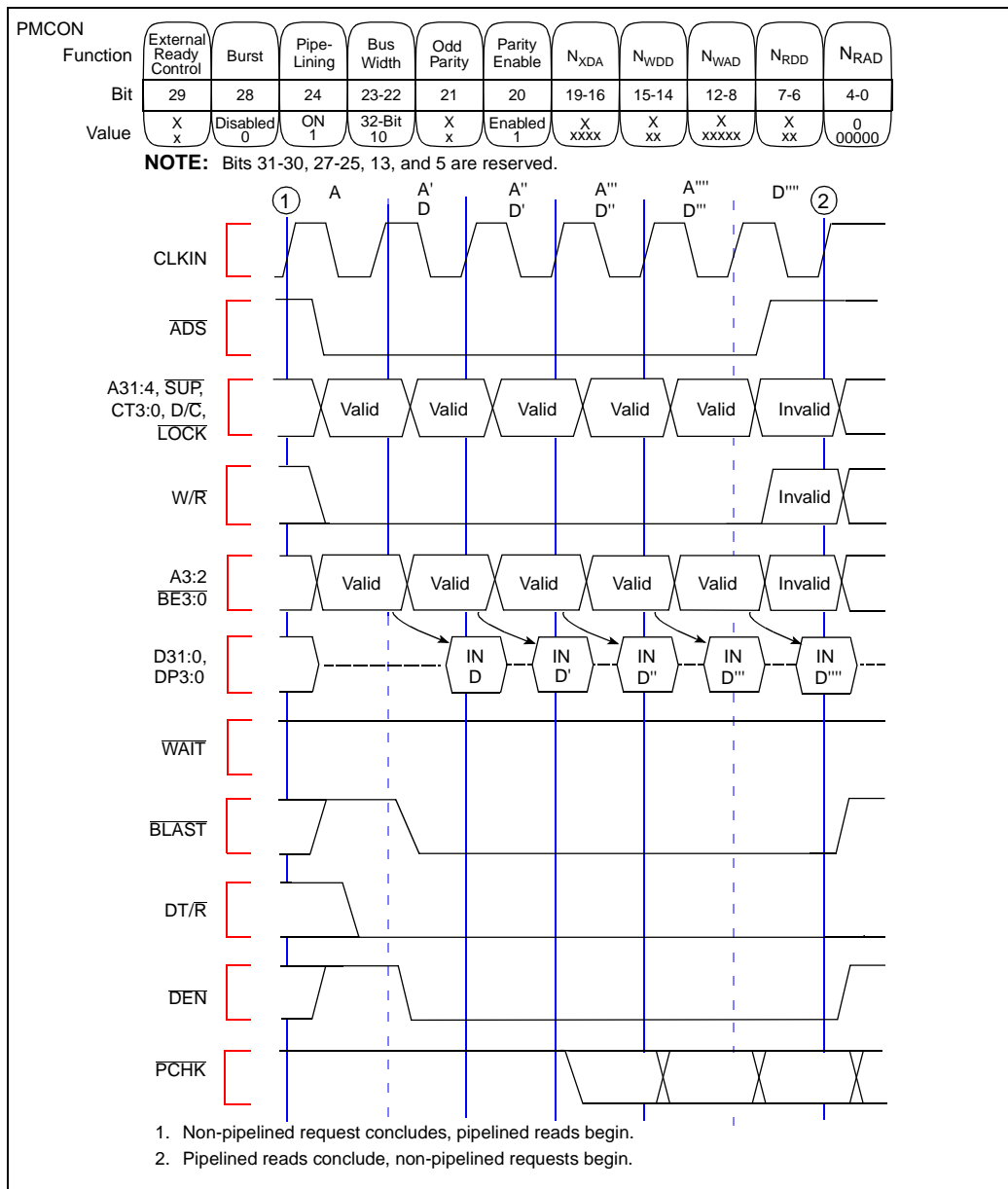


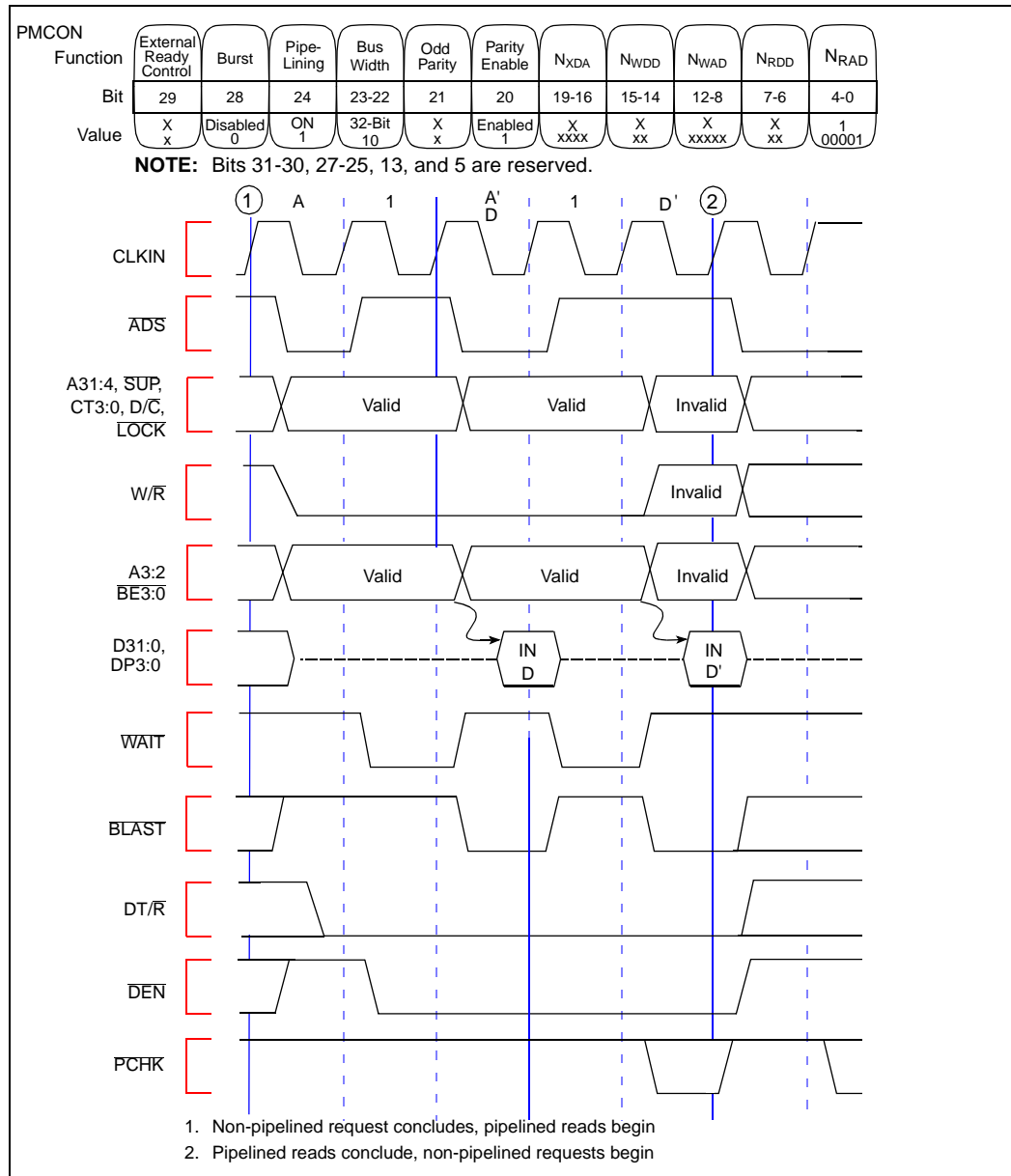
Figure 42. Non-Burst, Pipelined Read Request with Wait States, 32-Bit Bus


Figure 43. Burst, Pipelined Read Request without Wait States, 32-Bit Bus

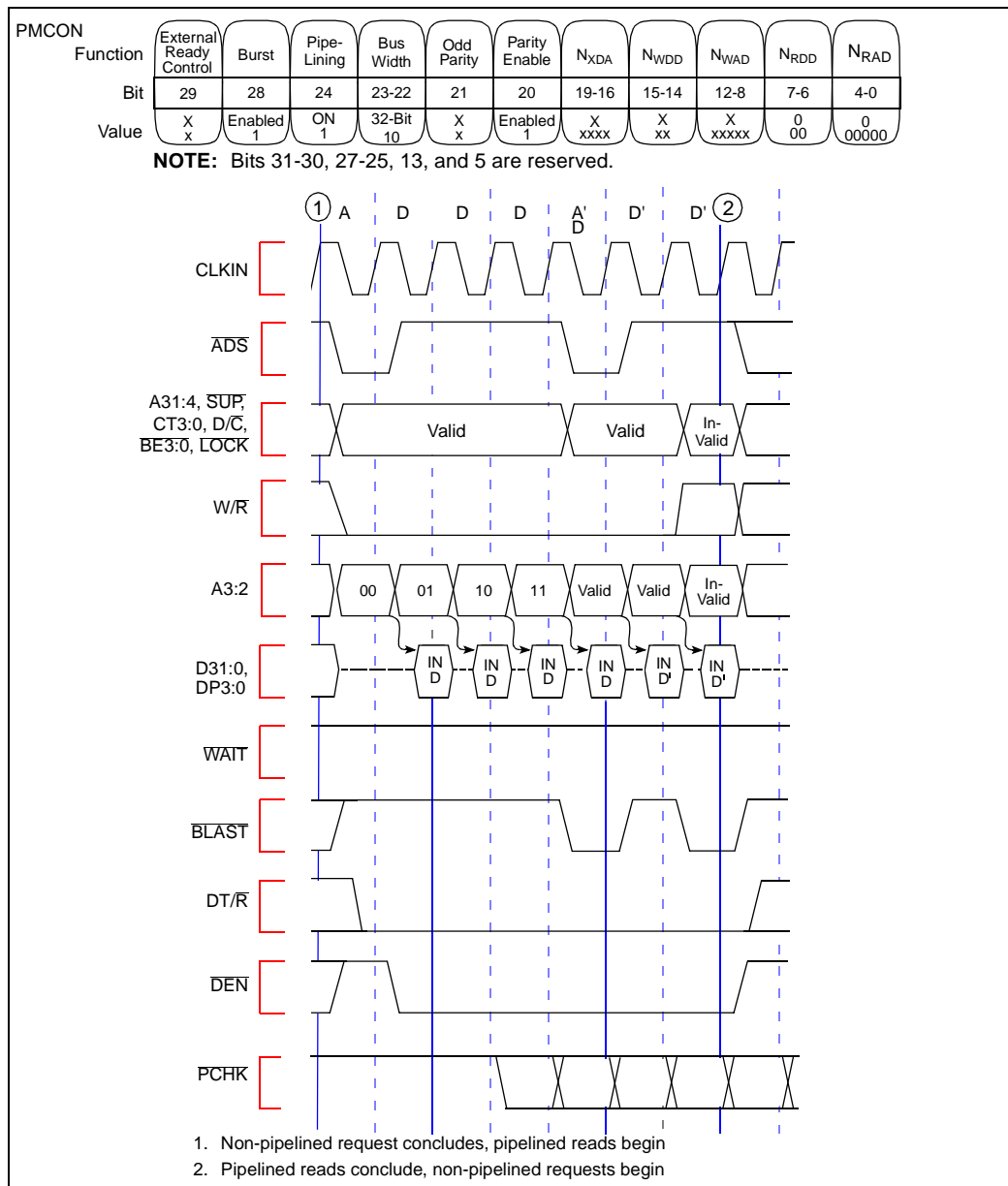


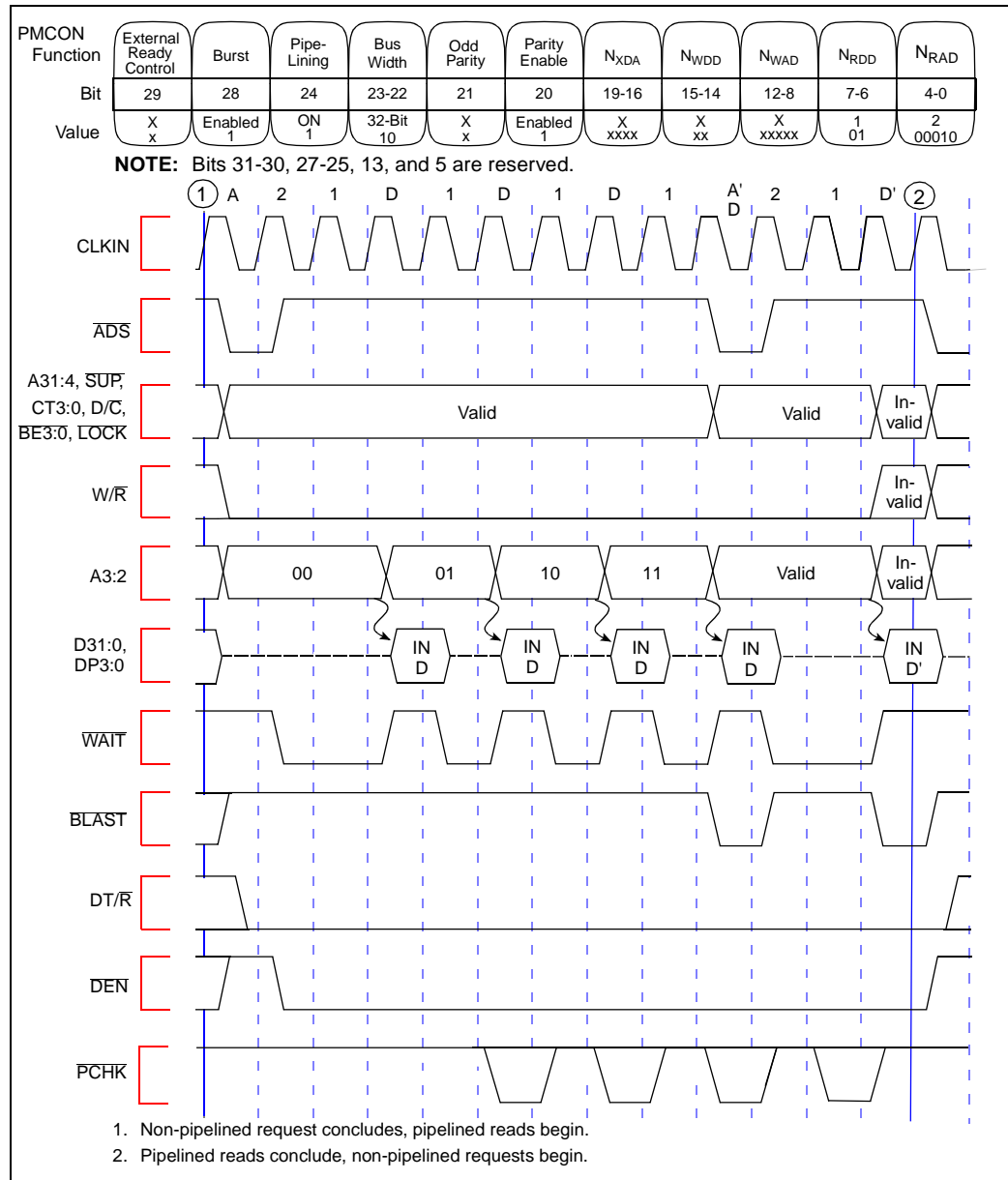
Figure 44. Burst, Pipelined Read Request with Wait States, 32-Bit Bus


Figure 45. Burst, Pipelined Read Request with Wait States, 8-Bit Bus

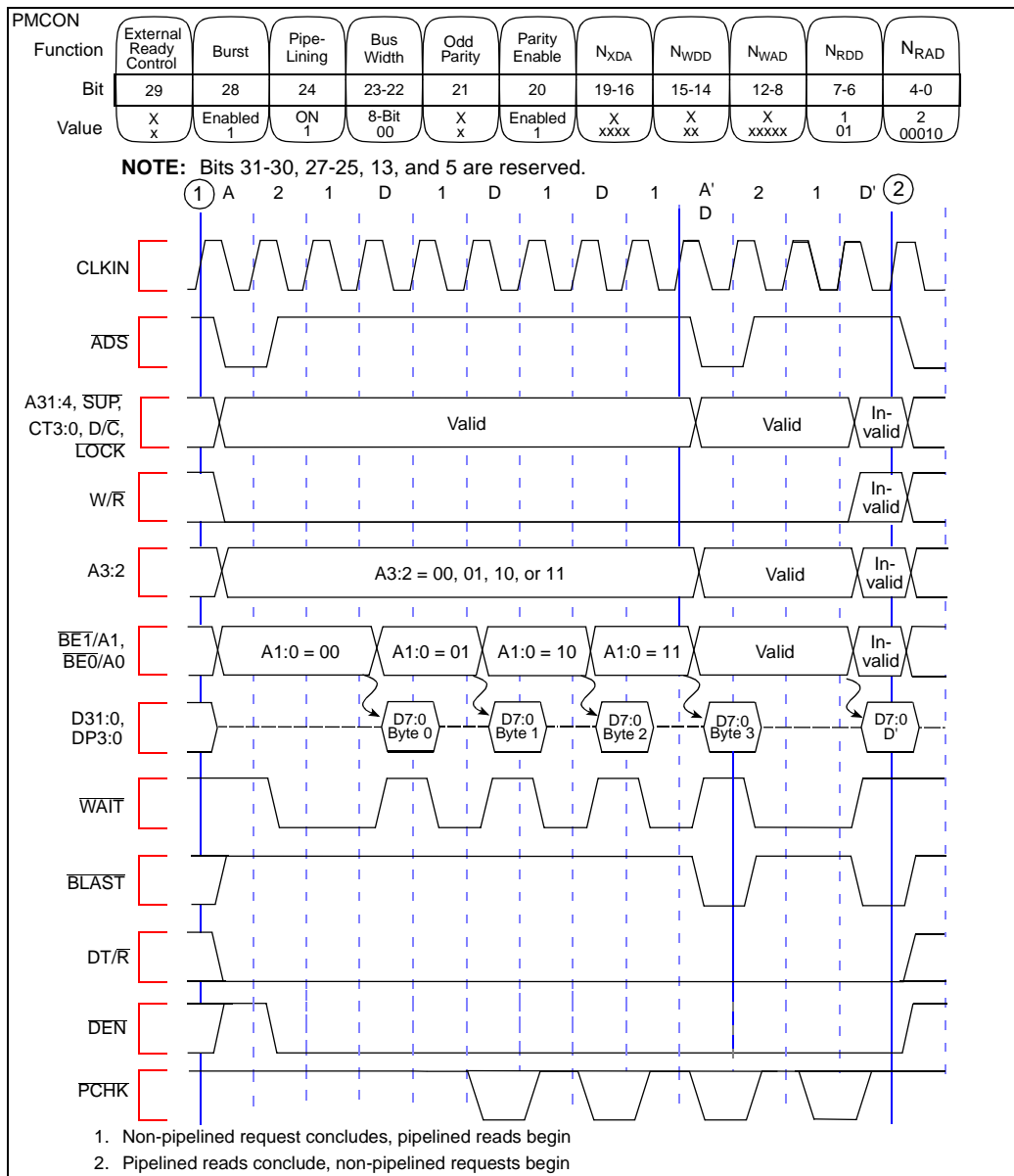


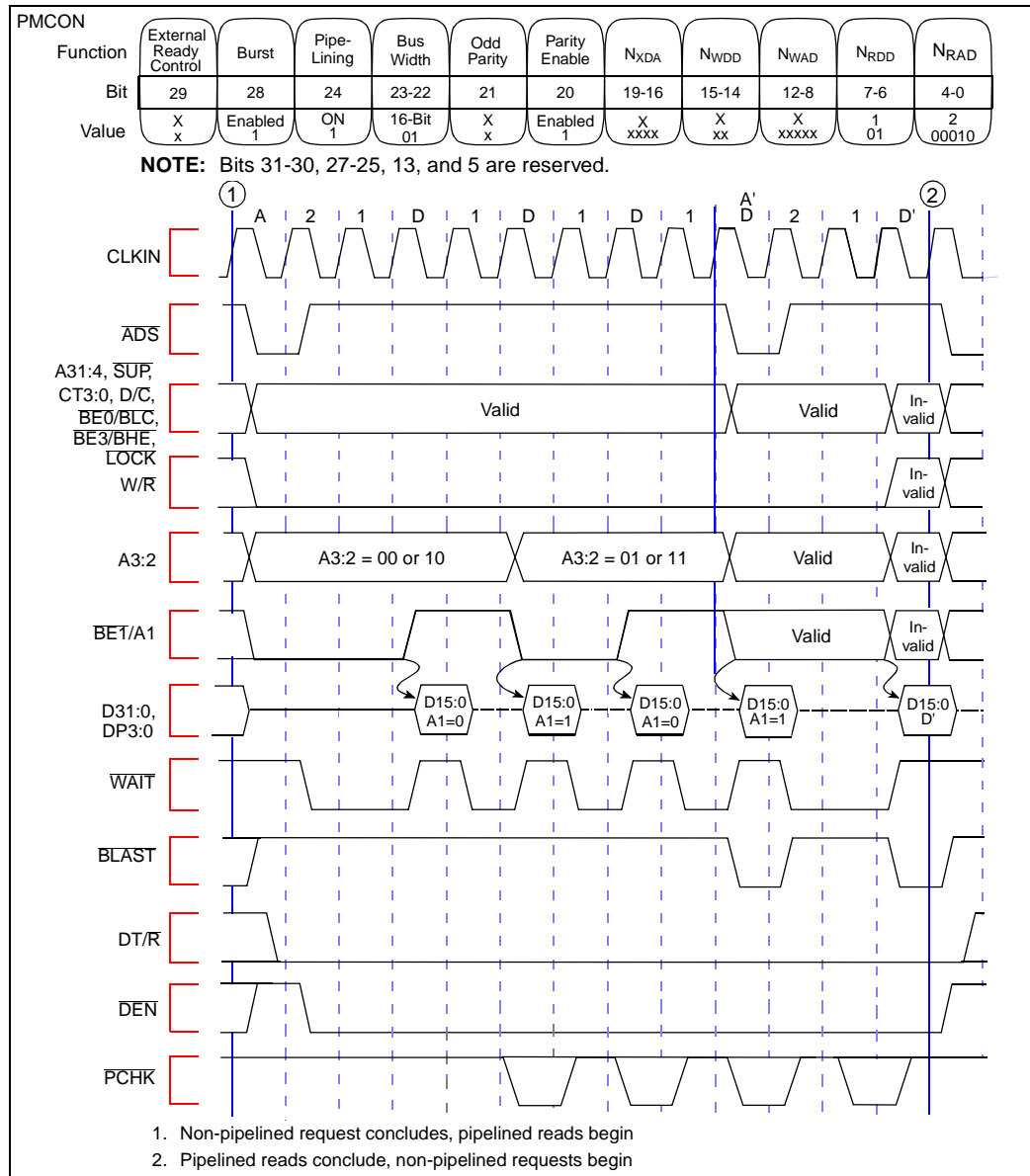
Figure 46. Burst, Pipelined Read Request with Wait States, 16-Bit Bus


Figure 47. Using External READY

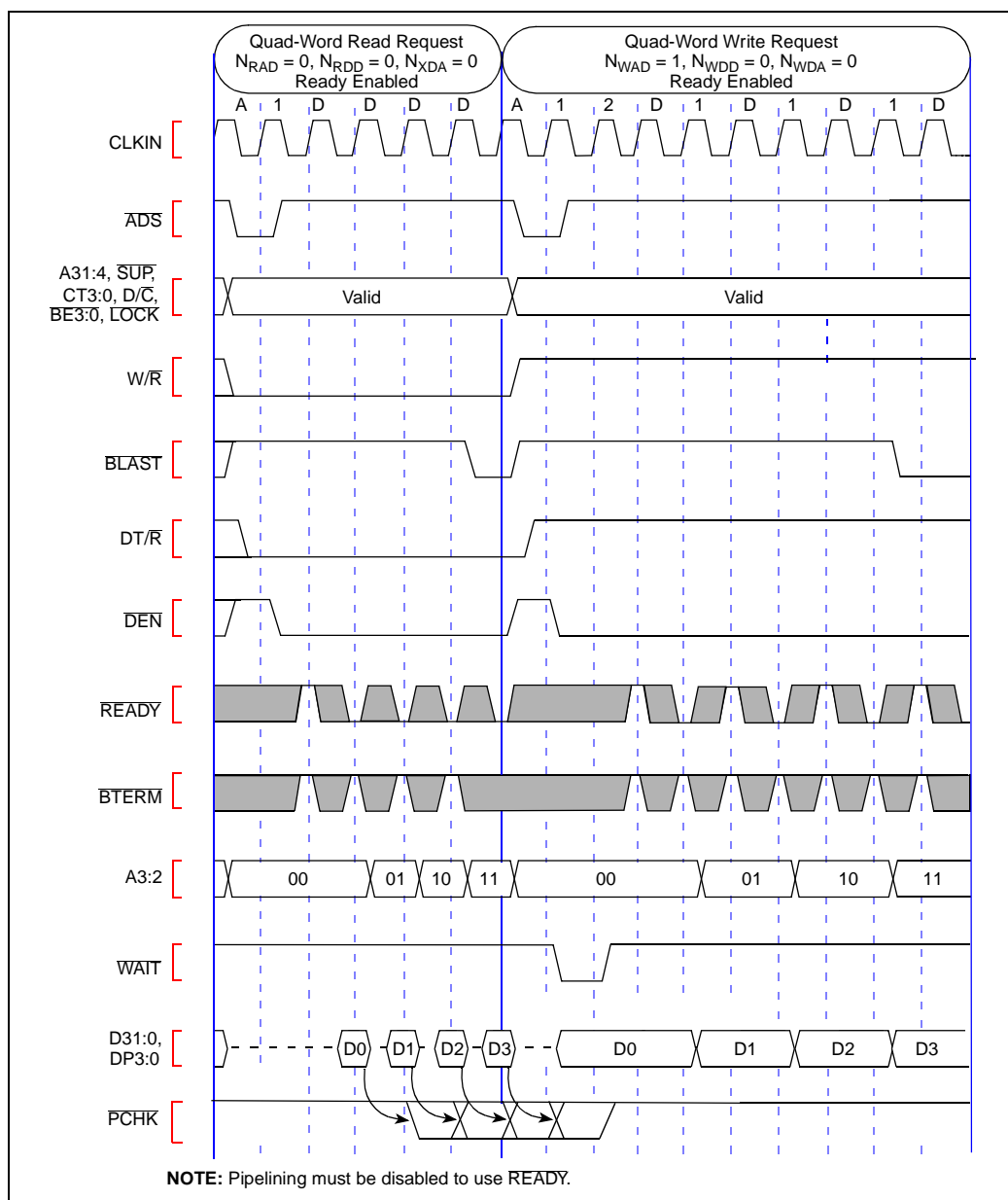


Figure 48. Terminating a Burst with BTERM

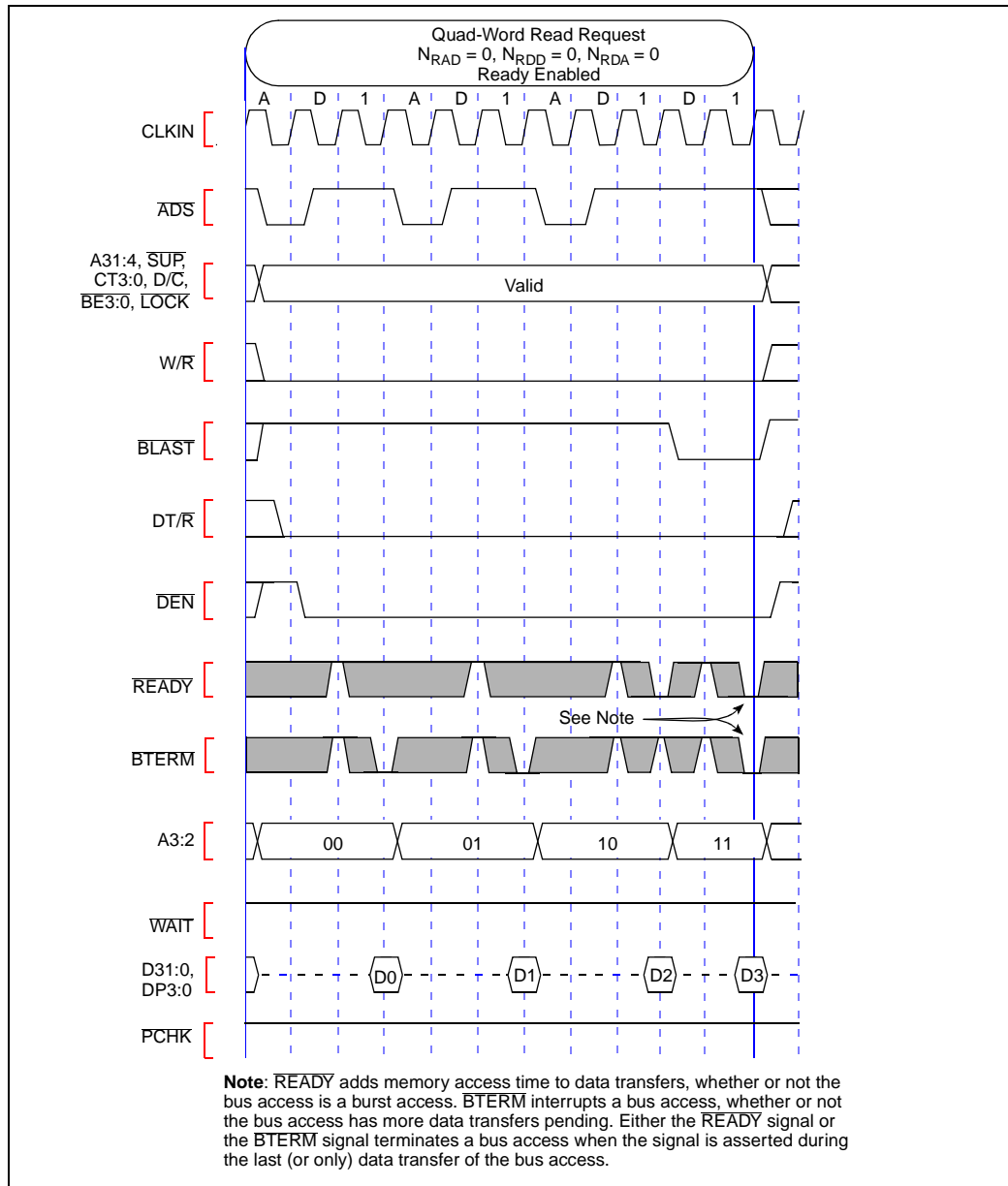
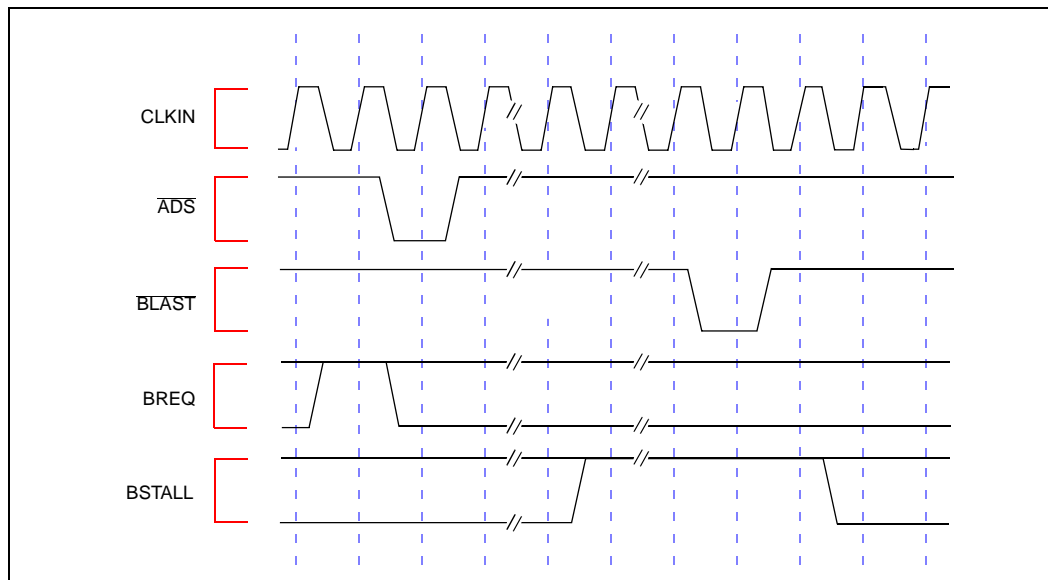


Figure 49. BREQ and BSTALL Operation



The processor can stall (BSTALL asserted) even with an empty bus queue (BREQ deasserted). Depending on the instruction stream and memory wait states, the two signals can be separated by several CLKIN cycles.

Bus arbitration logic that logically “ANDs” BSTALL and BREQ will not correctly grant the bus to the processor in all stall cases, potentially degrading processor performance.

Do not logically “AND” BSTALL and BREQ together in arbitration logic. Instead, the simplest bus arbitration should logically “OR” BSTALL and BREQ to determine the processor’s bus ownership requirements.

More sophisticated arbitration should recognize the priority nature of these two signals. Using a traffic light analogy, BREQ is a “yellow light” warning of a possible processor stall and BSTALL is a “red light” indicating a stall in progress.

Figure 50. $\overline{\text{BOFF}}$ Functional Timing. $\overline{\text{BOFF}}$ occurs during a burst or non-burst data cycle.

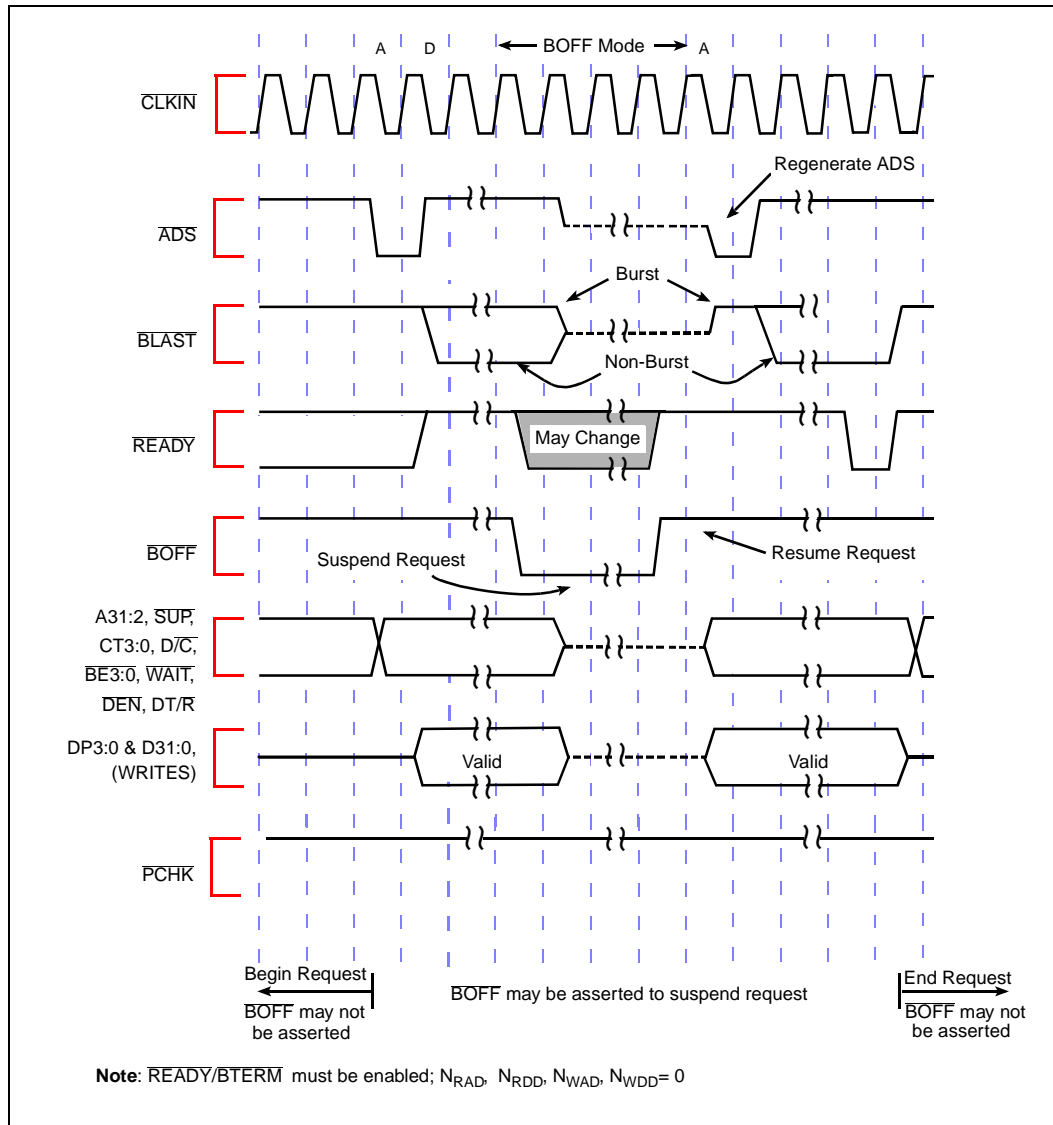


Figure 51. HOLD Functional Timing

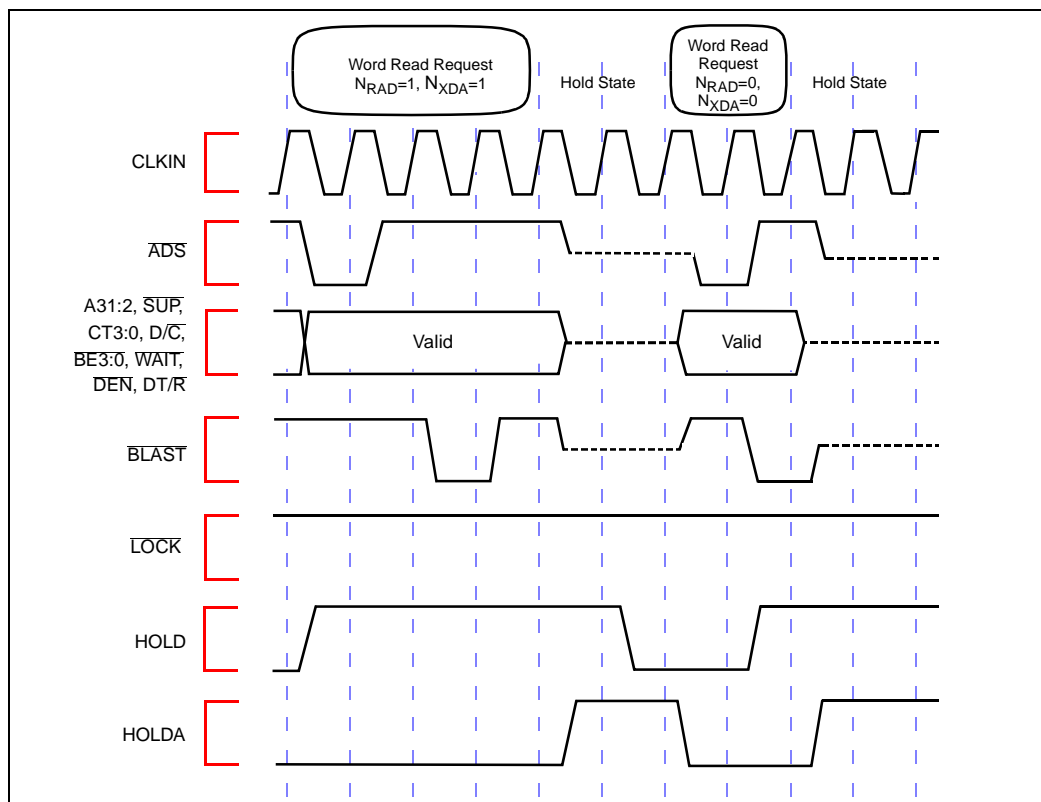


Figure 52. LOCK Delays HOLDA Timing

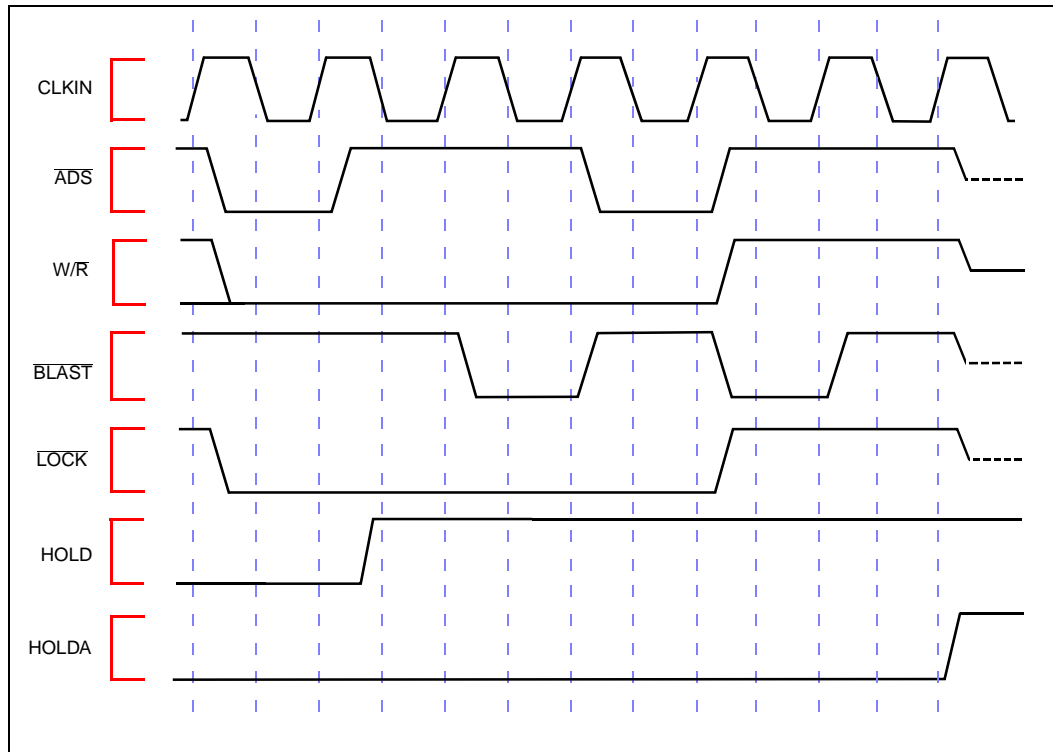


Figure 53. FAIL Functional Timing

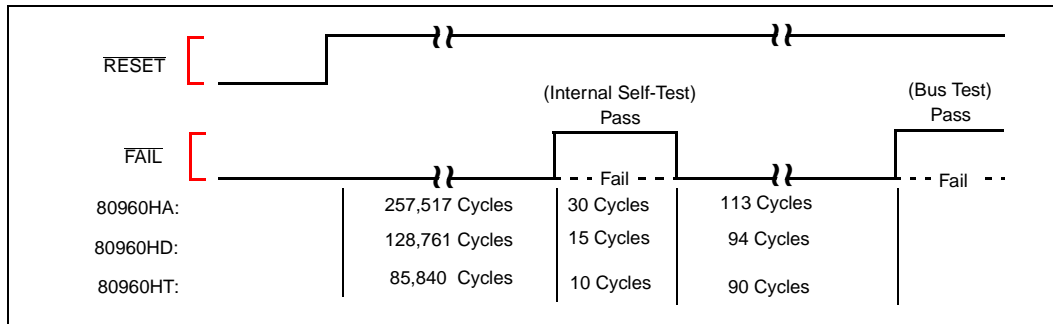


Figure 54. A Summary of Aligned and Unaligned Transfers for 32-Bit Regions

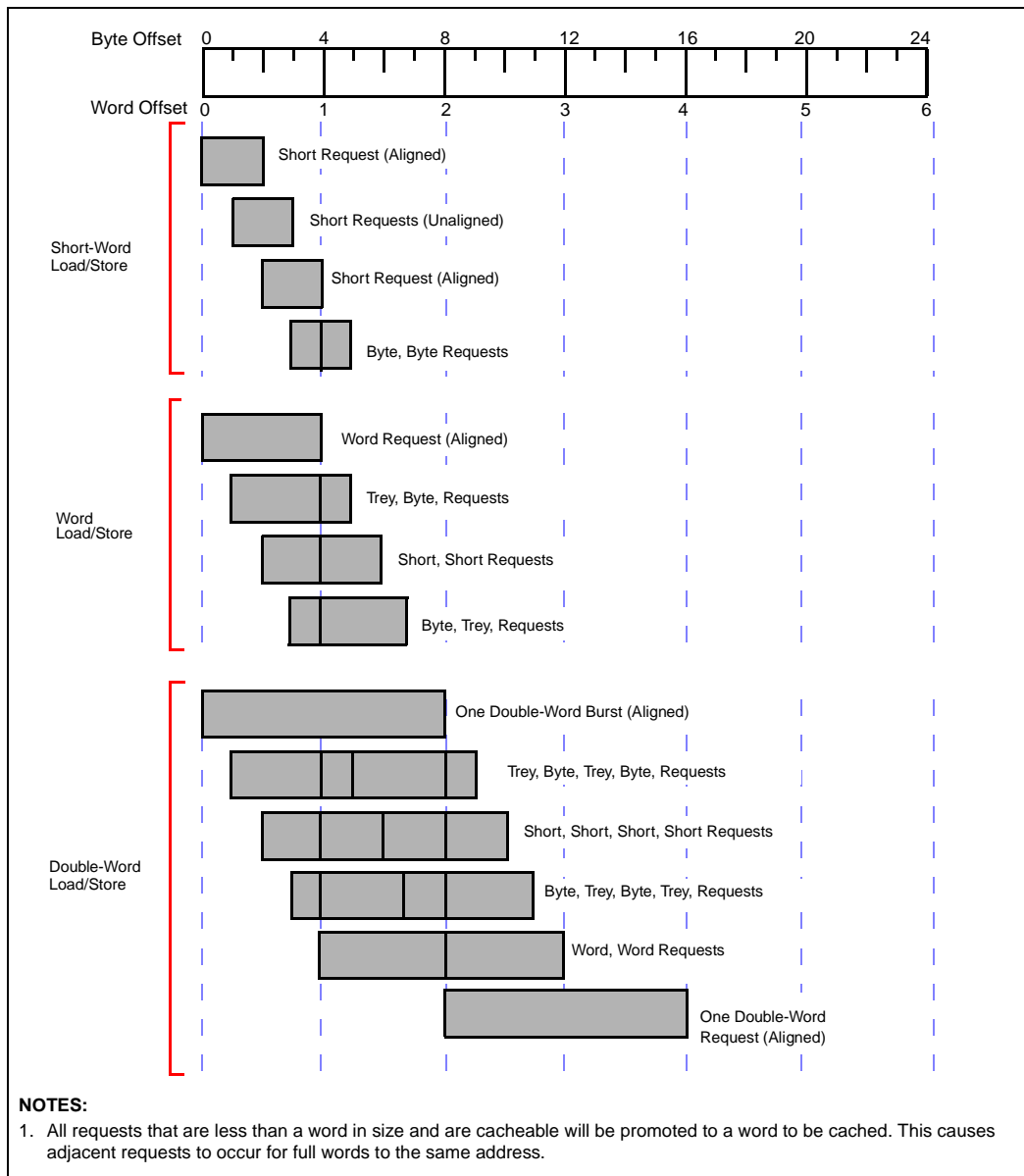


Figure 55. A Summary of Aligned and Unaligned Transfers for 32-Bit Regions (Continued)

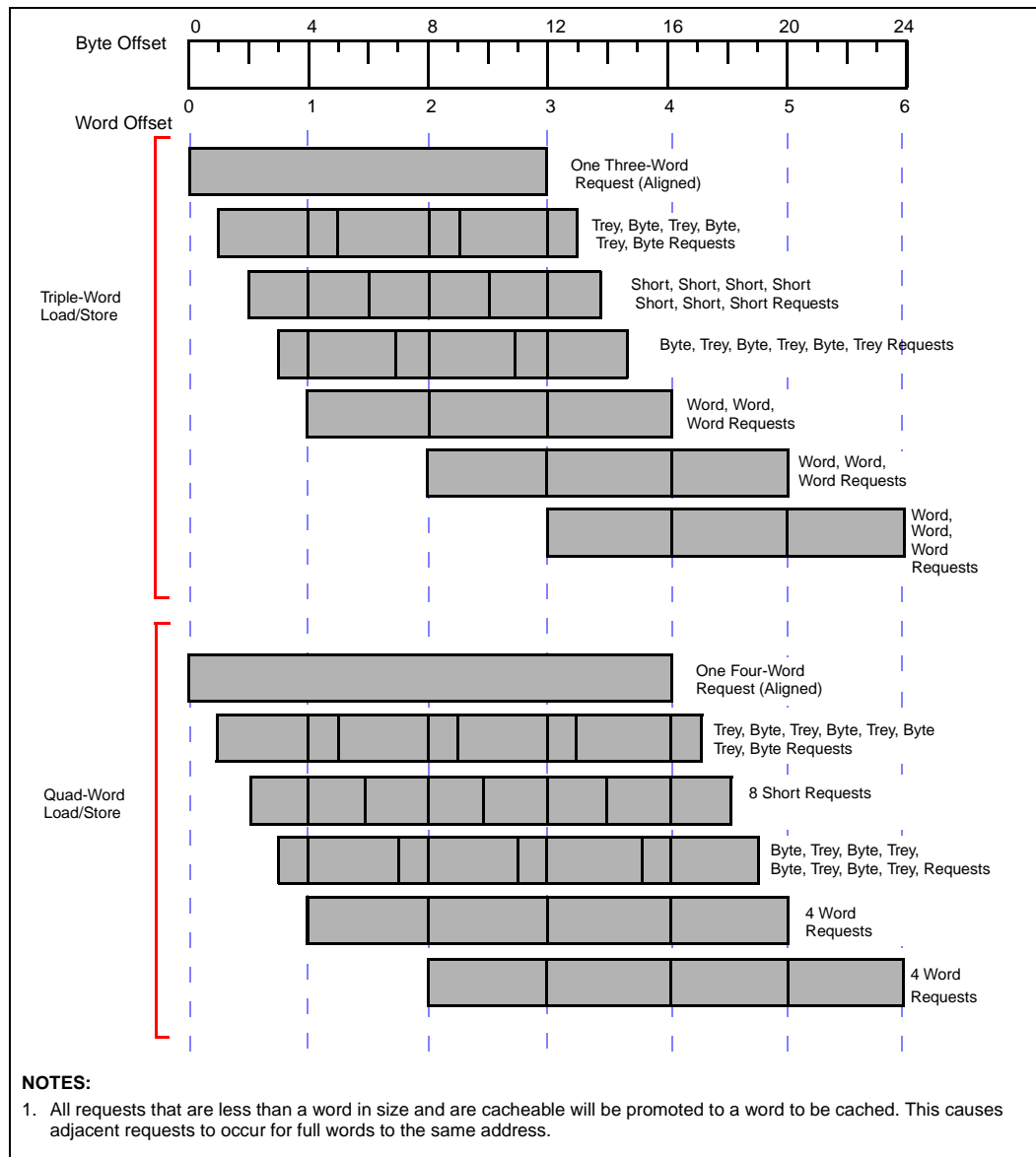


Figure 56. A Summary of Aligned and Unaligned Transfers for 16-Bit Bus

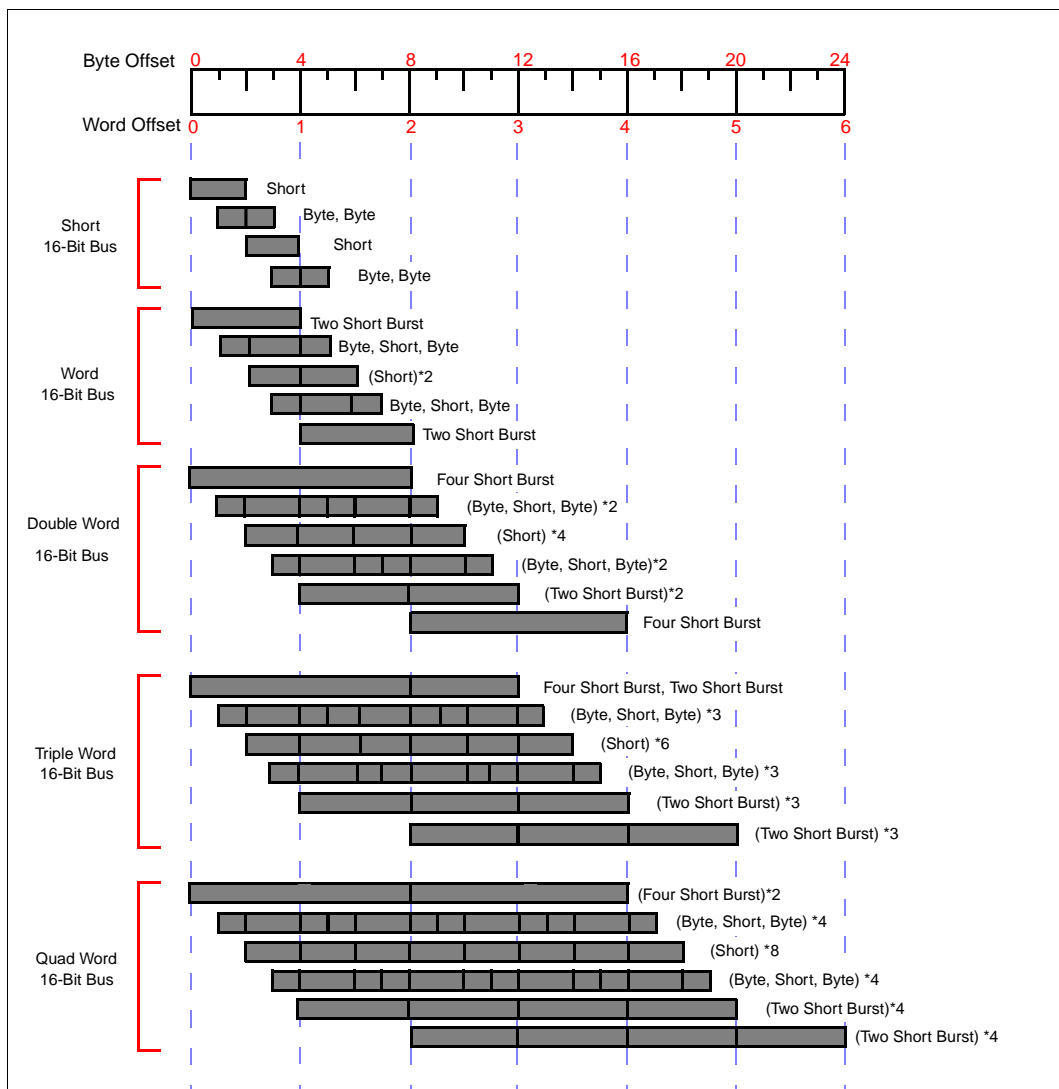


Figure 57. A Summary of Aligned and Unaligned Transfers for 8-Bit Bus

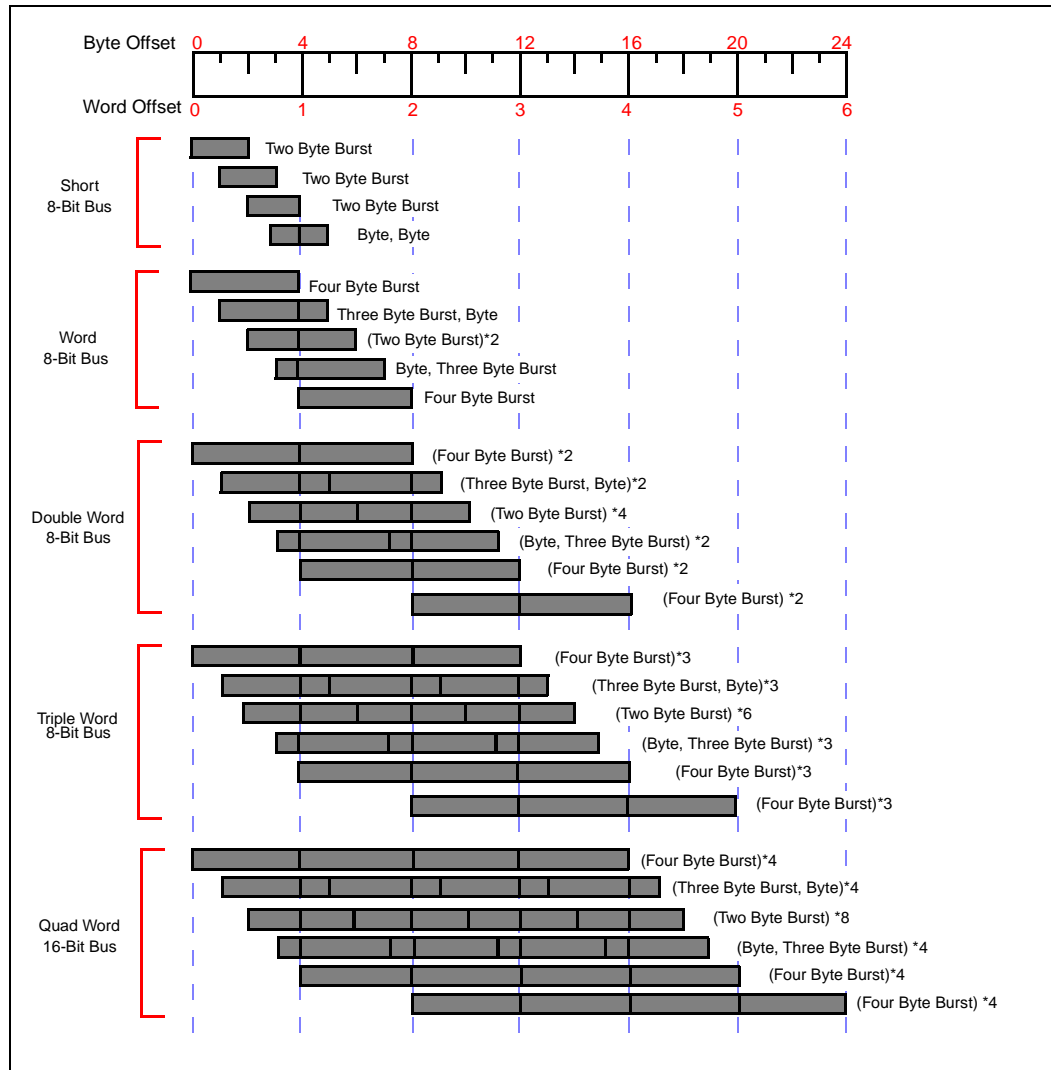


Figure 58. Idle Bus Operation

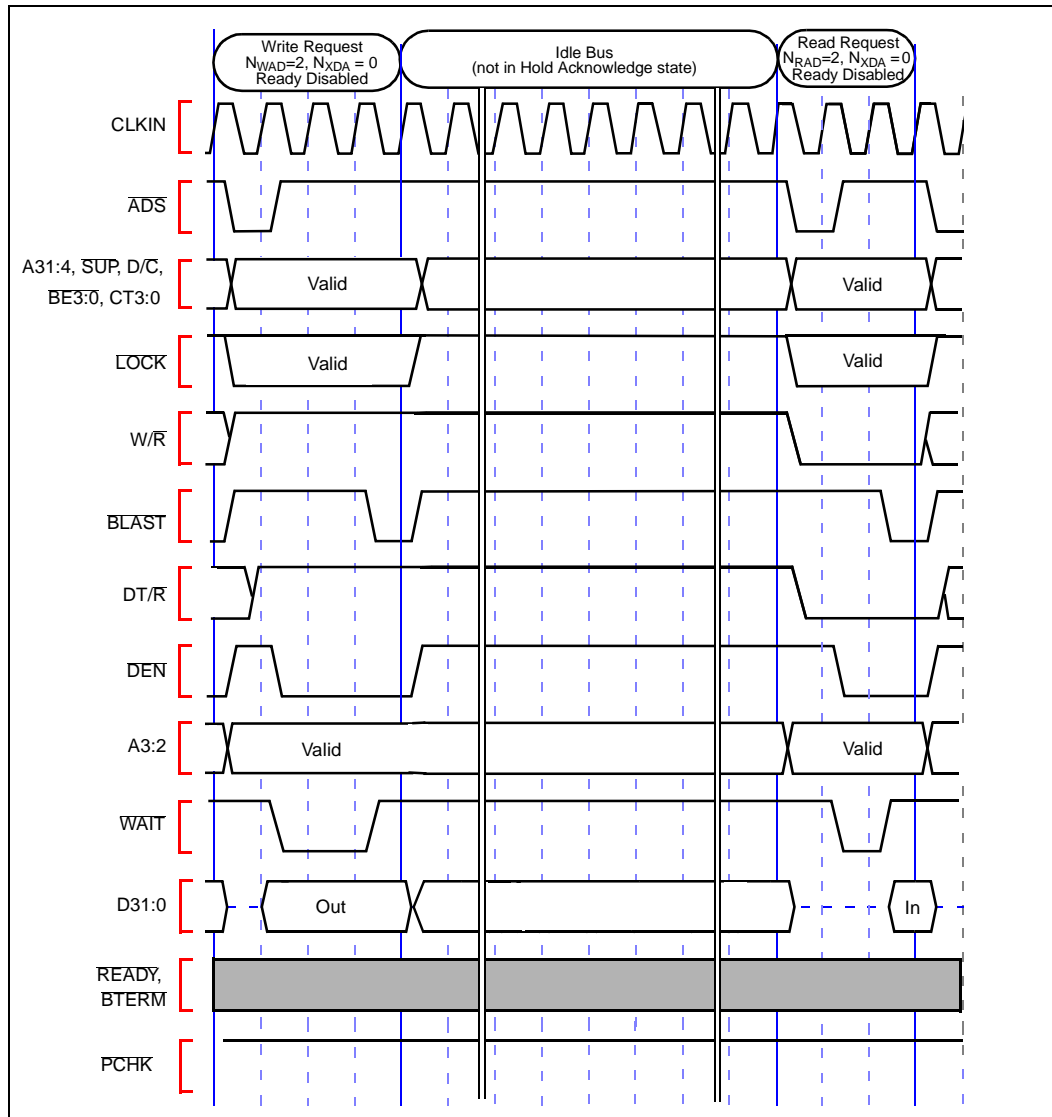
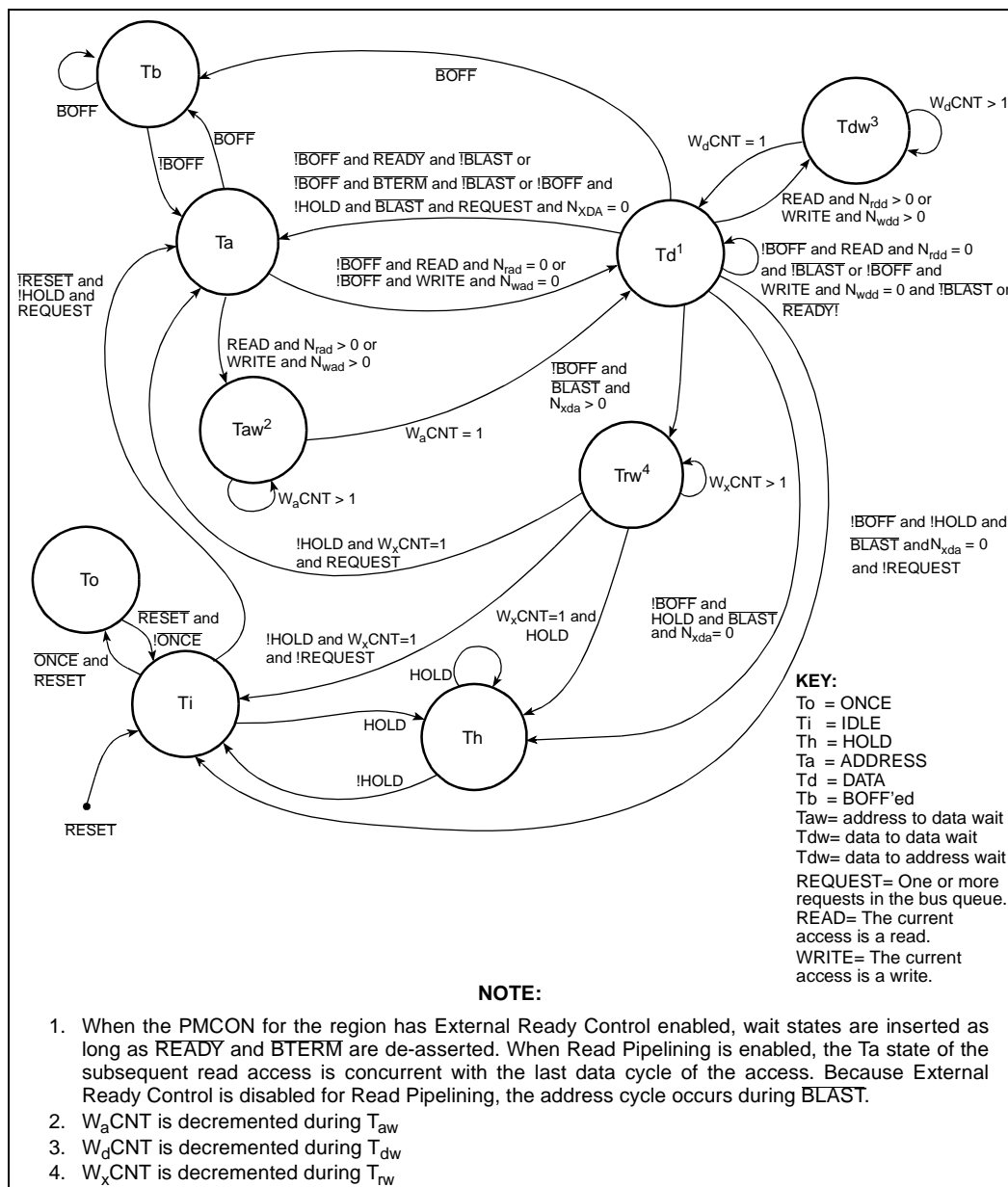


Figure 59. Bus States



5.1 80960Hx Boundary Scan Chain

Table 25. 80960Hx Boundary Scan Chain (Sheet 1 of 4)

| # | BOUNDARY SCAN CELL | CELL TYPE | COMMENT |
|---|-------------------------------------|---------------|---------|
| | DP3 | Bidirectional | |
| | DP2 | Bidirectional | |
| | DP0 | Bidirectional | |
| | DP1 | Bidirectional | |
| | STEST | Input | |
| | FAILBAR | Output | |
| | Enable for FAILBAR, BSTALL and BREQ | Control | |
| | ONCEBAR | Input | |
| | BOFFBAR | Input | |
| | D0 | Bidirectional | |
| | D1 | Bidirectional | |
| | D2 | Bidirectional | |
| | D3 | Bidirectional | |
| | D4 | Bidirectional | |
| | D5 | Bidirectional | |
| | D6 | Bidirectional | |
| | D7 | Bidirectional | |
| | Enable for DP(3:0) and D(31:0) | Control | |
| | D8 | Bidirectional | |
| | D9 | Bidirectional | |
| | D10 | Bidirectional | |
| | D11 | Bidirectional | |
| | D12 | Bidirectional | |
| | D13 | Bidirectional | |
| | D14 | Bidirectional | |
| | D15 | Bidirectional | |
| | D16 | Bidirectional | |
| | D17 | Bidirectional | |
| | D18 | Bidirectional | |
| | D19 | Bidirectional | |
| | D20 | Bidirectional | |

NOTES:

1. Cell#1 connects to TDO and cell #112 connects to TDI.
2. All outputs are three-state.
3. In output and bidirectional signals, a logical "1" on the enable signal enables the output. A logical "0" three-states the output.

Table 25. 80960Hx Boundary Scan Chain (Sheet 2 of 4)

| # | BOUNDARY SCAN CELL | CELL TYPE | COMMENT |
|---|--|---------------|-------------------------------------|
| | D21 | Bidirectional | |
| | D22 | Bidirectional | |
| | D23 | Bidirectional | |
| | D24 | Bidirectional | |
| | D25 | Bidirectional | |
| | D26 | Bidirectional | |
| | D27 | Bidirectional | |
| | D28 | Bidirectional | |
| | D29 | Bidirectional | |
| | D30 | Bidirectional | |
| | D31 | Bidirectional | |
| | BTERMBAR | Input | |
| | RDYBAR | Input | Appears as READYBAR in BSDL file. |
| | HOLD | Input | |
| | HOLDA | Output | |
| | Enable for HOLDA control | Control | |
| | ADSBAR | Output | |
| | BE3BAR | Output | Appears as BEBAR(3:0) in BSDL file. |
| | BE2BAR | Output | |
| | BE1BAR | Output | |
| | BE0BAR | Output | |
| | BLASTBAR | Output | |
| | DENBAR | Output | |
| | WRRDBAR | Output | Appears as WRBAR in BSDL file. |
| | DTRBAR | Output | |
| | Enable for DTRBAR | Control | |
| | WAITBAR | Output | |
| | BSTALL | Output | |
| | DATAODBAR | Output | Appears as DCBAR in BSDL file. |
| | USERSUPBAR | Output | Appears as SUPBAR in BSDL file. |
| | Enable for ADSBAR, BEBAR, BLASTBAR, DENBAR, WRRDBAR, WAITBAR, DCBAR, SUPBAR and LOCKBAR, | Control | |

NOTES:

1. Cell#1 connects to TDO and cell #112 connects to TDI.
2. All outputs are three-state.
3. In output and bidirectional signals, a logical "1" on the enable signal enables the output. A logical "0" three-states the output.

Table 25. 80960Hx Boundary Scan Chain (Sheet 3 of 4)

| # | BOUNDARY SCAN CELL | CELL TYPE | COMMENT |
|---|--------------------------------|-----------|---------|
| | LOCKBAR | Output | |
| | BREQ | Output | |
| | A31 | Output | |
| | A30 | Output | |
| | A29 | Output | |
| | A28 | Output | |
| | A27 | Output | |
| | A26 | Output | |
| | A25 | Output | |
| | A24 | Output | |
| | A23 | Output | |
| | A22 | Output | |
| | A21 | Output | |
| | A20 | Output | |
| | A19 | Output | |
| | A18 | Output | |
| | A17 | Output | |
| | A16 | Output | |
| | Enable for A(31:0) and CT(3:0) | Control | |
| | A15 | Output | |
| | A14 | Output | |
| | A13 | Output | |
| | A12 | Output | |
| | A11 | Output | |
| | A10 | Output | |
| | A9 | Output | |
| | A8 | Output | |
| | A7 | Output | |
| | A6 | Output | |
| | A5 | Output | |
| | A4 | Output | |
| | A3 | Output | |
| | A2 | Output | |
| | NMIBAR | Input | |

NOTES:

1. Cell#1 connects to TDO and cell #112 connects to TDI.
2. All outputs are three-state.
3. In output and bidirectional signals, a logical "1" on the enable signal enables the output. A logical "0" three-states the output.

Table 25. 80960Hx Boundary Scan Chain (Sheet 4 of 4)

| # | BOUNDARY SCAN CELL | CELL TYPE | COMMENT |
|---|--------------------|-----------|---------------------------------------|
| | XINT7BAR | Input | Appears as XINTBAR(7:0) in BSDL file. |
| | XINT6BAR | Input | |
| | XINT5BAR | Input | |
| | XINT4BAR | Input | |
| | XINT3BAR | Input | |
| | XINT2BAR | Input | |
| | XINT1BAR | Input | |
| | XINT0BAR | Input | |
| | RESETBAR | Input | |
| | CLKIN | Input | |
| | CT3 | Output | Appears as CT(3:0) in BSDL file. |
| | CT2 | Output | |
| | CT1 | Output | |
| | CT0 | Output | |
| | PCHK | Output | Appears as PCHKBAR in BSDL file. |
| | PCHK enable | Control | |

NOTES:

1. Cell#1 connects to TDO and cell #112 connects to TDI.
2. All outputs are three-state.
3. In output and bidirectional signals, a logical "1" on the enable signal enables the output. A logical "0" three-states the output.

5.2 Boundary Scan Description Language Example

Boundary-Scan Description Language (BSDL) example 14-2 meets the de facto standard means of describing essential features of ANSI/IEEE 1149.1-1993 compliant devices.

Example 1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 1 of 8)

```
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- - *****

- - Intel Corporation makes no warranty for the use of its products and assumes no
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- - *****

- - Boundary-Scan Description Language (BSDL Version 0.0) is a de-facto standard
means of describing essential features of ANSI/IEEE 1149.1-1990 compliant
devices. This language is under consideration by the IEEE for formal inclusion
within a supplement to the 1149.1-1990 standard. The generation of the supplement
entails an extensive IEEE review and a formal acceptance balloting procedure
which may change the resultant form of the language. Be aware that this process
may extend well into 1993, and at this time the IEEE does not endorse or hold an
opinion on the language.

- - *****

--

-- i960(R) Processor BSDL Model
```

Example 1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 2 of 8)

```
-- Project code HA
-- File **NOT** verified electrically
-----
-- Rev 0.7      18 Dec 1995 Updated for A-1 stepping.
-- Rev 0.6      08 Dec 1994
-- Rev 0.5      21 Nov 1994
-- Rev 0.4      31 Oct 1994
-- Rev 0.3      26 July 1994
-- Rev 0.2      22 June 1994
-- Rev 0.1      16 Mar 1994
-- Rev 0.0      30 Aug 1993
entity Ha_Processor is
    generic(PHYSICAL_PIN_MAP : string:= "PGA");

    port (A          : out    bit_vector(2 to 31);
          ADSBAR    : out    bit;
          BEBAR     : out    bit_vector(0 to 3);
          BLASTBAR  : out    bit;
          BOFFBAR   : in     bit;
          BREQ      : out    bit;
          BSTALL    : out    bit;
          BTERMBAR  : in     bit;
          CT        : out    bit_vector(0 to 3);
          CLKIN     : in     bit;
          D         : inout  bit_vector(0 to 31);
          DENBAR    : out    bit;
          DP        : inout  bit_vector(0 to 3);
          DTRBAR    : out    bit;
          DCBAR     : out    bit;
          FAILBAR   : out    bit;
          HOLD      : in     bit;
          HOLDA     : out    bit;
          LOCKBAR   : out    bit;
          NMIBAR    : in     bit;
          ONCEBAR   : in     bit;
          PCHKBAR   : out    bit;
          READYBAR  : in     bit;
          RESETBAR  : in     bit;
          STEST     : in     bit;
```

Example 1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 3 of 8)

```

        SUPBAR      : out      bit;
        TCK         : in       bit;
        TDI         : in       bit;
        TDO         : out      bit;
        TMS         : in       bit;
        TRST        : in       bit;
        WAITBAR     : out      bit;
        WRBAR       : out      bit;
        XINTBAR     : in       bit_vector(0 to 7);
        FIVEVREF    : linkage bit;
        VCCPLL      : linkage bit;
        VOLTDET     : out      bit;
        VCC1        : linkage bit_vector(0 to 23);
        VCC2        : linkage bit_vector(0 to 20);
        VSS1        : linkage bit_vector(0 to 25);
        VSS2        : linkage bit_vector(0 to 22);
        NC          : linkage bit_vector(0 to 4)

);

use STD_1149_1_1990.all;
use i960ha_a.all;

attribute PIN_MAP of Ha_Processor : entity is PHYSICAL_PIN_MAP;
constant PGA:PIN_MAP_STRING :=
    "A          : (D16, D17, E16, E17, F17, G16, G17, H17, J17,"&
    "          K17, L17, L16, M17, N17, N16, P17, Q17, P16,"&
    "          P15, Q16, R17, R16, Q15, S17, R15, S16, Q14, "&
    "          R14, Q13, S15),
    "ADSBAR     : R06,"&
    "BEBAR      : (R09, S07, S06, S05),"&
    "BLASTBAR   : S08,"&
    "BOFFBAR    : B01,"&
    "BREQ       : R13,"&
    "BSTALL     : R12,"&
    "BTERMBAR   : R04,"&
    "CT         : (A11, A12, A13, A14),"&
    "CLKIN      : C13,"&

```


Example 1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 4 of 8)

```

"D          : (E03, C02, D02, C01, E02, D01, F02, E01, F01,"&
"          G01, H02, H01, J01, K01, L02, L01, M01, N01,"&
"          N02, P01, P02, Q01, P03, Q02, R01, S01, Q03,"&
"          R02, Q04, S02, Q05, R03),"&
"DENBAR    : S09,"&
"DP        : (A03, B03, A04, B04),"&
"DTRBAR    : S11,"&
"DCBAR    : S13,"&
"FAILBAR   : A02,"&
"HOLD      : R05,"&
"HOLDA    : S04,"&
"LOCKBAR   : S14,"&
"NMIBAR    : D15,"&
"ONCEBAR   : C03,"&
"PCHKBAR   : B08,"&
"READYBAR  : S03,"&
"RESETBAR  : A16,"&
"STEST     : B02,"&
"SUPBAR    : Q12,"&
"TCK       : B05,"&
"TDI       : A07,"&
"TDO       : A08,"&
"TMS       : B06,"&
"TRST      : A06,"&
"WAITBAR   : S12,"&
"WRBAR     : S10,"&
" XINTBAR  : (B15, A15, A17, B16, C15, B17, C16, C17),"&
"FIVEVREF  : C05,"&
"VOLTDET   : A05,"&
"VCCPLL    : B10,"&
" VCC1     : (M02, K02, J02, G02, N03, F03, C06, B07, B09, B11,"&
"          B12, C14, E15, F16, H16, J16, K16, M16, N15, Q06,"&
"          R07, R08, R10, R11),"&
" VSS1     : (G03, H03, J03, K03, L03, M03, C07, C08, C09, C10,"&
"          C11, C12, Q07, Q08, Q09, Q10, Q11, F15, G15, H15,"&
"          J15, K15, L15, M15, A01, C04),"&
"NC        : (A09, A10, B13, B14, D03)";
    
```

Example 1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 5 of 8)

```

attribute Tap_Scan_In    of TDI    : signal is true;
attribute Tap_Scan_Mode of TMS    : signal is true;
attribute Tap_Scan_Out  of TDO    : signal is true;
attribute Tap_Scan_Reset of TRST   : signal is true;
attribute Tap_Scan_Clock of TCK    : signal is (66.0e6, BOTH);

attribute Instruction_Length of Ha_Processor: entity is 4;

attribute Instruction_Opcode of Ha_Processor: entity is

    "BYPASS      (1111)," &
    "EXTEST      (0000)," &
    "SAMPLE      (0001)," &
    "IDCODE      (0010)," &
    "RUBIST      (0111)," &
    "CLAMP       (0100)," &
    "HIGHZ       (1000)," &
    "Reserved    (1011, 1100)";

attribute Instruction_Capture of Ha_Processor: entity is "0001";

attribute Instruction_Private of Ha_Processor: entity is "Reserved" ;

attribute Idcode_Register of Ha_Processor: entity is
    "0010"           & --version,
    "1000100001000000" & --part number
    "00000001001"   & --manufacturers identity
    "1";             --required by the standard

attribute Register_Access of Ha_Processor: entity is
    "Runbist[32]    (RUBIST)," &
    "Bypass         (CLAMP, HIGHZ)";

{*****}
{ The first cell, cell 0, is closest to TDO }
{ BC_1:Control, Output3 CBSC_1:Bidir BC_4: Input, Clock }
{*****}

```

Example 1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 6 of 8)

```

attribute Boundary_Cells of Ha_Processor: entity is "BC_4, BC_1, CBSC_1";
attribute Boundary_Length of Ha_Processor: entity is 112;
attribute Boundary_Register of Ha_Processor: entity is

"0 (CBSC_1, DP(3),      bidir, X, 17, 1, Z)," &
"1 (CBSC_1, DP(2),      bidir, X, 17, 1, Z)," &
"2 (CBSC_1, DP(0),      bidir, X, 17, 1, Z)," &
"3 (CBSC_1, DP(1),      bidir, X, 17, 1, Z)," &
"4 (BC_4,  STEST,       input, X)," &
"5 (BC_1,  FAILBAR,     output3, X, 6, 1, Z)," &
"6 (BC_1,  *,           control, 1)," &
"7 (BC_4,  ONCEBAR,     input, X)," &
"8 (BC_4,  BOFFBAR,     input, X)," &
"9 (CBSC_1, D(0),       bidir, X, 17, 1, Z)," &
"10 (CBSC_1, D(1),      bidir, X, 17, 1, Z)," &
"11 (CBSC_1, D(2),      bidir, X, 17, 1, Z)," &
"12 (CBSC_1, D(3),      bidir, X, 17, 1, Z)," &
"13 (CBSC_1, D(4),      bidir, X, 17, 1, Z)," &
"14 (CBSC_1, D(5),      bidir, X, 17, 1, Z)," &
"15 (CBSC_1, D(6),      bidir, X, 17, 1, Z)," &
"16 (CBSC_1, D(7),      bidir, X, 17, 1, Z)," &
"17 (BC_1,  *,           control, 1)," &
"18 (CBSC_1, D(8),      bidir, X, 17, 1, Z)," &
"19 (CBSC_1, D(9),      bidir, X, 17, 1, Z)," &
"20 (CBSC_1, D(10),     bidir, X, 17, 1, Z)," &
"21 (CBSC_1, D(11),     bidir, X, 17, 1, Z)," &
"22 (CBSC_1, D(12),     bidir, X, 17, 1, Z)," &
"23 (CBSC_1, D(13),     bidir, X, 17, 1, Z)," &
"24 (CBSC_1, D(14),     bidir, X, 17, 1, Z)," &
"25 (CBSC_1, D(15),     bidir, X, 17, 1, Z)," &
"26 (CBSC_1, D(16),     bidir, X, 17, 1, Z)," &
"27 (CBSC_1, D(17),     bidir, X, 17, 1, Z)," &
"28 (CBSC_1, D(18),     bidir, X, 17, 1, Z)," &
"29 (CBSC_1, D(19),     bidir, X, 17, 1, Z)," &
"30 (CBSC_1, D(20),     bidir, X, 17, 1, Z)," &
"31 (CBSC_1, D(21),     bidir, X, 17, 1, Z)," &
"32 (CBSC_1, D(22),     bidir, X, 17, 1, Z)," &
"33 (CBSC_1, D(23),     bidir, X, 17, 1, Z)," &
"34 (CBSC_1, D(24),     bidir, X, 17, 1, Z)," &

```

Example 1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 7 of 8)

```

"35 (CBSC_1, D(25),      bidir,  X, 17, 1, Z)," &
"36 (CBSC_1, D(26),      bidir,  X, 17, 1, Z)," &
"37 (CBSC_1, D(27),      bidir,  X, 17, 1, Z)," &
"38 (CBSC_1, D(28),      bidir,  X, 17, 1, Z)," &
"39 (CBSC_1, D(29),      bidir,  X, 17, 1, Z)," &
"40 (CBSC_1, D(30),      bidir,  X, 17, 1, Z)," &
"41 (CBSC_1, D(31),      bidir,  X, 17, 1, Z)," &
"42 (BC_4,  BTERMBAR,    input,  X)," &
"43 (BC_4,  READYBAR,    input,  X)," &
"44 (BC_4,  HOLD,        input,  X)," &
"45 (BC_1,  HOLDA,        output3, X, 46, 1, Z)," &
"46 (BC_1,  *,            control, 1)," &
"47 (BC_1,  ADSBAR,        output3, X, 61, 1, Z)," &
"48 (BC_1,  BEBAR(3),      output3, X, 61, 1, Z)," &
"49 (BC_1,  BEBAR(2),      output3, X, 61, 1, Z)," &
"50 (BC_1,  BEBAR(1),      output3, X, 61, 1, Z)," &
"51 (BC_1,  BEBAR(0),      output3, X, 61, 1, Z)," &
"52 (BC_1,  BLASTBAR,      output3, X, 61, 1, Z)," &
"53 (BC_1,  DENBAR,        output3, X, 61, 1, Z)," &
"54 (BC_1,  WRBAR,         output3, X, 61, 1, Z)," &
"55 (BC_1,  DTRBAR,        output3, X, 56, 1, Z)," &
"56 (BC_1,  *,            control, 1)," &
"57 (BC_1,  WAITBAR,       output3, X, 61, 1, Z)," &
"58 (BC_1,  BSTALL,        output3, X, 6, 1, Z)," &
"59 (BC_1,  DCBAR,         output3, X, 61, 1, Z)," &
"60 (BC_1,  SUPBAR,        output3, X, 61, 1, Z)," &
"61 (BC_1,  *,            control, 1)," &
"62 (BC_1,  LOCKBAR,       output3, X, 61, 1, Z)," &
"63 (BC_1,  BREQ,          output3, X, 6, 1, Z)," &
"64 (BC_1,  A(31),         output3, X, 80, 1, Z)," &
"65 (BC_1,  A(30),         output3, X, 80, 1, Z)," &
"66 (BC_1,  A(29),         output3, X, 80, 1, Z)," &
"67 (BC_1,  A(28),         output3, X, 80, 1, Z)," &
"68 (BC_1,  A(27),         output3, X, 80, 1, Z)," &
"69 (BC_1,  A(26),         output3, X, 80, 1, Z)," &
"70 (BC_1,  A(25),         output3, X, 80, 1, Z)," &
"71 (BC_1,  A(24),         output3, X, 80, 1, Z)," &
"72 (BC_1,  A(23),         output3, X, 80, 1, Z)," &
"73 (BC_1,  A(22),         output3, X, 80, 1, Z)," &

```

Example 1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 8 of 8)

```

"74 (BC_1, A(21), output3, X, 80, 1, Z)," &
"75 (BC_1, A(20), output3, X, 80, 1, Z)," &
"76 (BC_1, A(19), output3, X, 80, 1, Z)," &
"77 (BC_1, A(18), output3, X, 80, 1, Z)," &
"78 (BC_1, A(17), output3, X, 80, 1, Z)," &
"79 (BC_1, A(16), output3, X, 80, 1, Z)," &
"80 (BC_1, *, control, 1)," &
"81 (BC_1, A(15), output3, X, 80, 1, Z)," &
"82 (BC_1, A(14), output3, X, 80, 1, Z)," &
"83 (BC_1, A(13), output3, X, 80, 1, Z)," &
"84 (BC_1, A(12), output3, X, 80, 1, Z)," &
"85 (BC_1, A(11), output3, X, 80, 1, Z)," &
"86 (BC_1, A(10), output3, X, 80, 1, Z)," &
"87 (BC_1, A(9), output3, X, 80, 1, Z)," &
"88 (BC_1, A(8), output3, X, 80, 1, Z)," &
"89 (BC_1, A(7), output3, X, 80, 1, Z)," &
"90 (BC_1, A(6), output3, X, 80, 1, Z)," &
"91 (BC_1, A(5), output3, X, 80, 1, Z)," &
"92 (BC_1, A(4), output3, X, 80, 1, Z)," &
"93 (BC_1, A(3), output3, X, 80, 1, Z)," &
"94 (BC_1, A(2), output3, X, 80, 1, Z)," &
"95 (BC_4, NMIBAR, input, X)," &
"96 (BC_4, XINTBAR(7), input, X)," &
"97 (BC_4, XINTBAR(6), input, X)," &
"98 (BC_4, XINTBAR(5), input, X)," &
"99 (BC_4, XINTBAR(4), input, X)," &
"100 (BC_4, XINTBAR(3), input, X)," &
"101 (BC_4, XINTBAR(2), input, X)," &
"102 (BC_4, XINTBAR(1), input, X)," &
"103 (BC_4, XINTBAR(0), input, X)," &
"104 (BC_4, RESETBAR, input, X)," &
"105 (BC_4, CLKIN, input, X)," &
"106 (BC_1, CT(3), output3, X, 80, 1, Z)," &
"107 (BC_1, CT(2), output3, X, 80, 1, Z)," &
"108 (BC_1, CT(1), output3, X, 80, 1, Z)," &
"109 (BC_1, CT(0), output3, X, 80, 1, Z)," &
"110 (BC_1, PCHKBAR, output3, X, 111, 1, Z)," &
"111 (BC_1, *, control, 1)";
end Ha_Processor;
    
```

Example 2. Boundary-Scan Description Language (BSDL) for PQ2 Package Example (Sheet 1 of 8)

```

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-- Boundary-Scan Description Language (BSDL Version 0.0) is a de-facto

-- standard means of describing essential features of ANSI/IEEE 1149.1-1990
compliant devices. This language is under consideration by the IEEE for formal
inclusion within a supplement to the 1149.1-1990 standard. The generation of the
supplement entails an extensive IEEE review and a formal acceptance balloting
procedure which may change the resultant form of the language. Be aware that this
process may extend well into 1993, and at this time the IEEE does not endorse or
hold an opinion on the language.

-- i960(R) Processor BSDL Model
-- Project code HA
-- File **NOT** verified electrically

-- -----
-- Rev 0.8      4 Apr 1996  Changed for PQ2 Package
-- Rev 0.7      18 Dec 1995  Updated for A-1 stepping.
-- Rev 0.6      08 Dec 1994
-- Rev 0.5      21 Nov 1994
-- Rev 0.4      31 Oct 1994
-- Rev 0.3      26 July 1994
-- Rev 0.2      22 June 1994
-- Rev 0.1      16 Mar 1994
-- Rev 0.0      30 Aug 1993

```

Example 2. Boundary-Scan Description Language (BSDL) for PQ2 Package Example (Sheet 2 of 8)

```
entity Ha_Processor is
  generic(PHYSICAL_PIN_MAP : string:= "PQ2");
  port (A          : out   bit_vector(2 to 31);
        ADSBAR    : out   bit;
        BEBAR     : out   bit_vector(0 to 3);
        BLASTBAR  : out   bit;
        BOFFBAR   : in    bit;
        BREQ      : out   bit;
        BSTALL    : out   bit;
        BTERMBAR  : in    bit;
        CT        : out   bit_vector(0 to 3);
        CLKIN     : in    bit;
        D         : inout  bit_vector(0 to 31);
        DENBAR    : out   bit;
        DP        : inout  bit_vector(0 to 3);
        DTRBAR    : out   bit;
        DCBAR     : out   bit;
        FAILBAR   : out   bit;
        HOLD      : in    bit;
        HOLDA     : out   bit;
        LOCKBAR   : out   bit;
        NMIBAR    : in    bit;
        ONCEBAR   : in    bit;
        PCHKBAR   : out   bit;
        READYBAR  : in    bit;
        RESETBAR  : in    bit;
        STEST     : in    bit;
        SUPBAR    : out   bit;
        TCK       : in    bit;
        TDI       : in    bit;
        TDO       : out   bit;
        TMS       : in    bit;
        TRST      : in    bit;
        WAITBAR   : out   bit;
        WRBAR     : out   bit;
        XINTBAR   : in    bit_vector(0 to 7);
        FIVEVREF  : linkage bit;
        VCCPLL    : linkage bit;
```

Example 2. Boundary-Scan Description Language (BSDL) for PQ2 Package Example (Sheet 3 of 8)

```

VCC1      : linkage bit_vector(0 to 23);
VCC2      : linkage bit_vector(0 to 23);
VSS1      : linkage bit_vector(0 to 23);
VSS2      : linkage bit_vector(0 to 23)

);

use STD_1149_1_1990.all;
use i960ha_a.all;

attribute PIN_MAP of Ha_Processor : entity is PHYSICAL_PIN_MAP;
constant PQ2:PIN_MAP_STRING :=

"A          : (151, 150, 147, 146, 145, 144, 141, 140, 139, 138,"&
"           135, 134, 133, 132, 127, 126, 125, 124, 121, 120,"&
"           119, 118, 113, 112, 111, 110, 107, 106, 105, 104),"&
"ADSBAR    : 77,"&
"BE BAR    : (83, 82, 79, 78),"&
"BLASTBAR  : 84,"&
"BOFFBAR   : 10,"&
"BREQ      : 100,"&
"BSTALL    : 91,"&
"BTERMBAR  : 67,"&
"CT        : (183, 182, 181, 180),"&
"CLKIN     : 175,"&
"D         : (12, 13, 14, 15, 20, 21, 22, 23, 26, 27, 28, 29,"&
"           34, 35, 36, 37, 39, 40, 41, 42, 45, 50, 51, 52,"&
"           54, 55, 56, 57, 61, 62, 63, 64),"&
"DENBAR    : 85,"&
"DP        : (206, 207, 203, 202),"&
"DTRBAR    : 89,"&
"DCBAR     : 96,"&
"FAILBAR   : 5,"&
"HOLD      : 69,"&
"HOLDA     : 72,"&
"LOCKBAR   : 99,"&
"NMIBAR    : 159,"&

```


Example 2. Boundary-Scan Description Language (BSDL) for PQ2 Package Example (Sheet 4 of 8)

```

"ONCEBAR      : 6,"&
"PCHKBAR      : 189,"&
"READYBAR     : 68,"&
"RESETBAR     : 174,"&
"STEST        : 208,"&
"SUPBAR        : 97,"&
"TCK           : 194,"&
"TDI           : 191,"&
"TDO           : 188,"&
"TMS           : 192,"&
"TRST         : 193,"&
"WAITBAR      : 90,"&
"WRBAR        : 88,"&
"XINTBAR      : (169, 168, 167, 166, 163, 162, 161, 160),"&
"FIVEVREF     : 197,"&
"VCCPLL       : 177,"&
"VCC1         : (1, 4, 9, 11, 17, 19, 25, 31, 33, 38, 44, 46,"&
"              49, 59, 60, 66, 71, 74, 76, 81, 87, 92, 95, 101),"&
"VCC2         : (102, 109, 115, 117, 123, 128, 131, 137, 143, 149,"&
"              153, 154, 158, 165, 171, 173, 176, 179, 185, 187,"&
"              196, 199, 201, 204),"&
"VSS1         : (2, 3, 7, 8, 16, 18, 24, 30, 32, 43, 47, 48,"&
"              53, 58, 65, 70, 73, 75, 80, 86, 93, 94, 98, 103),"&
"VSS2         : (108, 114, 116, 122, 129, 130, 136, 142, 148, 152,"&
"              155, 156, 157, 164, 170, 172, 178, 184, 186, 190,"&
"              195, 198, 200, 205)";

```

```

attribute Tap_Scan_In   of TDI   : signal is true;
attribute Tap_Scan_Mode of TMS   : signal is true;
attribute Tap_Scan_Out  of TDO   : signal is true;
attribute Tap_Scan_Reset of TRST  : signal is true;
attribute Tap_Scan_Clock of TCK   : signal is (66.0e6, BOTH);

```

```

attribute Instruction_Length of Ha_Processor: entity is 4;

```

```

attribute Instruction_Opcode of Ha_Processor: entity is

```

Example 2. Boundary-Scan Description Language (BSDL) for PQ2 Package Example (Sheet 5 of 8)

```

    "BYPASS      (1111)," &
    "EXTEST      (0000)," &
    "SAMPLE      (0001)," &
    "IDCODE      (0010)," &
    "RUBIST      (0111)," &
    "CLAMP       (0100)," &
    "HIGHZ       (1000)," &
    "Reserved    (1011, 1100)";

attribute Instruction_Capture of Ha_Processor: entity is "0001";

attribute Instruction_Private of Ha_Processor: entity is "Reserved" ;

attribute Idcode_Register of Ha_Processor: entity is
    "0001" & version,
    "1000100001000000" & part number
    "00000001001"& manufacturers identity
    "1";    required by the standard

attribute Register_Access of Ha_Processor: entity is
    "Runbist[32]    (RUBIST)," &
    "Bypass        (CLAMP, HIGHZ)";
*****
{ The first cell, cell 0, is closest to TDO                                }
{ BC_1:Control, Output3 CBSC_1:Bidir BC_4: Input, Clock                    }
*****

attribute Boundary_Cells of Ha_Processor: entity is "BC_4, BC_1, CBSC_1";
attribute Boundary_Length of Ha_Processor: entity is 112;
attribute Boundary_Register of Ha_Processor: entity is

    "0 (CBSC_1, DP(3),        bidir, X, 17, 1, Z)," &
    "1 (CBSC_1, DP(2),        bidir, X, 17, 1, Z)," &
    "2 (CBSC_1, DP(0),        bidir, X, 17, 1, Z)," &
    "3 (CBSC_1, DP(1),        bidir, X, 17, 1, Z)," &
    "4 (BC_4, STEST,          input, X)," &
    "5 (BC_1, FAILBAR,        output3, X, 6, 1, Z)," &

```

Example 2. Boundary-Scan Description Language (BSDL) for PQ2 Package Example (Sheet 6 of 8)

```

"6 (BC_1, *, control, 1)," &
"7 (BC_4, ONCEBAR, input, X)," &
"8 (BC_4, BOFFBAR, input, X)," &
"9 (CBSC_1, D(0), bidir, X, 17, 1, Z)," &
"10 (CBSC_1, D(1), bidir, X, 17, 1, Z)," &
"11 (CBSC_1, D(2), bidir, X, 17, 1, Z)," &
"12 (CBSC_1, D(3), bidir, X, 17, 1, Z)," &
"13 (CBSC_1, D(4), bidir, X, 17, 1, Z)," &
"14 (CBSC_1, D(5), bidir, X, 17, 1, Z)," &
"15 (CBSC_1, D(6), bidir, X, 17, 1, Z)," &
"16 (CBSC_1, D(7), bidir, X, 17, 1, Z)," &
"17 (BC_1, *, control, 1)," &
"18 (CBSC_1, D(8), bidir, X, 17, 1, Z)," &
"19 (CBSC_1, D(9), bidir, X, 17, 1, Z)," &
"20 (CBSC_1, D(10), bidir, X, 17, 1, Z)," &
"21 (CBSC_1, D(11), bidir, X, 17, 1, Z)," &
"22 (CBSC_1, D(12), bidir, X, 17, 1, Z)," &
"23 (CBSC_1, D(13), bidir, X, 17, 1, Z)," &
"24 (CBSC_1, D(14), bidir, X, 17, 1, Z)," &
"25 (CBSC_1, D(15), bidir, X, 17, 1, Z)," &
"26 (CBSC_1, D(16), bidir, X, 17, 1, Z)," &
"27 (CBSC_1, D(17), bidir, X, 17, 1, Z)," &
"28 (CBSC_1, D(18), bidir, X, 17, 1, Z)," &
"29 (CBSC_1, D(19), bidir, X, 17, 1, Z)," &
"30 (CBSC_1, D(20), bidir, X, 17, 1, Z)," &
"31 (CBSC_1, D(21), bidir, X, 17, 1, Z)," &
"32 (CBSC_1, D(22), bidir, X, 17, 1, Z)," &
"33 (CBSC_1, D(23), bidir, X, 17, 1, Z)," &
"34 (CBSC_1, D(24), bidir, X, 17, 1, Z)," &
"35 (CBSC_1, D(25), bidir, X, 17, 1, Z)," &
"36 (CBSC_1, D(26), bidir, X, 17, 1, Z)," &
"37 (CBSC_1, D(27), bidir, X, 17, 1, Z)," &
"38 (CBSC_1, D(28), bidir, X, 17, 1, Z)," &
"39 (CBSC_1, D(29), bidir, X, 17, 1, Z)," &
"40 (CBSC_1, D(30), bidir, X, 17, 1, Z)," &

```

Example 2. Boundary-Scan Description Language (BSDL) for PQ2 Package Example (Sheet 7 of 8)

```

"41 (CBSC_1, D(31),      bidir,   X,  17, 1, Z)," &
"42 (BC_4,  BTERMBAR,    input,   X)," &
"43 (BC_4,  READYBAR,    input,   X)," &
"44 (BC_4,  HOLD,        input,   X)," &
"45 (BC_1,  HOLDA,       output3, X,  46, 1, Z)," &
"46 (BC_1,  *,           control, 1)," &
"47 (BC_1,  ADSBAR,      output3, X,  61, 1, Z)," &
"48 (BC_1,  BEBAR(3),    output3, X,  61, 1, Z)," &
"49 (BC_1,  BEBAR(2),    output3, X,  61, 1, Z)," &
"50 (BC_1,  BEBAR(1),    output3, X,  61, 1, Z)," &
"51 (BC_1,  BEBAR(0),    output3, X,  61, 1, Z)," &
"52 (BC_1,  BLASTBAR,    output3, X,  61, 1, Z)," &
"53 (BC_1,  DENBAR,      output3, X,  61, 1, Z)," &
"54 (BC_1,  WRBAR,       output3, X,  61, 1, Z)," &
"55 (BC_1,  DTRBAR,      output3, X,  56, 1, Z)," &
"56 (BC_1,  *,           control, 1)," &
"57 (BC_1,  WAITBAR,     output3, X,  61, 1, Z)," &
"58 (BC_1,  BSTALL,      output3, X,  6,  1, Z)," &
"59 (BC_1,  DCBAR,       output3, X,  61, 1, Z)," &
"60 (BC_1,  SUPBAR,      output3, X,  61, 1, Z)," &
"61 (BC_1,  *,           control, 1)," &
"62 (BC_1,  LOCKBAR,     output3, X,  61, 1, Z)," &
"63 (BC_1,  BREQ,        output3, X,  6,  1, Z)," &
"64 (BC_1,  A(31),       output3, X,  80, 1, Z)," &
"65 (BC_1,  A(30),       output3, X,  80, 1, Z)," &
"66 (BC_1,  A(29),       output3, X,  80, 1, Z)," &
"67 (BC_1,  A(28),       output3, X,  80, 1, Z)," &
"68 (BC_1,  A(27),       output3, X,  80, 1, Z)," &
"69 (BC_1,  A(26),       output3, X,  80, 1, Z)," &
"70 (BC_1,  A(25),       output3, X,  80, 1, Z)," &
"71 (BC_1,  A(24),       output3, X,  80, 1, Z)," &
"72 (BC_1,  A(23),       output3, X,  80, 1, Z)," &
"73 (BC_1,  A(22),       output3, X,  80, 1, Z)," &
"74 (BC_1,  A(21),       output3, X,  80, 1, Z)," &
"75 (BC_1,  A(20),       output3, X,  80, 1, Z)," &

```

Example 2. Boundary-Scan Description Language (BSDL) for PQ2 Package Example (Sheet 8 of 8)

```

"76 (BC_1, A(19),      output3, X, 80, 1, Z)," &
"77 (BC_1, A(18),      output3, X, 80, 1, Z)," &
"78 (BC_1, A(17),      output3, X, 80, 1, Z)," &
"79 (BC_1, A(16),      output3, X, 80, 1, Z)," &
"80 (BC_1, *,          control, 1)," &
"81 (BC_1, A(15),      output3, X, 80, 1, Z)," &
"82 (BC_1, A(14),      output3, X, 80, 1, Z)," &
"83 (BC_1, A(13),      output3, X, 80, 1, Z)," &
"84 (BC_1, A(12),      output3, X, 80, 1, Z)," &
"85 (BC_1, A(11),      output3, X, 80, 1, Z)," &
"86 (BC_1, A(10),      output3, X, 80, 1, Z)," &
"87 (BC_1, A(9),       output3, X, 80, 1, Z)," &
"88 (BC_1, A(8),       output3, X, 80, 1, Z)," &
"89 (BC_1, A(7),       output3, X, 80, 1, Z)," &
"90 (BC_1, A(6),       output3, X, 80, 1, Z)," &
"91 (BC_1, A(5),       output3, X, 80, 1, Z)," &
"92 (BC_1, A(4),       output3, X, 80, 1, Z)," &
"93 (BC_1, A(3),       output3, X, 80, 1, Z)," &
"94 (BC_1, A(2),       output3, X, 80, 1, Z)," &
"95 (BC_4, NMIBAR,     input,  X)," &
"96 (BC_4, XINTBAR(7), input,  X)," &
"97 (BC_4, XINTBAR(6), input,  X)," &
"98 (BC_4, XINTBAR(5), input,  X)," &
"99 (BC_4, XINTBAR(4), input,  X)," &
"100 (BC_4, XINTBAR(3), input,  X)," &
"101 (BC_4, XINTBAR(2), input,  X)," &
"102 (BC_4, XINTBAR(1), input,  X)," &
"103 (BC_4, XINTBAR(0), input,  X)," &
"104 (BC_4, RESETBAR, input,  X)," &
"105 (BC_4, CLKIN,     input,  X)," &
"106 (BC_1, CT(3),     output3, X, 80, 1, Z)," &
"107 (BC_1, CT(2),     output3, X, 80, 1, Z)," &
"108 (BC_1, CT(1),     output3, X, 80, 1, Z)," &
"109 (BC_1, CT(0),     output3, X, 80, 1, Z)," &
"110 (BC_1, PCHKBAR,   output3, X, 111, 1, Z)," &
"111 (BC_1, *,        control, 1)";

end Ha_Processor;

```

Table 26. Data Sheet Version -006 to -007 Revision History

| Section | Description |
|---|--|
| Entire data sheet | Formatted in new template. |
| "32-Bit Parallel Architecture" on page 1 | Revised "1.2 Gbyte Internal Bandwidth (75 MHz) to "1.28 Gbyte ... (80 MHz)". |
| Copyright Page | Updated legal text. |
| Section 3.0, "Package Information" on page 6 | Added paragraph two and Table 5. |
| Table 7 "80960Hx Processor Family Pin Descriptions" on page 8 | Corrected minor typeset and spacing errors. BREQ; Revised description. ONCE; last sentence, changed "low" to "high". TDI and TMS; removed last sentence, "Pull this pin low when not in use." |
| Figure 2 "80960Hx 168-Pin PGA Pinout — View from Top (Pins Facing Down)" on page 12 | Added insert package marking diagram. |
| Figure 4 "80960Hx 208-Pin PQ4 Pinout" on page 18 | Added insert package marking diagram. |
| Table 10 "80960Hx PQ4 Pinout — Signal Name Order" on page 19 | Corrected TDO ("O" was zero) and revised alphabetical ordering. |
| Table 11 "80960Hx PQ4 Pinout — Pin Number Order" on page 21 | Corrected TDO ("O" was zero) and revised alphabetical ordering. |
| Section 4.1, "Absolute Maximum Ratings" on page 29 | Revised "V _{CC} " to "VCC5" for "Voltage on Other Pins ...". |
| Section 4.5, "VCCPLL Pin Requirements" on page 31 | Added section. |
| Table 21 "80960Hx DC Characteristics" on page 32 | Added footnote (1) to "I _{LO} " notes column for "TDO" pin. Added footnote (10) to "C _{IN} , C _{OUT} and C _{I/O} " pin. |
| Table 22 "80960Hx AC Characteristics" on page 34 | Added overbars where required. Modified "T _{DVNH} " to list separate specifications for 3.3 V and 5 V. Modified "T _{OV2} , T _{OH2} and T _{TVEL} " to reflect specific 80960HA, 80960HD and 80960HT values. |
| Figure 23 "I _{CC} Active (Power Supply) vs. Frequency" on page 43 | Changed "5" to "0" on "CLKIN Frequency" axis. |
| Figure 49 "BREQ and BSTALL Operation" on page 66 | Added figure and following text. |