809XBH/839XBH/879XBH
COMMERCIAL/EXPRESS HMOS MICROCONTROLLER

- **879XBH: an 809XBH with 8 Kbytes of On-Chip EPROM**
- **839XBH: an 809XBH with 8 Kbytes of On-Chip ROM**

- **232 Byte Register File**
- **Register-to-Register Architecture**
- **10-Bit A/D Converter with S/H**
- **Five 8-Bit I/O Ports**
- **20 Interrupt Sources**
- **Pulse-Width Modulated Output**
- **ROM/EPROM Lock**
- **Run-Time Programmable EPROM**
- **Extended Temperature Available**
- **High Speed I/O Subsystem**
- **Full Duplex Serial Port**
- **Dedicated Baud Rate Generator**
- **6.25 μs 16 x 16 Multiply**
- **6.25 μs 32/16 Divide**
- **16-Bit Watchdog Timer**
- **Four 16-Bit Software Timers**
- **Two 16-Bit Counter/Timers**
- **Extended Burn-In Available**

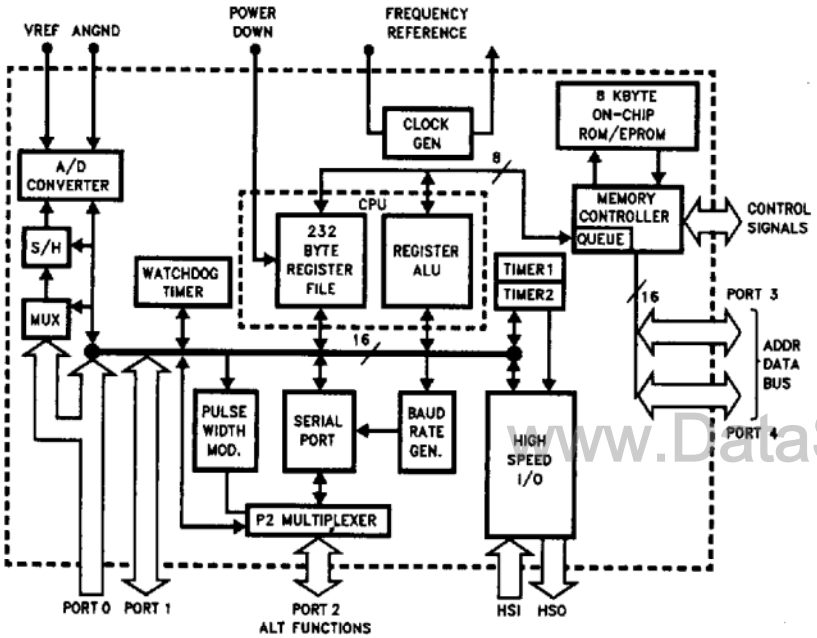
The MCS®-96 family of 16-bit microcontrollers consists of many members, all of which are designed for high-speed control functions. The MCS-96 family members produced using Intel's HMOS-III process are described in this data sheet.

The CPU supports bit, byte, and word operations. Thirty-two bit double-words are supported for a subset of the instruction set. With a 12 MHz input frequency the 8096BH can do a 16-bit addition in 1.0 μs and a 16 x 16-bit multiply or 32/16 divide in 6.25 μs. Instruction execution times average 1 to 2 μs in typical applications.

4

Four high-speed trigger inputs are provided to record the times at which external events occur. Six high-speed pulse generator outputs are provided to trigger external events at preset times. The high-speed output unit can simultaneously perform software timer functions. Up to four 16-bit software timers can be in operation at once.

The on-chip A/D converter includes a Sample and Hold, and converts up to 8 multiplexed analog input channels to 10-bit digital values. With a 12 MHz crystal, each conversion takes 22 μs. This feature is only available on the 8X95BHs and 8X97BHs, with the 8X95BHs having 4 multiplexed analog inputs.



270090-50

Figure 1. 8X9XBH Block Diagram

Also provided on-chip are a serial port, a Watchdog Timer and a pulse-width modulated output signal.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

With the extended burn-in option, the burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.5V, following the guidelines in MIL-STD-883, Method 1015.

See the Packaging Information for extended temperature and extended burn-in designators.

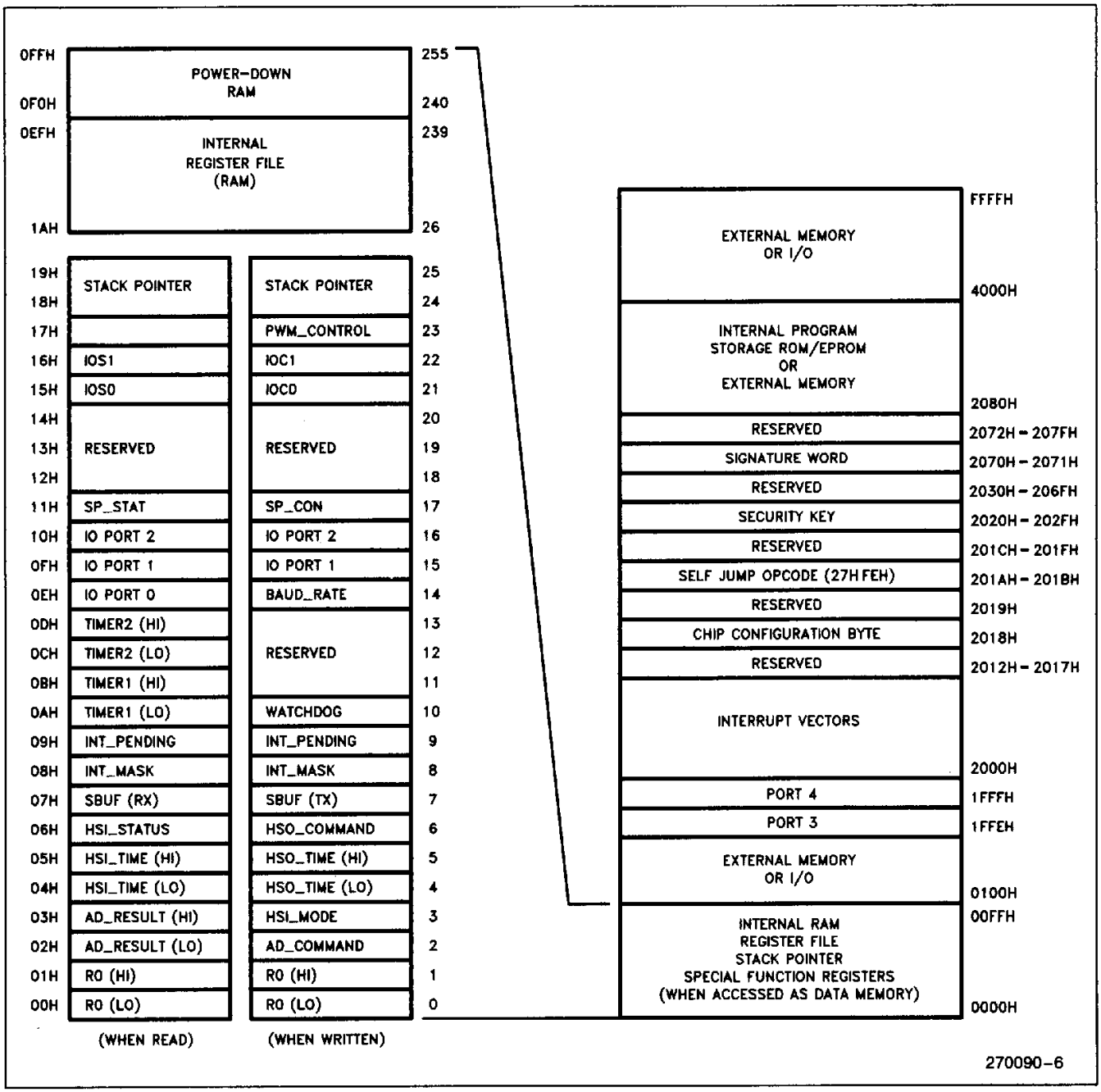


Figure 2. 8X9XBH Memory Map

PACKAGING

The 8096BH is available in 48-pin, 64-pin and 68-pin packages, with and without A/D, and with and without on-chip ROM or EPROM. The 8096BH numbering system is shown in Figure 3. Figures 5–10 show the pinouts for the 48-, 64- and 68-pin packages. The 48-pin version is offered in a Dual-In-Line package while the 68-pin versions come in a Plastic Leaded Chip Carrier (PLCC), a Pin Grid Array (PGA) or a Type "B" Leadless Chip Carrier.

	Factory Masked ROM			CPU			User Programmable					
							EPROM			OTP		
	68-Pin	64-Pin	48-Pin	68-Pin	64-Pin	48-Pin	68-Pin	64-Pin	48-Pin	68-Pin	64-Pin	48-Pin
ANALOG	8397BH	8397BH	8395BH	8097BH	8097BH	8095BH	8797BH		8795BH	8797BH	8797BH	
NO ANALOG	8396BH			8096BH								

Figure 3. 8X9X Packaging

Package Designators:
N = PLCC
C = Ceramic DIP
A = Ceramic Pin Grid Array
P = Plastic DIP
R = Ceramic LCC
U = Shrink DIP

Prefix Designators:
T = Extended Temperature
L = Extended Temperature with 160 Hours Burn-in

Package Type	θ_{ja}	θ_{jc}
68L PGA	35°C/W	10°C/W
68L PLCC	37°C/W	13°C/W
68L LCC	28°C/W	14°C/W
64L Shrink DIP	56°C/W	—
48L Plastic DIP	38°C/W	19°C/W
48L Ceramic DIP	26°C/W	6.5°C/W

Figure 4. 8X9XBH Thermal Characteristics

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

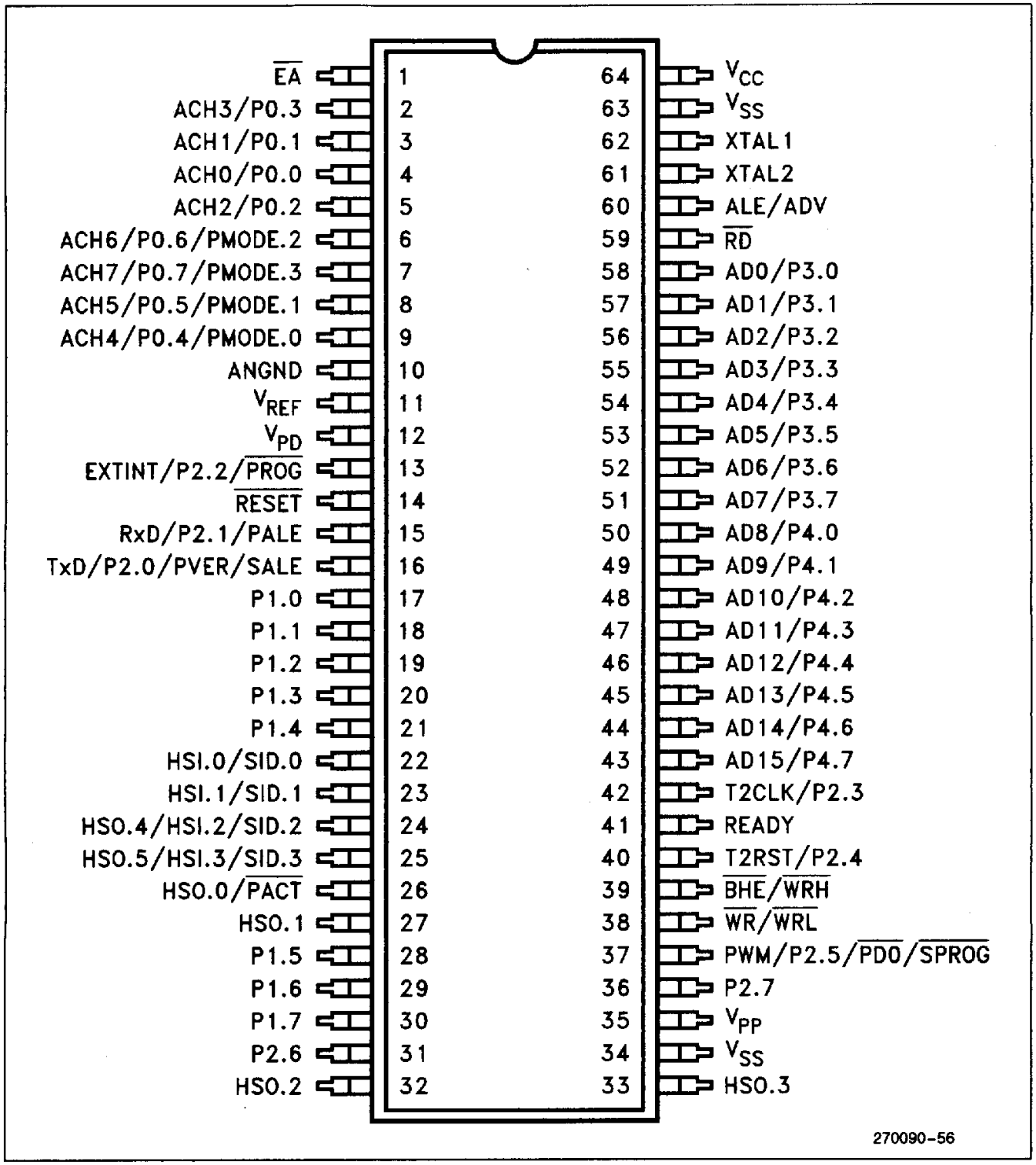


Figure 5. 64-Pin Shrink-DIP Package

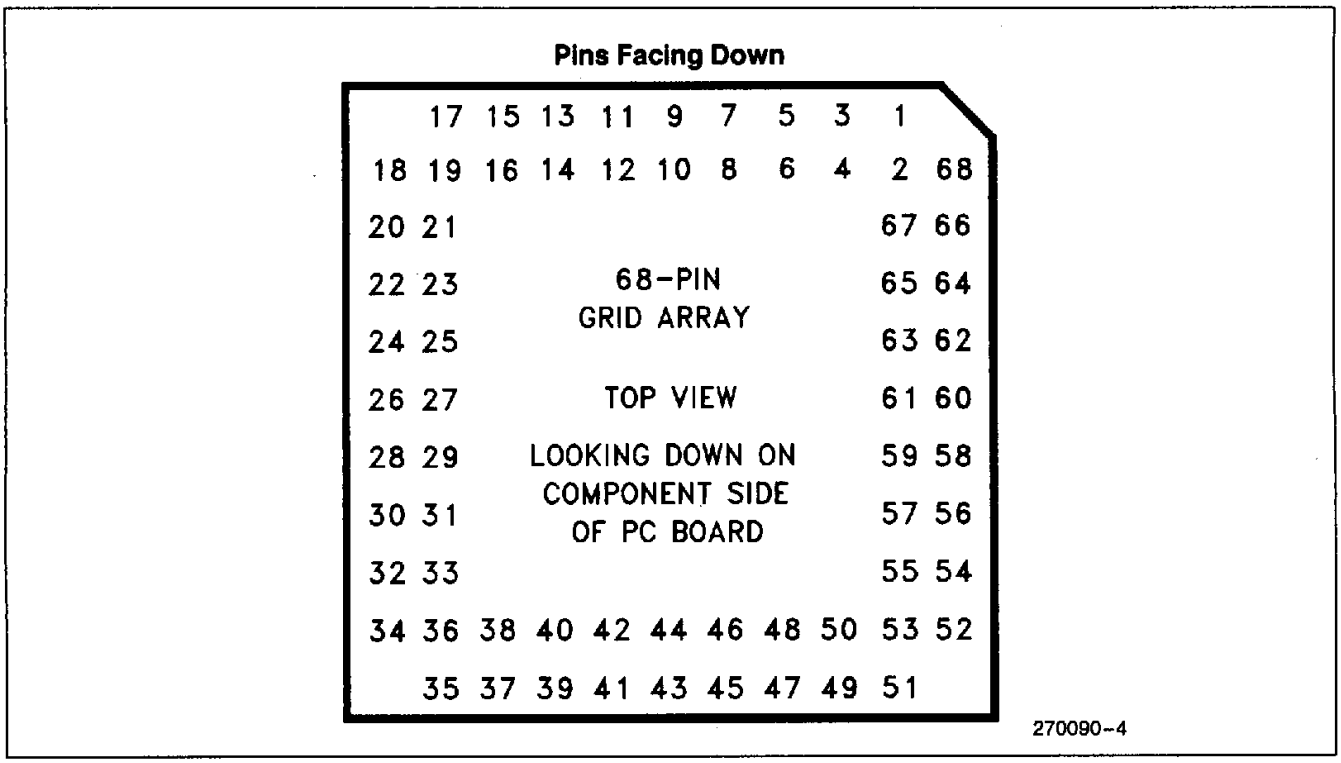


Figure 6. 68-Pin PGA Package

PGA	Description	PGA	Description	PGA	Description
1	ACH7/P0.7/PMODE.3	24	AD6/P3.6	47	P1.6
2	ACH6/P0.6/PMODE.2	25	AD7/P3.7	48	P1.5
3	ACH2/P0.2	26	AD8/P4.0	49	HSO.1
4	ACH0/P0.0	27	AD9/P4.1	50	HSO.0/$\overline{\text{PACT}}$
5	ACH1/P0.1	28	AD10/P4.2	51	HSO.5/HSI.3/SID.3
6	ACH3/P0.3	29	AD11/P4.3	52	HSO.4/HSI.2/SID.2
7	NMI	30	AD12/P4.4	53	HSI.1/SID.1
8	$\overline{\text{EA}}$	31	AD13/P4.5	54	HSI.0/SID.0
9	V_{CC}	32	AD14/P4.6	55	P1.4
10	V_{SS}	33	AD15/P4.7	56	P1.3
11	XTAL1	34	T2CLK/P2.3	57	P1.2
12	XTAL2	35	READY	58	P1.1
13	CLKOUT	36	T2RST/P2.4	59	P1.0
14	BUSWIDTH	37	$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	60	TXD/P2.0/PVER/SALE
15	INST	38	$\overline{\text{WR}}$/$\overline{\text{WRL}}$	61	RXD/P2.1/$\overline{\text{PALE}}$
16	ALE/$\overline{\text{ADV}}$	39	PWM/P2.5/$\overline{\text{PDO}}$/$\overline{\text{SPROG}}$	62	$\overline{\text{RESET}}$
17	$\overline{\text{RD}}$	40	P2.7	63	EXTINT/P2.2/$\overline{\text{PROG}}$
18	AD0/P3.0	41	V_{PP}	64	V_{PD}
19	AD1/P3.1	42	V_{SS}	65	V_{REF}
20	AD2/P3.2	43	HSO.3	66	ANGND
21	AD3/P3.3	44	HSO.2	67	ACH4/P0.4/PMODE.0
22	AD4/P3.4	45	P2.6	68	ACH5/P0.5/PMODE.1
23	AD5/P3.5	46	P1.7		

Figure 7. PGA Function Pinouts

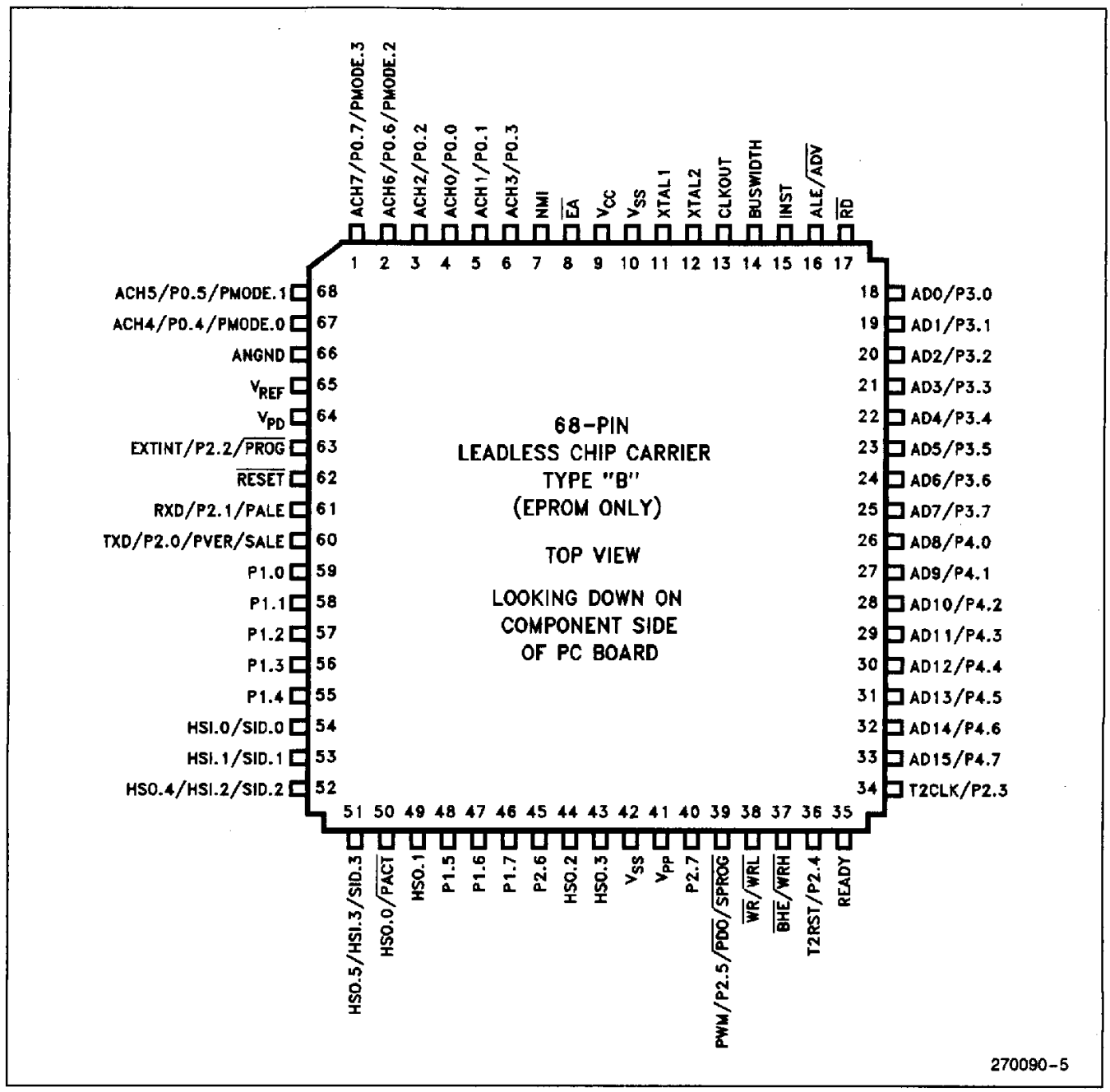


Figure 8. 68-Pin LCC Package

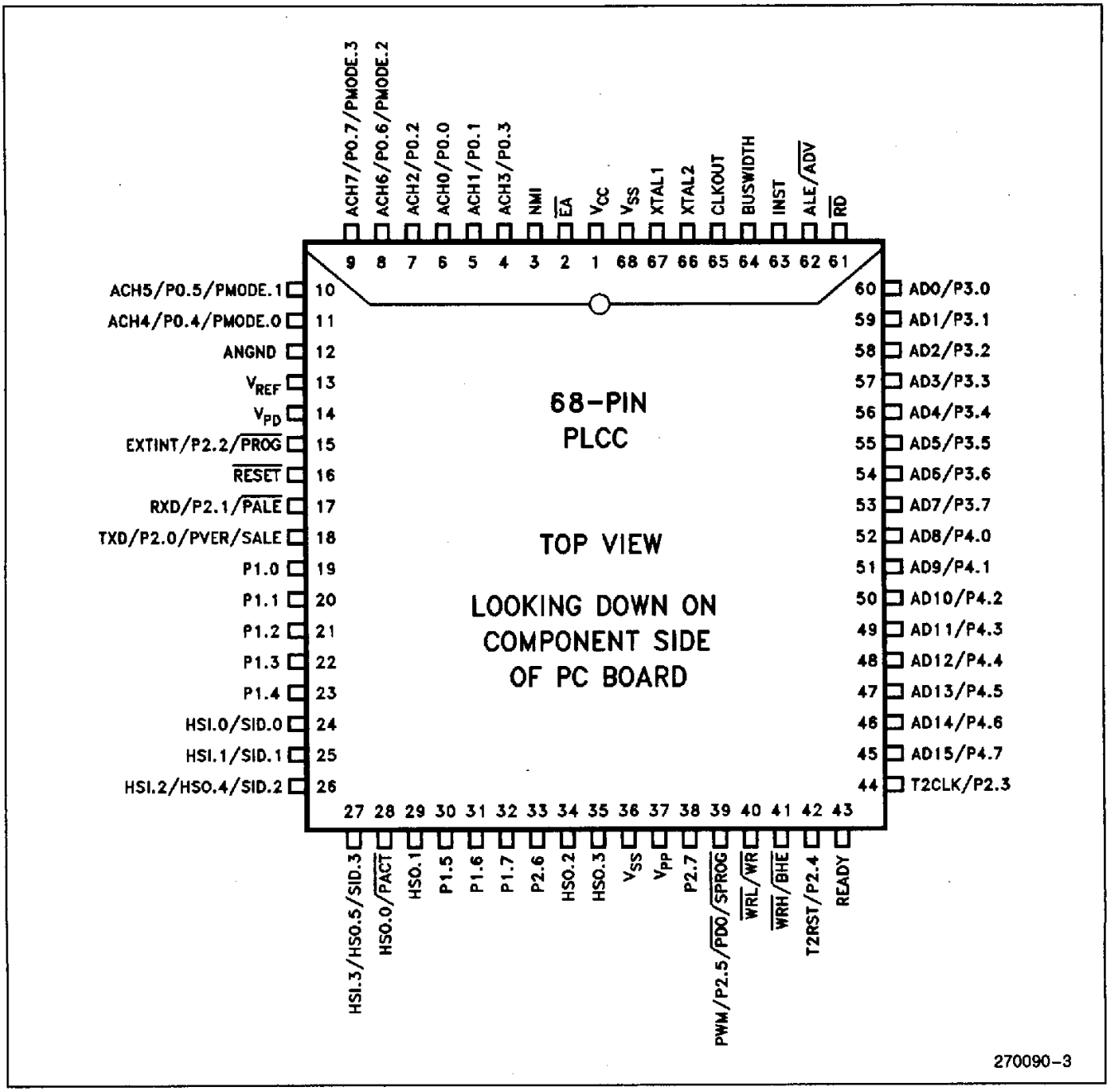


Figure 9. 68-Pin PLCC Package

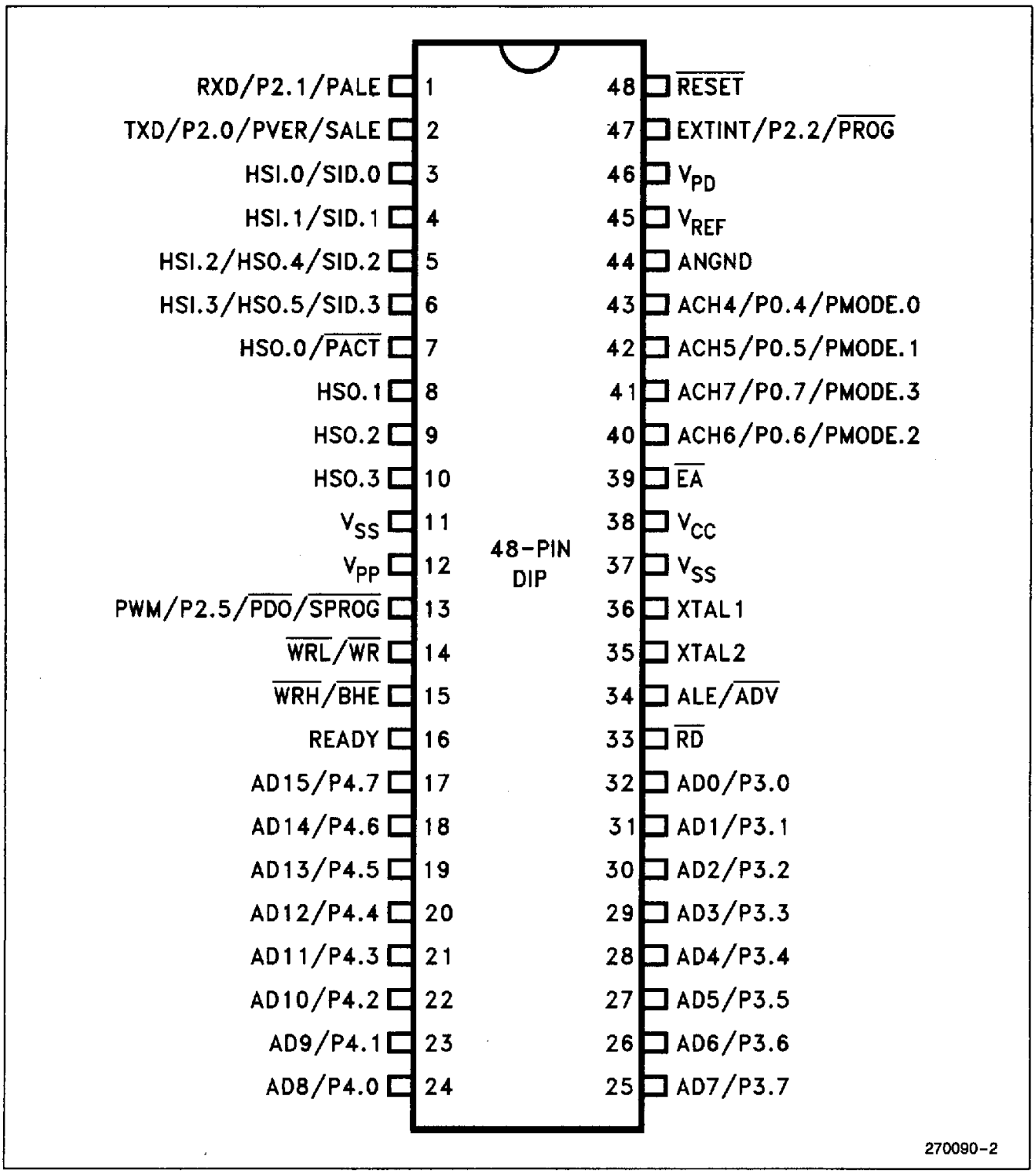


Figure 10. 48-Pin DIP Package

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are two V_{SS} pins, both of which must be connected.
V_{PD}	RAM standby supply voltage (5V). This voltage must be present during normal operation. In a Power Down condition (i.e. V_{CC} drops to zero), if $\overline{RESET}$ is activated before V_{CC} drops below spec and V_{PD} continues to be held within spec., the top 16 bytes in the Register File will retain their contents.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected to use A/D or Port 0.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the EPROM devices. It should be + 12.75V for programming and will float to 5V otherwise. The pin should not be above V_{CC} for ROM and CPU devices. This pin must be left floating in the application circuit for EPROM devices.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT*†	Output of the internal clock generator. The frequency of CLKOUT is 1/3 the oscillator frequency. It has a 33% duty cycle.
$\overline{RESET}$	Reset input to the chip. Input low for a minimum 10 XTAL1 cycles to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
BUSWIDTH*†	Input for bus width selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus. If this pin is left unconnected, it will rise to V_{CC}.
NMI*†	A positive transition causes a vector to external memory location 0000H.
INST*†	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ equal to 12.75V causes the device to enter the Programming Mode.
ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes high at the end of the bus cycle. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$/$\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is activated only during external memory writes.
$\overline{BHE}$/$\overline{WRH}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{BHE}$ will go low for external writes to the high byte of the data bus. $\overline{WRH}$ will go low for external writes where an odd byte is being written. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes.

4

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition of CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available in the CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0‡	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1†	8-bit quasi-bidirectional I/O port.
Port 2†	8-bit multi-functional port. Six of its pins are shared with other functions in the 8096BH, the remaining 2 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Ports 3 and 4 are also used as a command, address and data path by EPROM devices operating in the Programming Mode.*
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming Mode indicates that programming is in progress. A high signal indicates programming is complete.
PVAL	A low signal in Auto Programming Mode indicates that the device programmed correctly.
SALE	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (output from master).
$\overline{\text{SPROG}}$	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming data (output from master).
SID	Assigns a pin of Ports 3 and 4 to each slave to pass programming verification.
PALE	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that Ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
PVAL	A high signal in Slave Programming Mode indicates the device programmed correctly.
$\overline{\text{PDO}}$	A low signal in Slave Programming Mode indicates that the PROG pulse was applied for longer than allowed.

*Not available on Shrink-DIP package
†Not available on 48-pin device
‡Port 0.0.1.2.3 not available on 48-pin device

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias −55°C to +125°C

Storage Temperature .....−60°C to +150°C

Voltage from $\overline{EA}$ or V_{PP} to V_{SS} or ANGND .....−0.3V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND .....−0.3V to +7.0V(1)

Average Output Current from Any Pin .....10 mA

Power Dissipation(2) 1.5W

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM and CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature Under Bias **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	6.0	12	MHz
V_{PD}	Power-Down Supply Voltage	4.50	5.50	V

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current **Commercial** Temp.		240	mA	All Outputs Disconnected.
I_{CC}	V_{CC} Supply Current **Extended** Temp.		270	mA	
I_{CC1}	V_{CC} Supply Current ($T_A \geq 70°C$)		185	mA	
I_{PD}	V_{PD} Supply Current		1	mA	Normal operation and Power-Down.
I_{REF}	V_{REF} Supply Current **Commercial** Temp.		8	mA	
I_{REF}	V_{REF} Supply Current **Extended** Temp.		10	mA	
V_{IL}	Input Low Voltage	−0.3	+0.8	V	

DC CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input High Voltage (Except $\overline{RESET}$, NMI, XTAL1)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, $\overline{RESET}$ Rising	2.4	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage, $\overline{RESET}$ Falling (Hysteresis)	2.1	V_{CC} + 0.5	V	
V_{IH3}	Input High Voltage, NMI, XTAL1	2.2	V_{CC} + 0.5	V	
I_{LI}	Input Leakage Current to each pin of HSI, P3, P4, and to P2.1.		±10	µA	V_{in} = 0 to V_{CC}
I_{LI1}	DC Input Leakage Current to each pin of P0		+3	µA	V_{in} = 0 to V_{CC}
I_{IH}	Input High Current to $\overline{EA}$		100	µA	V_{IH} = 2.4V
I_{IL}	Input Low Current to each pin of P1, and to P2.6, P2.7 **Commercial** Temp.		−125	µA	V_{IL} = 0.45V
I_{IL}	Input Low Current to each pin of P1, and to P2.6, P2.7 **Extended** Temp.		−150	µA	V_{IL} = 0.45V
I_{IL1}	Input Low Current to $\overline{RESET}$	−0.25	−2	mA	V_{IL} = 0.45V
I_{IL2}	Input Low Current P2.2, P2.3, P2.4, READY, BUSWIDTH		−50	µA	V_{IL} = 0.45V
V_{OL}	Output Low Voltage on Quasi-Bidirectional port pins and P3, P4 when used as ports		0.45	V	I_{OL} = 0.8 mA (Note 1)
V_{OL1}	Output Low Voltage on Quasi-Bidirectional port pins and P3, P4 when used as ports		0.75	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OL2}	Output Low Voltage on Standard Output pins, $\overline{RESET}$ and Bus/Control Pins		0.45	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OH}	Output High Voltage on Quasi-Bidirectional pins	2.4		V	I_{OH} = −20 µA (Note 1)
V_{OH1}	Output High Voltage on Standard Output pins and Bus/Control pins	2.4		V	I_{OH} = −200 µA (Note 1)
I_{OH3}	Output High Current on $\overline{RESET}$	−50		µA	V_{OH} = 2.4V
C_S	Pin Capacitance (Any Pin to V_{SS})		10	pF	F_{TEST} = 1.0 MHz

NOTES:
1. Quasi-bidirectional pins include those on P1, for P2.6 and P2.7. Standard Output Pins include TXD, RXD (Mode 0 only), PWM, and HSO pins. Bus/Control pins include CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, INST and AD0–15.
2. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V.
   I_{OL} on quasi-bidirectional pins and Ports 3 and 4 when used as ports: 4.0 mA
   I_{OL} on standard output pins and $\overline{RESET}$: 8.0 mA
   I_{OL} on Bus/Control pins: 2.0 mA
3. During normal (non-transient) operation the following limits apply:
   Total I_{OL} on Port 1 must not exceed 8.0 mA.
   Total I_{OL} on P2.0, P2.6, $\overline{RESET}$ and all HSO pins must not exceed 15 mA.
   Total I_{OL} on Port 3 must not exceed 10 mA.
   Total I_{OL} on P2.5, P2.7, and Port 4 must not exceed 20 mA.

AC CHARACTERISTICS

Test Conditions: Load Capacitance on Output Pins = 80 pF

TIMING REQUIREMENTS (The system must meet these specifications to work with the 8X9XBH.)

Symbol	Parameter	Min	Max	Units
T_{CLYX}(2, 3)	READY Hold after CLKOUT Edge	0(1)		ns
T_{LLYV}	End of ALE/$\overline{ADV}$ to READY Valid		2 T_{OSC} − 70	ns
T_{LLYH}	End of ALE/$\overline{ADV}$ to READY High	2 T_{OSC} + 40	4 T_{OSC} − 80	ns
T_{YLYH}	Non-Ready Time		1000	ns
T_{AVDV}(4)	Address Valid to Input Data Valid		5 T_{OSC} − 120(5)	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		3 T_{OSC} − 100(5)	ns
T_{RHDX}	Data Hold after $\overline{RD}$ Inactive	0		ns
T_{RHDZ}	$\overline{RD}$ Inactive to Input Data Float	0	T_{OSC} − 25	ns
T_{AVGV}(2, 4)	Address Valid to BUSWIDTH Valid		2 T_{OSC} − 125	ns
T_{LLGX}(2, 3)	BUSWIDTH Hold after ALE/$\overline{ADV}$ Low	T_{OSC} + 40		ns
T_{LLGV}(2, 3)	ALE/$\overline{ADV}$ Low to BUSWIDTH Valid		T_{OSC} − 75	ns
T_{RLPV}	Reset Low to Ports Valid		10 T_{OSC}	ns

NOTES:

1. If the 48-pin or 64-pin device is being used then this timing can be generated by assuming that the CLKOUT falling edge has occurred at 2 T_{OSC} + 55 (TLLCH(max) + TCHCL(max)) after the falling edge of ALE.
2. Pins not bonded out on 64-pin devices.
3. Pins not bonded out on 48-pin devices.
4. The term "Address Valid" applies to AD0–15, $\overline{BHE}$ and INST.
5. If wait states are used, add 3 T_{OSC} * N where N = number of wait states.

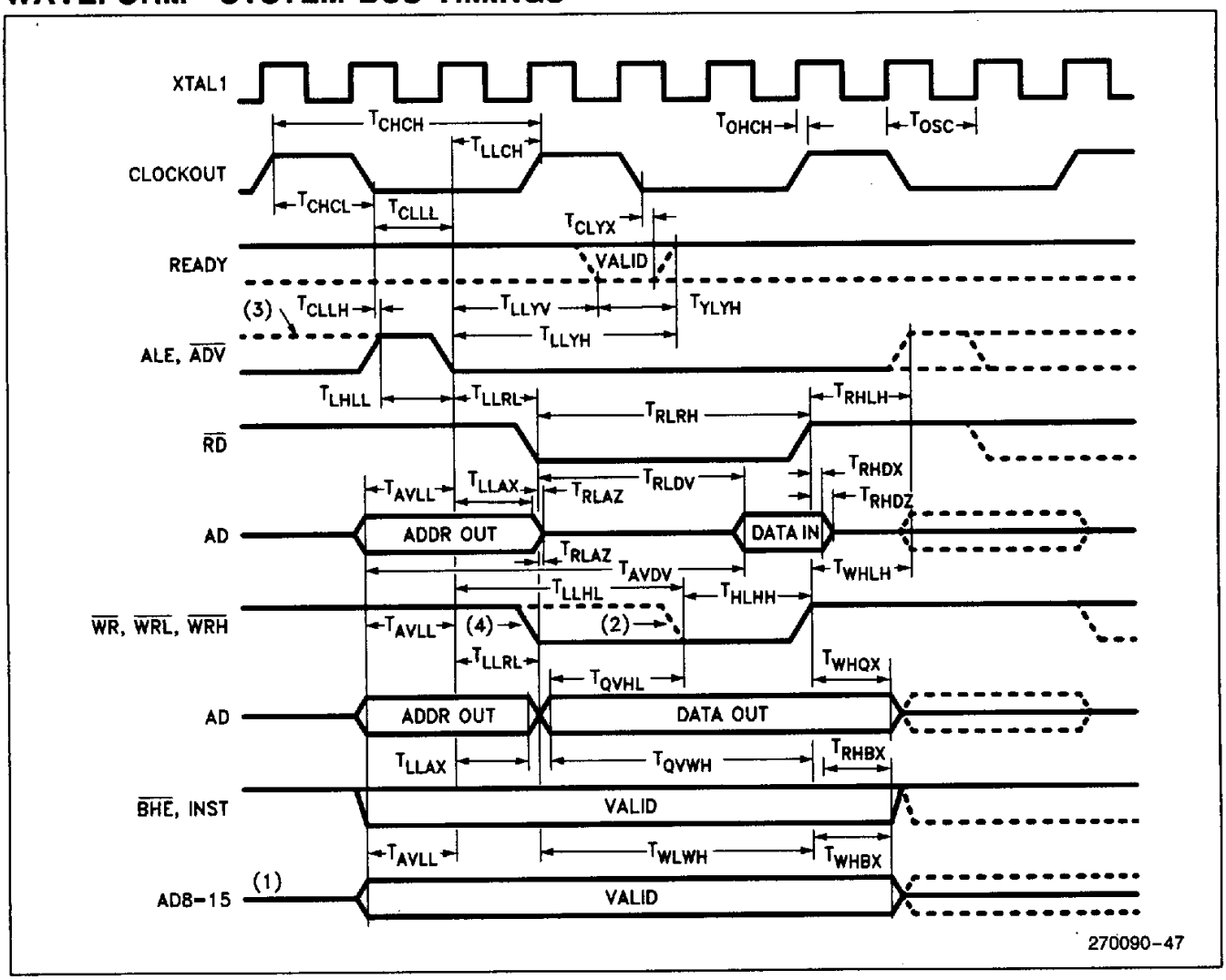
4

TIMING RESPONSES (MCS-96 devices meet these specs.)

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	6.0	12.0	MHz
T_{OSC}	Oscillator Period	83	166	ns
T_{OHCH}	XTAL1 Rising Edge to Clockout Rising Edge	0(4)	120(4)	ns
T_{CHCH}(1, 4)	CLKOUT Period(3)	3 T_{OSC}(3)	3 T_{OSC}(3)	ns
T_{CHCL}(1, 4)	CLKOUT High Time	T_{OSC} − 35	T_{OSC} + 10	ns
T_{CLLH}(1, 4)	CLKOUT Low to ALE High	−30	+15	ns
T_{LLCH}(4)	ALE/$\overline{ADV}$ Low to CLKOUT High(1)	T_{OSC} − 25	T_{OSC} + 45	ns
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 30	T_{OSC} + 35(5)	ns
T_{AVLL}(6)	Address Setup to End of ALE/$\overline{ADV}$	T_{OSC} − 50		ns
T_{RLAZ}(7)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Commercial** Temp.	Typ. = 0	10	ns
T_{RLAZ}(7)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Extended** Temp.		25	ns
T_{LLRL}	End of ALE/$\overline{ADV}$ to $\overline{RD}$ or $\overline{WR}$ Active	T_{OSC} − 40		ns
T_{LLAX}(7)	Address Hold after End of ALE/$\overline{ADV}$	T_{OSC} − 40		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	3 T_{OSC} − 35(2)		ns
T_{QVWH}	Output Data Valid to End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	3 T_{OSC} − 60(2)		ns
T_{WHQX}	Output Data Hold after $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	T_{OSC} − 50		ns
T_{WHLH}	End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$ to ALE/$\overline{ADV}$ High	T_{OSC} − 75		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	3 T_{OSC} − 30(2)		ns
T_{RHLH}	End of $\overline{RD}$ to ALE/$\overline{ADV}$ High	T_{OSC} − 45		ns
T_{CLLL}(4)	CLOCKOUT Low(1) to ALE/$\overline{ADV}$ Low	T_{OSC} − 40	T_{OSC} + 35	ns
T_{RHBX}(4)	$\overline{RD}$ High to INST(1), $\overline{BHE}$, AD8-15 Inactive	T_{OSC} − 25	T_{OSC} + 30	ns
T_{WHBX}(4)	$\overline{WR}$ High to INST(1), $\overline{BHE}$, AD8-15 Inactive	T_{OSC} − 50	T_{OSC} + 100	ns
T_{HLHH}	$\overline{WRL}$, $\overline{WRH}$ Low to $\overline{WRL}$, $\overline{WRH}$ High	2 T_{OSC} − 35	2 T_{OSC} + 40	ns
T_{LLHL}	ALE/$\overline{ADV}$ Low to $\overline{WRL}$, $\overline{WRH}$ Low	2 T_{OSC} − 30	2 T_{OSC} + 55	ns
T_{QVHL}	Output Data Valid to $\overline{WRL}$, $\overline{WRH}$ Low	T_{OSC} − 60		ns

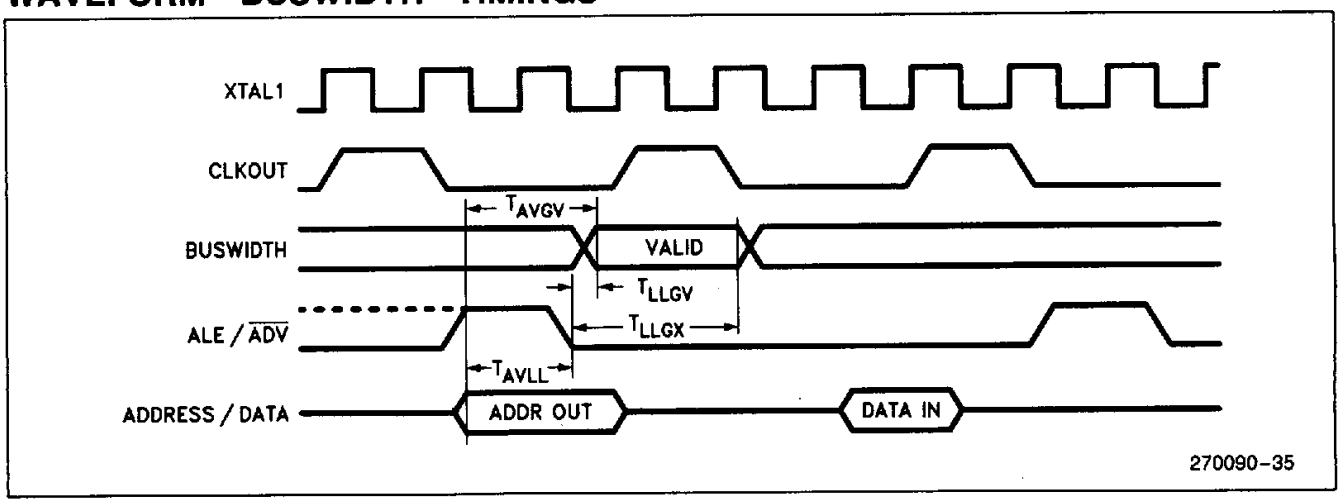
NOTES:
1. Pins not bonded out on 64-pin devices.
2. If more than one wait state is desired, add 3 T_{OSC} for each additional wait state.
3. CLKOUT is directly generated as a divide by 3 of the oscillator. The period will be 3 T_{OSC} ±10 ns if T_{OSC} is constant and the rise and fall times on XTAL1 are less than 10 ns.
4. CLKOUT, INST, and $\overline{BHE}$ pins not bonded out on 48-pin and 64-pin devices.
5. Max spec applies only to ALE. Min spec applies to both ALE and $\overline{ADV}$.
6. The term "Address Valid" applies to AD0–15, $\overline{BHE}$ and INST.
7. The term " Address" in this definition applies to AD0–7 for 8-bit cycles, and AD0–15 for 16-bit cycles.

WAVEFORM—SYSTEM BUS TIMINGS



NOTES:
1. 8-bit bus only.
2. 8-bit or 16-bit bus and write strobe mode selected.
3. When ADV selected.
4. 8- or 16-bit bus and no write strobe mode selected.

WAVEFORM—BUSWIDTH* TIMINGS

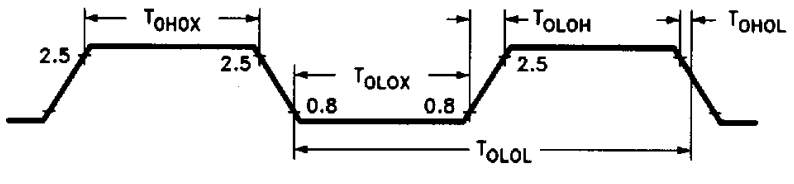


*Buswidth is not bonded out on 48- and 64-pin devices.

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{OLOL}$	Oscillator Frequency	6	12	MHz
T_{OHOX}	High Time	25		ns
T_{OLOX}	Low Time	30		ns
T_{OLOH}	Rise Time		15	ns
T_{OHOL}	Fall Time		15	ns

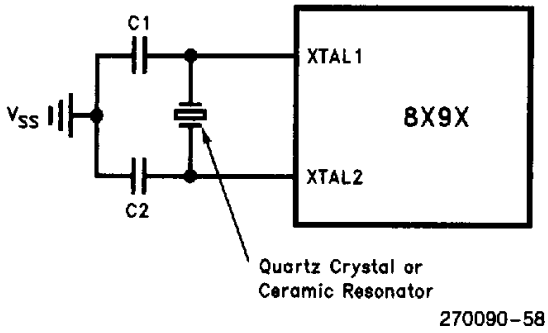
EXTERNAL CLOCK DRIVE WAVEFORMS



270090-48

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

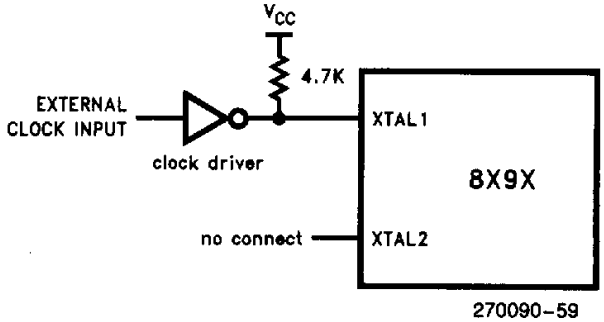
EXTERNAL CRYSTAL CONNECTIONS



270090-58

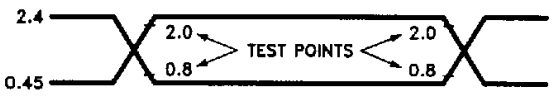
NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 30 pF and C2 = 30 pF. When using ceramic resonators, consult manufacturerer for recommended capacitor values.

EXTERNAL CLOCK CONNECTIONS



270090-59

AC TESTING INPUT, OUTPUT WAVEFORMS



270090-49

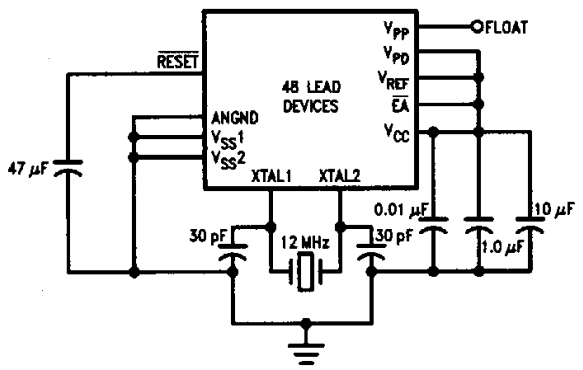
AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

AC TESTING FLOAT WAVEFORMS

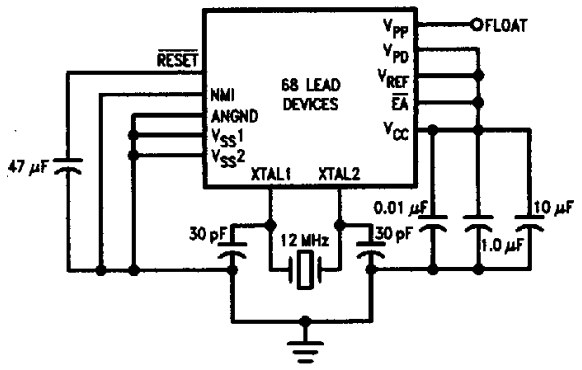
270090-51

For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs, and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \geq \pm 8$ mA.

MINIMUM HARDWARE CONFIGURATION CIRCUITS



270090-52



270090-53

AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

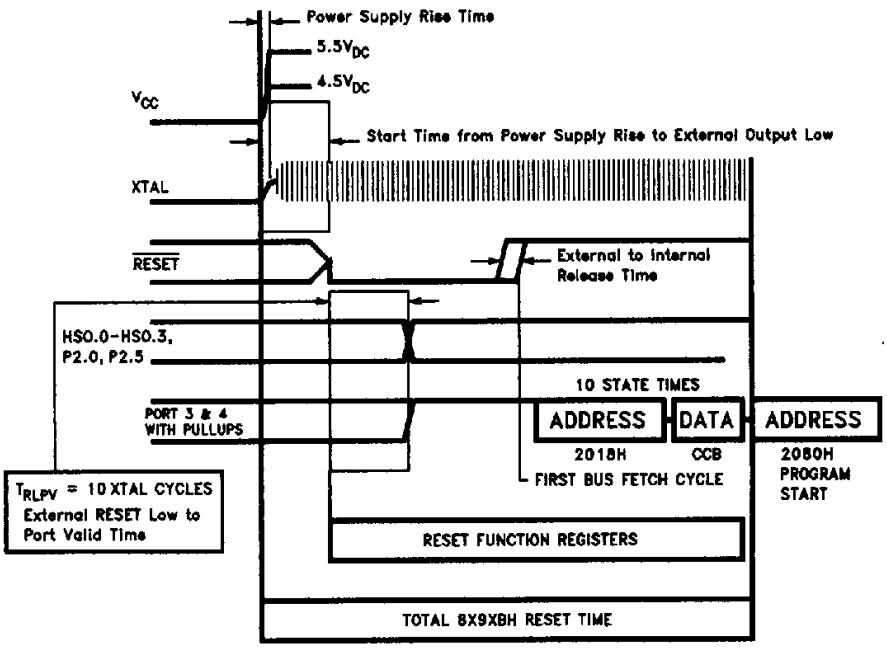
SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Load Capacitance = 80 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	2 T_{OSC} − 70		ns
T_{XHQV}	Next Output Data Valid After Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		5 T_{OSC}	ns

4

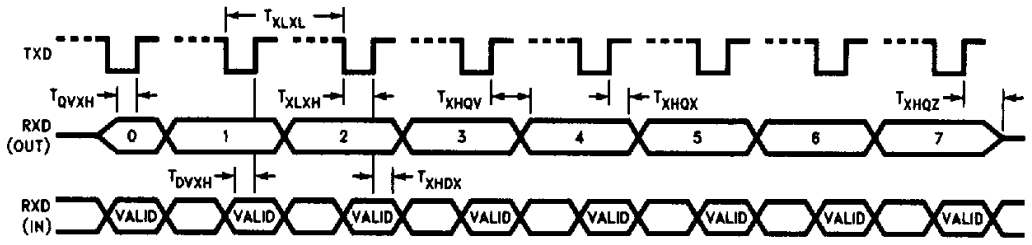
WAVEFORM—T_{RLPV}



270090-60

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



A/D CONVERTER SPECIFICATIONS

A/D Converter operation is verified only on the 8097BH, 8397BH, 8095BH, 8395BH, 8797BH, 8795BH.

The absolute conversion accuracy is dependent on the accuracy and stability of V_{REF}.

See the MCS-96 A/D Converter Quick Reference for definitions of A/D Converter terms.

Parameter	Typical*	Minimum	Maximum	Units**	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±4	LSBs	
Full Scale Error	−0.5 ±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±4	LSBs	
Differential Non-Linearity		>−1	+2	LSBs	
Channel-to-Channel Matching		0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 3
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Series Resistance		1K	5K	Ω	4
DC Input Leakage		0	3.0	μA	
Sample Delay		3 T_{OSC} − 50	3 T_{OSC} + 50	ns	2
Sample Time		12 T_{OSC} − 50	12 T_{OSC} + 50	ns	
Sampling Capacitor			2	pF	

NOTES:
* These values are expected for most devices at 25°C.
** An "LSB", as used here, is defined in the MCS-96 A/D Converter Quick Reference and has a value of approximately 5 mV.
1. DC to 100 KHz.
2. For starting the A/D with an HSO Command.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

EPROM SPECIFICATIONS

EPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages during Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	9.0	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
$F_{OSC}1$	Oscillator Frequency during Auto and Slave Programming	6.0	6.0	MHz
$F_{OSC}2$	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

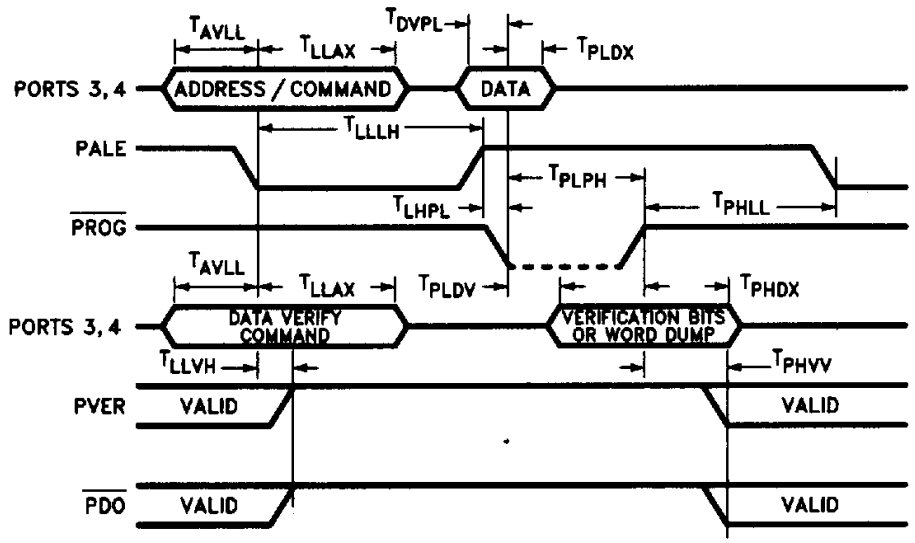
AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
T_{AVLL}	ADDRESS/COMMAND Valid to PALE Low	0		T_{OSC}
T_{LLAX}	ADDRESS/COMMAND Hold After PALE Low	80		T_{OSC}
T_{DVPL}	Output Data Setup Before $\overline{PROG}$ Low	0		T_{OSC}
T_{PLDX}	Data Hold After $\overline{PROG}$ Falling	80		T_{OSC}
T_{LLLH}	PALE Pulse Width	180		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	250 T_{OSC}	100 μs + 144 T_{OSC}	
T_{LHPL}	PALE High to $\overline{PROG}$ Low	250		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next PALE Low	600		T_{OSC}
T_{PHDX}	Data Hold After $\overline{PROG}$ High	30		T_{OSC}
T_{PHVV}	$\overline{PROG}$ High to PVER/$\overline{PDO}$ Valid	500		T_{OSC}
T_{LLVH}	PALE Low to PVER/$\overline{PDO}$ High	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to VERIFICATION/DUMP Data Valid	100		T_{OSC}
T_{SHLL}	RESET High to First PALE Low (not shown)	2000		T_{OSC}

DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (Whenever Programming)		100	mA

WAVEFORM—EPROM PROGRAMMING



8X9XBH ERRATA

Devices covered by this data sheet (see Revision History) have the following errata.

1. INDEXED, 3 OPERAND MULTIPLY

The displacement portion of an indexed, three operand (byte or word) multiply may not be in the range of 200H thru 17FFH inclusive. If you must use these displacements, execute an indexed, two operand multiply and a move if necessary.

2. HSI FIFO OPERATION

The High Speed Input (HSI) has three deviations from the specifications. Note that "events" are defined as one or more pin transitions. "Entries" are defined as the recording of one or more events.

A. The resolution is nine states instead of eight states. Events occurring on the same pin more frequently than once every nine states may be lost.

B. A mismatch between the nine state HSI resolution and the eight state hardware timer causes one time-lag value to be skipped every nine timer counts. Events may receive a time-tag one count later than expected.

C. If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register, leaving the FIFO empty again. The next event that occurs will be the first event loaded into the empty FIFO. If the first two events into an **empty** FIFO (not counting the Holding Register) occur coincident with each other, both are recorded as one entry with one time-tag. If the second event occurs within 9 states after the first, the events will be entered separately with time-tags at least one count apart. If the second event enters the FIFO coincident with the "skipped" time-tag situation (see B above) the time tags will be at least two counts apart.

3. RESERVED LOCATION 2019H

The 1990 Architectural Overview recommended that address 2019H be loaded with 0FFH. The recommendation is now 20H.

4. RESERVED LOCATION 201CH

Reading reserved location 201CH, either internally or externally, will return "201C" as data.

5. SERIAL PORT SECTION

Serial Port Flags—Reading SP_STAT may not clear the TI or RI flag if that flag was set within two state times prior to the read. In addition, the parity error bit (RPE/RB8) may not be correct if it is read within two state times after RI is set. Use the following code to replace ORB sp_image, SP_STAT.

```
SP_READ:  LDB TEMP, SP_STAT
          ORB SP_IMAGE, TEMP
          JBS TEMP,5,SP_READ; if TI is
          set then read again
          JBS TEMP,6,SP_READ; if RI is
          set then read again
          ANDB SP_IMAGE,#7FH; clear
          false RB8/RPE
          ORB SP_IMAGE, TEMP; load
          correct RB8/RPE
```

DATA SHEET REVISION HISTORY

This data sheet (270090-010) is valid for devices marked with an "E" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The difference between this data sheet (-010) and the previous one (-009) is the I_{OL}/I_{OH} for float waveform testing changed from ±15 mA to ±8 mA (this data sheet).

The following differences exist between (-009) data sheet and (-008).

1. The Express (extended temperature and burn-in options) were added to this data sheet. The 8X9XBH Express data sheet (270433-004) is now obsolete.
2. Changes were made to the format of the data sheet and the SFR descriptions were removed. No specification changes made.
3. Added Reserved Location 201CH errata.

The following differences exist between the -008 data sheet and the -007 data sheet.

1. The -007 data sheet was valid for devices marked with a "D" at the end of the top side tracking number.
2. The following errata were removed: RESET and the Quasi-Bidirectional Ports, Software RESET Timing, and Using T2CLK as the source for Timer2.
3. The HSI FIFO Operation errata definition was changed to match change in the HSI FIFO Operation.

The following differences exist between the -007 data sheet and the -006 data sheet.

1. T_{CCLH} changed from Min = −20 ns, Max = +25 ns to Min = −30 ns, Max = +15 ns.
2. T_{XHQX} changed from Min = 2 T_{OSC} − 50 ns to Min = 2 T_{OSC} − 70 ns.
3. T_{QLOX} changed from Min = 25 ns to Min = 30 ns.
4. An errata was added changing the recommendation for address 2019H from 0FFH to 20H.
5. The power supply sequencing section has been deleted. The information is in the Hardware Design Information.
6. The method of identifying the current change indicator was added to the differences between the -005 and -004 data sheets.
7. A bug was not documented in the -004 data sheet and was fixed before the -005 data sheet. Information on the bug was added to the difference between the -005 and -004 data sheets.

Differences between -006 and -005 data sheets.

1. All EPROM programming mode information has been deleted and moved to the Hardware Design Information chapter.
2. Shrink-DIP package information has been added.
3. A new RESET timing specification has been added for clarity.
4. Software Reset pin timing information has been added.
5. HSO I_{OL} specifications have been improved so that all HS0 pins have the same drive capability.
6. Port 3 and Port 4 pin descriptions were clarified, indicating the necessity of pullup if the pins are used as ports.
7. HSI FIFO overflow description added.

Differences between the -005 and the -004 data sheets.

1. The -005 data sheet corresponds to devices marked with a "D" at the end of the topside tracking number. The -004 data sheet corresponded to devices which are not marked with a "D".
2. Much of the description of device functionality has been deleted. All of this information is already in the MCS-96 Architectural Overview.
3. The A/D converter specification for Differential Non-linearity has been changed to be a minimum of > −1 lsbs to a maximum of +2 LSBs.
4. 8X9XBH errata section. The JBS and JBC on Port 0 errata has been fixed on the latest device stepping.
5. 8X9XBH errata section. The errata for the 48-pin devices has been fixed on the latest device stepping.This errata caused the upper 8 bits on the Address/Data bus to be latched when resetting into an 8-bit external memory system.
6. 8X9XBH errata section. An errata existed which caused the device to be held in RESET for extended periods of time with the internal RESET pin pulled down internally. The condition occurred when the XTAL inputs were driven before V_{CC} was stable and within the data sheet specification. The condition was worse at cold. This errata was not documented in the -004 data sheet. It has been fixed on the latest device stepping.
7. 8X9XBH errata section. Errata 3 and 4 have been added to the errata list. These errata exist for all steppings of the device.

Differences between the -004 and the -003 data sheets.

1. The bus control figures and bus timing diagrams were modified to more accurately describe their operation. In particular the 8-bit bus modes now reflect the use of Write Strobe Mode.
2. Additional text was added to the Analog/Digital description of the conversion process to clarify its operation and usefulness.
3. Text was added to the interrupt description section to indicate the maximum transition speed of the input signal relative to the CPU's state timing. A figure was included to graphically demonstrate the interrupt response timing.
4. The pin descriptions were modified to indicate that V_{PP} must normally float in the application.
5. The input low voltage specification (V_{IL1}) was deleted and is covered by the V_{IL} specification.
6. A suggested minimum configuration circuit was added to the material.
7. The A/D Converter Specifications for Differential Non-Linearity has been corrected to be a maximum of +2 LSB's.
8. The EPROM programming section figures were corrected to indicate the correct interface to a 2764A-2. A reset circuit was added to these figures and the signal $\overline{PVAL}$ (Port 3.X and Port 4.X) is now identified as the valid signal for program verification in the Auto Programming Mode. Text was added to this section to reference the requirement of using the Auto Configuration Byte Programming Mode for 48-lead devices. Figure 22A was edited for corrections to the text, and now indicates PVER (Port 2.0). The EPROM circuits were corrected to show 6 MHz operation for programming devices from internal microcode.
9. The protected memory section was edited to indicate that the CPU will enter a "JUMP ON SELF" condition when ROM/EPROM dump mode is complete.
10. An 8X9XBH ERRATA section was added.
11. This REVISION HISTORY was added.