

V.21 Modem

GENERAL DESCRIPTION

The XR-2100 is designed to provide the CCITT V.21 modem function. Complete circuitry is included for this 300 BPS FSK full duplex operation.

The XR-2100 can be used as a stand-alone modem under control of a standard microcontroller such as the 8031. Bus structured control interfaces have been implemented for direct microcontroller connection. The XR-2100 may also be programmed for serial control.

The XR-2100 can also be used to provide V.21 operation for other higher speed Exar modem chips such as the XR-2400and XR-2900 chip sets for V.29/V.27ter/V.22 bis/V.22/212A applications. The XR-2100 ties directly to the same control bus and line interface circuitry as the XR-2400 chip set.

The XR-2100 is constructed in silicon gate CMOS technology for low power operation. Available in a 20 pin dip (0.3" width) and PLCC package, the XR-2100 operates from ±5 volt power supplies.

FEATURES

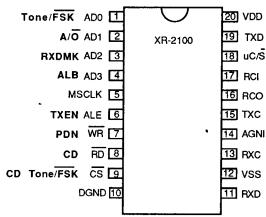
CCITT V.21 operation
300 BPS FSK, full duplex
Universal microcontroller or serial interface
Direct connection to:
 XR-2900/XR-2400, V.29/V.27ter/V.22bis/V.22/212A
Low power CMOS(100 mW TYP)
Analog loopback
Generator and detector for answer and calling tones
Power down mode

ABSOLUTE MAXIMUM RATINGS

Derate Above 25°C

Plastc Dip 5mW/°C Storage Temperature Range -65°C to +150°C

PIN ASSIGNMENT



Bold type indicates uC/STD = 0

(For other pin assignments refer to the end of this datasheet)

ORDERING INFORMATION

Part umber	Package	Operating Temperature
XR-2100CP	Plastic	0°C to 70°C
XR-2100CJ	PLCC	0°C to 70°C

APPLICATIONS

Stand-alone V.21 Modem V.21 Mode for 1200/2400 BPS Systems Internal Type Modem

SYSTEM DESCRIPTION

The XR-2100, when connected to a microcontroller and line interface circuit, forms a complete CCITT V.21 300 BPS modem. Utilizing a universal bus interface, the XR-2100 can be used as a stand-alone modem or for providing the V.21 to existing modem chip sets such as the XR-2400 and XR-2900 modems.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25^{\circ}C$, $V_{DD} = 5V^{\pm}5\%$, $V_{SS} = -5V^{\pm}5\%$, $MS_{CLK} = 11.0592$ MHz \pm 0.05% unless otherwise specified.

SYMBOL	PARAMETER	MIN	ТҮР	мах	UNITS	CONDITIONS
l _{DD}	Positive Supply Current		11		mA	
טטי	Power Down Mode		7		mA	Guaranteed but not tested.
	Negative Supply Current		- 11		mA	tested.
¹ ss	Power Down Mode		7		mA	Guaranteed but not
	Fower Down Mode					tested.
V _{IH}	High Level Input Voltage	2.0			٧	
VIL	Low Level Input Voltage			8.0	V	0.434
ЮН	High Level Output Current			300	μΑ	$V_{OH} = 2.4 V$
lOL	Low Level Output Current			2	mA	V4 0 to V
ų .	Input Current	'		50	μА	V1 = 0 to V _{DD}
VO	Transmit Carrier Output	+6.5	7	8.2	dBm	FSK Carrier calling or
VOCAR	Transmit Gamer Golper	+5.7	7	8.2		ANS Tone, calling tone
VCAR RNG	Input Carrier Range	-43		-10	dBm	ANS, ORIG mode.
CD off		-49	-48	-47 -41	dBm dBm	FSK FSK
CD on	Carrier Detect Hysteresis	-43 2	-43 6	20	dB	FSK,
CD HYS	Carrier Detect Trystereore	ļ				
S/N	Signal-to-noise Ratio		7		dB	ANS/ORIG
						$R_{XC} = -40 \text{ dBM}$ $T_{XC} = -10 \text{ dBM}$
					Ì	C0, C2, or B/B line
						conditions
		İ				BER≤1/10-5
BIAS DIST	Bias Distortion		4 5		%	ORIG mode ANS mode
			3		1	Alto mode
fAMARK	Mark Frequency Answer		1650		Hz	
fASPACE	Space Frequency Answer		1850		Hz	
fomark	Mark Frequency Originate		980		Hz	
foSPACE	Space Frequency Originate		1180		Hz	
fANS	Answer Tone Frequency		2100		Hz	

Carrier Frequencies fMSCLK - 11.0592 MHz

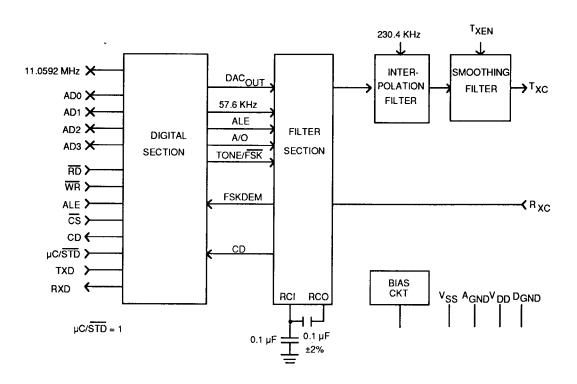
Desired (Hz)	Actual (Hz)	Error (Hz)
980	978.34	-1.6 6
1180	1181.54	+1.54
1650	1651.61	+1.61
1850	1850.60	+0.60
1300	1301.69	+1.69
2100	2104.11	+4.11

Table 1. Frequency Accuracy

	Fre	insmit quency (Hz)	Receive Frequency (Hz)		
Mode	Mark	Space	Mark	Space	
Originate	980	1180	1650	1850	
Answer	1650	1850	980	1180	

Table 2. CCITT V.21 Frequency Parameters

CCITT V.25 Answer Tone: 2100 Hz



System Block Diagram For XR-2100

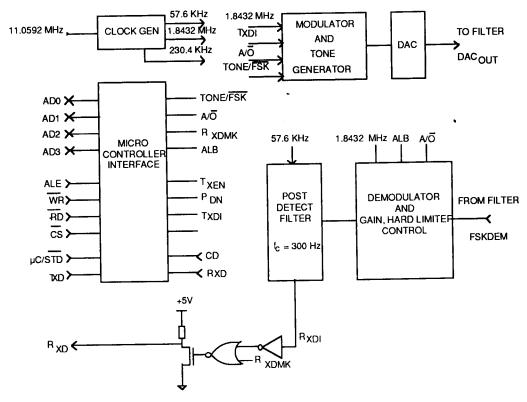


Figure 1. Digital Section Block Diagram For XR-2100

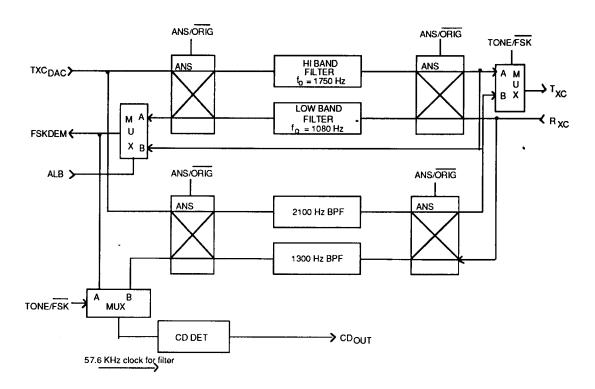


Figure 2. Block Diagram of XR-2100 Filter Section

XR-2100

PIN DESCRIPTIONS

Name 1	Pin #	I/O	Description	Name	Pin#	1/0	Description
AD0 (Tone/FSK) 1		I/O	Address/data bus bit 0 for μ C. Select tone or FSK mode	DGND	10	I	Digital ground. This pin should be routed separate to the AGND to the power supply.
			for stand-alone (Tone = 1, FSK = 0).	R _{XD}	11	0	Receive data output from the demodulator output
AD1 (A/O)	2	1/0	Address/data bus bit 1 for μC.				(1 = mark, 0 = space).
AD2			Mode select for stand- alone (ANS = 1, Orig = 0).	V _{SS}	12	I	Negative power supply, $-5V \pm 5\%$. A 0.1uF ceramic bypass capacitor should be placed near the device.
(RX _{DMK})	3	1/0	Address/data bus bit 2 for	_	40	,	Analog recieve carrier input.
			μC. R _{XD} control for stand-	RXC	13	ı	Analog recieve carrier input.
			alone (R _{XD} clamped to mark = 1, R _{XD} from DEMOD = 0).	AGND	14	1	Analog ground. This pin should be routed separate to the DGND to the power supply.
AD3 (ALB)	4	1/0	Address/data bus bit 3 for ALB control for stand- alone (ALB = 1, normal	T _{XC}	15	0	Analog transmit carrier output.
MSCLK	5	1	receive = 0). Master clock input of 11.0592 MHz.	R _{CO}	16	0	Receive filter output. Connected to the R _{CI} through a 0.1 µF capacitor.
ALE (TXEN) 6	l	Address latch enable for μC. Transmit carrier control for stand-alone (1 = enable0 = disable).	R _{CI}	17	•	Demod input. Connected to $R_{\hbox{\footnotesize CO}}$ through a 0.1 $\mu\hbox{\footnotesize F}$ capacitor
WR (P _{DN})	7	l	Write enable 'or" for μC. Power down control for stand-alone (1 = power	μC/STD	18	1	Control input for selecting μC or stand-alone interface. (1 = μC , 0 = standalone).
			down, 0 = normal	T_{XD}	19	1	Transmit data input
			operation).				(1 = mark, 0 = space).
RD (CD)	8	1/0	Read enable 'not' for µC. Carrier detect status for stand-alone.	v_{DD}	20	ì	Positive power supply voltage, +5V±5%. A 0.1 μF bypass capacitor
CS (CD Tone/F stand-	SK))	Chip select 'not' for μC. Energy output control				should be placed near this pin.
			alone. (1 = Tone Energy, 0 = FSK Energy)				

CONTROL REGISTERS

With $\mu C/\overline{STD} = 1$ (μC interface selected)

	ADDRESS BITS				DATA BITS				
AD3	AD2	AD1	AD0	Bit 3	Bit 2	Bit 1	Bit 0		
WR =0									
1	0	0	0	ALB	RXDMK	A/O	Tone/FSK		
1	0	0	1	CD Tone/FSK	• -	PDN	TXEN		
<u>RD</u> = 0							•		
1	0	0	0	-	-	CD	RXD		

Table 3. μ C Control Bit Assignments

STAND-ALONE MODE SELECTIONS With μ C/STD = 0 (Stand-alone mode selected).

Mode	I/O State	Mode Descriptions	Mode	I/O State	Mode Descriptions
Tone/FSK	1	Answer or calling tone, 2100 Hz for $\overline{A/O} = 1$ and	TXEN	1	T _{XC} is enabled.
		1300 Hz for $\overline{AVO} = 0$.		0	T _{XC} is disabled.
	0	FSK mode, 980 Hz/ 1180 HZ for mark/space in ORIG and 1650 Hz/	P _{DN}	1	Power down mode
		1850 Hz for mark/space		0	Normal operation.
		in ANS.	CD	1	CD is on.
A/O	1	Answer mode.		0	CD is off.
	0	Originate mode.			CD depends on the mode
RXDMK	1	R _{XD} is clamped to mark.			selected, it can be:
	0	R _{XD} is demod output.			Normal receive HI band: FSK Orig. Normal receive LO band:
ALB	1	ALB			. Normal receive LO band. FSK Ans Ans Tone Detect: Tone Orig Calling Tone Detect: Tone Ans.

DA0~DA3

127 ALE ADDR DATA OUT DA0~DA3 400 200 RD 43 ζŝ **Read Cycle** ALE ADDR DATA IN DAO~ DA3 203 WR · cs. Write Cycle

Note: 12 MHz Oscillator All units in nanoseconds (minimum), unless otherwise specified.

Figure 3. Read/Write Timing Waveforms for XR-2100 Using 8031/51 Controller

APPLICATIONS INFORMATION

Figures 4 and 5 illustrate the XR-2100 used in various applications. In each, several precautions should be followed in order to ensure optimum performance.

- Analog (AGND) and digital (DGND) grounds should be routed separately to the power supply. They should be single point connected at the supply. This will minimize higher digital currents from interfering with more sensitive analog sections.
- 2) The power supply pins should be bypassed with 0.1 μF ceramic capacitors close to the IC.

Figure 4 shows the XR-2100 used in a stand-alone configuration as selected by $\mu C/STD=0$. The various modes of operation are selected by switches S1-S7.

The XR-2100 is shown in the XR-2400 schematic to provide the V.21 operation for a V.22 bis (2400BPS) modem. Here the XR-2401/XR-2402 chips support V.22 bis, V.22 and Bell 212A modes. The control for both the XR-2100 and XR-2401/XR-2402 come from the XR-2403B microcontroller. User-specified firmware can be added to drive the XR-2100.

Should your future application require combined V.21 and V.23 communications, the design shown in Figure 5 can be easily retrofitted with the pincompatible XR-2321. By a simple drop-in replacement and one jumper modification, the resulting solution will support all four CCITT Standards (V.22bis, V.22, V.23 and V.21) providing "Quad" modem capabilities.

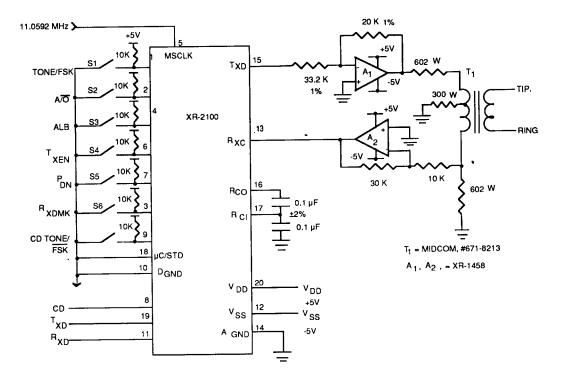


Figure 4. Standalone V.21 Modem With Serial Control

