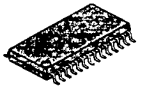
SONY CXK58267AM -70L/85L/10L/12L -70LL/85LL/10LL/12LL

32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58267AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. The CXK58267AM's two chip enable inputs are useful for battery back up operation for nonvolatility.

28 pin SOP (Plastic)



Features

- Fast access time: (Access time)
  - CXK58267AM-70L,70LL 70ns (Max.)
  - CXK58267AM-85L,85LL 85ns (Max.)
  - CXK58267AM-10L,10LL 100ns (Max.)
  - CXK58267AM-12L,12LL 120ns (Max.)
- Low power operation:
  - CXK58267AM-70LL,85LL,10LL,12LL;
  - Standby : 1 μW (Typ.)
  - Operation : 15mW (Typ.)
  - CXK58267AM-70L,85L,10L,12L;
  - Standby : 2.5 μW (Typ.)
  - Operation : 15mW (Typ.)
- Single +5V supply:+5V ± 10%
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 450mil SOP

Function

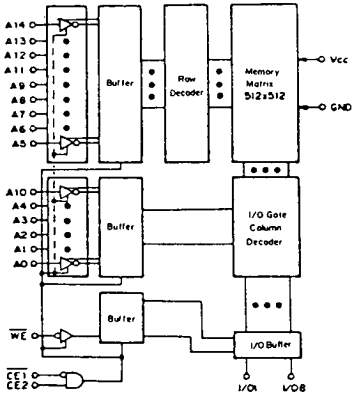
32768-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

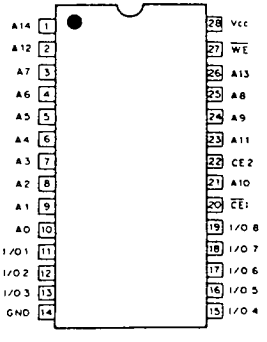
5

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
Vcc	+5V power supply
GND	Ground

E90523A22 - ST

Absolute Maximum Ratings (Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$	−0.5 * to Vcc+0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	260 • 10	°C • sec

* V_{IN}, $V_{I/O}$=−3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	L	Write	Data in	I_{CC1}, I_{CC2}

×: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3 *	—	0.8	V

* V_{IL}=−3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		–70L/85L/10L/12L			–70LL/85LL/10LL/12LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		–0.5	—	0.5	–0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to Vcc		–0.5	—	0.5	–0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, I_{OUT}=0mA		—	3	10	—	3	10	mA
		$\overline{CE1}$=0.2V, CE2=Vcc–0.2V V_{IN}=0.2V or Vcc–0.2V		—	1	5	—	1	5	
Average operating current	I_{CC2}	Min. cycle Duty=100%, I_{OUT}=0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I_{SB1}	CE2 ≦ 0.2V or ($\overline{CE1}$ ≧ Vcc–0.2V, CE2 ≧ Vcc–0.2V)	0 to 70°C	—	—	25	—	—	5	µA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
	I_{SB2}	CE2=V_{IL}, or $\overline{CE1}$=V_{IH}		—	0.6	3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH}=–1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

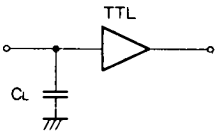
5

AC characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH}=2.2V
Input pulse low level		V_{IL}=0.8V
Input rise time		tr=5ns
Input fall time		tf=5ns
Input and output reference level		1.5V
Output load conditions	85L/85LL/10L/10LL/12L/12LL	C_L * =100pF, 1TTL
	70L/70LL	C_L * =30pF, 1TTL



* C_L includes scope and jig capacitances.

• **Read cycle**

Item	Symbol	− 70L/70LL		− 85L/85LL		− 10L/10LL		− 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time ($\overline{CE1}$, CE2)	t_{CO1}, t_{CO2}	—	70	—	85	—	100	—	120	ns
Output hold from address change	t_{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1} *, t_{HZ2} *	0	30	0	30	0	30	0	30	ns

* t_{HZ1} and t_{HZ2} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• **Write cycle**

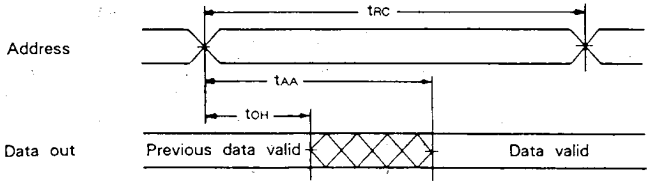
Item	Symbol	− 70L/70LL		− 85L/85LL		− 10L/10LL		− 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ} *	0	25	0	25	0	25	0	25	ns

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

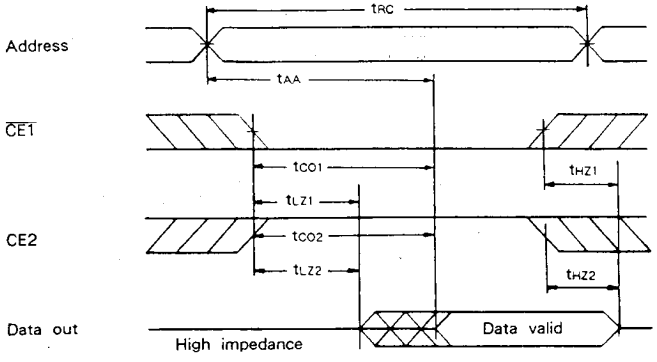
5

Timing Waveform

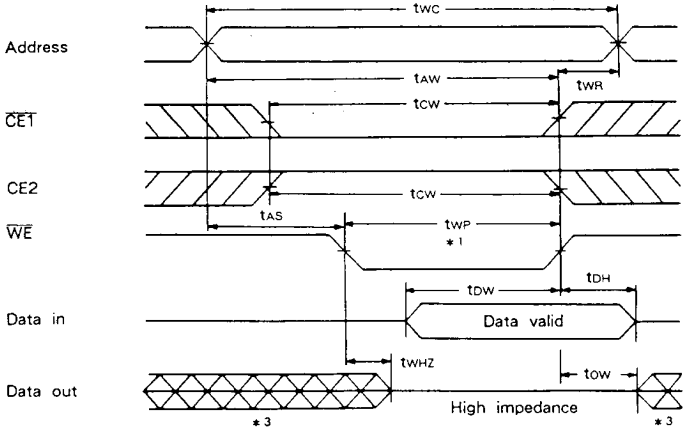
• Read cycle (1) : $\overline{CE1}$=VIL, CE2=VIH, $\overline{WE}$=VIH



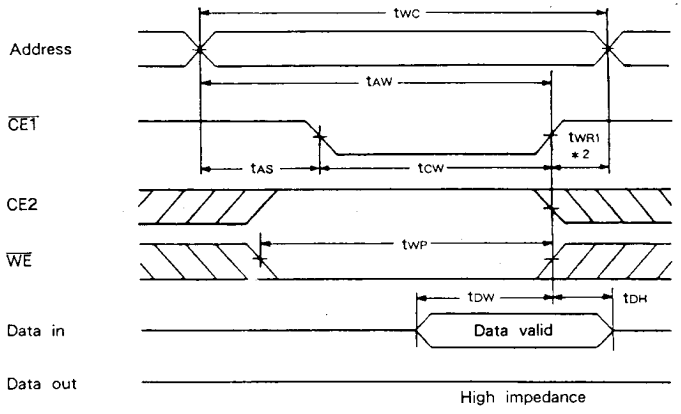
• Read cycle (2) : $\overline{WE}$=VIH



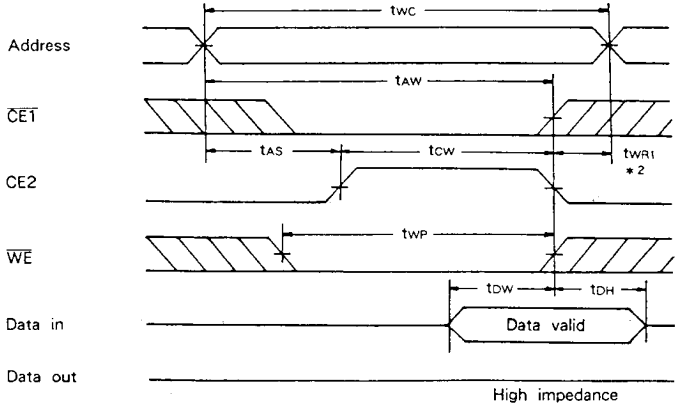
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



*1. A write occurs during the period of $\overline{CE1}$ and $\overline{WE}$ being low and CE2 being high.
*2. t_{WR1} is measured from the earlier of $\overline{CE1}$ or $\overline{WE}$ going high and CE2 going low to the end of write cycle.
*3. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

5

Data Retention Characteristics

(Ta=0 to 70 °C)

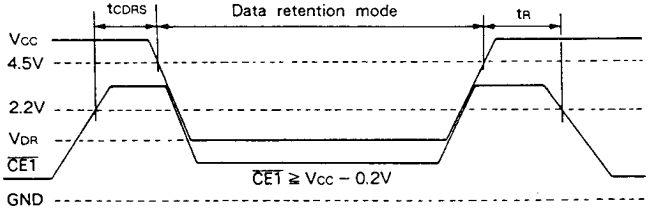
Item	Symbol	Test conditions		− 70L/85L/10L/12L			− 70LL/85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V *1	0 to 70 °C	—	—	10	—	—	3	µA
			0 to 40 °C	—	—	2	—	—	0.6	
			25 °C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	Vcc=2.0 to 5.5V *1		—	0.5	25	—	0.2	5	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC} *2	—	—	t_{RC} *2	—	—	ns

*1. $\overline{CE1} \geqq$ Vcc−0.2V, CE2 ≧ Vcc−0.2V ($\overline{CE1}$ control) or CE2 ≦ 0.2V (CE2 control)

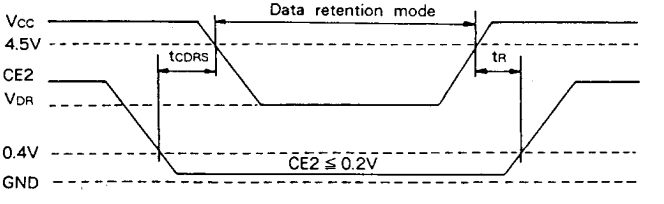
*2. t_{RC}: Read cycle time

Data retention waveform

• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

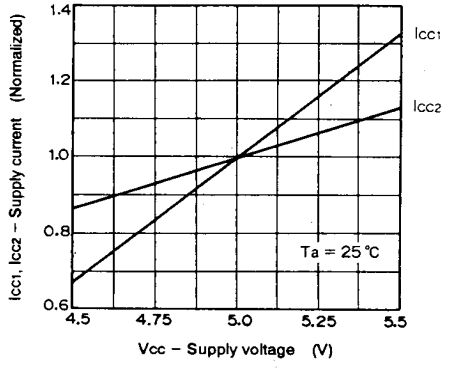


• Low supply voltage data retention waveform (2) (CE2 control)

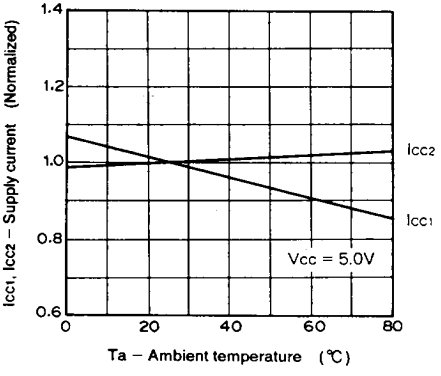


Example of Representative Characteristics

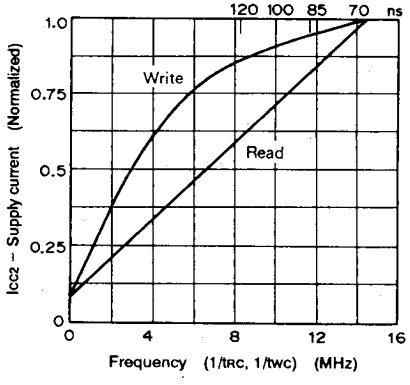
Supply current vs. Supply voltage



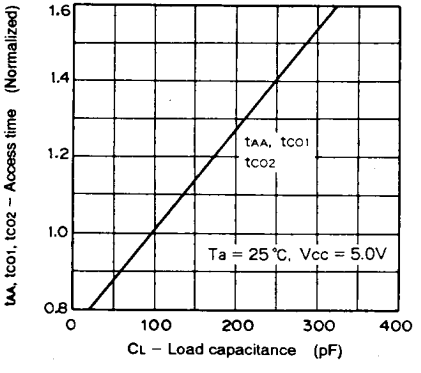
Supply current vs. Ambient temperature



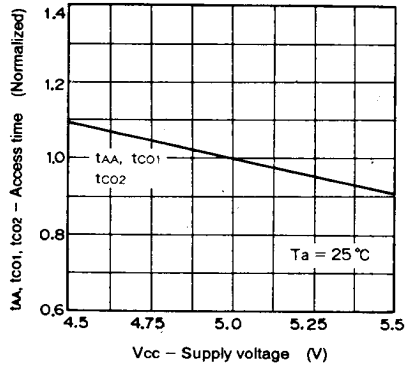
Supply current vs. Frequency



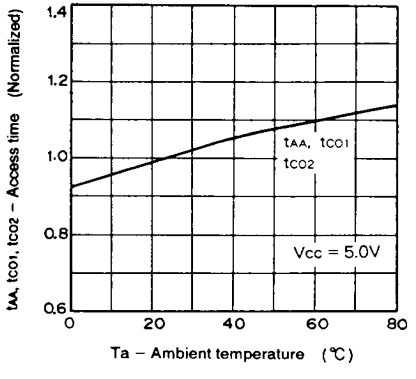
Access time vs. Load capacitance



Access time vs. Supply voltage

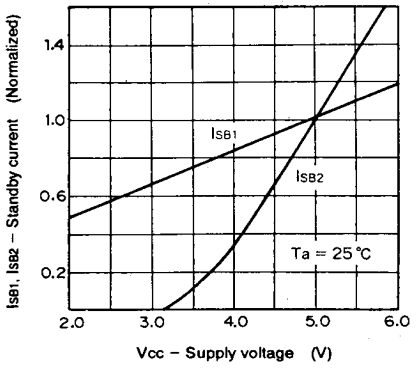


Access time vs. Ambient temperature

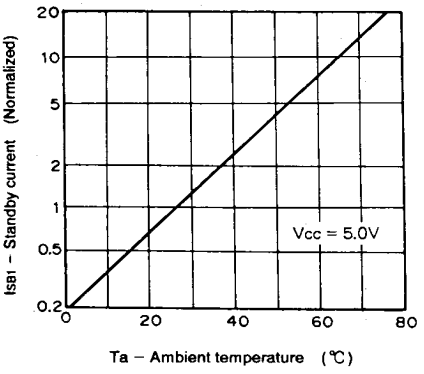


5

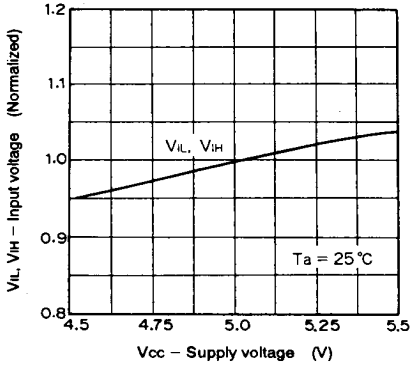
Standby current vs. Supply voltage



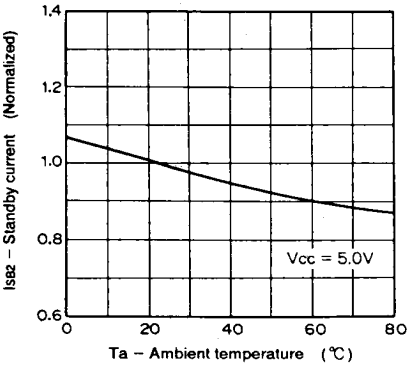
Standby current vs. Ambient temperature



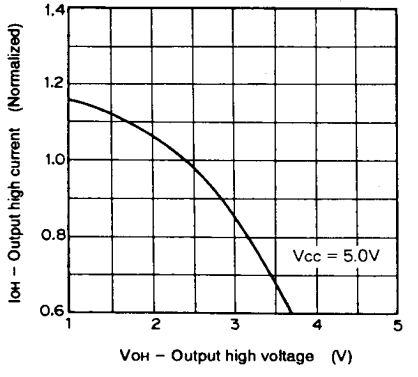
Input voltage level vs. Supply voltage



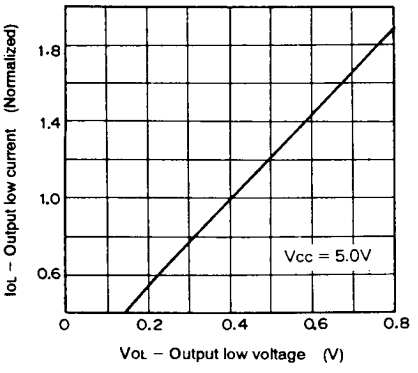
Standby current vs. Ambient temperature



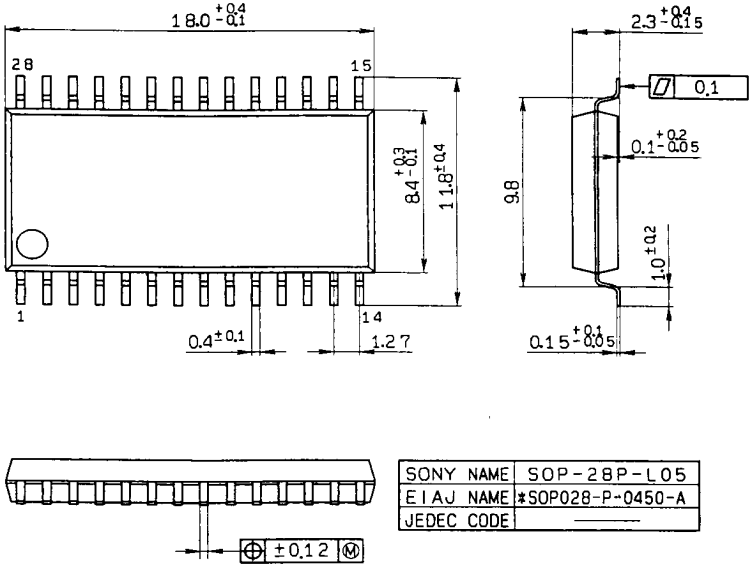
Output high current vs. Output high voltage



Output low current vs. Output low voltage



Package Outline Unit : mm



SONY NAME	SOP-28P-L05
EIAJ NAME	*SOP028-P-0450-A
JEDEC CODE	———

5