

NBSG14

2.5V/3.3V SiGe Differential 1:4 Clock/Data Driver with RSECL* Outputs

*Reduced Swing ECL

The SG14 is a Silicon Germanium 1-to-4 clock/data distribution chip, optimized for ultra-low skew and jitter.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), TTL, CMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

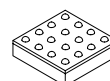
- Maximum Input Clock Frequency up to 12 GHz (See Figure 3)
- 30 ps Typical Rise and Fall Times
- 125 ps Typical Propagation Delay
- RSPECL Output with Operating Range: $V_{CC} = 2.375$ V to 3.465 V with $V_{EE} = 0$ V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.465 V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices



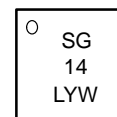
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



FCBGA-16
BA SUFFIX
CASE 489



L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG14BA	4x4 mm FCBGA-16	100 Units/Tray
NBSG14BAR2	4x4 mm FCBGA-16	500/Tape & Reel

Board	Description
SG14EVB	NBSG14BA Evaluation Board

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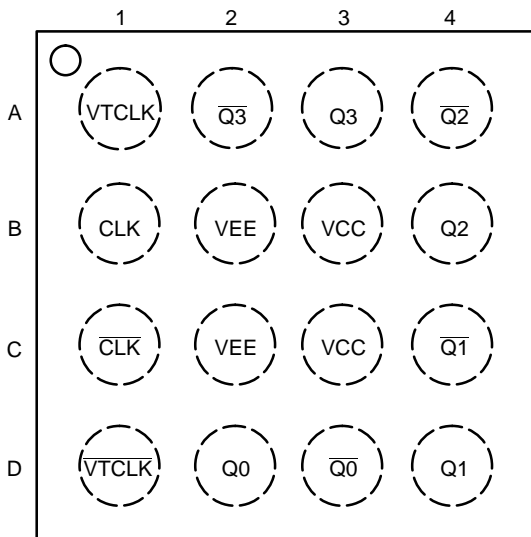


Figure 1. Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
CLK*, CLK**	ECL, TTL, CMOS, CML, LVDS Compatible Inputs
Q0:3, Q0:3	RSECL Data Outputs
VTCLK, VTCLK	50 Ω Internal Input Termination Resistor
VCC	Positive Supply
VEE	Negative Supply

- * Pin will default low when left open.
- ** Pin will default to a higher potential than CLK when VTCLK/VTCLK and CLK/CLK are left open.

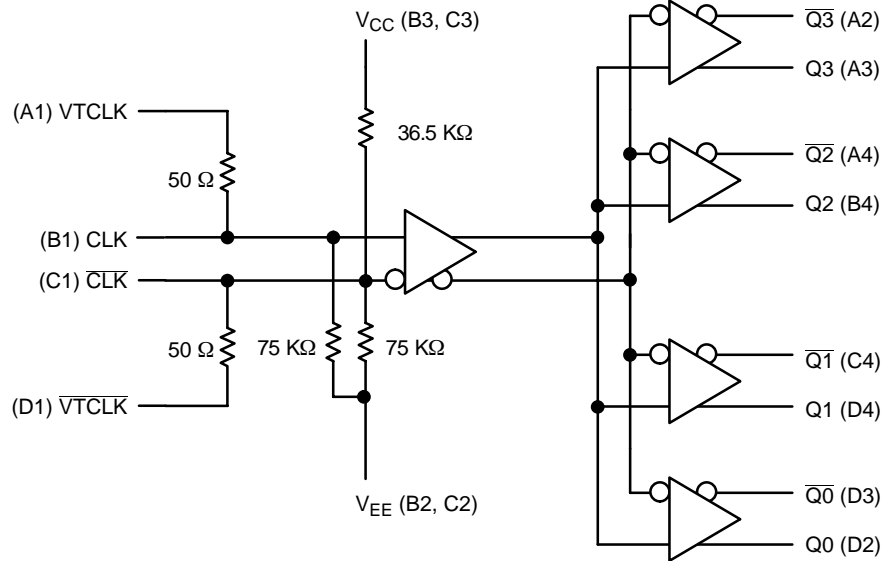


Figure 2. Logic Diagram

INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK and VTCLK to VCC
LVDS	Connect VTCLK and VTCLK Together
AC-COUPLED	Bias VTCLK and VTCLK Inputs within Common Mode Range (V_{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTTL, LVC MOS	An External Voltage (V_{THR}) should be Applied to the Unused Differential Input. Nominal V_{THR} is 1.5 V for LVTTTL and $V_{CC}/2$ for LVC MOS Inputs. This Voltage must be within the V_{THR} Specification.

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ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor (CLK, $\overline{\text{CLK}}$)	75 k Ω
Internal Input Pullup Resistor ($\overline{\text{CLK}}$)	36.5 k Ω
ESD Protection	Human Body Model Machine Model
	> 2 kV > 100 V
Moisture Sensitivity (Note 1)	Level 3
Flammability Rating	UL 94 V-0 @ 0.125 in
Oxygen Index	28 to 34
Transistor Count	158
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	Positive Power Supply	V _{EE} = 0 V		3.6	V
V _{EE}	Negative Power Supply	V _{CC} = 0 V		-3.6	V
V _I	Positive Input Negative Input	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	3.6 -3.6	V V
V _{INPP} (IN-IN)	Differential Input Voltage (CLK- $\overline{\text{CLK}}$)	V _{CC} - V _{EE} ≥ 2.8 V V _{CC} - V _{EE} < 2.8 V		2.8 V _{CC} -V _{EE}	V
I _{IN}	Input Current Through R _T (50 Ω Resistor)	Static Surge		45 80	mA mA
I _{OUT}	Output Current	Continuous Surge		25 50	mA mA
T _A	Operating Temperature Range			-40 to +70	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 LFPM 500 LFPM	16 FCBGA 16 FCBGA	108 86	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 3)	16 FCBGA	5	°C/W
T _{sol}	Wave Solder	< 15 Seconds		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.

3. JEDEC standard 51-6, multilayer board - 2S2P (2 signal, 2 power).

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DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT $V_{CC} = 2.5\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 4)

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 5)	1525	1575	1625	1550	1610	1650	1575	1635	1675	mV
V_{OUTpp}	Output p-p Voltage	315	405	495	315	405	495	315	405	495	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 7 and 9)	$V_{CC} - 1435$	$V_{CC} - 1000^*$	V_{CC}	$V_{CC} - 1435$	$V_{CC} - 1000^*$	V_{CC}	$V_{CC} - 1435$	$V_{CC} - 1000^*$	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 8 and 9)	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{IH} - 150$	mV
V_{THR}	Input Threshold Voltage (Single-Ended) (Note 9)	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

4. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.125 V to -0.5 V.

5. All outputs loaded with 50 Ω to $V_{CC} - 1.5$ volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).

6. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

7. V_{IH} cannot exceed V_{CC} . $|V_{IH} - V_{THR}| < 2600$ mV.

8. V_{IL} always $\geq V_{EE}$. $|V_{IL} - V_{THR}| < 2600$ mV.

9. V_{THR} is the voltage applied to one input when running in single-ended mode.

*Typicals used for testing purposes.

DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 10)

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 11)	2325	2375	2425	2350	2410	2450	2375	2435	2475	mV
V_{OUTpp}	Output p-p Voltage	350	440	530	350	440	530	350	440	530	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 13 and 15)	$V_{CC} - 1435$	$V_{CC} - 1000^*$	V_{CC}	$V_{CC} - 1435$	$V_{CC} - 1000^*$	V_{CC}	$V_{CC} - 1435$	$V_{CC} - 1000^*$	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 14 and 15)	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{IH} - 150$	mV
V_{THR}	Input Threshold Voltage (Single-Ended) (Note 15)	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 12)	1.2		3.3	1.2		3.3	1.2		3.3	V
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

10. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -0.165 V.

11. All outputs loaded with 50 Ω to $V_{CC} - 1.5$ volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).

12. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

13. V_{IH} cannot exceed V_{CC} . $|V_{IH} - V_{THR}| < 2600$ mV.

14. V_{IL} always $\geq V_{EE}$. $|V_{IL} - V_{THR}| < 2600$ mV.

15. V_{THR} is the voltage applied to one input when running in single-ended mode.

*Typicals used for testing purposes.

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DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT $V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V (Note 16)

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 17)	-975	-925	-875	-950	-890	-850	-925	-865	-825	mV
V_{OUTpp}	Output p-p Voltage $-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$ $-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$	350 315	440 405	530 495	350 315	440 405	530 495	350 315	440 405	530 495	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 19 and 21)	$V_{CC} - 1435$	$V_{CC} - 1000^*$	V_{CC}	$V_{CC} - 1435$	$V_{CC} - 1000^*$	V_{CC}	$V_{CC} - 1435$	$V_{CC} - 1000^*$	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 20 and 21)	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2500$	$V_{CC} - 1400^*$	$V_{IH} - 150$	mV
V_{THR}	Input Threshold Voltage (Single-Ended) (Note 21)	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 18)	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	V
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

16. Input and output parameters vary 1:1 with V_{CC} .

17. All outputs loaded with $50\ \Omega$ to $V_{CC} - 1.5$ volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).

18. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

19. V_{IH} cannot exceed V_{CC} . $|V_{IH} - V_{THR}| < 2600\text{ mV}$.

20. V_{IL} always $\geq V_{EE}$. $|V_{IL} - V_{THR}| < 2600\text{ mV}$.

21. V_{THR} is the voltage applied to one input when running in single-ended mode.

*Typicals used for testing purposes.

AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V or $V_{CC} = 2.375\text{ V}$ to 3.465 V ; $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 3) (Note 22)	10.7 (Note 27)	12		10.7 (Note 27)	12		10.7 (Note 27)	12		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	100	125	150	100	125	150	100	125	150	ps
t_{SKEW}	Duty Cycle Skew (Note 23) Within-Device Skew (Note 24) Device-to-Device Skew (Note 25)		2 6 25	10 15 50		2 6 25	10 15 50		2 6 25	10 15 50	ps
t_{JITTER}	Cycle-to-Cycle Jitter (RMS) (See Figure 3) (Note 22)		0.5	< 1		0.5	< 1		0.5	< 1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential) (Note 26)	75		2600	75		2600	75		2600	mV
t_r , t_f	Output Rise/Fall Times (20% - 80%)	20	30	55	20	30	55	20	30	55	ps

22. Measured using a 500 mV source, 50% duty cycle clock source. All outputs loaded with $50\ \Omega$ to $V_{CC} - 1.5\text{ V}$.

23. See Figure 5. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% Differential Clock Input Waveform.

24. Within-Device skew is measured between outputs under identical transitions and conditions on any one device.

25. Device-to-device skew for identical transitions at identical V_{CC} levels.

26. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$ (applicable only when $V_{CC} - V_{EE} < 2600\text{ mV}$).

27. Conditions include input amplitude of 500 mV. Minimum output amplitude guarantee of 100 mV (see Output P-P Spec in Figure 3).

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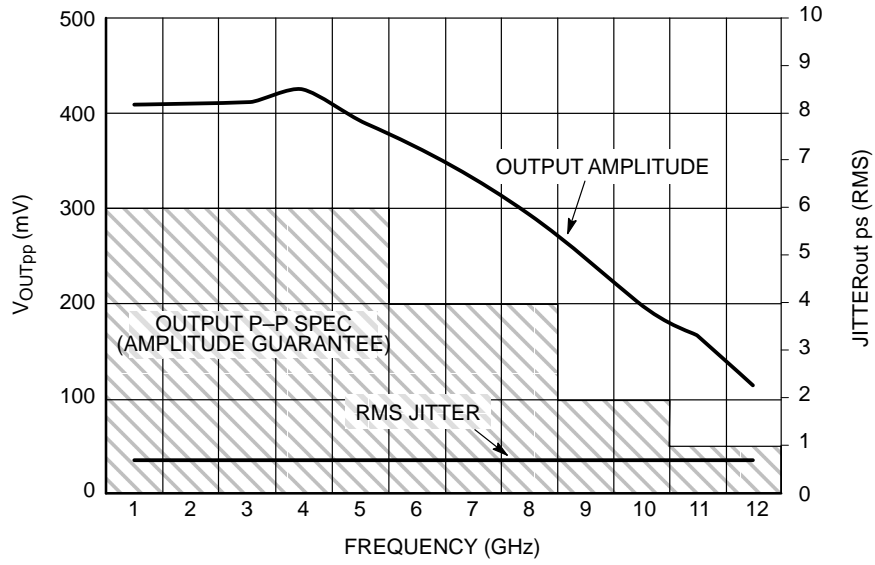
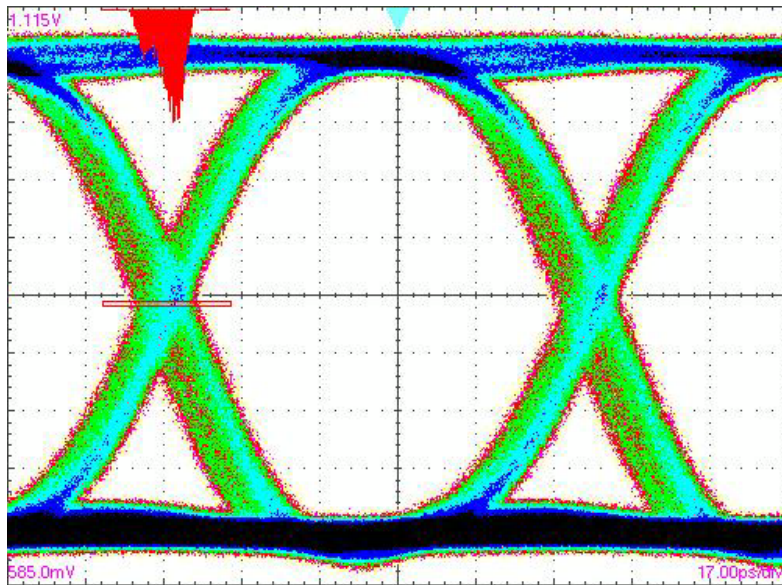


Figure 3. $V_{OUT}/Jitter$ vs. Frequency
($V_{CC} - V_{EE} = 3.3V @ 25^{\circ}C$)



X = 17 ps/DIV, Y = 53 mV/DIV

Figure 4. Eye Diagram at 10.8 Gbps
($V_{CC} - V_{EE} = 3.3 V @ 25^{\circ}C$ with Input Data Pattern of $2^{31}-1$ PRBS.
Total Pk-Pk System Jitter Including Signal Generator is 18 ps.
This Data was taken by Acquiring 7000 Waveforms.)

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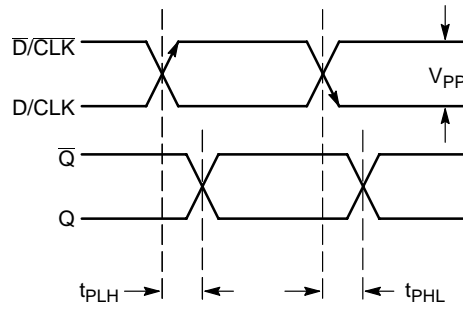


Figure 5. AC Reference Measurement

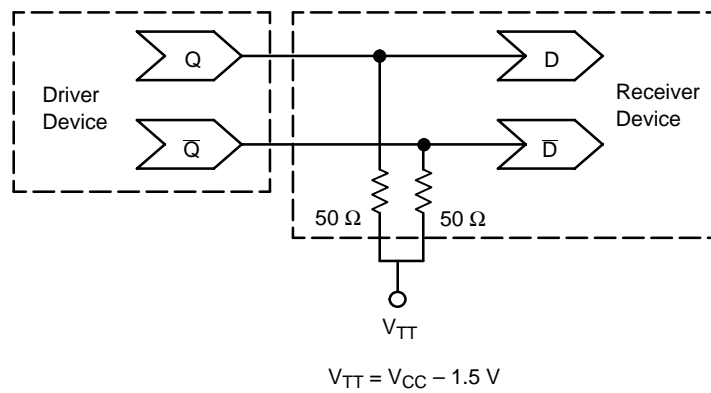


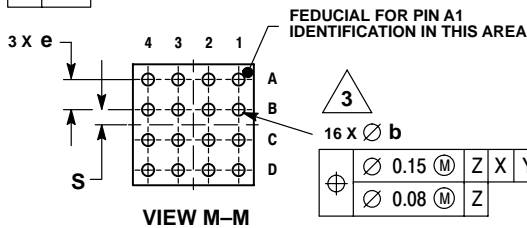
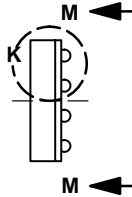
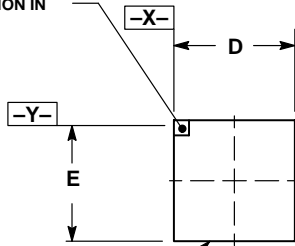
Figure 6. Typical Termination for Output Driver and Device Evaluation
(Refer to Application Note AND8020 – Termination of ECL Logic Devices)

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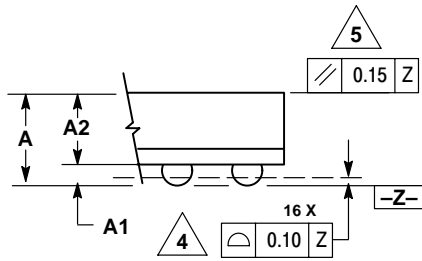
PACKAGE DIMENSIONS

FCBGA-16
BA SUFFIX
 PLASTIC 4X4 (mm) BGA FLIP CHIP PACKAGE
 CASE 489-01
 ISSUE O

LASER MARK FOR PIN 1
 IDENTIFICATION IN
 THIS AREA



⊕	∅ 0.15 (M)	Z	X	Y
	∅ 0.08 (M)	Z		




DETAIL K
 ROTATED 90° CLOCKWISE

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

DIM	MILLIMETERS	
	MIN	MAX
A	1.40	MAX
A1	0.25	0.35
A2	1.20	REF
b	0.30	0.50
D	4.00	BSC
E	4.00	BSC
e	1.00	BSC
S	0.50	BSC

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