PM5347

S/UNI-155-PLUS™

SATURN USER NETWORK INTERFACE (155.52 MBIT/S & 51.84 MBIT/S, "PLUS")

DATA SHEET

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3	June 1995	
2	Nov. 1994	
1	April, 1994	Creation of Document

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1 FEATURES

- Monolithic Saturn User Network Interface that implements the ATM physical layer for Broadband ISDN according to ANSI, ITU, and ATM Forum specifications.
- Processes duplex 155.52 Mbit/s STS-3c/STM-1 or 51.84 Mbit/s STS-1 data streams with on-chip clock and data recovery and clock synthesis.
- Provides Saturn Compliant Interface - PHYsical layer (SCI-PHY™) FIFO buffers in both transmit and receive paths with parity support.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Low power, +5 Volt, CMOS technology.
- 208 pin high performance plastic quad flat pack (PQFP) 28 mm x 28 mm package.
- Industrial temperature range operation (-40°C to +85°C).

The receiver section:

- Provides a serial interface at 155.52 or 51.84 Mbit/s.
- Recovers the clock and data.
- Frames to and descrambles the recovered stream.
- Filters and captures the automatic protection switch channel (K1, K2) bytes in readable registers and detects APS byte failure.
- Captures the synchronization status (S1) byte in a readable register.
- Interprets the received payload pointer (H1, H2) and extracts the STS-3c/1 (STM-1) synchronous payload envelope and path overhead.

- Extracts ATM cells from the received STS-3c/1 (STM-1) synchronous payload envelope using ATM cell delineation and provides optional ATM cell payload descrambling, header check sequence (HCS) error detection and correction, and idle/unassigned cell filtering.

- Provides a generic 16 bit or 8 bit wide datapath interface to read extracted cells from an internal four cell FIFO buffer.

- Extracts all transport overhead bytes and serializes them at 5.184 Mbit/s for optional external processing.

- Extracts the section user channel (F1) and the orderwire channels (E1, E2) and serializes them into three independent 64 kbit/s streams for optional external processing.

- Extracts the data communication channels (D1-D3, D4-D12) and serializes them at 192 kbit/s (D1-D3) and 576 kbit/s (D4-D12) for optional external processing.

- Extracts all path overhead bytes and serializes them at 576 kbit/s for optional external processing.

- Extracts the 16 or 64 byte section trace (J0) sequence and the 16 or 64 byte path trace (J1) sequence into internal register banks.

- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line alarm indication signal (LAIS), line remote defect indication (LRDI), loss of pointer (LOP), path alarm indication signal (PAIS), path remote defect indication signal (PRDI) and loss of cell delineation (LCD).

- Counts received section BIP-8 (B1) errors, received line BIP-24/8 (B2) errors, line far end block errors (M0 or M1), received path BIP-8 (B3) errors and path far end block errors (G1) for performance monitoring purposes.

- Counts received cells written into the receive FIFO, received HCS errored cells that are discarded, and received HCS errored cells that are corrected and passed through the receive FIFO.

- Extracts and serializes the GFC field from all received cells (including idle/unassigned cells) for external processing.

The transmitter section:

- Provides an internal four cell FIFO into which cells are written using a generic 16-bit or 8-bit wide datapath interface.
- Inserts the generic flow control (GFC) bits via a simple serial interface and provides a transmit XOFF function to allow for local flow control.
- Counts transmit cells read from the transmit FIFO.
- Provides idle/unassigned cell insertion, HCS generation/insertion, and ATM cell payload scrambling.
- Inserts ATM cells into the transmitted STS-3c/1 (STM-1) synchronous payload envelope.
- Inserts a register programmable path signal label (C2).
- Generates the transmit payload pointer (H1, H2) and inserts the path overhead.
- Optionally inserts the 16 or 64 byte section trace (J0) sequence and the 16 or 64 byte path trace (J1) sequence from internal register banks.
- Optionally inserts externally generated path overhead bytes received via a 576 kbit/s serial interface.
- Optionally inserts externally generated data communication channels (D1-D3, D4-D12) via a 192 kbit/s (D1-D3) serial stream and a 576 kbit/s (D4-D12) serial stream.
- Optionally inserts externally generated section user channel (F1) and externally generated orderwire channels (E1, E2) via three 64 kbit/s serial interfaces.
- Optionally inserts externally generated transport overhead bytes received via a 5.184 Mbit/s serial interface.
- Scrambles the transmitted STS-3c/1 (STM-1) stream and inserts the framing bytes (A1, A2).

- Synthesizes the 155.52 MHz or 51.84 MHz transmit clock from a 19.44 MHz or 6.48 MHz reference.

- Provides a serial interface at 155.52 Mbit/s or 51.84 Mbit/s.

- Optionally inserts path alarm indication signal (PAIS), path remote defect indication (PRDI), line alarm indication signal (LAIS) and line remote defect indication (LRDI) indication.

- Optionally inserts register programmable APS (K1, K2) and synchronization status (S1) bytes.

- Inserts path BIP-8 codes (B3), path far end block error (G1) indications, line BIP-24/8 codes (B2), line far end block error (M0 or M1) indications, section BIP-8 codes (B1) to allow performance monitoring at the far end.

- Allows forced insertion of all zeros data (after scrambling), the corruption of the framing bytes or the corruption of the section, line, or path BIP-8 codes for diagnostic purposes.

2 APPLICATIONS

- SONET/SDH Based ATM Switching Systems
- SONET/SDH Based ATM Terminals
- B-ISDN User Network Interfaces
- B-ISDN Test Equipment

3 REFERENCES

1. ITU Recommendation G.709 DRAFT - "Synchronous Multiplexing Structure", COM XVIII-R 105-E.

2. ITU Recommendation I.432 DRAFT - "B-ISDN User-Network Interface-Physical Interface Specification", COM XVIII-R 80-E.

3. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 1, December 1994.

4. ATM Forum - ATM User-Network Interface Specification, V3.0, October, 1993.

5. ATM Forum - BISDN Inter Carrier Interface Specification, V1.0, August, 1993.

6. IEEE 1149.1 - Standard Test Access Port and Boundary Scan Architecture, May 21, 1990.

7. T1.105, American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specifications (SONET), 1991

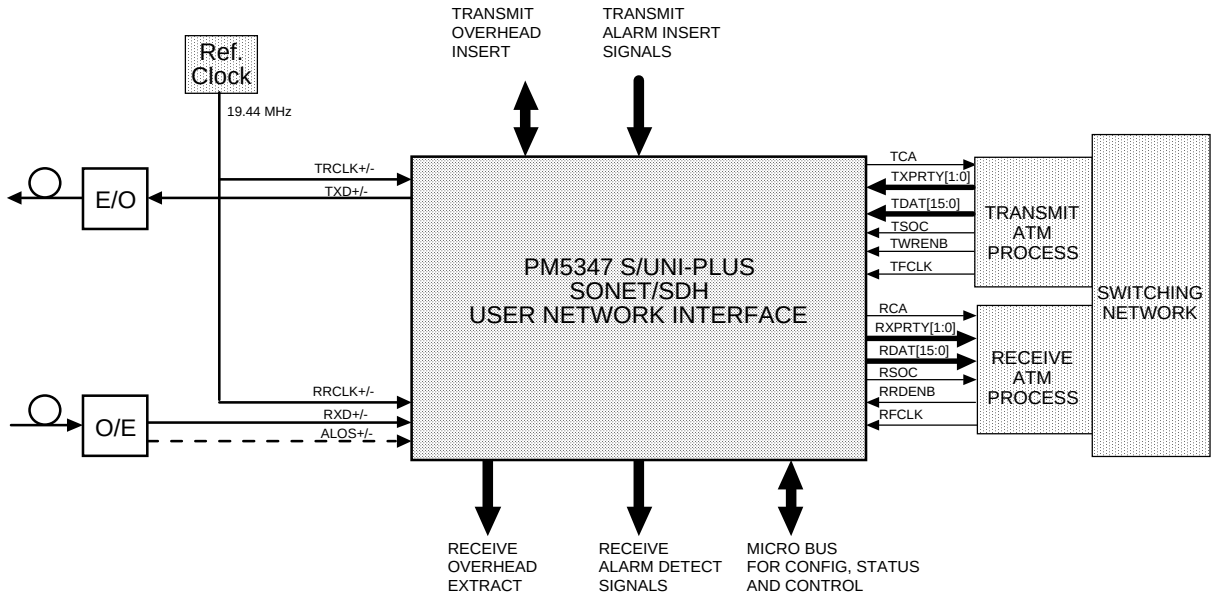
8. T1X1.3/93-006R3, Draft American National Standard for Telecommunications, Synchronous Optical Network (SONET): Jitter at Network Interfaces

9. T1E1.2/94-002R1, Draft American National Standard for Telecommunications, Broadband ISDN and DS1/ATM User Network Interfaces: Physical Layer Specification

4 APPLICATION EXAMPLES

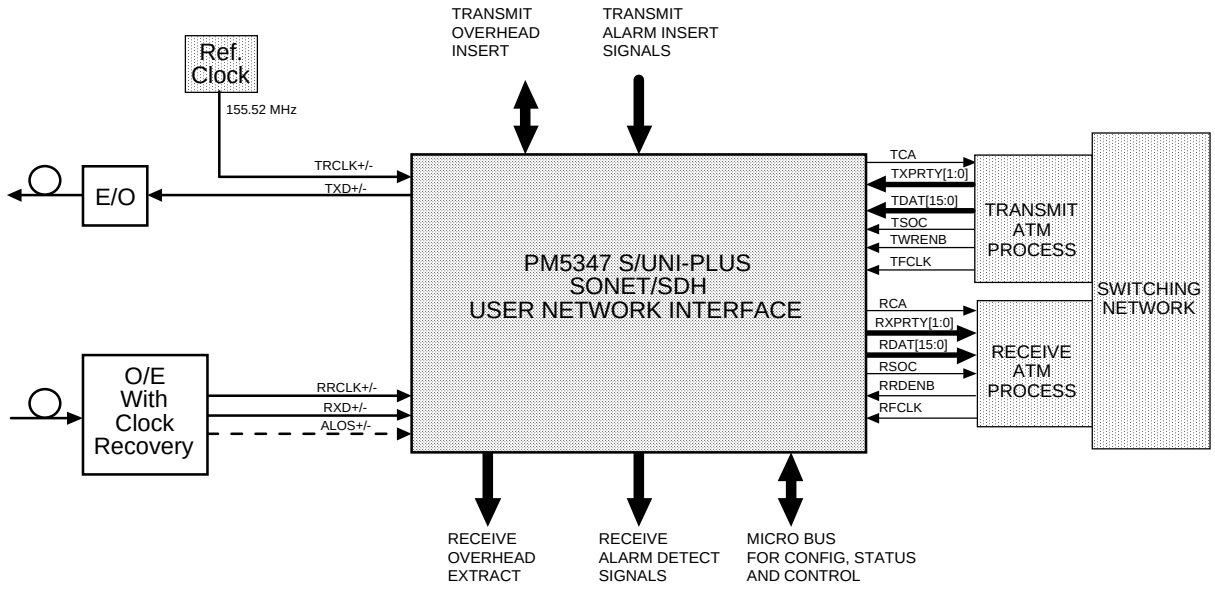
The S/UNI-PLUS is used to implement the core physical layer functions of an ATM User Network Interface or BISDN Inter Carrier Interface. The S/UNI-PLUS may find application at either end of switch-to-switch links or switch-to-terminal links, both in public network (WAN) and private network (LAN) situations. In a typical STS-3c (STM-1) application, the S/UNI-PLUS performs clock and data recovery for the receive direction and clock synthesis for the transmit direction of the line interface. On the drop side, the S/UNI-PLUS interfaces directly with ATM layer processors and switching or adaptation functions using a SCI-PHY™ synchronous FIFO style interface. The initial configuration and ongoing control and monitoring of the S/UNI-PLUS are normally provided via a generic microprocessor interface. This application is shown in Figure 1.

Figure 1 - Typical STS-3c ATM Switch Port Interface



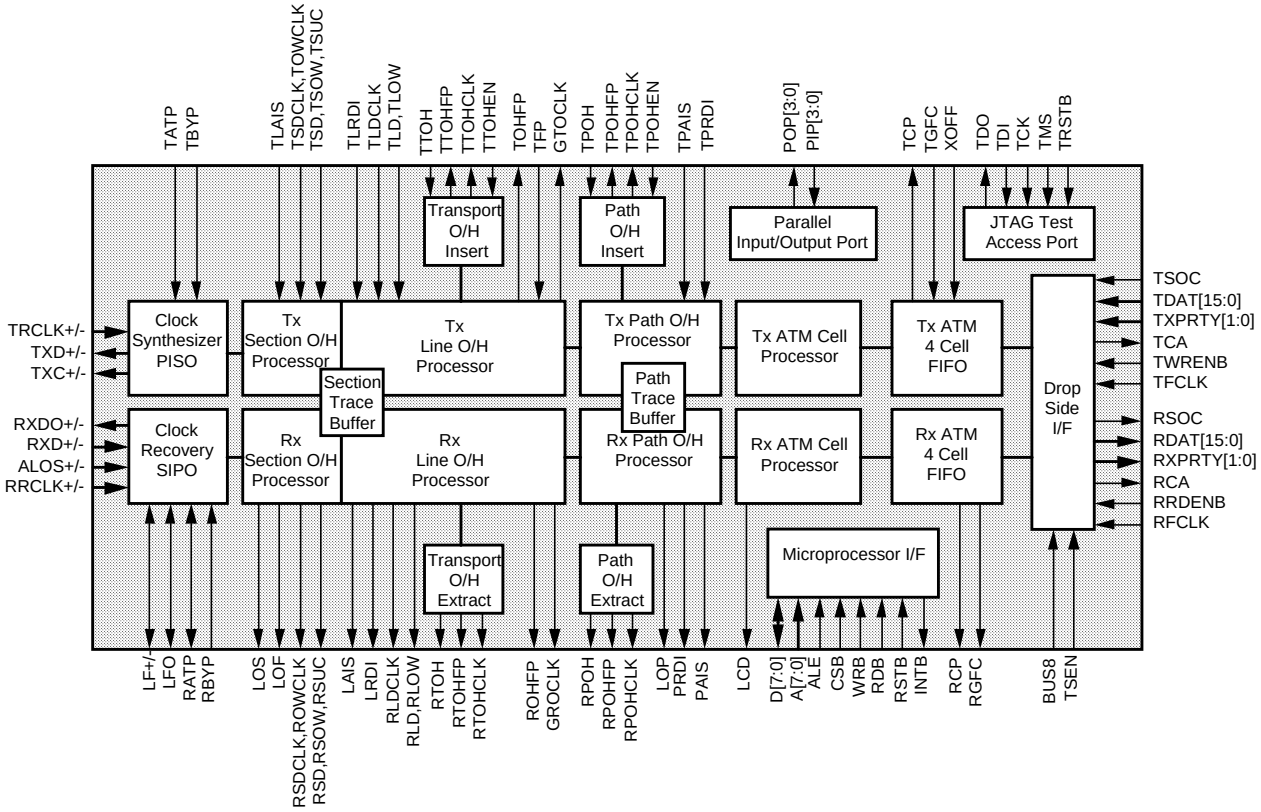
The clock recovery function of the S/UNI-PLUS may by bypassed. This is useful in applications where clock recovery is not required such as when optical receivers are utilized that have integral clock recovery. Similarly, the clock synthesis function of the S/UNI-PLUS may be bypassed. This is useful in applications where clock synthesis is not required, for example where a 155 MHz transmit clock source is available. An example of an application where clock recovery and clock synthesis are bypassed is shown in Figure 2.

Figure 2 - Application With Clock Recovery & Clock Synthesis Bypassed

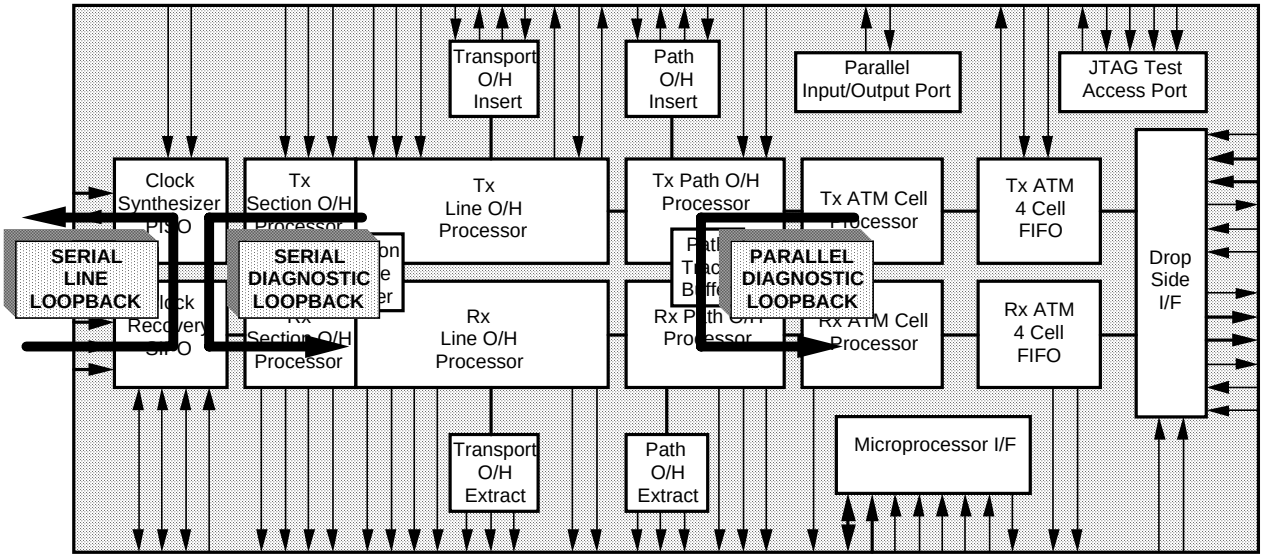


5 BLOCK DIAGRAM

Normal Operating Mode



Loopback Modes



6 DESCRIPTION

The PM5347 S/UNI-PLUS SATURN User Network Interface is a monolithic integrated circuit that implements the SONET/SDH processing and ATM mapping functions of a 155 or 51 Mbit/s ATM User Network Interface.

The S/UNI-PLUS receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section, line, and path overhead. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (M0 or M1, G1) are also accumulated. The S/UNI-PLUS interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload. In addition to its basic processing of the received SONET/SDH overhead, the S/UNI-PLUS provides convenient access to all overhead bytes, which are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The S/UNI-PLUS frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled. The ATM cells that are passed are written to a four cell FIFO buffer. The received cells are read from the FIFO using a generic 16- or 8-bit wide datapath interface. Counts of received ATM cell headers that are errored and uncorrectable and also those that are errored and correctable are accumulated independently for performance monitoring purposes.

The S/UNI-PLUS transmits SONET/SDH streams using a bit serial interface and formats section, line, and path overhead appropriately. It synthesizes the transmit clock from a lower frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (M0 or M1, G1) are also inserted. The S/UNI-PLUS generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. In addition to its basic formatting of the transmitted SONET/SDH overhead, the S/UNI-PLUS provides convenient access to all overhead bytes, which are optionally inserted from lower rate serial interfaces, allowing external sourcing of overhead, if desired. The S/UNI-PLUS also supports the insertion of

a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

ATM cells are written to an internal four cell FIFO using a generic 16- or 8-bit wide datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell. The S/UNI-PLUS provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

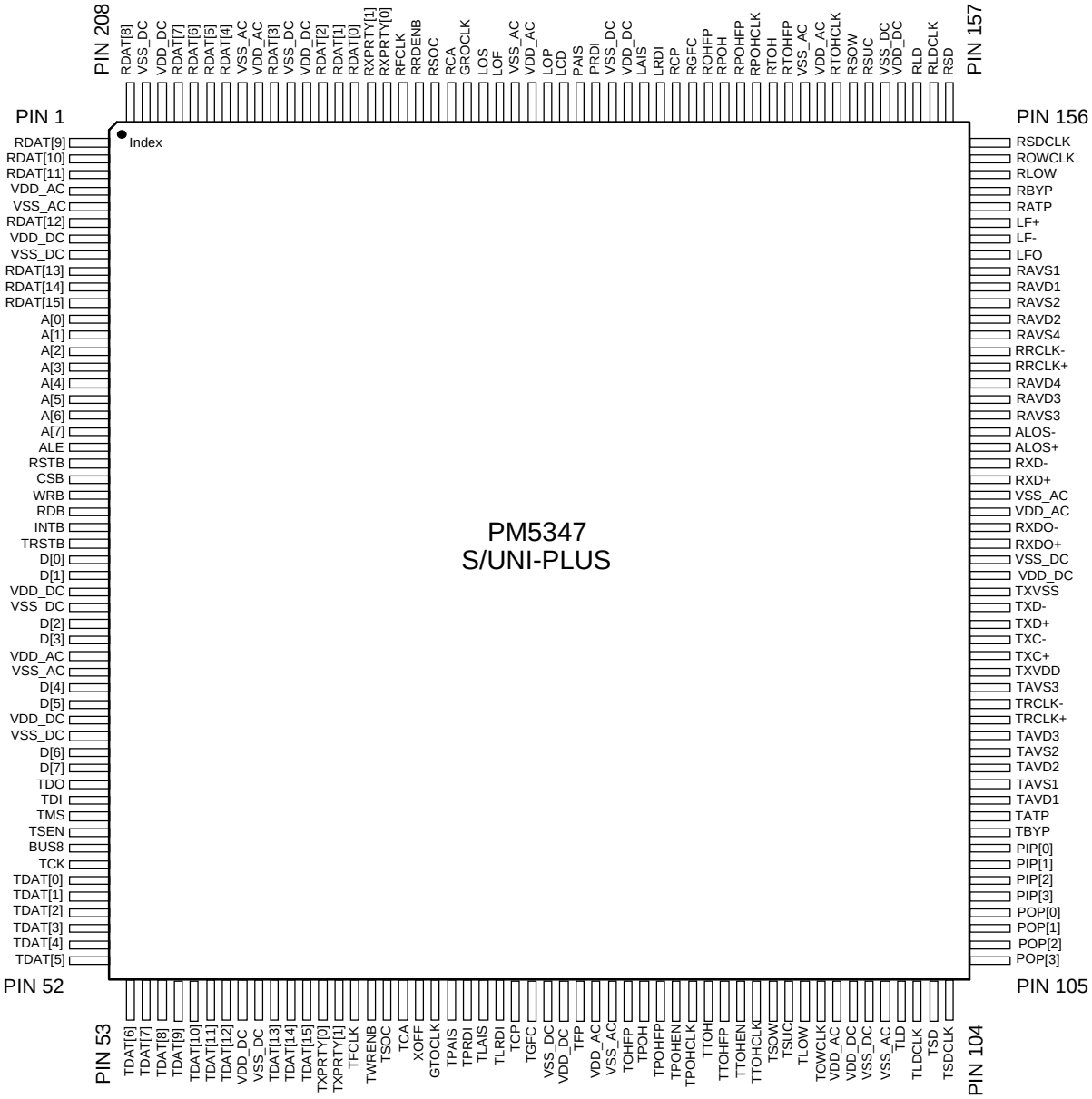
No line rate clocks are required directly by the S/UNI-PLUS as it synthesizes the transmit clock and recovers the receive clock using a 19.44 MHz or 6.48 MHz reference clock. Optionally, receive clock recovery or transmit clock synthesis may be bypassed.

The S/UNI-PLUS is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. The S/UNI-PLUS also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI-PLUS is implemented in low power, +5 Volt, CMOS technology. It has TTL and pseudo-ECL (PECL) compatible inputs and TTL/CMOS compatible outputs and is packaged in a 208 pin PQFP package.

7 PIN DIAGRAM

The S/UNI-PLUS is packaged in a 208 pin plastic QFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.5 mm.



8 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
RBYP	Input	153	The receive bypass (RBYP) input disables clock recovery. If RBYP is high, RXD+/- is sampled on the rising edge of RRCLK+/-. If RBYP is low, the receive clock is recovered from the RXD+/- bit stream. RBYP requires an external pull-down resistor.
RXD+ RXD-	PECL Input	135 136	The receive differential data inputs (RXD+, RXD-) contain the NRZ bit serial receive stream. RXD+/- is sampled on the rising edge of RRCLK+/- when clock recovery is bypassed (the falling edge may be used by reversing RRCLK+/-), otherwise the receive clock is recovered from the RXD+/- bit stream. Please refer to the Operation section for a discussion of PECL interfacing issues.
RXDO+ RXDO-	Output	131 132	The receive differential data outputs (RXDO+, RXDO-) are sliced versions of the RXD+ and RXD- inputs. These outputs are provided to allow decision feedback equalization (DFE) to correct baseline wander. It is intended that these outputs be low pass filtered and attenuated to create an appropriate correction signal that is summed with incoming data to recover the low frequency components.
RRCLK+ RRCLK-	PECL Input	142 143	The receive differential reference clock inputs (RRCLK+, RRCLK-) must be a jitter-free 19.44 MHz or 6.48 MHz reference clock when clock recovery is enabled. When clock recovery is bypassed, RRCLK+/- is nominally a 155.52 MHz or 51.84 MHz 50% duty cycle clock and provides timing for the S/UNI-PLUS receive functions. In this case, RXD+/- is sampled on the rising edge of RRCLK+/-. Please refer to the Operation section for a discussion of PECL interfacing issues.

Pin Name	Type	Pin No.	Function
ALOS+ ALOS-	PECL Input	137 138	The analog loss of signal (ALOS+/-) differential inputs are used to indicate a loss of receive signal power. When ALOS+/- is asserted, the data on the receive data (RXD+/-) pins is forced to all zeros and the phase locked loop switches to the reference clock (RRCLK+/-) to keep the recovered clock in range. These inputs must be DC coupled. Please refer to the Operation section for a discussion of PECL interfacing issues.
RATP	Analog	152	This analog test point (RATP) is provided for production test purposes. Connect this pin to ground.
LF+, LF-, LFO	Analog	151 150 149	Passive components connected to the recovery loop filter (LF+, LF- and LFO) pins determine the dynamics of the clock recovery unit. Refer to the Operation section for details.
TBYP	Input	113	If the transmit bypass (TBYP) input is high, transmit clock synthesis is disabled and TRCLK+/- becomes the line rate clock of 155.52 MHz or 51.84 MHz. If TBYP is low, the transmit clock is synthesized from a 19.44 MHz or 6.48 MHz reference. TBYP requires an external pull down resistor.
TRCLK+ TRCLK-	PECL Input	120 121	The transmit differential reference clock inputs (TRCLK+, TRCLK-) must be a jitter-free 19.44 MHz or 6.48 MHz reference clock when clock synthesis is enabled. When clock synthesis is bypassed, TRCLK+/- is nominally a 155.52 MHz or 51.84 MHz 50% duty cycle clock. This clock provides timing for the S/UNI-PLUS transmit functions. TRCLK+/- may be left unconnected when S/UNI-PLUS loop timing is enabled, or when the transmit clock is synthesized from the receive reference (RRCLK+/-). Please refer to the Operation section for a discussion of PECL interfacing issues.

Pin Name	Type	Pin No.	Function
TXD+ TXD-	Output	126 127	The transmit differential data outputs (TXD+, TXD-) contain the transmit stream. TXD+/- is updated on the falling edge of TXC+/-
TXC+ TXC-	Output	124 125	The transmit clock (TXC+, TXC-) outputs are available when the transmit data rate is 51.84 Mbit/s. TXD+/- is updated on the falling edge of TXC+ and on the rising edge of TXC-. When STS-3c (STM-1) is selected, TXC+ is held low and TXC- is held high.
TATP	Analog	114	This analog test point (TATP) is provided for production test purposes. Connect this pin to ground.
GROCLK	Output	187	The generated receive clock (GROCLK) is nominally a 6.48 MHz or 19.44 MHz, 50% duty cycle clock. Receive outputs that are timed from the line are updated with timing aligned to GROCLK. When configured for receive clock recovery (RBYP low), GROCLK is the recovered line clock divided down by 8. When receive clock recovery is bypassed (RBYP high), GROCLK is equal to RRCLK+/- divided down by 8.

Pin Name	Type	Pin No.	Function
TFP	Input	81	The active high transmit frame pulse (TFP) signal is used to align the SONET/SDH transport frame generated by the S/UNI-PLUS device to a system reference. TFP should be brought high for a single GTOCLK period every 810 (STS-1), or 2430 (STS-3c/STM-1) GTOCLK cycles or a multiple thereof. TFP may be tied low if such synchronization is not required. The offset between an active TFP input and the resultant frame alignment on TOHFP is 16 GTOCLK periods in STS-1 mode and 24 GTOCLK periods in STS-3c mode. TFP is sampled on the rising edge of GTOCLK.
GTOCLK	Output	72	The generated transmit output clock (GTOCLK) is nominally a 6.48 MHz or 19.44 MHz, 50% duty cycle clock. Transmit inputs and outputs that are timed from the line are updated with timing aligned to GTOCLK. When configured for transmit clock synthesis (TBYP low), GTOCLK is the synthesized line clock divided by 8. When transmit clock synthesis is bypassed (TBYP high), GTOCLK is equal to TRCLK+/- divided by 8.
TOHFP	Output	84	The transmit overhead frame pulse (TOHFP) signal identifies the start of a byte on outputs TSOW, TSUC and TLOW. If required, TOHFP is one GTOCLK clock cycle wide and can be used as a reset pulse for an external counter. Please refer to the functional timing diagrams for details.

Pin Name	Type	Pin No.	Function
LOS	Output	186	The loss of signal (LOS) signal is set high when loss of signal is declared. This occurs when a violating period (20 ± 3 µs) of consecutive all zeros bytes is detected on the incoming STS-3c/1 (STM-1) signal (before descrambling). LOS is removed when two valid framing words (A1, A2) are detected and during the intervening time, no violating period of consecutive all zeros patterns is detected. This alarm indication is also available via register access. LOS is updated on the falling edge of GROCLK.
LOF	Output	185	The loss of frame (LOF) signal is set high when loss of frame is declared. This occurs when an out-of-frame condition persists for a period of 3 ms. LOF is removed when an in-frame condition persists for a period of 3 ms. This alarm indication is also available via register access. LOF is updated on the falling edge of GROCLK.
LAIS	Output	176	The line alarm indication signal (LAIS) is set high when line AIS is declared. This occurs when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames (as selected in the RLOP Control/Status register). LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. This alarm indication is also available via register access. LAIS is updated on the falling edge of GROCLK.

Pin Name	Type	Pin No.	Function
LRDI	Output	175	The line remote defect indication (LRDI) signal is set high when line RDI is declared. This occurs when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames (as selected in the RLOP Control/Status register). LRDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. This alarm indication is also available via register access. LRDI is updated on the falling edge of GROCLK.
LOP	Output	182	The loss of pointer (LOP) signal is set high when loss of pointer is declared. This occurs when a valid pointer (H1, H2) is not found in eight consecutive frames, or if eight consecutive new data flags are detected. LOP is removed when the same valid and normal pointer with a normal new data flag is detected in three consecutive frames. The loss of pointer state is not entered if the receive stream contains path AIS. This alarm indication is also available via register access. LOP is updated on the falling edge of GROCLK.
PAIS	Output	180	The path AIS (PAIS) signal is set high when path AIS is declared. This occurs when an all ones pattern is observed in the pointer bytes (H1, H2) for three consecutive frames. Path AIS is removed when the same valid and normal pointer is detected for three consecutive frames or a legal pointer with an active new data flag (NDF) is received. This alarm indication is also available via register access. PAIS is updated on the falling edge of GROCLK.

Pin Name	Type	Pin No.	Function
PRDI	Output	179	The path remote defect indication (PRDI) signal is set high when path RDI is declared. This occurs when bit 5 of the path status byte (G1) is set high for five or ten consecutive frames. Path RDI is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames (as selected in the RPOP Pointer MSB and RDI Filter Control register). This alarm indication is also available via register access. PRDI is updated on the falling edge of GROCLK.
LCD	Output	181	The loss of cell delineation (LCD) signal indicates when cell delineation can not be found. LCD transitions high when an out of cell delineation (OCD) anomaly has persisted for 4 ms. Once asserted, LCD remains high until no OCD anomaly has been detected for 4 ms at which time, LCD is set low. The OCD state is entered when the cell delineation state machine is not in the SYNC state. Please refer to the Functional Description section for an explanation of the cell delineation state machine. This alarm indication is also available via register access. LCD is updated on the falling edge of GROCLK.
TLAIS	Input	75	The active high transmit line alarm indication (TLAIS) signal controls the insertion of line AIS. Line AIS is inserted by overwriting the SONET/SDH frame contents with all ones (before scrambling). The section overhead is not overwritten. This function can also be performed via register access. Line AIS insertion is internally synchronized to frame boundaries. The TLAIS input takes precedence over the TTOH and TTOHEN inputs. TLAIS is sampled on the rising edge of GTOCLK.

Pin Name	Type	Pin No.	Function
TLRDI	Input	76	The active high transmit line remote defect indication (TLRDI) signal controls the insertion of line RDI. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte. This function can also be performed via register access, or be enabled to occur automatically upon detection of receive line AIS, loss of signal, or loss of frame. The TLRDI input takes precedence over the TTOH and TTOHEN inputs. TLRDI is sampled on the rising edge of GTOCLK.
TPAIS	Input	73	The active high transmit path alarm indication (TPAIS) signal controls the insertion of STS-path AIS. A high level on TPAIS forces the insertion of an all ones pattern into the complete synchronous payload envelope, and the payload pointer bytes (H1, H2). Path AIS insertion is internally synchronized to SPE frame boundaries. This function can also be performed via register access. TPAIS is sampled on the rising edge of GTOCLK.
TPRDI	Input	74	The transmit path remote defect indication (TPRDI) signal controls the insertion of path RDI. A high level on TPRDI forces a logic one to be inserted in the path RDI bit position in the path status byte (G1). This function can also be performed via register access, or be enabled to occur automatically upon detection of receive line AIS, loss of frame, loss of signal, loss of pointer, or path AIS. The TPOH and TPOHEN inputs take precedence over the TPRDI input. TPRDI is sampled on the rising edge of GTOCLK.

Pin Name	Type	Pin No.	Function
RFCLK	Input	191	The receive FIFO clock (RFCLK) is used to read words from the synchronous FIFO interface. RFCLK must cycle at a 52 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflow. RRDENB is sampled using the rising edge of RFCLK. RSOC, RCA, RXPRTY[1:0] and RDAT[15:0] are updated on the rising edge of RFCLK.
RRDENB	Input	190	The active low receive read enable input (RRDENB) is used to initiate reads from the receive FIFO. When sampled low using the rising edge of RFCLK, a word is read from the internal synchronous FIFO and output on bus RDAT[15:0]. When sampled high using the rising edge of RFCLK, no read is performed and outputs RDAT[15:0], RXPRTY[1:0] and RSOC are tristated if the TSEN input is high. RRDENB must operate in conjunction with RFCLK to access the FIFO at a high enough instantaneous rate as to avoid FIFO overflows.

Pin Name	Type	Pin No.	Function
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Tristate	194 195 196 199 202 203 204 205 208 1 2 3 6 9 10 11	The receive cell data (RDAT[15:0]) bus carries the ATM cell octets that are read from the receive FIFO. When the 16-bit SCI-PHY interface is selected, (BUS8 is tied low), RDAT[15:0] contains the 16 bit wide word bus. When the 8-bit SCI-PHY interface is selected (BUS8 is tied high), RDAT[7:0] contains the 8-bit wide word bus (RDAT[15:8] is not used). RDAT[15:0] is updated on the rising edge of RFCLK. When the S/UNI-PLUS is configured for tristate operation using the TSEN input, tristating of output bus RDAT[15:0] is controlled by input RRDENB.
RXPRTY[0] RXPRTY[1]	Tristate	192 193	The receive parity (RXPRTY[1:0]) signals indicate the parity of the RDAT[15:0] bus. RXPRTY[1] is the parity calculation over the RDAT[15:8] bus. RXPRTY[0] is the parity calculation over the RDAT[7:0] bus. Alternately, the device can be configured so that RXPRTY[1] is the parity calculation over the entire RDAT[15:0] bus. RXPRTY[0] is not used in this case. Odd or even parity selection can be made using the RACP Control register. RXPRTY[1:0] is updated on the rising edge of RFCLK. When the S/UNI-PLUS is configured for tristate operation using the TSEN input, tristating of output bus RXPRTY[1:0] is control by input RRDENB.

Pin Name	Type	Pin No.	Function
RSOC	Tristate	189	The receive start of cell (RSOC) signal marks the start of cell on the RDAT[15:0] bus. When RSOC is high, the first word of the cell structure is present on the RDAT[15:0] bus. RSOC is updated on the rising edge of RFCLK. When the S/UNI-PLUS is configured for tristate operation using the TSEN input, tristating of output RSOC is control by input RRDENB.
RCA	Output	188	The receive cell available (RCA) signal indicates when a cell is available in the receive FIFO. When asserted, RCA indicates that the receive FIFO has at least one cell available to be read. When RCA is deasserted, the receive FIFO contains only four words or is empty (as selected in the RACP Interrupt Enable/Control register). RCA default state can be selected in the S/UNI-PLUS Master Control register. RCA is updated on the rising edge of RFCLK. The active polarity of this signal is programmable and defaults to active high.
BUS8	Input	45	The bus width select (BUS8) input selects the transmit and receive SCI-PHY interface types. When BUS8 is tied high, the 8-bit wide SCI-PHY interface is enabled. When BUS8 is tied low, the 16-bit wide SCI-PHY interface is selected.
TSEN	Input	44	The tristate enable (TSEN) signal allows tristate control over outputs RDAT[15:0], RXPRTY[1:0] and RSOC. When TSEN is high, the active low receive read enable input, RRBENB controls when outputs RDAT[15:0], RXPRTY[1:0] and RSOC are driven. When TSEN is low, outputs RDAT[15:0], RXPRTY[1:0] and RSOC are always driven.

Pin Name	Type	Pin No.	Function
TFCLK	Input	67	The transmit FIFO clock (TFCLK) is used to write words to the synchronous FIFO interface. TFCLK must cycle at a 52 MHz or lower instantaneous rate. TWRENB, TSOC, TXPRTY[1:0] and TDAT[15:0] are sampled on the rising edge of TFCLK. In addition, TCA is updated on the rising edge of TFCLK.
TWRENB	Input	68	The active low transmit write enable input (TWRENB) is used to initiate writes to the transmit FIFO. When sampled low using the rising edge of TFCLK, the 16-bit word on TDAT[15:0] is written into the transmit FIFO. When sampled high using the rising edge of TFCLK, no write is performed. A complete 53 octet cell must be written to the FIFO before it is inserted into the STS-3c/1 (STM-1) SPE. Idle/unassigned cells are inserted when a complete cell is not available.

Pin Name	Type	Pin No.	Function
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	Input	47 48 49 50 51 52 53 54 55 56 57 58 59 62 63 64	The transmit cell data (TDAT[15:0]) bus carries the ATM cell octets that are written to the transmit FIFO. When the 16-bit SCI-PHY interface is selected, (BUS8 is tied low), TDAT[15:0] contains the 16-bit wide word bus. When the 8-bit SCI-PHY interface is selected (BUS8 is tied high), TDAT[7:0] contains the 8-bit wide word bus (TDAT[15:8] is not used). TDAT[15:0] is sampled on the rising edge of TFCLK and is considered valid only when TWRENB is simultaneously asserted.
TXPRTY[0] TXPRTY[1]	Input	65 66	The transmit parity (TXPRTY[1:0]) signals indicate the parity of the TDAT[15:0] bus. TXPRTY[1] is expected to be the parity calculation over the TDAT[15:8] bus. TXPRTY[0] is expected to be the parity calculation over the TDAT[7:0] bus. Alternately, the device can be configured so that TXPRTY[1] is expected to be the parity calculation over the entire TDAT[15:0] bus. TXPRTY[0] should be tied low in this case. Odd or even parity selection can be made using the TACP FIFO Control register. TXPRTY[1:0] is sampled on the rising edge of TFCLK and is considered valid only when TWRENB is simultaneously asserted.

Pin Name	Type	Pin No.	Function
TSOC	Input	69	The transmit start of cell (TSOC) signal marks the start of cell on the TDAT[15:0] bus. When TSOC is high, the first word of the cell structure is present on the TDAT[15:0] bus. It is not necessary for TSOC to be present at each cell. An interrupt may be generated if TSOC is high during any word other than the first word of the cell structure. TSOC is sampled on the rising edge of TFCLK and is considered valid only when TWRENB is simultaneously asserted.
TCA	Output	70	The transmit cell available (TCA) signal indicates when a cell is available in the transmit FIFO. When asserted, TCA indicates that the transmit FIFO is not full. When TCA is deasserted, it indicates that either the transmit FIFO is near full and can accept no more than four writes or that the transmit FIFO is full (as selected in the TACP FIFO Control register) In addition, to reduce FIFO latency, the FIFO full level can be programmed in the TACP FIFO Control register. The default state of TCA can be selected in the S/UNI-PLUS Master Control register. TCA is updated on the rising edge of TFCLK. The active polarity of this signal is programmable and defaults to active high.
XOFF	Input	71	The transmit off (XOFF) input prevents the insertion of cells from the transmit FIFO. If XOFF is set high, the next cell transmitted is an idle/unassigned cell regardless of the number of cells in the FIFO. Idle/unassigned cells are transmitted until XOFF is deasserted. XOFF may be treated as an asynchronous signal. XOFF must be tied low if it is not used.

Pin Name	Type	Pin No.	Function
RTOH	Output	168	The receive transport overhead output (RTOH) contains the receive transport overhead bytes (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, M0 or M1/Z2, and E2) extracted from the receive stream. RTOH is updated on the falling edge of RTOHCLK.
RTOHCLK	Output	164	The receive transport overhead clock (RTOHCLK) is nominally a 5.184 MHz clock (STM-1/STS-3c) or a 1.728 MHz clock (STS-1) which provides timing to process the extracted receive transport overhead. When STS-3c (STM-1) mode is selected, RTOHCLK is a gapped 6.48 MHz clock. When STS-1 mode is selected, RTOHCLK is a gapped 2.16 MHz clock. RTOHCLK is updated on the falling edge of GROCLK.
RTOHFP	Output	167	The receive transport overhead frame position (RTOHFP) signal is used to locate the individual receive transport overhead bits in the transport overhead output, RTOH. RTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is present in the RTOH stream. RTOHFP is updated on the falling edge of RTOHCLK.
RPOH	Output	171	The receive path overhead data (RPOH) signal contains the path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the received STS-3c/1 frame. RPOH is updated on the falling edge of RPOHCLK.
RPOHCLK	Output	169	The receive path overhead clock (RPOHCLK) is nominally a 576 kHz clock which provides timing to process the extracted receive path overhead. RPOHCLK is a gapped 648 KHz clock. RPOHCLK is updated on the falling edge of GROCLK.

Pin Name	Type	Pin No.	Function
RPOHFP	Output	170	The receive path overhead frame position (RPOHFP) signal may be used to locate the individual receive path overhead bits in the path overhead data stream, RPOH. RPOHFP is logic one while bit 1 (the most significant bit) of the path trace byte (J1) is present in the RPOH stream. RPOHFP is updated on the falling edge of RPOHCLK.
RSDCLK	Output	156	The receive section DCC clock (RSDCLK) is a 192 kHz clock used to update the RSD output. RSDCLK is generated by gapping a 216 kHz clock.
RSD	Output	157	The receive section DCC (RSD) signal contains the serial section data communications channel (D1, D2, D3) extracted from the receive stream. RSD is updated on the falling edge of RSDCLK.
RLDCLK	Output	158	The receive line DCC clock (RLDCLK) is a 576 kHz clock used to update the RLD output. RLDCLK is generated by gapping a 2.16 MHz clock.
RLD	Output	159	The receive line DCC (RLD) signal contains the serial line data communications channel (D4 - D12) extracted from the receive stream. RLD is updated on the falling edge of RLDCLK.
ROWCLK	Output	155	The receive orderwire clock (ROWCLK) is a 64 kHz clock used to update the RSOW, RSUC, and RLOW outputs. ROWCLK is generated by gapping a 72 kHz clock.
RSOW	Output	163	The receive section orderwire (RSOW) signal contains the section orderwire channel (E1) extracted from the receive stream. RSOW is updated on the falling edge of ROWCLK.

Pin Name	Type	Pin No.	Function
RSUC	Output	162	The receive section user channel (RSUC) signal contains the section user channel (F1) extracted from the receive stream. RSUC is updated on the falling edge of ROWCLK.
RLOW	Output	154	The receive line orderwire (RLOW) signal contains the line orderwire channel (E2) extracted from the receive stream. RLOW is updated on the falling edge of ROWCLK.
ROHFP	Output	172	The receive overhead frame pulse (ROHFP) signal identifies the start of a byte on outputs RSOW, RSUC and RLOW. If required, ROHFP is one GROCLK clock cycle wide and can be used as a reset pulse for an external counter. Please refer to the functional timing diagrams for details.
TTOH	Input	89	The transmit transport overhead input (TTOH) contains the transport overhead bytes (A1, A2, J0/Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, S1/Z1, M0 or M1/Z2, and E2) and error masks (H1, H2, B1, and B2) which may be inserted, or used to insert bit interleaved parity errors or payload pointer bit errors into the overhead byte positions in the transmit stream. Insertion is controlled by the TTOHEN input. TTOH is sampled on the rising edge of TTOHCLK.

Pin Name	Type	Pin No.	Function
TTOHEN	Input	91	The transmit transport overhead insert enable (TTOHEN) signal, together with internal register bits, controls the source of the transport overhead data which is transmitted. While TTOHEN is high, values sampled on the TTOH input are inserted into the corresponding transport overhead bit position (for the A1, A2, J0/Z0, E1, F1, D1-D3, K1, K2, H3, D4-D12, S1/Z1, M0 or M1/Z2, and E2 bytes). While TTOHEN is low, default values are inserted into these transport overhead bit positions. A high level on TTOHEN during the B1, B2 or H1-H2 bit positions enables an error mask. While the error mask is enabled, a high level on input TTOH causes the corresponding B1, B2 or H1-H2 bit position to be inverted. A low level on TTOH allows the corresponding bit position to pass through the S/UNI-PLUS uncorrupted. TTOHEN is sampled on the rising edge of TTOHCLK.
TTOHCLK	Output	92	The transmit transport overhead clock (TTOHCLK) is nominally a 5.184 MHz clock (STS-3c/STM-1) or a 1.728 MHz clock (STS-1) clock which provides timing for circuitry that sources the transport overhead stream, TTOH. When STS-3c (STM-1) mode is selected, TTOHCLK is a gapped 6.48 MHz clock. When STS-1 mode is selected, TTOHCLK is a gapped 2.16 MHz clock. TTOHCLK is updated in the rising edge of GTOCLK.
TTOHFP	Output	90	The transmit transport overhead frame position (TTOHFP) signal is used to locate the individual transport overhead bits in the transport overhead input, TTOH. TTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is expected on TTOH. TTOHFP is updated on the falling edge of TTOHCLK.

Pin Name	Type	Pin No.	Function
TPOH	Input	85	The transmit path overhead data (TPOH) signal contains the path overhead bytes (J1, C2, G1, F2, H4, Z3, Z4, and Z5) and error masks (B3) which may be inserted, or used to insert path BIP-8 errors into the path overhead byte positions in the transmit stream. Insertion is controlled by the TPOHEN input, or by bits in internal registers. TPOH is sampled on the rising edge of TPOHCLK.
TPOHEN	Input	87	The transmit path overhead insert enable (TPOHEN) signal, together with internal register bits, controls the source of the path overhead data which is transmitted. While TPOHEN is high, values sampled on the TPOH input are inserted into the corresponding path overhead bit position (for the J1, C2, G1, H4, F2, Z3, Z4, and Z5 bytes). While TPOHEN is low, values obtained from internal registers are inserted into these path overhead bit positions. A high level on TPOHEN during the B3 bit positions enables an error mask. While the error mask is enabled, a high level on input TPOH causes the corresponding B3 bit position to be inverted. A low level on TPOH allows the corresponding bit position to pass through the S/UNI-PLUS uncorrupted. TPOHEN is sampled on the rising edge of TPOHCLK.
TPOHCLK	Output	88	The transmit path overhead clock (TPOHCLK) is nominally a 576 kHz clock which provides timing for circuitry that sources the path overhead stream, TPOH. TPOHCLK is a gapped 810 KHz clock. TPOHCLK is updated in the falling edge of GTOCLK.

Pin Name	Type	Pin No.	Function
TPOHFP	Output	86	The transmit path overhead frame position (TPOHFP) signal may be used to locate the individual path overhead bits in the path overhead data stream, TPOH. TPOHFP is logic one while bit 1 (the most significant bit) of the path trace byte (J1) is expected in the TPOH stream. TPOHFP is updated on the falling edge of TPOHCLK.
TOWCLK	Output	96	The transmit orderwire clock (TOWCLK) is a 64 kHz clock used to sample the TSOW, TSUC, and TLOW inputs. TOWCLK is generated by gapping a 72 kHz clock.
TSOW	Input	93	The transmit section orderwire (TSOW) signal contains the section orderwire channel (E1) inserted into the transmit stream. When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH and TTOHEN takes precedence over overhead sourced using TSOW. TSOW is sampled on the rising edge of TOWCLK.
TSUC	Input	94	The transmit section user channel (TSUC) signal contains the section user channel (F1) inserted into the transmit stream. When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH and TTOHEN takes precedence over overhead sourced using TSUC. TSUC is sampled on the rising edge of TOWCLK.
TLOW	Input	95	The transmit line orderwire (TLOW) signal contains the line orderwire channel (E2) inserted into the transmit stream. When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH and TTOHEN takes precedence over overhead sourced using TLOW. TLOW is updated on the rising edge of TOWCLK.

Pin Name	Type	Pin No.	Function
TSDCLK	Output	104	The transmit section DCC clock (TSDCLK) is a 192 kHz clock used to sample the TSD input. TSDCLK is generated by gapping a 216 kHz clock.
TSD	Input	103	The transmit section DCC (TSD) signal contains the serial section data communications channel (D1, D2, D3). When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH and TTOHEN takes precedence over overhead sourced using TSD. TSD is sampled on the rising edge of TSDCLK.
TLDCLK	Output	102	The transmit line DCC clock (TLDCLK) is a 576 kHz clock used to sample the TLD input. TLDCLK is generated by gapping a 2.16 MHz clock.
TLD	Input	101	The transmit line DCC (TLD) signal contains the serial line data communications channel (D4 - D12). When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH and TTOHEN takes precedence over overhead sourced using TLD. TLD is sampled on the rising edge of TLDCLK.
RCP	Output	174	The receive cell pulse (RCP) signal marks the most significant bit (MSB) of a cell header's GFC field on output, RGFC. RCP is updated on the falling edge of GROCLK.
RGFC	Output	173	The receive generic flow control (RGFC) signal contains the serialized GFC field extracted from receive cells. The GFC field is output MSB first. The RCP output can be used to identify the MSB bit of every GFC field. The GFC Control register can be used to gate off individual GFC bits. RGFC is updated on the falling edge of GROCLK.

Pin Name	Type	Pin No.	Function
TCP	Output	77	The transmit cell pulse (TCP) signal is provided to locate the most significant GFC bit (GFC[3]) of a cell's GFC field sourced on input TGFC. TCP pulses high for one SPECLK period to identify the SPECLK cycle before the cycle the GFC[3] bit is output on TGFC. TCP is updated on the falling edge of GTOCLK.
TGFC	Input	78	The transmit generic flow control (TGFC) input contains GFC bits that can be inserted into the GFC fields of transmitted cells (including idle/unassigned cells). Insertion is controlled using bits in the TACP Fixed Stuff/GFC register. TGFC is sampled on the rising edge of GTOCLK.
POP[3] POP[2] POP[1] POP[0]	Output	105 106 107 108	The parallel output port (POP[3:0]) is used to control the operation of PMD devices. The signal levels on this parallel output port correspond to the bit values contained in the S/UNI-PLUS Parallel I/O Port Register.
PIP[3] PIP[2] PIP[1] PIP[0]	Input	109 110 111 112	The parallel input port (PIP[3:0]) is used to monitor the operation of PMD devices. An interrupt may be generated when state changes are detected on the monitored signals. The real-time signal levels on this port are available in the S/UNI-PLUS Parallel I/O Port register. Each of the inputs contains an internal pull-down resistor.
CSB	Input	22	The active low chip select (CSB) signal is low during S/UNI-PLUS register accesses. Note when not being used, CSB should be tied high. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.

Pin Name	Type	Pin No.	Function
RDB	Input	24	The active low read enable (RDB) signal is low during S/UNI-PLUS register read accesses. The S/UNI-PLUS drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	23	The active low write strobe (WRB) signal is low during a S/UNI-PLUS register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	27 28 31 32 35 36 39 40	The bidirectional data bus D[7:0] is used during S/UNI-PLUS register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]/TRS	Input	12 13 14 15 16 17 18 19	The address bus A[7:0] selects specific registers during S/UNI-PLUS register accesses. The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.

Pin Name	Type	Pin No.	Function
RSTB	Input	21	The active low reset (RSTB) signal provides an asynchronous S/UNI-PLUS reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
ALE	Input	20	The address latch enable (ALE) is active high and latches the address bus A[7:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-PLUS to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
INTB	Output	25	The active low interrupt (INTB) signal goes low when a S/UNI-PLUS interrupt source is active, and that source is unmasked. The S/UNI-PLUS may be enabled to report many alarms or events via interrupts. Examples are loss of signal (LOS), loss of frame (LOF), line AIS, line remote defect indication (LRDI), loss of pointer (LOP), path AIS, path RDI, and many others. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
TCK	Input	46	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	43	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	42	The test data input (TDI) signal carries test data into the S/UNI-PLUS via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
TDO	Tristate	41	The test data output (TDO) signal carries test data out of the S/UNI-PLUS via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is tristate except when scanning of data is in progress.
TRSTB	Input	26	The active low test reset (TRSTB) signal provides an asynchronous S/UNI-PLUS test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence. Note that when not being used, TRSTB must be connected to the RSTB input.
VDD_DC1 VDD_DC2 VDD_DC3 VDD_DC4 VDD_DC5 VDD_DC6 VDD_DC7 VDD_DC8 VDD_DC9 VDD_DC10 VDD_DC11	Power	7 29 37 60 80 98 129 160 177 197 206	The DC power (VDD_DC1 - VDD_DC11) pins should be connected to a well decoupled +5 V DC in common with VDD_AC.

Pin Name	Type	Pin No.	Function
VSS_DC1 VSS_DC2 VSS_DC3 VSS_DC4 VSS_DC5 VSS_DC6 VSS_DC7 VSS_DC8 VSS_DC9 VSS_DC10 VSS_DC11	Ground	8 30 38 61 79 99 130 161 178 198 207	The DC ground (VSS_DC1 - VSS_DC11) pins should be connected to GND in common with VSS_AC.
VDD_AC1 VDD_AC2 VDD_AC3 VDD_AC4 VDD_AC5 VDD_AC6 VDD_AC7 VDD_AC8	Power	4 33 82 97 133 165 183 200	The pad ring power (VDD_AC1 - VDD_AC8) pins should be connected to a well decoupled +5 V DC in common with VDD_DC
VSS_AC1 VSS_AC2 VSS_AC3 VSS_AC4 VSS_AC5 VSS_AC6 VSS_AC7 VSS_AC8	Ground	5 34 83 100 134 166 184 201	The pad ring ground (VSS_AC1 - VSS_AC8) pins should be connected to GND in common with VSS_DC.

Pin Name	Type	Pin No.	Function
TAVD1	Power	115	The power (TAVD1) pin for the transmit clock synthesizer reference circuitry. TAVD1 should be connected to a clean, well decoupled, +5V supply.
TAVS1	Ground	116	The ground (TAVS1) pin for the transmit clock synthesizer reference circuitry. TAVS1 should be connected to a clean ground reference.
TAVD2	Power	117	The power (TAVD2) pin for the transmit clock synthesizer oscillator. TAVD2 should be connected to a clean, well decoupled, +5V supply.
TAVS2	Ground	118	The ground (TAVS2) pin for the transmit clock synthesizer oscillator. TAVS2 should be connected to a clean ground reference.
TAVD3	Power	119	The power (TAVD3) pin for the transmit reference clock (TRCLK+/-) inputs. TAVD3 should be connected to a clean, well decoupled, +5V supply.
TAVS3	Ground	122	The ground (TAVS3) pin for the transmit reference clock (TRCLK+/-) inputs. TAVS3 should be connected to a clean ground reference.
TXVDD	Power	123	The transmit pad power (TXVDD) supplies the TXC+/- and TXD+/- outputs. TXVDD is physically isolated from the other device power pins and should be a clean, well decoupled +5 V supply to minimize the noise coupled into the transmit stream.
TXVSS	Ground	128	The transmit pad ground (TXVSS) is the return path for the TXC+/- and TXD+/- outputs. TXVSS is physically isolated from the other device ground pins and should be clean to minimize the noise coupled into the transmit stream.
RAVD1	Power	147	The power (RAVD1) pin for receive clock and data recovery block reference circuitry. RAVD1 should be connected to a clean, well decoupled, +5V supply.

Pin Name	Type	Pin No.	Function
RAVS1	Ground	148	The ground (RAVS1) pin for receive clock and data recovery block reference circuitry. RAVS1 should be connected to a clean ground reference.
RAVD2	Power	145	The power (RAVD2) pin for receive clock and data recovery block active loop filter and oscillator. RAVD2 should be connected to a clean, well decoupled, +5V supply.
RAVS2	Ground	146	The ground (RAVS2) pin for receive clock and data recovery block active loop filter and oscillator. RAVS2 should be connected to a clean ground reference.
RAVD3	Power	140	The power (RAVD3) pin for the RXD+/- and ALOS+/- PECL inputs. RAVD3 should be connected to a clean, well decoupled, +5V supply.
RAVS3	Ground	139	The ground (RAVS3) pin for the RXD+/- and ALOS+/- PECL inputs. RAVS3 should be connected to a clean ground reference.
RAVD4	Power	141	The power (RAVD4) pin for the RRCLK+/- PECL inputs. RAVD4 should be connected to a clean, well decoupled, +5V supply..
RAVS4	Ground	144	The ground (RAVS4) pin for the RRCLK+/- PECL inputs. RAVS4 should be connected to a clean ground reference.

Notes on Pin Description:

1. All S/UNI-PLUS inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels except for the RXD+/-, ALOS+/-, RRCLK+/-, and TRCLK+/- inputs which operate at pseudo-ECL (PECL) logic levels.

2. The TXD+/- and TXC+/- outputs have a 6 mA drive capability. The GTOCLK, GROCLK, RSOC, RDAT[15:0], RXPRTY[1:0], RCA, TCA and D[7:0] outputs and bidirectionals have a 4 mA drive capability. All other S/UNI-PLUS digital outputs and bidirectionals have 2 mA drive capability.

3. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.

4. The VSS_DC, VSS_AC, TXVSS, and AVS ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-PLUS.

5. The VDD_AC , VDD_AC, TXVDD, and AVD power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-PLUS.

6. The TAVD[3:1] and RAVD[4:1] pins provide power to sensitive analog circuitry in the S/UNI-PLUS. These signals should be connected to the PCB VDD power plane at a point where the supply is clean and as free as possible of digitally induced switching noise. In a typical system, TAVD and RAVD should be "starred" back to a clean reference point on the PCB, for example at the card edge connector where the system VDD enters the PCB. In some systems a clean VDD supply cannot be readily obtained, and RAVD and TAVD may require separate regulation.

7. Each TAVD and RAVD pin should be separately decoupled using ceramic decoupling capacitors located as close as possible to the S/UNI-PLUS.

8. The TAVS[3:1] and RAVS[4:1] pins provide the ground return path for sensitive analog circuitry in the S/UNI-PLUS. These signals should be connected to the PCB ground plane at a point where the ground is clean and as free as possible of digital return currents. In a typical system, TAVS and RAVS should be "starred" back to a clean reference point on the PCB, for example at the card edge connector where the system ground reference enters the PCB.

9. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence.

10. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

11. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

12. Ensure that all digital power is applied simultaneously, and it is applied before the analog power is applied.

9 FUNCTIONAL DESCRIPTION

9.1 Clock Recovery

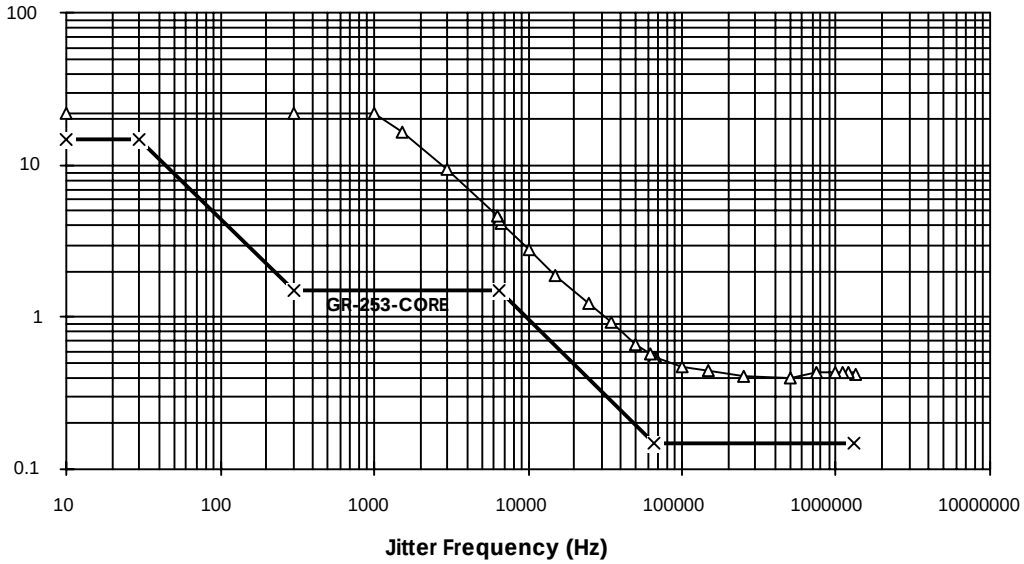
The clock recovery unit recovers the clock from the incoming bit serial data stream. The clock recovery unit is fully compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit continues to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit can be configured to utilize reference clocks at 6.48 or 19.44 MHz. The clock recovery unit provides status bits that indicate whether it is locked to data or the reference. The clock recovery unit also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially, the PLL locks to the reference clock, RRCLK+/-. When the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 80 bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the RRCLK+/- reference accuracy in the case of a loss of signal condition. To meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-20ppm. When not loop timed, the RRCLK+/- accuracy may be relaxed to +/-50ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by GR-253-CORE (Figure 3). The jitter tolerance illustrated is associated with the external loop filter components recommended in the Operation section.

Figure 3 - STS-3c/STM-1 and STS-1 Jitter Tolerance



9.2 Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) converts the received bit serial stream to a byte serial stream. The SIPO searches for the SONET/SDH framing pattern (A1, A2) in the receive stream, and performs serial to parallel conversion on octet boundaries.

9.3 Receive Section Overhead Processor

The Receive Section Overhead Processor (RSOP) provides frame synchronization, descrambling, section level alarm and performance monitoring. In addition, it extracts the section orderwire channel, the section user channel, the section data communication channel from the section overhead and provides it serially on outputs RSOW, RSUC and RSD respectively.

Framer

The Framer Block determines the in-frame/out-of-frame status of the receive stream.

While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received.

While out-of-frame, the SIPO block monitors the receive stream for an occurrence of the framing pattern. When a framing pattern has been recognized, the Framer block verifies that an error free framing pattern is present in the next frame before declaring in-frame.

Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the receive stream. The generating polynomial is $x^7 + x^6 + 1$ and the sequence length is 127. Details of the descrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the trace/growth bytes (J0/Z0) are not descrambled. A register bit is provided to disable the descrambling operation.

Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-3c/1 (STM-1) frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section level bit errors in a 16-bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

Loss of Signal

The Loss of Signal Block monitors the scrambled data of the receive stream for the absence of 1's. When 20 ± 3 µs of all zeros patterns is detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. LOS is updated on the falling edge of GROCLK.

Loss of Frame

The Loss of Frame Block monitors the in-frame / out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame condition persists for 3 ms. The LOF is cleared when an in-frame condition persists for a period of 3 ms. To provide for intermittent out-of-frame (or in-frame) conditions, the 3 ms timer is not reset to zero until an in-frame (or out-of-frame) condition persists for 3 ms. LOF is updated on the falling edge of GROCLK.

9.4 Receive Line Overhead Processor

The Receive Line Overhead Processor (RLOP) provides line level alarm and performance monitoring. In addition, it extracts the line orderwire channel and the line data communication channel from the line overhead and provides it serially on outputs RLOW and RLD respectively.

Line RDI Detect

The Line RDI Detect Block detects the presence of Line Remote Defect Indication (LRDI) in the receive stream. Output LRDI is asserted when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. LRDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. LRDI is updated on the falling edge of GROCLK.

Line AIS Detect

The Line AIS Block detects the presence of a Line Alarm Indication Signal (LAIS) in the receive stream. Output LAIS is asserted when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. LAIS is updated with on the falling edge of GROCLK.

Automatic Protection Switch Control Block

The Automatic Protection Switch Control (APSC) Block filters and captures the receive automatic protection switch channel bytes (K1 and K2) allowing them to be read via the S/UNI-PLUS Receive K1 Register and the S/UNI-PLUS Receive K2 Register. The bytes are filtered for three frames before being written to these registers. A protection switching byte failure alarm is declared when twelve

successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the S/UNI-PLUS Receive K1 Register and the S/UNI-PLUS Receive K2 Register.

Error Monitor

The Error Monitor Block calculates the received line BIP-8/24 error detection code (B2) based on the line overhead and synchronous payload envelope of the receive stream. The line BIP code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is compared with the BIP code extracted from the B2 bytes of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 192000 (24 x 8000) bit errors can be detected per second.

The Error Monitor Block accumulates these line layer bit errors in a 20 bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, this counter should be polled at least once per second to avoid saturation which in turn may result in missed bit error events.

The Error Monitor Block also accumulates line far end block error indications (contained in the M0 or M1 byte) in a similar manner.

9.5 Transport Overhead Extract Port

The Transport Overhead Extract Port extracts the entire receive transport overhead on RTOH for optional external TOH processing. RTOHFP is provided to identify the most significant bit of the A1 framing byte on RTOH. The transport overhead clock, RTOHCLK is nominally a 5.184 MHz (STS-3c/STM-1 mode) or a 1.728 MHz (STS-1 mode) clock. RTOH and RTOHFP are updated on the falling edge of RTOHCLK.

9.6 Receive Path Overhead Processor

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope, and path level alarm indication and performance monitoring.

Pointer Interpreter

The Pointer Interpreter Block interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead in the receive stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm, three states are defined as shown in Figure 4:

NORM_state (NORM)

AIS_state (AIS)

LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

The following events (indications) are defined:

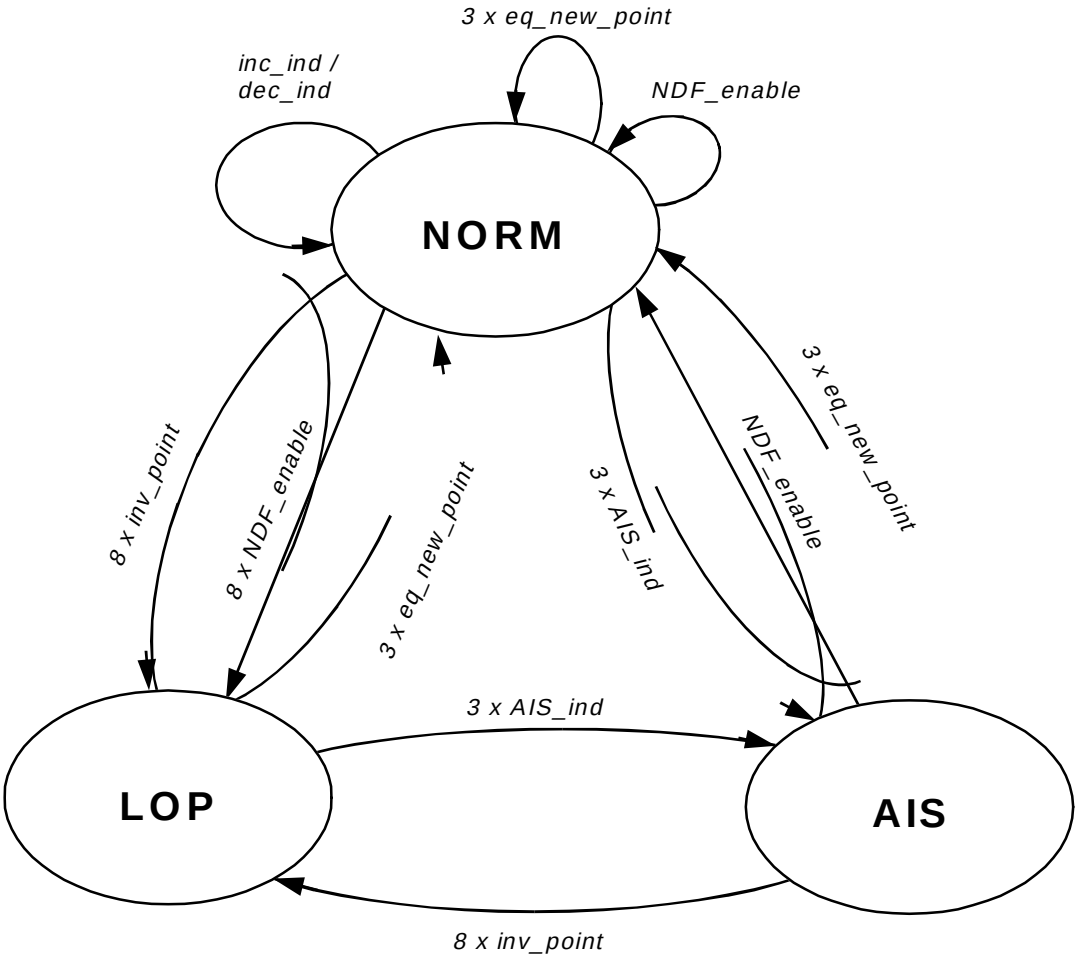
norm_point :	disabled NDF + ss + offset value equal to active offset
NDF_enable:	enabled NDF + ss + offset value in range of 0 to 782
AIS_ind:	H1 = 'hFF, H2 = 'hFF
inc_ind:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
dec_ind:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
inv_point:	not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind)

new_point: disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Notes:

1. Active offset is defined as the accepted current phase of the SPE in the NORM_state and is undefined in the other states.
2. Enabled new data flag (NDF) is defined as the following bit patterns: 1001, 0001, 1101, 1011, 1000.
3. Disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, 0111.
4. The remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_point indication.
5. Ss bits are unspecified in SONET and has bit pattern 10 in SDH
6. The use of ss bits in definition of indications may be optionally disabled.
7. The requirement for previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.
8. New_point is also an inv_point.

Figure 4 - Pointer Interpretation State Diagram



The transitions indicated in the state diagram are defined as follows:

- inc_ind/dec_ind: offset adjustment (increment or decrement indication)
- 3 x eq_new_point: three consecutive equal new_point indications
- NDF_enable: single NDF_enable indication
- 3 x AIS_ind: three consecutive AIS indications
- 8 x inv_point: eight consecutive inv_point indications

- 8 x NDF_enable eight consecutive NDF_enable indications

Notes:

1. The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

2. 3 x new_point takes precedence over 8 x inv_point.

3. All three offset values received in 3 x eq_new_point must be identical.

4. "Consecutive event counters" are reset to zero on a change of state.

The Pointer Interpreter Block detects loss of pointer (LOP) in the receive stream. LOP is declared (LOP output set high) on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive new data flag (NDF) enabled indications. LOP is removed (LOP output set low) when the same valid pointer with normal NDF is detected for three consecutive frames. Incoming STS Path AIS (pointer bytes set to all ones) does not cause entry into the LOP state.

The Pointer Interpreter Block detects path AIS in the receive stream. PAIS is declared (PAIS output set high) on entry to the AIS_state after three consecutive AIS indications. PAIS is removed (PAIS set low) when the same valid pointer with normal NDF is detected for three consecutive frames or when a valid pointer with NDF enabled is detected.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF enabled or NDF disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset is updated with the receive pointer value. An illegal pointer change is defined as a inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The pointer value is used to extract the path overhead from the receive stream. The current pointer value can be read from an internal register.

SPE Timing

The SPE Timing Block provides SPE timing information to the Error Monitor and the Extract blocks. The block contains a free running timeslot counter that is initialized by a J1 byte identifier (which identifies the first byte of the SPE). Control signals are provided to the Error Monitor and the Extract blocks to identify the Path Overhead bytes and to downstream circuitry to extract the ATM cell payload.

Error Monitor

The Error Monitor Block contains two 16-bit counters that are used to accumulate path BIP-8 errors (B3), and far end block errors (FEBEs). The contents of the two counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame.

FEBEs are detected by extracting the 4-bit FEBE field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path Remote Defect Indication (PRDI) and auxiliary PRDI (APRDI) are detected by extracting bit 5 and bit 6 of the path status byte. PRDI (APRDI) is declared when bit 5 (bit 6) is high for five or ten consecutive frames. PRDI (APRDI) is removed when bit 5 (bit 6) is low for five or ten consecutive frames.

9.7 Path Overhead Extract

The Path Overhead Extract Block extracts and serializes the receive path overhead bytes on RPOH. Output RPOHFP is provided to identify the most significant bit of the path trace byte (J1) on RPOH. The path overhead clock, RPOHCLK is nominally a 576 kHz clock. RPOH and RPOHFP are updated on the falling edge of RPOHCLK.

9.8 Receive ATM Cell Processor

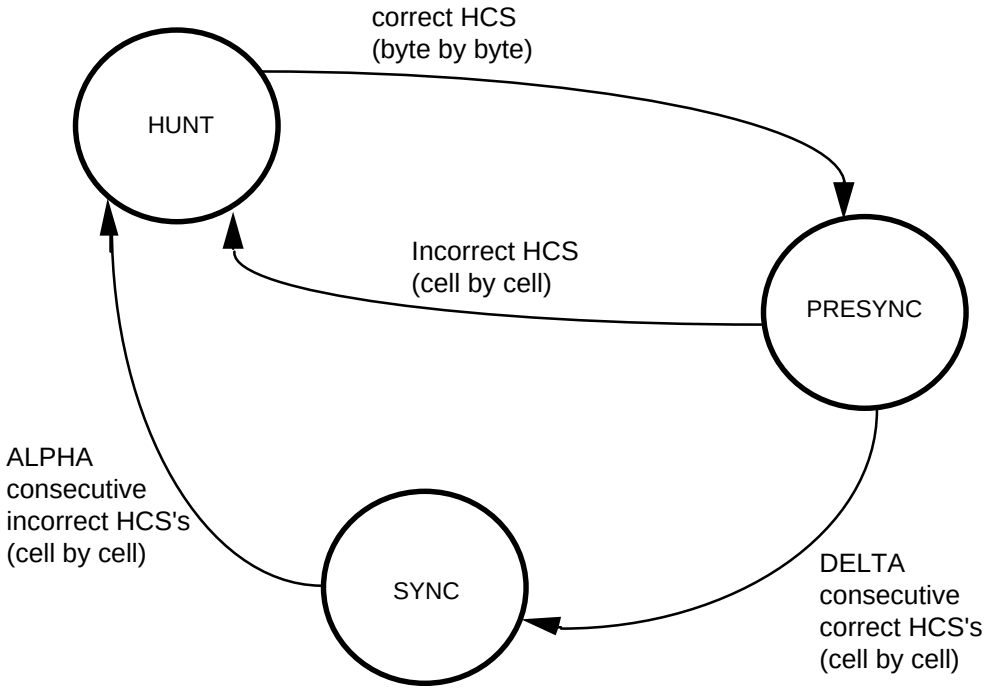
The Receive ATM Cell Processor (RACP) performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling. The RACP also

provides a four cell deep receive FIFO. This FIFO is used to separate the STS-3c/1 (STM-1) line timing from the higher layer ATM system timing.

Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells are assumed to be byte-aligned to the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates individually to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary, corresponding to the correct HCS, and enters the PRESYNC state. The PRESYNC state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which time a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 5.

Figure 5 - Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of 100.98 µs and 33.66 µs for the STS-1 and STS-3c rates, respectively.

Descrambler

The self synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the header and HCS fields and may optionally be disabled for the payload.

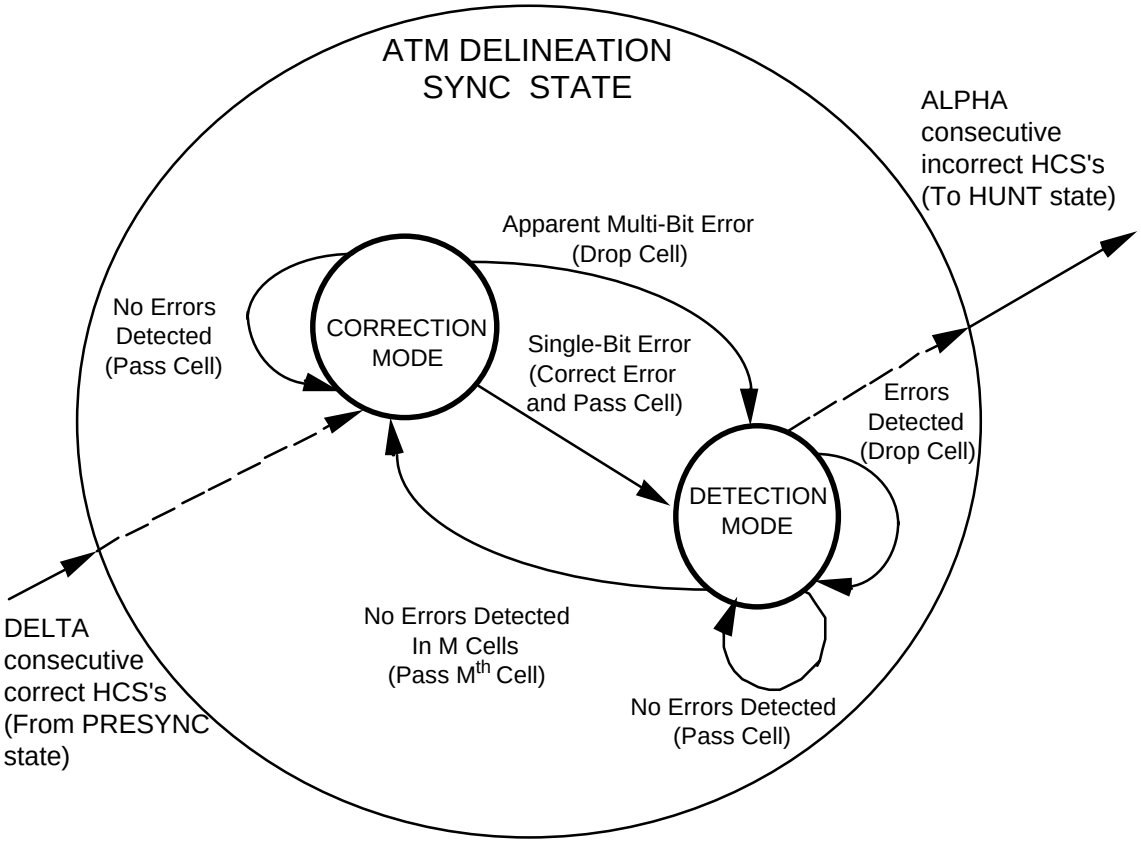
Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RACP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the

SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if uncorrectable HCS errors are detected, or if the corrected header contents match the pattern contained in the RACP Match Header Pattern and RACP Match Header Mask registers. Idle or unassigned cell filtering is accomplished by writing the appropriate cell header pattern into the RACP Match Header Pattern and RACP Match Header Mask registers. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The RACP Match Header Pattern and RACP Match Header Mask registers allow filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RACP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the received HCS octet before comparison with the calculated result. While the cell delineation state machine (described above) is in the SYNC state, the HCS verification circuit implements the state machine shown in Figure 6.

Figure 6 - HCS Verification State Diagram



In normal operation, the HCS verification state machine remains in the 'Correction Mode' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single-bit error or a multi-bit error, the state machine transitions to the 'Detection Mode' state. In this state, programmable HCS error filtering is provided. The detection of any HCS error causes the corresponding cell to be dropped. The state machine transitions back to the 'Correction Mode' state when M (where M = 1, 2, 4, 8) cells are received with correct HCSs. The Mth cell is not discarded.

Performance Monitor

The Performance Monitor consists of two 12-bit saturating HCS error event counters and a 21-bit saturating receive cell counter. One of the counters accumulates correctable HCS errors which are HCS single-bit errors detected

and corrected while the HCS Verification state machine is in the 'Correction Mode' state. The second counter accumulates uncorrectable HCS errors which are HCS bit errors detected while the HCS Verification state machine is in the 'Detection Mode' state or HCS bit errors detected but not corrected while the state machine is in the 'Correction Mode' state. The 21-bit receive cell counter counts all cells written into the receive FIFO. Filtered cells are not counted.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss HCS error events.

GFC Extraction Port

The GFC Extraction Port outputs the received GFC bits in a serial stream. The four GFC bits are presented for each received cell, with the RCP output indicating the position of the most significant bit. The updating of RGFC by particular GFC bits may be disabled through an internal register. The serial link is forced low if cell delineation is lost.

Receive FIFO

The Receive FIFO provides FIFO management and the asynchronous interface between the S/UNI-PLUS device and the external environment. The receive FIFO can accommodate four cells. The receive FIFO provides for the separation of the STS-3c/1 (STM-1) line or physical layer timing from the ATM layer timing.

The FIFO supports two data structures. The first data structure consists of twenty-seven 16-bit words comprising the five octet cell header, a cell header status octet and the forty-eight octet payload. The second data structure consists of fifty three 8-bit words comprising the five octet cell header and the forty-eight octet payload. Refer to the Operation section for more detail on these data structures.

Management functions include filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun, the FIFO is automatically reset. Up to four cells may be lost during the FIFO reset operation. Upon detection of an underrun, the offending read is ignored. FIFO overruns are indicated through a maskable

interrupt and register bit. The FIFO interface provided to the system is a synchronous interface emulating commercial synchronous FIFOs. All receive FIFO signals, RSOC, RRDENB, RCA, RXPRTY[1:0] and RDAT[15:0] are either sampled or updated on the rising edge of the RFCLK clock input.

9.9 Clock Synthesis

The transmit clock may be synthesized from a 19.44 MHz or 6.48 MHz reference. The transfer function yields a typical low pass corner of 500 kHz with a 19.44 MHz reference and 170 kHz with a 6.48 MHz reference, above which reference jitter is attenuated at 12dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free 19.44 MHz reference, the intrinsic jitter is typically less than 0.01 UI RMS when measured using a high pass filter with a 12 kHz cutoff frequency.

The TRCLK+/- reference should be within ±20 ppm to meet the SONET free-run accuracy requirements specified in GR-253-CORE.

9.10 Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts the transmit byte serial stream to a bit serial stream.

9.11 Transmit Section Overhead Processor

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion.

Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 before scrambling except for the section overhead. The Line AIS Insert Block substitutes all ones as described when enabled by the TLAIS input or through an internal register accessed through the microprocessor interface. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

BIP-8 Insert

The BIP-8 Insert Block calculates and inserts the BIP-8 error detection code (B1) into the transmit stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-3c/1 (STM-1) frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

Framing and Identity Insert

The Framing and Identity Insert Block inserts the framing bytes (A1, A2) and trace/growth bytes (J0/Z0) into the STS-3c/1 (STM-1) frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $x^7 + x^6 + 1$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

9.12 Transmit Line Overhead Processor

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion, and line BIP-24/8 insertion (B2).

APS Insert

The APS Insert Block inserts the two automatic protection switch (APS) channel bytes in the Line Overhead (K1 and K2) into the transmit stream when enabled by an internal register.

Line BIP Calculate

The Line BIP Calculate Block calculates the line BIP-24/8 error detection code (B2) based on the line overhead and synchronous payload envelope of the transmit stream. The line BIP-24/8 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-24/8 code is inserted into the B2 byte positions of the following frame.

BIP-24/8 errors may be continuously inserted under register control for diagnostic purposes.

Line RDI Insert

The Line RDI Insert Block controls the insertion of line remote defect indication. Line RDI insertion is enabled using the TLRDI input, or register control. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in the transmit stream.

Line FEBE Insert

The Line FEBE Insert Block accumulates line BIP-24/8 errors (B2) detected by the Receive Line Overhead Processor and encodes far end block error indications in the transmit Z2 byte.

9.13 Transport Overhead Insert Port

The Transport Overhead Insert Port allows the complete transport overhead to be inserted using input TTOH, along with the transport overhead clock, TTOHCLK, and the transport overhead frame position, TTOHFP. The transport overhead clock, TTOHCLK, is nominally a 5.184 MHz (STS-3c/STM-1 mode) or a 1.728 MHz (STS-1 mode) clock. The transport overhead enable signal, TTOHEN, controls the insertion of transport overhead from TTOH.

The state of the TTOHEN input determines whether the data sampled on TTOH, or the default overhead byte values (shown in Figure 7 and Figure 8) are inserted in the transmit stream. For example, when configured for STS-3c (STM-1) mode, a high level on TTOHEN during the section user channel (F1) bit positions causes the eight values shifted in the TTOH input to be inserted in the F1 byte position in the transmit stream. A low level on TTOHEN during the section user channel bit positions causes the default value (0x00) to be inserted in the transmit stream.

During the H1, H2, B1 and B2 byte positions in the TTOH stream, a high level on TTOHEN enables an error insertion mask. While the error mask is enabled, a high level on TTOH causes the corresponding bit in the H1, H2, B1 or B2 byte to be inverted. A low level on TTOH causes the corresponding bit in the H1, H2, B1 or B2 byte to be transmitted uncorrupted.

Figure 7 - STS-3c Default Transport Overhead Values

A1 (0xF6)	A1 (0xF6)	A1 (0xF6)	A2 (0x28)	A2 (0x28)	A2 (0x28)	J0 (0x01)	Z0 (0x02)	Z0 (0x03)
B1 (*)	(0x00)	(0x00)	E1 (0x00)	(0x00)	(0x00)	F1 (0x00)	(0x00)	(0x00)
D1 (0x00)	(0x00)	(0x00)	D2 (0x00)	(0x00)	(0x00)	D3 (0x00)	(0x00)	(0x00)
H1 (0x62)	H1 (0x93)	H1 (0x93)	H2 (0x0A)	H2 (0xFF)	H2 (0xFF)	H3 (0x00)	H3 (0x00)	H3 (0x00)
B2 (*)	B2 (*)	B2 (*)	K1 (0x00)	(0x00)	(0x00)	K2 (0x00)	(0x00)	(0x00)
D4 (0x00)	(0x00)	(0x00)	D5 (0x00)	(0x00)	(0x00)	D6 (0x00)	(0x00)	(0x00)
D7 (0x00)	(0x00)	(0x00)	D8 (0x00)	(0x00)	(0x00)	D9 (0x00)	(0x00)	(0x00)
D10 (0x00)	(0x00)	(0x00)	D11 (0x00)	(0x00)	(0x00)	D12 (0x00)	(0x00)	(0x00)
S1 (0x00)	Z1 (0x00)	Z1 (0x00)	Z2 (0x00)	Z2 (0x00)	M1 (*)	E2 (0x00)	(0x00)	(0x00)

*** : B1, B2 values depend on payload contents**
M1 value depends on incoming line bit errors

Figure 8 - STS-1 Default Transport Overhead Values

A1 (0xF6)	**A2 (0x28)**	**J0 (0x01)**
B1 (*)	**E1 (0x00)**	**F1 (0x00)**
D1 (0x00)	**D2 (0x00)**	**D3 (0x00)**
H1 (0x62)	**H2 (0x0A)**	**H3 (0x00)**
B2 (*)	**K1 (0x00)**	**K2 (0x00)**
D4 (0x00)	**D5 (0x00)**	**D6 (0x00)**
D7 (0x00)	**D8 (0x00)**	**D9 (0x00)**
D10 (0x00)	**D11 (0x00)**	**D12 (0x00)**
S1 (0x00)	**M0 (*)**	**E2 (0x00)**

*** : B1, B2 values depend on payload contents**
M0 value depends on incoming line bit errors

9.14 Transmit Path Overhead Processor

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion and the insertion of path level alarm signals.

Pointer Generator

The Pointer Generator Block generates the outgoing payload pointer (H1, H2) as specified in the references. The concatenation indication (the NDF field set to

1001, I-bits and D-bits set to all ones, and unused bits set to all zeros) is inserted in the second and third pointer byte locations in the transmit stream.

1. A "normal pointer value" locates the start of the SPE. Note: 0 ≤ "normal pointer value" ≤ 782, and the new data flag (NDF) field is set to 0110. Note that values greater than 782 may be inserted, using internal registers, to generate a loss of pointer alarm in downstream circuitry.

2. Arbitrary "pointer values" may be generated using internal registers. These new values may optionally be accompanied by a programmable new data flag. New data flags may also be generated independently using internal registers.

3. Positive pointer movements may be generated using a bit in an internal register. A positive pointer movement is generated by inverting the five I-bits of the pointer word. The SPE is not inserted during the positive stuff opportunity byte position, and the pointer value is incremented by one. Positive pointer movements may be inserted once per frame for diagnostic purposes.

4. Negative pointer movements may be generated using a bit in an internal register. A negative pointer movement is generated by inverting the five D-bits of the pointer word. The SPE is inserted during the negative stuff opportunity byte position , the H3 byte, and the pointer value is decremented by one. Negative pointer movements may be inserted once per frame for diagnostic purposes.

The pointer value is used to insert the path overhead into the transmit stream. The current pointer value may be read via internal registers.

BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE of the transmit stream. Details are provided in the references. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

FEBE Calculate

The FEBE Calculate Block accumulates far end block errors on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the

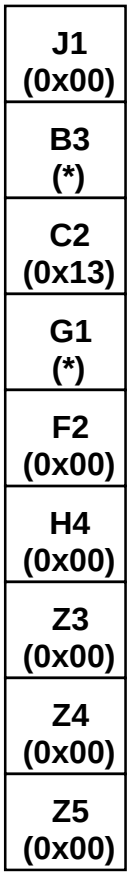
FEBE bit positions of the path status (G1) byte. The FEBE information is derived from path BIP-8 errors detected by the receive path overhead processor, RPOP. Far end block errors may be inserted under register control for diagnostic purposes.

9.15 Path Overhead Insert

The Path Overhead Insert Port allows the complete path overhead to be inserted using input TPOH, along with the path overhead clock, TPOHCLK, and the path overhead frame position, TPOHFP. The path overhead clock, TPOHCLK, is nominally a 576 kHz clock. The state of the TPOHEN input, together with an internal register, determines whether the data sampled on TPOH, or the default path overhead byte values (shown in Figure 9) are inserted in the transmit stream. For example, a high level on TPOHEN during the path signal label (C2) bit positions causes the eight values shifted in on TPOH to be inserted in the C2 byte position in the transmit stream. A low level on TPOHEN during the path signal label bit positions causes the default value (0x13) to be inserted in the transmit stream.

During the B3 byte position in the TPOH stream, a high level on TPOHEN enables an error insertion mask. While the error mask is enabled, a high level on input TPOH causes the corresponding bit in the B3 byte to be inverted. A low level on TPOH causes the corresponding bit in the B3 byte to be transmitted uncorrupted.

Figure 9 - Default Path Overhead Values



*** : B3 value depends on payload contents**
G1 value depends on incoming path bit errors

9.16 Transmit ATM Cell Processor

The Transmit ATM Cell Processor (TACP) provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. The TACP contains a four cell transmit FIFO. An idle or unassigned cell is transmitted if a complete ATM cell has not been written into the FIFO.

Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self synchronous scrambler described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be disabled.

HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

GFC Insertion Port

The GFC Insertion Port provides the ability to insert the GFC value downstream of the FIFO. The four GFC bits are received on a serial stream that is synchronized to the transmit cell by a framing pulse. The GFC enable register bits control the insertion of each serial bit. If the enable is cleared, the default GFC value is inserted. For idle/unassigned cells, the default is the contents of the TACP Idle/Unassigned Cell Header Control register. For assigned cells, the default is the value received from TDAT[15:0].

Transmit FIFO

The Transmit FIFO provides FIFO management and the synchronous interface between the S/UNI-PLUS device and the external environment. The transmit FIFO can accommodate four cells. It provides for the separation of the STS-3c/1 (STM-1) line or physical layer timing from the ATM layer timing.

The FIFO supports two data structures. The first data structure consists of twenty-seven 16-bit words comprising the five octet cell header, a cell header

error control octet and the forty-eight octet payload. The second data structure consists of fifty-three 8-bit words comprising the five octet cell header and the forty-eight octet payload. Refer to the Operation section for more detail on these data structures.

Management functions include filling the transmit FIFO, indicating when cells are available to be written to the transmit FIFO, maintaining the transmit FIFO read and write pointers, and detecting a FIFO overrun condition. The FIFO depth can be programmed to be one to four cells deep. The TCA output signal transitions low to indicate a full FIFO when the FIFO contains the same number of cells as the programmed FIFO depth. Note, a cell is not transmitted by the S/UNI-PLUS until the full cell has been written into the FIFO.

When the FIFO is full as indicated by TCA and the upstream device writes into the FIFO, the TACP indicates a FIFO overrun condition using a maskable interrupt and register bits. The offending write and all subsequent writes are ignored until there is room in the FIFO.

The FIFO interface provided to the system is a synchronous interface emulating commercial synchronous FIFOs. All transmit FIFO signals, TSOC, TWRENB, TCA, TXPRTY[1:0] and TDAT[15:0] are either sampled or updated on the rising edge of the TFCLK clock input.

9.17 SONET/SDH Section and Path Trace Buffers

The SONET/SDH Section Trace Buffer (SSTB) block and the SONET/SDH Path Trace Buffer (SPTB) block are identical. The blocks can handle both 64-byte CLLI messages in SONET and 16-byte E.164 messages in SDH. The generic SONET/SDH Trace Buffer (STB) block is described below.

9.17.1 Receive Trace Buffer (RTB)

The RTB consists of two parts: the Trace Message Receiver and the Overhead Byte Receiver.

1. Trace Message Receiver:

   The Trace Message Receiver (TMR) processes the trace message, and consists of three sub-processes: Framer, Persistency, and Compare.

   Framer:

The TMR handles the incoming 16-byte message by synchronizing to the byte with the most significant bit set high, and places that byte in the first location in the capture page of the internal RAM. In the case of the 64-byte message, the TMR synchronizes to the trailing carriage return (0x0D), line feed (0x0A) sequence and places the next byte in the first location in the capture page of the internal RAM. The Framer block maintains an internal representation of the resulting 16-byte or 64-byte "frame" cycle. If the phase of the start of frame shifts, the framer adjusts accordingly and resets the persistency counter and increments the unstable counter.

Frame synchronization may be disabled, in which case the RAM acts as a circular buffer.

Persistency:

The Persistency process checks for repeated reception of the same 16-byte or 64-byte trace message. An unstable counter is incremented for each message that differs from the previous received message. For example, a single corrupted message in a field of constant messages causes the unstable count to increment twice, once on receipt of the corrupted message, and again on the next (uncorrupted) message. A section/path trace message unstable alarm is declared when the count reaches eight.

The persistency counter is reset to zero, the unstable alarm is removed, and the trace message is accepted when the same 16-byte or 64-byte message is received three or five times consecutively (as determined by an internal register bit). The accepted message is passed to the Compare process for comparison with the expected message.

Compare:

A receive trace message mismatch alarm is declared if the accepted message (i.e. the message that passed the persistency check) does not match the expected message (previously downloaded to the receive expected page by the microprocessor). The mismatch alarm is removed if the accepted message is all-zero, or if the accepted message is identical to the expected message.

2. Overhead Byte Receiver:

   The Overhead Byte Receiver (OBR) processes the path signal label byte (C2). The OBR consists of two sub-processes: Persistency and Compare.

Persistency:

The Persistency process checks for the repeated reception of the same C2 byte. An unstable counter is incremented for each received C2 byte that differs from the byte received in the previous frame. For example, a single corrupted byte value in a sequence of constant values causes the unstable count to increment twice, once on receipt of the corrupted value, and again on the next (uncorrupted) value. A path signal label unstable alarm or a synchronization status unstable alarm is declared when either unstable counter reaches five.

The unstable counter is reset to zero, the unstable alarm is removed, and the byte value is accepted when the same label is received in five consecutive frames. The accepted value is passed to the Compare process for comparison with the expected value.

Compare:

A path signal label mismatch alarm or a synchronization status mismatch alarm is declared if the accepted C2 byte (i.e. the byte value that has passed the persistency check) does not match the expected C2 byte (previously downloaded by the microprocessor).

The OBR mismatch mechanism follows the following table:

Table 1 -

Expect	Receive	Action
00	00	Match
00	01	Mismatch
00	XX	Mismatch
01	00	Mismatch
01	01	Match
01	XX	Match
XX	00	Mismatch
XX	01	Match
XX	XX	Match
XX	YY	Mismatch

Note:

XX, YY = anything except 00H or 01H (XX not equal YY).

9.17.2 Transmit Trace Buffer (TTB)

The TTB sources the 16-byte or 64-byte trace identifier message. The TTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and inserted in the transmit stream. When the microprocessor is updating the transmit page buffer, the TTB may be programmed to transmit null characters to prevent transmission of partial messages.

9.18 Drop Side Interface

9.18.1 Receive Interface

The drop side receive interface can be accessed through a generic 19-bit wide interface. External circuitry is notified, using the RCA signal, when a cell is available in the receive FIFO. External circuitry may then read the cell from the

buffer as a word wide stream (along with a bit marking the first word of the cell) at instantaneous rates of up to 52 MHz.

The cell data structure supported is described in the Operation section.

9.18.2 Transmit Interface

The drop side transmit interface can be accessed through a generic 19-bit wide interface. External circuitry is notified using the TCA signal when a cell may be written to the transmit FIFO. The cell is written to the FIFO as a word wide stream (along with a bit marking the first word of the cell) at instantaneous rates of up to 52 MHz.

The cell data structure supported is described in the Operation section.

9.19 Parallel I/O Port

The Parallel Input/Output Port block provides four generic outputs and four generic inputs that can be used to control and monitor front end PMD devices.

9.20 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-PLUS identification code is 053470CD hexadecimal.

9.21 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-PLUS.

9.22 Register Memory Map

Address	Register
0x00	S/UNI-PLUS Master Reset and Identity / Load Performance Meters
0x01	S/UNI-PLUS Master Configuration
0x02	S/UNI-PLUS Master Interrupt Status
0x03	S/UNI-PLUS Master Control
0x04	S/UNI-PLUS Master Auto Alarm/Monitor
0x05	S/UNI-PLUS Clock Synthesis Control and Status
0x06	S/UNI-PLUS Clock Recovery Control and Status
0x07	S/UNI-PLUS Parallel I/O Port
0x08	S/UNI-PLUS Parallel Input Port Interrupt
0x09	S/UNI-PLUS Parallel Input Port Enable
0x0A	S/UNI-PLUS Transmit J0/Z0
0x0B	S/UNI-PLUS APS Control/Status
0x0C	S/UNI-PLUS Receive K1
0x0D	S/UNI-PLUS Receive K2
0x0E	S/UNI-PLUS Receive S1
0x0F	S/UNI-PLUS Transmit S1
0x10	RSOP Control/Interrupt Enable
0x11	RSOP Status/Interrupt Status
0x12	RSOP Section BIP-8 LSB
0x13	RSOP Section BIP-8 MSB
0x14	TSOP Control
0x15	TSOP Diagnostic
0x16-0x17	TSOP Reserved
0x18	RLOP Control/Status
0x19	RLOP Interrupt Enable/Interrupt Status

Address	Register
0x1A	RLOP Line BIP-24/8 LSB
0x1B	RLOP Line BIP-24/8
0x1C	RLOP Line BIP-24/8 MSB
0x1D	RLOP Line FEBE LSB
0x1E	RLOP Line FEBE
0x1F	RLOP Line FEBE MSB
0x20	TLOP Control
0x21	TLOP Diagnostic
0x22	TLOP Transmit K1
0x23	TLOP Transmit K2
0x24-0x27	Reserved
0x28	SSTB Control
0x29	SSTB Status
0x2A	SSTB Indirect Address
0x2B	SSTB Indirect Data
0x2C	SSTB Reserved
0x2D	SSTB Reserved
0x2E-0x2F	SSTB Reserved
0x30	RPOP Status/Control
0x31	RPOP Interrupt Status
0x32	RPOP Pointer Interrupt Status
0x33	RPOP Interrupt Enable
0x34	RPOP Pointer Interrupt Enable
0x35	RPOP Pointer LSB
0x36	RPOP Pointer MSB and RDI Filter Control
0x37	RPOP Path Signal Label
0x38	RPOP Path BIP-8 LSB

Address	Register
0x39	RPOP Path BIP-8 MSB
0x3A	RPOP Path FEBE LSB
0x3B	RPOP Path FEBE MSB
0x3C	RPOP Auxiliary RDI
0x3D	RPOP Error Event Control
0x3E-0x3F	RPOP Reserved
0x40	TPOP Control/Diagnostic
0x41	TPOP Pointer Control
0x42	TPOP Reserved
0x43	TPOP Current Pointer LSB
0x44	TPOP Current Pointer MSB
0x45	TPOP Arbitrary Pointer LSB
0x46	TPOP Arbitrary Pointer MSB
0x47	TPOP Path Trace
0x48	TPOP Path Signal Label
0x49	TPOP Path Status
0x4A	TPOP Path User Channel
0x4B	TPOP Path Growth #1 (Z3)
0x4C	TPOP Path Growth #2 (Z4)
0x4D	TPOP Path Growth #3 (Z5)
0x4E-0x4F	TPOP Reserved
0x50	RACP Control
0x51	RACP Interrupt Status
0x52	RACP Interrupt Enable/Control
0x53	RACP Match Header Pattern
0x54	RACP Match Header Mask
0x55	RACP Correctable HCS Error Count (LSB)

Address	Register
0x56	RACP Correctable HCS Error Count (MSB)
0x57	RACP Uncorrectable HCS Error Count (LSB)
0x58	RACP Uncorrectable HCS Error Count (MSB)
0x59	RACP Receive Cell Counter (LSB)
0x5A	RACP Receive Cell Counter
0x5B	RACP Receive Cell Counter (MSB)
0x5C	RACP GFC Control
0x5D-0x5F	RACP Reserved
0x60	TACP Control/Status
0x61	TACP Idle/Unassigned Cell Header Pattern
0x62	TACP Idle/Unassigned Cell Payload Octet Pattern
0x63	TACP FIFO Control
0x64	TACP Transmit Cell Counter (LSB)
0x65	TACP Transmit Cell Counter
0x66	TACP Transmit Cell Counter (MSB)
0x67	TACP Fixed Stuff / GFC
0x68	SPTB Control
0x69	SPTB Status
0x6A	SPTB Indirect Address
0x6B	SPTB Indirect Data
0x6C	SPTB Expected Path Signal Label
0x6D	SPTB Path Signal Label Status
0x6E-0x6F	SPTB Reserved
0x70	BERM Control
0x71	BERM Interrupt
0x72	BERM Line BIP Accumulation Period LSB
0x73	BERM Line BIP Accumulation Period MSB

Address	Register
0x74	BERM Line BIP Threshold LSB
0x75	BERM Line BIP Threshold MSB
0x76-0x7F	Reserved
0x80	S/UNI Master Test
0x81-0xFF	Reserved for Test

For all register accesses, CSB must be low.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-PLUS. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[7]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-PLUS to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-PLUS operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-PLUS operates as intended, reserved register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

Register 0x00: S/UNI-PLUS Master Reset and Identity / Load Performance Meters

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[2]	1
Bit 5	R	TYPE[1]	0
Bit 4	R	TYPE[0]	0
Bit 3	R	TIP	X
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

This register allows the revision of the S/UNI-PLUS to be read by software permitting graceful migration to newer, feature enhanced versions of the S/UNI-PLUS.

ID[2:0]:

The ID bits can be read to provide a binary S/UNI-PLUS revision number.

TIP:

The TIP bit is set to a logic one when any value is written to this register. Such a write initiates an accumulation interval transfer and loads all the performance meter registers in the RSOP, RLOP, RPOP, RACP, and TACP blocks. TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

TYPE[2:0]:

The TYPE bits can be read to distinguish the S/UNI-PLUS from the other members of the S/UNI family of devices.

RESET:

The RESET bit allows the S/UNI-PLUS to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-PLUS is held in reset. This bit is not self-clearing; therefore, a logic zero must be written to bring the

S/UNI-PLUS out of reset. Holding the S/UNI-PLUS in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise the effect of a software reset is equivalent to that of a hardware reset.

Register 0x01: S/UNI-PLUS Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	TPTBEN	0
Bit 6	R/W	TSTBEN	0
Bit 5	R/W	SDH_J0/Z0	0
Bit 4	R/W	FIXPTR	1
Bit 3	R/W	TRATE[1]	1
Bit 2	R/W	TRATE[0]	1
Bit 1	R/W	RRATE[1]	1
Bit 0	R/W	RRATE[0]	1

RRATE[1:0]:

The RRATE[1:0] bits select the operation rate of the S/UNI-PLUS's receive side. The default configuration selects STS-3c rate operation. The S/UNI-PLUS will not operate correctly if a Reserved mode is selected.

RRATE[1:0]	MODE
00	Reserved
01	Reserved
10	51.84 Mbit/s, STS-1
11	155.52 Mbit/s, STS-3c/STM-1

TRATE[1:0]:

The TRATE[1:0] bits select the operation rate of the S/UNI-PLUS's transmit side. The default configuration selects STS-3c rate operation. The S/UNI-PLUS will not operate correctly if a Reserved mode is selected.

TRATE[1:0]	MODE
00	Reserved
01	Reserved

TRATE[1:0]	MODE
10	51.84 Mbit/s, STS-1
11	155.52 Mbit/s, STS-3c/STM-1

FIXPTR:

The FIXPTR bit disables transmit payload pointer adjustments. If the FIXPTR bit is a logic one, the transmit payload pointer is set at 522. If FIXPTR is a logic zero, the payload pointer is controlled by the contents of the TPOP Pointer Control register.

SDH_J0/Z0

The SDH_J0/Z0 bit selects whether to insert SONET or SDH formatted section overhead bytes into the transmit stream. When SDH_J0/Z0 is a logic one, SDH format section overhead bytes are selected for insertion. For this case, the J0 byte (in STS-1) or the J0/Z0 bytes (in STS-3c) in the transmitted signal are forced to the value programmed in the S/UNI-PLUS Transmit J0/Z0 register. When SDH_J0/Z0 is a logic zero, SONET formatted section overhead bytes are selected for insertion. For this case, the J0/Z0 bytes of the transmitted STS-N signal are numbered incrementally from 1 to N (i.e., the J0 byte will be set to 0x01, the first Z0 will be set to 0x02, the second Z0 will be set to 0x03, etc.).

Note, for both cases, the transmit section trace buffer enable bit, TSTBEN can be used to overwrite the J0 byte of the transmitted STS-3c/1 (STM-1) signal.

TSTBEN

The TSTBEN bit controls whether the section trace message stored in the SSTB block is inserted into the transmit stream (i.e. the J0 byte). When TSTBEN is a logic one, the message stored in the SSTB is inserted into the transmit stream. When TSTBEN is a logic zero, the section trace message is supplied by the TSOP block or via the TTOH input.

TPTBEN

The TPTBEN bit controls whether the path trace message stored in the SPTB block is inserted into the transmit stream (i.e. the J1 byte). When TPTBEN is a logic one, the message stored in the SPTB is inserted into the transmit stream. When TPTBEN is a logic zero, the path trace message is supplied by the TPOP block or via the TPOH input.

Register 0x02: S/UNI-PLUS Master Interrupt Status

Bit	Type	Function	Default
Bit 7	R	MISCI	X
Bit 6	R	SSTBI	X
Bit 5	R	SPTBI	X
Bit 4	R	TACPI	X
Bit 3	R	RACPI	X
Bit 2	R	RPOPI	X
Bit 1	R	RLOPI	X
Bit 0	R	RSOPI	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOPI:

The RSOPI bit is a logic one when an interrupt request is active from the RSOP block. The RSOP interrupt sources are enabled in the RSOP Control/Interrupt Enable Register.

RLOPI:

The RLOPI bit is a logic one when an interrupt request is active from the RLOP block. The RLOP interrupt sources are enabled in the RLOP Interrupt Enable/Status Register.

RPOPI:

The RPOPI bit is a logic one when an interrupt request is active from the RPOP block. The RPOP interrupt sources are enabled in the RPOP Interrupt Enable Register.

RACPI:

The RACPI bit is a logic one when an interrupt request is active from the RACP block. The RACP interrupt sources are enabled in the RACP Interrupt Enable/Status Register.

TACPI:

The TACPI bit is a logic one when an interrupt request is active from the TACP block. The TACP interrupt sources are enabled in the TACP Interrupt Control/Status Register.

SPTBI:

The SPTBI bit is a logic one when an interrupt request is active from the SPTB block. The SPTB interrupt sources are enabled in the SPTB Control Register and the SPTB Path Signal Label Status Register.

SSTBI:

The SSTBI bit is a logic one when an interrupt request is active from the SSTB block. The SSTB interrupt sources are enabled in the SSTB Control Register and the SSTB Synchronization Message Status Register.

MISCI:

The MISCI bit is a logic one when an interrupt request is active from the Parallel Input/Output block, the S1 Change Block, the Clock Synthesis Block, the Clock Recovery Block, the BERM block or the APS Block. The Parallel Input/Output interrupt sources are enabled in the S/UNI-PLUS Parallel Input Port Enable Register. The S1 Change interrupt and the APS interrupt sources are enabled in the S/UNI-PLUS APS Control/Status Register. The Clock Synthesis interrupt soure is enabled in the S/UNI-PLUS Clock Synthesis Control and Status Register. The Clock Recovery interrupt soure is enabled in the S/UNI-PLUS Clock Recovery Control and Status Register. The BERM interrupt source is enabled in the BERM Control Register.

Register 0x03: S/UNI-PLUS Master Control

Bit	Type	Function	Default
Bit 7	R/W	TCAINV	0
Bit 6	R/W	RCAINV	0
Bit 5	R/W	RXDINV	0
Bit 4	R/W	LLE	0
Bit 3	R/W	SDLE	0
Bit 2	R/W	PDLE	0
Bit 1	R/W	TTIME[1]	0
Bit 0	R/W	TTIME[0]	0

This register provides polarity control for outputs RCA and TCA, loopback control and transmit timing control.

TTIME[1:0]:

The TTIME[1:0] bits select the timing source for the transmit section of the S/UNI-PLUS.

TTIME[1:0]	TIMING SOURCE
00	TRCLK+ and TRCLK-
01	RRCLK+ and RRCLK-
10	Loop Timing
11	Loop Timing

When Loop Timing is enabled, the transmitter timing is derived from the receiver inputs RXD+ and RXD- when clock recovery is enabled and from RRCLK+ and RRCLK- when clock recovery is disabled.

PDLE:

The PDLE bit enables the parallel diagnostic loopback. When PDLE is a logic one, the transmit parallel stream is connected to the receive stream. The loopback point is between the TPOP and the RPOP blocks. Blocks upstream

of the loopback point continue to operate normally. For example line AIS may be inserted in the transmit stream upstream of the loopback point using the TSOP Control register.

SDLE:

The SDLE bit enables the serial diagnostic loopback. When SDLE is a logic one, the transmit serial stream is connected to the receive stream. The SDLE and the LLE bits should not be set high simultaneously.

LLE:

The LLE bit enables the S/UNI-PLUS line loopback. When LLE is a logic one, RXD+ and RXD- are connected internally to TXD+ and TXD- respectively. The SDLE and the LLE bits should not be set high simultaneously.

RXDINV:

The RXDINV bits select the polarity of the RXD+/- signals. The default configuration selects RXD+ (RXD-) to be high (low) when the receive stream contains a logic one. When RXDINV is a logic one, RXD+/- is inverted; RXD+(RXD-) is low (high) when the receive stream contains a logic one.

RCAINV:

The RCAINV bits select the active polarity of the RCA signal. The default configuration selects RCA to be active high, indicating that a received cell is available when high. When RCAINV is a logic one, the RCA signal becomes active low.

TCAINV:

The TCAINV bits select the active polarity of the TCA signal. The default configuration selects TCA to be active high, indicating that a cell is available in the transmit FIFO when high. When TCAINV is a logic one, the TCA signal becomes active low.

Register 0x04: S/UNI-PLUS Master Auto Alarm/Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFCLKA	X
Bit 5	R	TFCLKA	X
Bit 4	R	RRCLKA	X
Bit 3	R	TRCLKA	X
Bit 2	R/W	AUTOFEBE	1
Bit 1	R/W	AUTOLRDI	1
Bit 0	R/W	AUTOPRDI	1

AUTOPRDI

The AUTOPRDI bit determines whether the path remote defect indication is sent immediately upon detection of an incoming alarm. When AUTOPRDI is a logic one, the path remote defect indication is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF), line AIS (LAIS), loss of pointer (LOP), or STS path AIS (PAIS).

AUTOLRDI

The AUTOLRDI bit determines whether line remote defect indication (LRDI) is sent immediately upon detection of an incoming alarm. When AUTOLRDI is a logic one, line RDI is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF), or line AIS (LAIS).

AUTOFEBE

The AUTOFEBE bit determines whether line and path far end block errors are sent upon detection of an incoming line and path BIP error events. When AUTOFEBE is a logic one, one line or path FEBE is inserted for each line or path BIP error event. When AUTOFEBE is a logic zero, incoming line or path BIP error events do not generate FEBE events.

TRCLKA:

The TRCLK active bit monitors for low to high transitions on the TRCLK+ and TRCLK- inputs. TRCLKA is set high on a rising edge of TRCLK+/-, and is set low when this register is read.

TTCLKA:

The TTCLK active bit monitors for low to high transitions on the TTCLK+ and TTCLK- inputs. TTCLKA is set high on a rising edge of TTCLK+/-, and is set low when this register is read.

TFCLKA:

The TFCLK active bit monitors for low to high transitions on the TFCLK input. TFCLKA is set high on a rising edge of TFCLK, and is set low when this register is read.

RFCLKA:

The RFCLK active bit monitors for low to high transitions on the RFCLK input. RFCLKA is set high on a rising edge of RFCLK, and is set low when this register is read.

Register 0x05: S/UNI-PLUS Clock Synthesis Control and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	TROOLV	X
Bit 2	R	TROOLI	X
Bit 1	R/W	TROOLE	0
Bit 0	R/W	TREFSEL	0

This register controls the clock synthesis and reports the state of the transmit phase locked loop.

TREFSEL:

The transmit reference select (TREFSEL) bit determines the expected frequency of TRCLK+/- to synthesize the line clock frequency. If TREFSEL is a logic zero, the reference frequency must be 19.44 MHz. If TREFSEL is a logic one, the reference frequency must be 6.48 MHz. TREFSEL only has effect if the TBYP input is low.

TROOLE:

The TROOLE bit is an interrupt enable for the transmit reference out of lock status. When TROOLE is a logic one, an interrupt is generated when the TROOLV bit changes state.

TROOLI:

The TROOLI bit is the transmit reference out of lock interrupt status bit. TROOLI is a logic one when the TROOLV bit changes state. TROOLI is cleared when this register is read.

TROOLV:

The transmit reference out of lock status indicates the clock synthesis phase locked loop is unable to lock to the reference. TROOLV is a logic one if the

divided down synthesized clock frequency not within 488 ppm of the transmit reference frequency.

Register 0x06: S/UNI-PLUS Clock Recovery Control and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	RROOLV	X
Bit 3	R	RDOOLV	X
Bit 2	R	RDOOLI	X
Bit 1	R/W	RDOOLE	0
Bit 0	R/W	RREFSEL	0

This register controls the clock recovery and reports the state of the receive phase locked loop.

RREFSEL:

The receive reference select (RREFSEL) bit determines the expected frequency of RRCLK+/-. If RREFSEL is a logic zero, the reference frequency is 19.44 MHz. If RREFSEL is a logic one, the reference frequency must be 6.48 MHz. RREFSEL only has effect if the RBYP input is low.

RDOOLE:

The RDOOLE bit is an interrupt enable for the receive data out of lock status. When RDOOLE is a logic one, an interrupt is generated when the RDOOLV bit changes state.

RDOOLI:

The RDOOLI bit is the receive data out of lock interrupt status bit. RDOOLI is a logic one when the RDOOLV bit changes state. RDOOLI is cleared when this register is read.

RDOOLV:

The receive data out of lock status indicates the clock recovery phase locked loop is unable to lock to the receive stream. RDOOLV is a logic one if the divided down recovered clock frequency not within 488 ppm of the RRCLK+/-

frequency or if no transitions have occurred on the RXD+/- inputs for more than 80 bit periods.

RROOLV:

The receive reference out of lock status indicates the clock recovery phase locked loop is unable to lock to the receive reference (RRCLK+/-). RROOLV should be polled after a power up reset to determine when the CRU PLL is operational. When RROOLV is a logic 1, the CRU is unable to lock to the receive reference. When RROOLV is a logic 0, the CRU is locked to the receive reference. The RROOLV bit may remain set at logic 1 for several hundred milliseconds after the removal of the power on reset as the CRU PLL locks to the receive reference clock.

Register 0x07: S/UNI-PLUS Parallel I/O Port

Bit	Type	Function	Default
Bit 7	R/W	POP[3]	1
Bit 6	R/W	POP[2]	1
Bit 5	R/W	POP[1]	0
Bit 4	R/W	POP[0]	0
Bit 3	R	PIPV[3]	X
Bit 2	R	PIPV[2]	X
Bit 1	R	PIPV[1]	X
Bit 0	R	PIPV[0]	X

PIPV[3:0]:

The PIPV[3:0] bits are real-time input port state indications. A logic one in any bit location indicates that the signal on the corresponding PIP[3:0] input is a logic one. A logic zero in any bit location indicates that the signal on the corresponding PIP[3:0] input is a logic zero.

POP[3:0]:

The values written to the POP[3:0] bit in the S/UNI-PLUS Parallel Output Port register directly correspond to the states set on the POP[3:0] output pins. This provides a generic port useful for controlling an external PMD device. The default states for this port are chosen so that POP[3:2] controls active high signals while POP[1:0] controls active low signals.

Register 0x08: S/UNI-PLUS Parallel Input Port Interrupt

Bit	Type	Function	Default
Bit 7	R	PIPI[7]	X
Bit 6	R	PIPI[6]	X
Bit 5	R	PIPI[5]	X
Bit 4	R	PIPI[4]	X
Bit 3	R	PIPI[3]	X
Bit 2	R	PIPI[2]	X
Bit 1	R	PIPI[1]	X
Bit 0	R	PIPI[0]	X

PIPI[7:0]:

The PIPI[7:0] bits are interrupt indications. A logic one in any bit location indicates that an event has occurred on the corresponding PIP[3:0] input. More specifically, a logic one in any of the PIPI[7:4] bit locations indicates that the signal on the corresponding PIP[3:0] input has transitioned from logic zero to logic one (i.e. upon detection of a rising edge); a logic one in any of the PIPI[3:0] bit locations indicates that the signal on the corresponding PIP[3:0] input has transitioned either from logic zero to logic one or from logic one to logic zero (i.e. upon a change of state). The PIPI[7:0] bits are cleared by reading this register.

These register bits function independently from the S/UNI-PLUS Parallel Input Port Enable register bits. The PIPI[7:0] bits will indicate events occurring on the PIP[3:0] inputs regardless of whether or not these events are enabled to generate an interrupt. It is intended that the PIP[3:0] inputs monitor the status of an external PMD device.

Register 0x09: S/UNI-PLUS Parallel Input Port Enable

Bit	Type	Function	Default
Bit 7	R/W	PIPE[7]	0
Bit 6	R/W	PIPE[6]	0
Bit 5	R/W	PIPE[5]	0
Bit 4	R/W	PIPE[4]	0
Bit 3	R/W	PIPE[3]	0
Bit 2	R/W	PIPE[2]	0
Bit 1	R/W	PIPE[1]	0
Bit 0	R/W	PIPE[0]	0

PIPE[7:0]:

The PIPE[7:0] bits are interrupt enables. When a logic one is written to these locations, the occurrence of an event on the corresponding PIP[7:0] input activates the interrupt, INTB. The interrupt is cleared by reading the S/UNI-PLUS Parallel Input Port Interrupt Register. When a logic zero is written to these locations, the occurrence of an event on the corresponding PIP[7:0] input is inhibited from activating the interrupt.

Register 0x0A: S/UNI-PLUS Transmit J0/Z0

Bit	Type	Function	Default
Bit 7	R/W	J0/Z0[7]	1
Bit 6	R/W	J0/Z0[6]	1
Bit 5	R/W	J0/Z0[5]	0
Bit 4	R/W	J0/Z0[4]	0
Bit 3	R/W	J0/Z0[3]	1
Bit 2	R/W	J0/Z0[2]	1
Bit 1	R/W	J0/Z0[1]	0
Bit 0	R/W	J0/Z0[0]	0

J0/Z0[7:0]:

The value written to these bit positions is inserted into the J0/Z0 byte positions of the transmit stream when enabled using the SDH_J0/Z0 bit in the S/UNI-PLUS Master Configuration register. J0/Z0[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. J0/Z0[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted.

Register 0x0B: S/UNI-PLUS APS Control/Status

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	S1E	0
Bit 4	R	S1I	X
Bit 3	R	PSBFI	X
Bit 2	R	COAPSI	X
Bit 1		Unused	X
Bit 0	R	PSBFV	X

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state. The alarm is declared (PSBFV is a logic one) when twelve successive frames have been received where no three consecutive frames contain identical K1 bytes. The alarm is removed (PSBFV is a logic zero) when three consecutive frames containing identical K1 bytes have been received.

COAPSI:

The COAPSI bit is a logic one when a new APS code value has been extracted into the S/UNI-PLUS Receive K1/K2 Registers. The registers are updated when the same new K1/K2 byte values are observed for three consecutive frames. This bit is cleared when the S/UNI-PLUS APS Control/Status Register is read.

PSBFI:

The PSBFI bit is a logic one when the protection switching byte failure alarm is declared or removed. This bit is cleared when the S/UNI-PLUS APS Control/Status Register is read.

S1I:

The S1I bit is a logic one when a new S1 byte value has been extracted into the S/UNI-PLUS Receive S1 Register. The register is updated when a S1 byte value is extracted that is different than the S1 byte value extracted in the

previous frame. This bit is cleared when the S/UNI-PLUS APS Control/Status Register is read.

S1E:

The change of S1 interrupt enable is an interrupt mask for changes in the receive S1 byte value. When S1E is a logic one, an interrupt is generated when the extracted S1 byte is different from the S1 byte extracted in the previous frame.

COAPSE:

The change of APS byte interrupt enable is an interrupt mask for events detected by the receive APS processor. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value has been extracted into the S/UNI-PLUS Receive K1/K2 Registers.

PSBFE:

The change of protection switch byte failure alarm interrupt enable is an interrupt mask for events detected by the receive APS processor. When PSBFE is a logic one, an interrupt is generated upon a change in the protection switch byte failure alarm state.

Register 0x0C: S/UNI-PLUS Receive K1

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the S/UNI-PLUS APS Control Register). K1[7] is the most significant bit, corresponding to the first bit (bit 1) received. K1[0] is the least significant bit, corresponding to the last bit (bit 8) received.

Register 0x0D: S/UNI-PLUS Receive K2

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the S/UNI-PLUS APS Control Register). K2[7] is the most significant bit, corresponding to the first bit (bit 1) received. K2[0] is the least significant bit, corresponding to the last bit (bit 8) received.

Register 0x0E: S/UNI-PLUS Receive S1

Bit	Type	Function	Default
Bit 7	R	S1[7]	X
Bit 6	R	S1[6]	X
Bit 5	R	S1[5]	X
Bit 4	R	S1[4]	X
Bit 3	R	S1[3]	X
Bit 2	R	S1[2]	X
Bit 1	R	S1[1]	X
Bit 0	R	S1[0]	X

S1[7:0]:

The first S1 byte contained in the receive stream is extracted into this register. The S1 byte is used to carry synchronization status messages between line terminating network elements. S1[7] is the most significant bit, corresponding to the first bit (bit 1) received. S1[0] is the least significant bit, corresponding to the last bit (bit 8) received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame using the S1E bit in the APS Control/Status Register.

Register 0x0F: S/UNI-PLUS Transmit S1

Bit	Type	Function	Default
Bit 7	R/W	S1[7]	0
Bit 6	R/W	S1[6]	0
Bit 5	R/W	S1[5]	0
Bit 4	R/W	S1[4]	0
Bit 3	R/W	S1[3]	0
Bit 2	R/W	S1[2]	0
Bit 1	R/W	S1[1]	0
Bit 0	R/W	S1[0]	0

S1[7:0]:

The value written to these bit positions is inserted in the first S1 byte position of the transmit stream. The S1 byte is used to carry synchronization status messages between line terminating network elements. S1[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. S1[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted.

Register 0x10: RSOP Control/Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	FPSEL	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable for the out of frame alarm. When OOFE is set to logic one, an interrupt is generated when the out of frame alarm changes state.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is a logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is a logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is a logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

FPSEL:

The FPSEL bit selects the framing pattern used for in-frame validation, and out-of-frame declaration. When FPSEL is a logic one, the framing pattern

consists of the first A1 byte, and the first four bits of the first A2 byte (12 bits total). In the presence of a 10^{-3} bit error rate, the mean time between OOF declarations is 103 minutes for both STS-1 and STS-3c/STM-1 rates.

When FPSEL is a logic zero, the framing pattern consists of all the A1 bytes and all the A2 bytes (48 bits for STS-3c/STM-1 and 16 bits for STS-1). In the presence of a 10^{-3} bit error rate, the mean time between OOF declarations is 26 seconds for STS-3c/STM-1, and 33 minutes for STS-1.

FOOF:

The FOOF bit controls the framing of the RSOP. When a logic one is written to FOOF, the RSOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit, register reads may yield a logic one or a logic zero.

DDS:

The DDS bit enables the frame synchronous descrambling of the receive stream. When DDS is a logic one, descrambling is disabled. When DDS is a logic zero, descrambling is enabled.

BIPWORD:

The BIPWORD bit controls the accumulation of B1 block errors. When BIPWORD is a logic one, one or more B1 errors per frame result in a single error accumulated in the B1 error counter. When BIPWORD is a logic zero, each B1 error is accumulated in the B1 error counter.

Register 0x11: RSOP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is read to determine the out of frame state. When OOFV is a logic one, the S/UNI-PLUS is out-of-frame. When OOFV is a logic zero, the S/UNI-PLUS is in-frame.

LOFV:

The LOFV bit is read to determine the loss of frame state. When LOFV is a logic one, the S/UNI-PLUS has declared loss of frame.

LOSV:

The LOSV bit is read to determine the loss of signal state. When LOSV is a logic one, the S/UNI-PLUS has declared loss of signal.

OOFI:

The OOFI bit is the out-of-frame interrupt status bit. OOFI is a logic one when a change in the out-of-frame state occurs. This bit is cleared when this register is read.

LOFI:

The LOFI bit is the loss of frame interrupt status bit. LOFI is a logic one when a change in the loss of frame state occurs. This bit is cleared when this register is read.

LOSI:

The LOSI bit is the loss of signal interrupt status bit. LOSI is a logic one when a change in the loss of signal state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is a logic one when a B1 error is detected. This bit is cleared when this register is read.

Register 0x12: RSOP Section BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0x13: RSOP Section BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:

SBE[15:0] represent the number of B1 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RSOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 2 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-PLUS Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x14: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (LAIS). When LAIS is a logic one, the TSOP inserts AIS into the transmit stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bytes of the SONET frame being set to 0xFF prior to scrambling except for the section overhead. The LAIS bit is logically ORed with the external TLAIS input.

DS:

The DS bit enables the frame synchronous scrambling of the transmit stream. When DS is a logic one, scrambling is disabled. When DS is a logic zero, scrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x15: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 7		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is a logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the B1 byte. When DBIP8 is a logic one, the B1 byte is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the transmit stream. When DLOS is a logic one, the transmit stream is forced to 0x00.

Register 0x18: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	ALLONES	0
Bit 5	R/W	AISDET	0
Bit 4	R/W	LRDIDET	0
Bit 3	R/W	FEBEGEN	0
Bit 2		Unused	X
Bit 1	R	LAISV	X
Bit 0	R	LRDIV	X

LRDIV:

The LRDIV bit is read to determine the remote defect indication state. When LRDIV is a logic one, the S/UNI-PLUS has declared line RDI.

LAISV:

The LAISV bit is read to determine the line AIS state. When LAISV is a logic one, the S/UNI-PLUS has declared line AIS.

FEBEGEN:

The FEBEGEN bit controls the indication of B2 errors reported to the TLOP block for insertion as FEBEs. When FEBEGEN is a logic one, a single FEBE is indicated each frame whenever one or more B2 errors occur during that frame. When FEBEGEN is a logic zero, a single FEBE is indicated for each B2 bit error that occurs during that frame (maximum of 24 FEBEs per frame for STS-3c/STM-1). The accumulation of B2 error events functions independently and is controlled by the BIPWORD register bit.

LRDIDET:

The LRDIDET bit determines the line RDI alarm detection algorithm. When LRDIDET is a logic one, line RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When LRDIDET is a logic zero, line RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

AISDET:

The AISDET bit determines the line AIS alarm detection algorithm. When AISDET is a logic one, line AIS is declared when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When AISDET is a logic zero, line AIS is declared when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

ALLONES:

The ALLONES bit controls the conditioning that occurs whenever line AIS is detected in the recovered data. When ALLONES is a logic one, the recovered data is forced to logic one immediately when the line AIS alarm is detected. When line AIS is removed, the recovered data is passed unconditioned. When ALLONES is a logic zero, recovered data conditioning is disabled regardless of the state of the line AIS alarm.

BIPWORD:

The BIPWORD bit controls the accumulation of B2 block errors. When BIPWORD is a logic one, one or more B2 errors per frame result in a single error accumulated in the B2 error counter. When BIPWORD is a logic zero, each B2 error is accumulated in the B2 error counter.

Register 0x19: RLOP Interrupt Enable/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	FEBEE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	LRDIE	0
Bit 3	R	FEBEI	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	LRDII	X

LRDII:

The LRDII bit is the line remote defect indication interrupt status bit. LRDII is a logic one when a change in the line RDI state occurs. This bit is cleared when this register is read.

LAISI:

The LAISI bit is the line AIS interrupt status bit. LAISI is a logic one when a change in the line AIS state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the line BIP-24/8 interrupt status bit. BIPEI is a logic one when a B2 error is detected. This bit is cleared when this register is read.

FEBEI:

The FEBEI bit is the line far end block error interrupt status bit. FEBEI is a logic one when a line layer FEBE (M0/M1) is detected. This bit is cleared when this register is read.

LRDIE:

The LRDIE bit is an interrupt enable for the line remote defect indication alarm. When LRDIE is a logic one, an interrupt is generated when the line RDI state changes.

LAISE:

The LAISE bit is an interrupt enable for line AIS. When LAISE is a logic one, an interrupt is generated when line AIS changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the line BIP-24/8 errors. When BIPEE is a logic one, an interrupt is generated when a B2 error is detected.

FEBEE:

The FEBEE bit is an interrupt enable for the line far end block errors. When FEBEE is a logic one, an interrupt is generated when a FEBE is detected.

Register 0x1A: RLOP Line BIP-24/8 LSB

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Register 0x1B: RLOP Line BIP-24/8

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Register 0x1C: RLOP Line BIP-24/8 MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]

Bits LBE[19:0] represent the number of line BIP-24/8 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-24/8 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line BIP-24/8 Registers within approximately 2 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-PLUS Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x1D: RLOP Line FEBE LSB

Bit	Type	Function	Default
Bit 7	R	LFE[7]	X
Bit 6	R	LFE[6]	X
Bit 5	R	LFE[5]	X
Bit 4	R	LFE[4]	X
Bit 3	R	LFE[3]	X
Bit 2	R	LFE[2]	X
Bit 1	R	LFE[1]	X
Bit 0	R	LFE[0]	X

Register 0x1E: RLOP Line FEBE

Bit	Type	Function	Default
Bit 7	R	LFE[15]	X
Bit 6	R	LFE[14]	X
Bit 5	R	LFE[13]	X
Bit 4	R	LFE[12]	X
Bit 3	R	LFE[11]	X
Bit 2	R	LFE[10]	X
Bit 1	R	LFE[9]	X
Bit 0	R	LFE[8]	X

Register 0x1F: RLOP Line FEBE MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LFE[19]	X
Bit 2	R	LFE[18]	X
Bit 1	R	LFE[17]	X
Bit 0	R	LFE[16]	X

LFE[19:0]

Bits LFE[19:0] represent the number of line FEBE errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-24/8 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line FEBE Registers within approximately 2 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-PLUS Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x20: TLOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LRDI	0

LRDI:

The LRDI bit controls the insertion of line remote defect indication (LRDI). When LRDI is a logic one, the S/UNI-PLUS inserts line RDI into the transmit stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7, and 8 of the K2 byte of the transmit stream. The LRDI bit is logically ORed with the external TLRDI input.

APSREG:

The APSREG bit selects the source for the transmit APS channel. When APSREG is a logic zero, 0x0000 hexadecimal is inserted in the transmit APS channel. When APSREG is a logic one, the transmit APS channel is inserted from the TLOP Transmit K1 Register and the TLOP Transmit K2 Register. The APS bytes may also be inserted using the TTOHEN and TTOH inputs. Values inserted using the TTOHEN input take precedence over the source selected by the APSREG bit.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x21: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DBIP24/8	0

DBIP24/8:

The DBIP24/8 bit controls the insertion of bit errors continuously in the B2 byte(s). When DBIP24/8 is a logic one, the B2 byte(s) are inverted.

Register 0x22: TLOP Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]:

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control Register is a logic one. K1[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. K1[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the TLOP Transmit K2 Register are inserted in the transmit stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Register 0x23: TLOP Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]:

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register is a logic one. K2[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. K2[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the TLOP Transmit K1 Register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing the TLOP Transmit K1 Register.

Register 0x28: SSTB Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SSTB.

LEN16:

The LEN16 bit selects the length of the section trace message to be 16 bytes or 64 bytes. When LEN16 is a logic one, a 16 byte section trace message is selected. When LEN16 is a logic zero, a 64 byte section trace message is selected.

NOSYNC:

The NOSYNC bit disables the writing of the section trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is a logic one and NOSYNC is a logic zero, the receive section trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 and NOSYNC are logic zero, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is a logic one, synchronization is disabled, and the section trace message buffer behaves as a circular buffer.

TNULL:

The TNULL bit controls the insertion of an all-zero section trace identifier message in the transmit stream. When TNULL is a logic one, the contents of the transmit buffer is ignored and all-zeros bytes are inserted. When TNULL is a logic zero, the contents of the transmit section trace buffer is sent to TSOP for insertion into the J0 transmit section overhead byte. TNULL should

be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The PER5 bit controls the number of times a section trace identifier message must be received unchanged before being accepted. When PER5 is a logic one, a message is accepted when it is received unchanged five times consecutively. When PER5 is a logic zero, the message is accepted after three identical repetitions.

RRAMACC:

The RRAMACC bit directs read and writes access to either the receive or transmit section trace buffer. When RRAMACC is a logic one, microprocessor accesses are directed to the receive section trace buffer. When RRAMACC is a logic zero, microprocessor accesses are directed to the transmit section trace buffer.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x29: SSTB Section Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports the section trace identifier status of the SSTB.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set to a logic one immediately upon writing to the SSTB Indirect Address register, and stays high until the initiated access is completed (about 0.6 µs in STS-3 or 1.8 µs in STS-1). This register should be polled to determine when new data is available in the SSTB Indirect Data register.

Register 0x2A: SSTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into section trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) are used to address the section trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the captured message page while addresses 64 to 127 reference the expected message page of the receive section trace buffer. The captured message page contains the identifier bytes extracted from the receive stream. The expected message page contains the section trace message to which the captured message page is compared. When RRAMACC is set low, addresses 0 to 63 reference the transmit section trace buffer which contains the section trace message inserted in the transmit stream.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the selected section trace buffer (receive or transmit as determined by the RRAMACC bit). Writing to this register initiates an access to the selected section trace buffer. When RWB is a logic one, a read access is initiated. The addressed location's contents are placed in the SSTB Indirect Data register. When RWB is a logic zero, a write access is initiated. The data in the SSTB Indirect Data register is written to the addressed location in the selected buffer.

Register 0x2B: SSTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the section trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) contains the data read from either the transmit or receive section trace buffer after an indirect read operation is completed. The data that is written to a buffer is set up in this register before initiating the indirect write operation.

Register 0x30: RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	LOPV	X
Bit 4		Unused	X
Bit 3	R	PAISV	X
Bit 2	R	PRDIV	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

This register allows the status of path level alarms to be monitored.

NEWPTRE:

The NEWPTRE bit is the interrupt enable for the receive new pointer status. When NEWPTRE is a logic one, an interrupt is generated when the pointer interpreter validates a new pointer.

NEWPTRI:

The NEWPTRI bit is the receive new pointer interrupt status bit. NEWPTRI is a logic one when the pointer interpreter has validated a new pointer value (H1, H2). NEWPTRI is cleared when this register is read.

PRDIV:

The PRDIV bit is read to determine the remote defect indication state. When PRDIV is a logic one, the S/UNI-PLUS has declared path RDI.

PAISV:

The PAISV bit is read to determine the path AIS state. When PAISV is a logic one, the S/UNI-PLUS has declared path AIS.

PLOPV:

The PLOPV bit is read to determine the loss of pointer state. When PLOPV is a logic one, the S/UNI-PLUS has declared LOP.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x31: RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSLI	X
Bit 6		Unused	X
Bit 5	R	LOPI	X
Bit 4		Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

This register allows identification and acknowledgment of path level alarm and error event interrupts.

FEBEI:

The FEBEI bit is the path FEBE interrupt status bit. FEBEI is a logic one when a FEBE error is detected. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the path BIP-8 interrupt status bit. BIPEI is a logic one when a B3 error is detected. This bit is cleared when this register is read.

PRDII:

The PRDII bit is the path remote defect indication interrupt status bit. PRDII is a logic one when a change in the path RDI state or the auxiliary path RDI state occurs. This bit is cleared when this register is read.

PAISI:

The PAISI bit is the path alarm indication signal interrupt status bit. PAISI is a logic one when a change in the path AIS state occurs. This bit is cleared when this register is read.

LOPI:

The LOPI bit is the loss of pointer interrupt status bit. LOPI is a logic one when a change in the LOP state occurs. This bit is cleared when this register is read.

PSLI:

The PSLI bit is the change of path signal label interrupt status bit. PSLI is a logic one when a change is detected in the path signal label register. The current path signal label can be read from the RPOP Path Signal Label register. This bit is cleared when this register is read.

Register 0x32: RPOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6		Unused	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	ILLPTRI	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts.

NDFI:

The NDFI bit is the new data flag interrupt status bit. NDFI is a logic one when the NDF field is active in the received pointer (H1, H2). This bit is cleared when this register is read.

PSEI:

The PSEI bit is the positive stuff event interrupt status bit. PSEI is a logic one when a positive stuff event is detected in the received pointer (H1, H2). This bit is cleared when this register is read.

NSEI:

The NSEI bit is the negative stuff event interrupt status bit. NSEI is a logic one when a negative stuff event is detected in the received pointer (H1, H2). This bit is cleared when this register is read.

ILLPTRI:

The ILLPTRI bit is the illegal pointer interrupt status bit. ILLPTRI is a logic one when an illegal pointer value is detected. This bit is cleared when this register is read.

INVNDFI:

The INVNDFI bit is the illegal new data field value interrupt status bit. INVNDFI is a logic one when an illegal NDF field value is detected in the receive payload pointer. An illegal NDF field is any one of the following six values: 0x0, 0x3, 0x5, 0xA, 0xC, and 0xF. This bit is cleared when this register is read.

DISCOPAI:

The DISCOPAI bit is the discontinuous change of pointer interrupt status bit. DISCOPAI is a logic one when a new pointer value is validated without an accompanying NDF indication. This bit is cleared when this register is read.

ILLJREQI:

The ILLJREQI bit is the illegal justification request interrupt status bit. ILLJREQI is a logic one when the pointer interpreter detects an illegal pointer justification request event. This bit is cleared when this register is read.

Register 0x33: RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

This register allows interrupt generation to be enabled for path level alarm and error events.

FEBEE:

The FEBEE bit is the interrupt enable for path FEBEs. When FEBEE is a logic one, an interrupt is generated when a path FEBE is detected.

BIPEE:

The BIPEE bit is the interrupt enable for path BIP-8 errors. When BIPEE is a logic one, an interrupt is generated when a B3 error is detected.

PRDIE:

The PRDIE bit is the interrupt enable for path RDI. When PRDIE is a logic one, an interrupt is generated when the path RDI state changes.

PAISE:

The PAISE bit is the interrupt enable for path AIS. When PAISE is a logic one, an interrupt is generated when the path AIS state changes.

LOPE:

The LOPE bit is the interrupt enable for LOP. When LOPE is a logic one, an interrupt is generated when the LOP state changes.

PSLE:

The PSLE bit is the interrupt enable for changes in the received path signal label. When PSLE is a logic one, an interrupt is generated when the received C2 byte changes.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x34: RPOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	ILLPTRE	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register is used to enable pointer event interrupts.

NDFE:

The NDFE bit is the interrupt enable for NDF events. When NDFE is a logic one, an interrupt is generated when an NDF event is detected.

PSEE:

The PSEE bit is the interrupt enable for positive stuff events. When PSEE is a logic one, an interrupt is generated when a positive stuff event is detected.

NSEE:

The NSEE bit is the interrupt enable for negative stuff events. When NSEE is a logic one, an interrupt is generated when a negative stuff event is detected.

ILLPTRE:

The ILLPTRE bit is the interrupt enable for illegal pointers. When ILLPTRE is a logic one, an interrupt is generated when an illegal pointer is detected.

INVNDFE:

The INVNDFE bit is the interrupt enable for invalid new data flags. When INVNDFE is a logic one, an interrupt is generated when an invalid NDF is detected.

DISCOPAE:

The DISCOPAE bit is the interrupt enable for discontinuous pointer change events. When DISCOPAE is a logic one, an interrupt is generated when a discontinuous pointer change is detected.

ILLJREQE:

The ILLJREQE bit is the interrupt enable for illegal pointer justification events. When ILLJREQE is a logic one, an interrupt is generated when an illegal justification request is detected.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x35: RPOP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

PTR[7:0]:

The PTR[7:0] bits contain the eight LSBs of the current pointer value that is interpreted from the H1 and H2 bytes. The NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not change during the register read.

Register 0x36: RPOP Pointer MSB and RDI Filter Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RDI10	0
Bit 4		Unused	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

PTR[9:8]:

The PTR[9:8] bits contain the two MSBs of the current pointer value that is interpreted from the H1 and H2 bytes. The NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not change during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced by reading this register at least twice.

RDI10:

The RDI10 bit controls the filtering of the remote defect indication and the auxiliary remote defect indication. When RDI10 is a logic one, the PRDI and APRDI status is updated when the same value is received in the corresponding bit of the G1 byte for ten consecutive frames. When RDI10 is a logic zero, the PRDI and APRDI status is updated when the same value is received for five consecutive frames.

Register 0x37: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

PSL[7:0]:

The PSL[7:0] bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for two consecutive frames.

Register 0x38: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	PBE[7]	X
Bit 6	R	PBE[6]	X
Bit 5	R	PBE[5]	X
Bit 4	R	PBE[4]	X
Bit 3	R	PBE[3]	X
Bit 2	R	PBE[2]	X
Bit 1	R	PBE[1]	X
Bit 0	R	PBE[0]	X

Register 0x39: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	PBE[15]	X
Bit 6	R	PBE[14]	X
Bit 5	R	PBE[13]	X
Bit 4	R	PBE[12]	X
Bit 3	R	PBE[11]	X
Bit 2	R	PBE[10]	X
Bit 1	R	PBE[9]	X
Bit 0	R	PBE[8]	X

PBE[15:0]:

PBE[15:0] represent the number of B3 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path BIP-8 registers within a maximum of 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-PLUS Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x3A: RPOP Path FEBE LSB

Bit	Type	Function	Default
Bit 7	R	PFE[7]	X
Bit 6	R	PFE[6]	X
Bit 5	R	PFE[5]	X
Bit 4	R	PFE[4]	X
Bit 3	R	PFE[3]	X
Bit 2	R	PFE[2]	X
Bit 1	R	PFE[1]	X
Bit 0	R	PFE[0]	X

Register 0x3B: RPOP Path FEBE MSB

Bit	Type	Function	Default
Bit 7	R	PFE[15]	X
Bit 6	R	PFE[14]	X
Bit 5	R	PFE[13]	X
Bit 4	R	PFE[12]	X
Bit 3	R	PFE[11]	X
Bit 2	R	PFE[10]	X
Bit 1	R	PFE[9]	X
Bit 0	R	PFE[8]	X

These registers allow path FEBEs to be accumulated.

PFE[15:0]:

PFE[15:0] represent the number of path FEBE errors (G1) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path FEBE Registers within a maximum of 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-PLUS Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x3C: RPOP Auxiliary RDI

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	BLKFEBE	0
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	APRDIE	0
Bit 0	R	APRDIV	X

APRDIE:

The APRDIE bit is the interrupt enable for auxiliary path RDI. When APRDIE is a logic one, an interrupt is generated when the auxiliary path RDI state changes.

APRDIV:

The APRDIV bit is read to determine the auxiliary path RDI state. When APRDIV is a logic one, the S/UNI-PLUS has declared auxiliary path RDI.

BLKFEBE:

The BLKFEBE bit controls the accumulation of path FEBE events. When BLKFEBE is a logic one, a single FEBE is accumulated if the received FEBE code indicates between one and eight B3 errors have been detected by the far end. When BLKFEBE is a logic zero, the literal number of FEBEs is accumulated.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x3D: RPOP Error Event Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	DISFS	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register contains error event control bits.

BLKBIPO:

When BLKBIPO is a logic one, path FEBE indications are generated on a block basis. A single FEBE is transmitted if one or more path B3 error indications are detected per frame. When BLKBIPO is a logic zero, the transmitted FEBE indicates the number of B3 errors detected (between 0 and 8 errors per frame).

DISFS:

When DISFS is a logic one, the B3 calculation ignores the fixed stuff columns in an AU-3 carrying a VC-3. When DISFS is a logic zero, the B3 calculation includes the fixed stuff columns in an STS-1 stream. This bit is ignored when the S/UNI-PLUS is processing an STS-3c (STM-1) stream.

BLKBIP:

When BLKBIP is a logic one, B3 errors are reported and accumulated on a block basis. A single B3 error is accumulated and reported to the TPOP if one or more B3 errors are detected per frame. When BLKBIP is a logic zero, each B3 error is accumulated and reported.

ENSS:

The ENSS bit controls whether the SS bits in the payload pointer are included in the pointer interpreter state machine. When ENSS is a logic one, an

incorrect SS bit pattern causes the pointer interpreter to enter the LOP (loss of pointer) state and prevents a new pointer indication. When ENSS is a logic zero, the SS bits are ignored by the pointer interpreter.

SOS:

The SOS controls the spacing between consecutive pointer justification events in the receive stream. When SOS is a logic one, the definition of inc_ind and dec_ind indications (from Figure 4) includes the requirement that active offset changes have occurred at least three frames ago. When SOS is a logic zero, pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x40: TPOP Control/Diagnostic

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EXCFS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	PAIS	0

This register allows insertion of path level alarms and diagnostic signals.

PAIS:

The PAIS bit controls the insertion of STS path alarm indication signal. This register bit value is logically ORed with the input TPAIS. When a logic one is written to this bit position, the complete SPE, and the pointer bytes (H1, H2, and H3) are overwritten with the all-ones pattern. When a logic zero is written to this bit position, the pointer bytes and the SPE are processed normally.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the B3 byte. When DBIP8 is a logic one, the B3 byte is inverted.

EXCFS:

The EXCFS bit controls the inclusion of bytes in the fixed stuff columns of the STS-1/AU-3 payload in B3 calculations. When EXCFS is a logic one, the contents of the bytes in columns 30 and 59 do not affect the value of the B3 byte. When EXCFS is a logic zero, the fixed stuff bytes are included in the B3 calculations. This bit is only active if the S/UNI-PLUS is transmitting an STS-1 stream.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x41: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved	0

This register allows control over the transmitted payload pointer for diagnostic purposes.

PSE:

The PSE bit controls the insertion of positive pointer movements. A logic zero to logic one transition on this bit enables the insertion of a single positive pointer justification in the transmit stream. This register bit is automatically cleared when the pointer movement is inserted.

NSE:

The NSE bit controls the insertion of negative pointer movements. A logic zero to logic one transition on this bit enables the insertion of a single negative pointer justification in the transmit stream. This register bit is automatically cleared when the pointer movement is inserted.

NDF:

The NDF bit controls the insertion of new data flags in the inserted payload pointer. When a logic one is written to this bit position, the pattern contained in the NDF[3:0] bit positions in the TPOP Arbitrary Pointer MSB Register is inserted continuously in the payload pointer. When a logic zero is written to this bit position, the normal pattern (0110) is inserted in the payload pointer.

PLD:

The PLD bit controls the loading of the pointer value contained in the TPOP Arbitrary Pointer Registers. Normally the TPOP Arbitrary Pointer Registers are written to set up the arbitrary new pointer value, the S-bit values, and the NDF pattern. A logic one is then written to this bit position to load the new pointer value. The new data flag bit positions are set to the programmed NDF pattern for the first frame; subsequent frames have the new data flag bit positions set to the normal pattern (0110) unless the NDF bit described above is set to a logic one. This bit is automatically cleared after the new payload pointer has been loaded.

Note: When loading an out of range pointer (that is a pointer with a value greater than 782), the TPOP continues to operate with timing based on the last valid pointer value. The out of range pointer value is inserted in the transmit stream. Although a valid SPE will continue to be generated, it is unlikely to be extracted by downstream circuitry which should be in a loss of pointer state.

SOS:

The SOS bit controls the stuff opportunity spacing between consecutive SPE positive or negative stuff events. When SOS is a logic zero, stuff events may be generated every frame as controlled by the PSE and NSE register bits described above. When SOS is a logic one, stuff events may be generated at a maximum rate of once every four frames.

FTPTR:

The force transient pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the transmit stream for diagnostic purposes. When FTPTR is a logic one, the APTR[9:0] bits of the Arbitrary Pointer Registers are inserted into the H1 and H2 bytes of the transmit stream. At least one corrupted pointer is guaranteed to be sent. When FTPTR is a logic zero, the pointer value in the Current Pointer registers is inserted in the transmit stream.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x43: TPOP Current Pointer LSB

Bit	Type	Function	Default
Bit 7	R	CPTR[7]	X
Bit 6	R	CPTR[6]	X
Bit 5	R	CPTR[5]	X
Bit 4	R	CPTR[4]	X
Bit 3	R	CPTR[3]	X
Bit 2	R	CPTR[2]	X
Bit 1	R	CPTR[1]	X
Bit 0	R	CPTR[0]	X

CPTR[7:0]:

The CPTR[7:0] bits, along with the CPTR[9:8] bits in the TPOP Current Pointer MSB Register reflect the value of the current payload pointer being inserted in the transmit stream. The value may be changed by loading a new pointer value using the TPOP Arbitrary Pointer LSB and MSB Registers, or by inserting positive and negative pointer movements using the PSE and NSE register bits.

Register 0x44: TPOP Current Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CPTR[9]	X
Bit 0	R	CPTR[8]	X

CPTR[9:8]:

The CPTR[9:8] bits, along with the CPTR[7:0] bits in the TPOP Current Pointer LSB Register reflect the value of the current payload pointer being inserted in the transmit stream. The value may be changed by loading a new pointer value using the TPOP Arbitrary Pointer LSB and MSB Registers, or by inserting positive and negative pointer movements using the PSE and NSE register bits.

It is recommended the CPTR[9:0] value be software debounced to ensure a correct value is received.

Register 0x45: TPOP Arbitrary Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[7:0]:

The APTR[7:0] bits, along with the APTR[9:8] bits in the TPOP Arbitrary Pointer MSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the transmit stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

Register 0x46: TPOP Arbitrary Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	0
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[9:8]:

The APTR[9:8] bits, along with the APTR[7:0] bits in the TPOP Arbitrary Pointer LSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the transmit stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

S[1], S[0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions (also referred to as the unused bits) in the payload pointer.

NDF[3:0]:

The NDF[3:0] bits contain the value inserted in the NDF bit positions when an arbitrary new payload pointer value is inserted (using the PLD bit in the TPOP Pointer Control Register) or when new data flag generation is enabled using primary input NDF, or the NDF bit in the TPOP Pointer Control Register.

Register 0x47: TPOP Path Trace

Bit	Type	Function	Default
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

This register allows control over the path trace byte.

J1[7:0]:

The J1[7:0] bits are inserted in the J1 byte position in the transmit stream when insertion from the transmit path overhead port is disabled, and insertion from the SPTB is disabled.

Register 0x48: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	1
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	1
Bit 0	R/W	C2[0]	1

This register allows control over the path signal label. Upon reset the register defaults to 13H, which signifies an equipped ATM payload.

C2[7:0]:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream when insertion from the transmit path overhead port is disabled.

Register 0x49: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	APRDI	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

This register allows control over the path status byte.

G1[1], G1[0]:

The G1[1:0] bits are inserted in the unused bit positions in the path status byte when the SRCG1 bit of the TPOP Source Control Register is logic zero and primary input TPOHEN is low during the unused bit positions in the path overhead input stream, TPOH.

APRDI:

The APRDI bit controls the insertion of the auxiliary path remote defect indication. When APRDI is a logic one, the APRDI bit position in the path status byte is set high. When APRDI is a logic zero, the APRDI bit position in the path status byte is set low. This bit has no effect if the SRCG1 bit of the TPOP Source Control Register is logic one or primary input TPOHEN is high during the path status remote defect indication bit position in the path overhead input stream in which case the value is inserted from TPOH.

PRDI:

The PRDI bit controls the insertion of the path remote defect indication. This register bit value is logically ORed with the input TPRDI. When PRDI is a logic one, the PRDI bit position in the path status byte is set high. When PRDI is a logic zero, the PRDI bit position in the path status byte is set low. This bit has no effect if the SRCG1 bit of the TPOP Source Control Register is logic one or primary input TPOHEN is high during the path status remote

defect indication bit position in the path overhead input stream in which case the value is inserted from TPOH.

FEBE[3:0]:

The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte when the SRCG1 bit of the TPOP Source Control Register is logic zero and primary input TPOHEN is low during the path status FEBE bit positions in the path overhead input stream, TPOH. The value contained in FEBE[3:0] is cleared after being inserted in the path status byte. Any non-zero FEBE value overwrites the value that would normally have been inserted based on the number of receive B3 errors during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

Register 0x4A: TPOP Path User Channel

Bit	Type	Function	Default
Bit 7	R/W	F2[7]	0
Bit 6	R/W	F2[6]	0
Bit 5	R/W	F2[5]	0
Bit 4	R/W	F2[4]	0
Bit 3	R/W	F2[3]	0
Bit 2	R/W	F2[2]	0
Bit 1	R/W	F2[1]	0
Bit 0	R/W	F2[0]	0

This register allows control over the path user channel.

F2[7:0]:

The F2[7:0] bits are inserted in the F2 byte position in the transmit stream when insertion from the transmit path overhead port is disabled.

Register 0x4B: TPOP Path Growth #1 (Z3)

Bit	Type	Function	Default
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

This register allows control over path growth byte #1 (Z3).

Z3[7:0]:

The Z3[7:0] bits are inserted in the Z3 byte position in the transmit stream when insertion from the transmit path overhead port is disabled.

Register 0x4C: TPOP Path Growth #2 (Z4)

Bit	Type	Function	Default
Bit 7	R/W	Z4[7]	0
Bit 6	R/W	Z4[6]	0
Bit 5	R/W	Z4[5]	0
Bit 4	R/W	Z4[4]	0
Bit 3	R/W	Z4[3]	0
Bit 2	R/W	Z4[2]	0
Bit 1	R/W	Z4[1]	0
Bit 0	R/W	Z4[0]	0

This register allows control over path growth byte #2 (Z4).

Z4[7:0]:

The Z4[7:0] bits are inserted in the Z4 byte position in the transmit stream when insertion from the transmit path overhead port is disabled.

Register 0x4D: TPOP Path Growth #3 (Z5)

Bit	Type	Function	Default
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

This register allows control over path growth byte #3 (Z5).

Z5[7:0]:

The Z5[7:0] bits are inserted in the Z5 byte position in the transmit stream when insertion from the transmit path overhead port is disabled.

Register 0x50: RACP Control

Bit	Type	Function	Default
Bit 7	R/W	FSEN	1
Bit 6	R/W	RXPTYPE	0
Bit 5	R/W	PASS	0
Bit 4	R/W	DISCOR	0
Bit 3	R/W	HCSPASS	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DDSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell receive FIFO. When FIFORST is a logic zero, the FIFO operates normally. When FIFORST is a logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until FIFORST is cleared.

DDSCR:

The DDSCR bit controls the descrambling of the cell payload. When DDSCR is a logic one, cell payload descrambling is disabled. When DDSCR is a logic zero, payload descrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is compared. HCSADD can also be used to force the S/UNI-PLUS out of cell delineation.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of an HCS error. When HCSPASS is a logic zero, cells are dropped based on the criteria of the HCS verification state machine. When HCSPASS is a logic one,

cells are passed to the receive FIFO regardless of errors detected in the HCS, and the HCS verification finite state machine never exits the correction mode. Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states.

DISCOR:

The DISCOR bit disables the HCS error correction algorithm. When DISCOR is a logic zero, the error correction algorithm is enabled, and single-bit errors detected in the cell header are corrected. When DISCOR is a logic one, the error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HCS error.

PASS:

The PASS bit controls the function of the cell filter. When PASS is a logic zero, cells which match the header cell filter and which have VPI and VCI fields set to 0 are dropped. When PASS is a logic one, the match header pattern registers are ignored and filtering of cells with VPI and VCI fields set to 0 is not performed. The default state of this bit together with the default states of the bits in the Match Mask and Match Pattern registers enable the dropping of cells containing all zero VCI and VPI fields.

RXPTYPE:

The RXPTYPE bit selects even or odd parity for outputs RXPRTY[1:0]. When RXPTYPE is a logic one, even parity is calculated for the output data on RDAT[15:0]; conversely, when RXPTYPE is a logic zero, odd parity is calculated for the output data. When RXPTYPE is set to logic one in word parity mode, output RXPRTY[1] is the even parity bit for outputs RDAT[15:0]. When RXPTYPE is set to logic zero in word parity mode, output RXPRTY[1] is the odd parity bit for outputs RDAT[15:0]. In word parity mode, RXPRTY[0] is held low.

When RXPTYPE is set to logic one in byte parity mode, output RXPRTY[1] is the even parity bit for outputs RDAT[15:8] and output RXPRTY[0] is the even parity bit for outputs RDAT[7:0]. When RXPTYPE is a logic zero in byte parity mode, output RXPRTY[1] is the odd parity bit for outputs RDAT[15:8] and output RXPRTY[0] is the odd parity bit for outputs RDAT[7:0].

FSEN:

The FSEN bit determines the payload mapping of ATM cells when STS-1 (AU-3) mapping is selected. When FSEN is set to logic one, the S/UNI-PLUS

does not insert ATM cells into the two fixed stuff columns in the SPE. When FSEN is set to logic zero, the S/UNI-PLUS inserts cells into the entire SPE.

Register 0x51: RACP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	OCDV	X
Bit 6	R	LCDV	X
Bit 5	R	OCDI	X
Bit 4	R	LCDI	X
Bit 3	R	CHCSI	X
Bit 2	R	UHCSI	X
Bit 1	R	FOVRI	X
Bit 0		Unused	X

FOVRI:

The FOVRI bit is the FIFO overrun interrupt status bit. FOVRI is a logic one when a FIFO overrun occurs. This bit is cleared when this register is read.

UHCSI:

The UHCSI bit is the uncorrectable HCS error interrupt status bit. UHCSI is a logic one when an uncorrectable HCS error is detected. This bit is cleared when this register is read.

CHCSI:

The CHCSI bit is the correctable HCS error interrupt status bit. CHCSI is a logic one when a correctable HCS error is detected. This bit is cleared when this register is read.

LCDI:

The LCDI bit is the loss of cell delineation interrupt status bit. LCDI is a logic one when a change in the LCD state occurs. This bit is cleared when this register is read.

OCDI:

The OCDI bit is the out of cell delineation interrupt status bit. OCDI is a logic one when a change in the OCD state occurs. This bit is cleared when this register is read.

LCDV:

The LCDV bit indicates the loss of cell delineation state. Loss of cell delineation is declared (LCDV is a logic one) when out of cell delineation persists for 4 ms or more. Loss of cell delineation is removed (LCDV is a logic zero) when out of cell delineation is absent for 4 ms.

OCDV:

The OCDV bit indicates the out of cell delineation state. When OCDV is a logic one, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states, and is hunting for the cell boundaries in the synchronous payload envelope. When OCDV is a logic zero, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

The cell delineation state machine transitions from the SYNC state to the HUNT state immediately when either loss of signal (LOS), loss of frame (LOF), loss of pointer (LOP), line AIS or path AIS is declared or when seven consecutive cells with incorrect HCS's are detected. The cell delineation state machine remains in HUNT state as long as one of the above alarms is active or if cells with a correct HCS cannot be found.

Register 0x52: RACP Interrupt Enable/Control

Bit	Type	Function	Default
Bit 7	R/W	OCDE	0
Bit 6	R/W	LCDE	0
Bit 5	R/W	HCSE	0
Bit 4	R/W	FIFOE	0
Bit 3	R/W	LCDDROP	0
Bit 2	R/W	RCALEVEL0	1
Bit 1	R/W	HCSFTR[1]	0
Bit 0	R/W	HCSFTR[0]	0

HCSFTR[1:0]:

The HCS filter bits, HCSFTR[1:0], indicate the number of error free cells required while in detection mode before reverting back to correction mode. Please refer to Figure 6 for details.

Table 2 -

HCSFTR[1:0]	Cell Acceptance Threshold
00	One ATM cell with correct HCS before resumption of cell correction.
01	Two ATM cells with correct HCS before resumption of cell correction.
10	Four ATM cells with correct HCS before resumption of cell correction.
11	Eight ATM cells with correct HCS before resumption of cell correction.

RCALEVEL0:

The RCALEVEL0 bit controls the function of the RCA output. When RCALEVEL0 is a logic one, a high to low transition on output RCA indicates that the receive FIFO is empty. When RCALEVEL0 is a logic zero, a high to low transition on output RCA indicates that the receive FIFO is almost empty

and contains only four words. Refer to the Drop Side Receive Interface timing diagrams in the Functional Timing section.

LCDDROP:

The LCD drop bit, LCDDROP, enables the dropping of cells while in the loss of cell delineation state. When LCDDROP is set to logic one, received cells are not written into the FIFO until the LCD indication is deasserted, which occurs after being continuously in the SYNC state for 4 ms. If LCDDROP is set to logic zero, cells are written to the FIFO when in the SYNC state, regardless of the LCD state.

FIFOE:

The FIFOE bit is the interrupt enable for FIFO overruns. When FIFOE is a logic one, an interrupt is generated when the FIFO overruns.

HCSE:

The HCSE bit is the interrupt enable for HCS errors. When HCSE is a logic one, an interrupt is generated when an HCS error is detected.

LCDE:

The LCDE bit is the interrupt enable for loss of cell delineation. When LCDE is a logic one, an interrupt is generated when the LCD state changes.

OCDE:

The OCDE bit is the interrupt enable for out of cell delineation. When OCDE is a logic one, an interrupt is generated when the OCD state changes.

Register 0x53: RACP Match Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third and fourth bits of the first octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control Register must be a logic zero to enable dropping of cells matching this pattern. Note that an all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control Register must be a logic zero to enable dropping of cells matching this pattern.

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53 octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control Register must be a logic zero to enable dropping of cells matching this pattern.

Register 0x54: RACP Match Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	0
Bit 6	R/W	MGFC[2]	0
Bit 5	R/W	MGFC[1]	0
Bit 4	R/W	MGFC[0]	0
Bit 3	R/W	MPTI2]	0
Bit 2	R/W	MPTI[1]	0
Bit 1	R/W	MPTI[0]	0
Bit 0	R/W	MCLP	0

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third and fourth bits of the first octet of the 53 octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MPTI3:0]:

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth and seventh bits of the fourth octet of the 53 octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MCLP:

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53 octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

Register 0x55: RACP Correctable HCS Error Count (LSB)

Bit	Type	Function	Default
Bit 7	R	CHCS[7]	X
Bit 6	R	CHCS[6]	X
Bit 5	R	CHCS[5]	X
Bit 4	R	CHCS[4]	X
Bit 3	R	CHCS[3]	X
Bit 2	R	CHCS[2]	X
Bit 1	R	CHCS[1]	X
Bit 0	R	CHCS[0]	X

Register 0x56: RACP Correctable HCS Error Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	CHCS[11]	X
Bit 2	R	CHCS[10]	X
Bit 1	R	CHCS[9]	X
Bit 0	R	CHCS[8]	X

CHCS[11:0]:

The CHCS[11:0] bits indicate the number of correctable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 2 µs after a transfer is triggered by a write to the receive cell count register space, the correctable HCS error count register space, or to the uncorrectable HCS error count register space.

The count can also be polled by writing to the S/UNI-PLUS Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x57: RACP Uncorrectable HCS Error Count (LSB)

Bit	Type	Function	Default
Bit 7	R	UHCS[7]	X
Bit 6	R	UHCS[6]	X
Bit 5	R	UHCS[5]	X
Bit 4	R	UHCS[4]	X
Bit 3	R	UHCS[3]	X
Bit 2	R	UHCS[2]	X
Bit 1	R	UHCS[1]	X
Bit 0	R	UHCS[0]	X

Register 0x58: RACP Uncorrectable HCS Error Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	UHCS[11]	X
Bit 2	R	UHCS[10]	X
Bit 1	R	UHCS[9]	X
Bit 0	R	UHCS[8]	X

UHCS[11:0]:

The UHCS[11:0] bits indicate the number of uncorrectable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 2 µs after a transfer is triggered by a write to the receive cell count register space, the correctable HCS error count register space, or to the uncorrectable HCS error count register space.

The count can also be polled by writing to the S/UNI-PLUS Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x59: RACP Receive Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 0x5A: RACP Receive Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 0x5B: RACP Receive Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	RCELL[20]	X
Bit 3	R	RCELL[19]	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[20:0]:

The RCELL[20:0] bits indicate the number of cells received and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle/Unassigned cell matches are not counted. The counter should be polled every second to avoid saturation. The contents of these registers are valid 2 µs after a transfer is triggered by a write to the receive cell count register space, the correctable HCS error count register space, or to the uncorrectable HCS error count register space.

The count can also be polled by writing to the S/UNI-PLUS Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x5C: RACP GFC Control and Miscellaneous Control

Bit	Type	Function	Default
Bit 7	R/W	CDDIS	0
Bit 6	R/W	RXBYTEPRTY	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RGFCE[3]	1
Bit 2	R/W	RGFCE[2]	1
Bit 1	R/W	RGFCE[1]	1
Bit 0	R/W	RGFCE[0]	1

RGFCE[3:0]:

The RGFCE[3:0] bits are used to enable the GFC[3:0] bits serialized on output RGFC. For example, when RGFCE[3] is a logic one, the GFC[3] bit is output on RGFC. When RGFCE[3] is a logic zero, the GFC[3] bit is not output on RGFC.

RXBYTEPRTY:

The receive byte parity, RXBYTEPRTY, mode bit selects between byte and word parity mode for outputs RXPRTY[1:0]. When the RXBYTEPRTY bit is set to logic one, byte parity mode is selected; otherwise, word parity mode is selected. In byte parity mode, RXPRTY[1] is the parity bit for outputs RDAT[15:8], and RXPRTY[0] is the parity bit for outputs RDAT[7:0]. In word parity mode, RXPRTY[1] is the parity bit for outputs RDAT[15:0], and RXPRTY[0] is held low. Word parity mode can only be selected when the BUS8 input is low (i.e., the 16-bit FIFO interface is selected).

CDDIS:

The cell delineation disable bit, CDDIS, is used to defeat the cell delineation function. When the CDDIS bit is set to logic one, HCS errors are ignored, which makes every byte appear like a valid cell boundary. Ignoring HCS errors causes the cell delineation state machine to lock onto an arbitrary cell boundary and to enter and remain in the SYNC state. Once in the SYNC state, the incoming data is written to the FIFO.

Register 0x60: TACP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	FIFOE	0
Bit 6	R	TSOCI	X
Bit 5	R	FOVRI	X
Bit 4	R/W	DHCS	0
Bit 3	R/W	HCSB	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell transmit FIFO. When FIFORST is a logic zero, the FIFO operates normally. When FIFORST is a logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until FIFORST is cleared. Idle/unassigned cells are transmitted until a subsequent cell is written to the transmit FIFO.

DSCR:

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the transmit stream. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted. HCSADD takes effect unconditionally regardless of whether an idle/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO.

HCSB:

The HCSB bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCSB is a logic zero, the HCS is generated and inserted internally. When HCSB is a logic one, the HCS octet read from the FIFO is inserted unaltered into the transmit cell stream. An HCS is generated for idle/unassigned cells regardless of the state of this bit.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is a logic one, the HCS octet is inverted prior to insertion in the transmit stream. DHCS takes effect unconditionally regardless of whether an idle/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO.

FOVRI:

The FOVRI bit is the transmit FIFO overrun interrupt status bit. FOVRI is a logic one when a FIFO overrun occurs. This bit is cleared when this register is read.

TSOCI:

The TSOCI bit is a logic one when the TSOC input is sampled high during any position other than the first word of the cell data structure. The write address counter is reset to the first word of the data structure when TSOC is sampled high. This bit is cleared when this register is read.

FIFOE:

The FIFOE bit enables the generation of an interrupt due to a FIFO overrun error condition, or when the TSOC input is sampled high during any position other than the first word of the cell data structure. When FIFOE is a logic one, the interrupt is enabled.

Register 0x61: TACP Idle/Unassigned Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

GFC[3:0]:

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. The all-zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

PTI[2:0]:

The PTI[2:0] bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

CLP:

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

Register 0x62: TACP Idle/Unassigned Cell Payload Octet Pattern

Bit	Type	Function	Default
Bit 7	R/W	ICP[7]	0
Bit 6	R/W	ICP[6]	1
Bit 5	R/W	ICP[5]	1
Bit 4	R/W	ICP[4]	0
Bit 3	R/W	ICP[3]	1
Bit 2	R/W	ICP[2]	0
Bit 1	R/W	ICP[1]	1
Bit 0	R/W	ICP[0]	0

ICP[7:0]:

The ICP[7:0] bits contain the pattern inserted in the payload octets of the idle or unassigned cell. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. Bit ICP[7] corresponds to the most significant bit of the octet, and the first bit transmitted.

Register 0x63: TACP FIFO Control

Bit	Type	Function	Default
Bit 7	R/W	TXPTYPE	0
Bit 6	R/W	TXPRTYE	0
Bit 5	R	TXPRTYI[1]	X
Bit 4	R	TXPRTYI[0]	X
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	TCALEVEL0	0
Bit 0	R/W	HCSCTLEB	1

HCSCTLEB:

The HCSCTLEB bit enables the XORing of the HCS Control byte with the generated HCS before insertion into the transmit stream. When HCSCTLEB is a logic zero, the HCS Control byte provided in the third word of the 27 word data structure is XORed with the generated HCS. When HCSCTLEB is a logic one, the HCS Control byte is ignored.

TCALEVEL0:

The TCALEVEL0 bit controls the function of the TCA output. When TCALEVEL0 is a logic one, a high to low transition on output TCA indicates that the transmit FIFO is full. When TCALEVEL0 is a logic zero, a high to low transition on output TCA indicates that the transmit FIFO is almost full and can accept no more than four additional writes. Refer to the Drop Side Transmit Interface timing diagram in the Functional Timing section.

FIFODP[1:0]:

The FIFODP[1:0] bits determine the transmit FIFO cell depth. FIFO depth control is important in systems where the cell latency through the transmit FIFO must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal, TCA transitions to logic zero. The selectable FIFO cell depths are shown below:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

TXPRTYI[1:0]:

The TXPRTYI[1:0] bits indicate if a parity error was detected on the TDAT[15:0] bus. When TXPRTYI[1] is a logic one, a parity error has been detected over inputs, TDAT[15:8]. Similarly, when TXPRTYI[0] is a logic one, a parity error has been detected over inputs, TDAT[7:0]. Both bits are cleared when this register is read. Odd or even parity is selected using the TXPTYPE bit.

TXPRTYE:

The TXPRTYE bit enables transmit parity interrupts. When TXPRTYE is a logic one, parity errors on inputs TDAT[15:0] generate an interrupt.

TXPTYPE:

The TXPTYPE bit selects even or odd parity for inputs TXPRTY[1:0]. When TXPTYPE is a logic one, input TXPRTY[1] is the even parity bit for inputs TDAT[15:8] while input TXPRTY[0] is the even parity bit for inputs TDAT[7:0]. When TXPTYPE is a logic zero, inputs TXPRTY[1:0] are the odd parity bits for inputs TDAT[15:0].

Register 0x64: TACP Transmit Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 0x65: TACP Transmit Cell Counter

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x66: TACP Transmit Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	TCELL[20]	X
Bit 3	R	TCELL[19]	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[20:0]:

The TCELL[20:0] bits indicate the number of cells read from the transmit FIFO and inserted into the transmit stream during the last accumulation interval. Idle/Unassigned cells inserted in the transmit stream are not counted. The counter should be polled every second to avoid saturation. The contents of these registers are valid 2µs after a transfer is triggered by a write to the transmit cell count register space.

The count can also be polled by writing to the S/UNI-PLUS Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x67: TACP Fixed Stuff / GFC

Bit	Type	Function	Default
Bit 7	R/W	TGFCE[3]	0
Bit 6	R/W	TGFCE[2]	0
Bit 5	R/W	TGFCE[1]	0
Bit 4	R/W	TGFCE[0]	0
Bit 3	R/W	FSEN	1
Bit 2	R/W	TXBYTEPRTY	0
Bit 1	R/W	FIXBYTE[1]	0
Bit 0	R/W	FIXBYTE[0]	0

FIXBYTE[1:0]:

The FIXBYTE[1:0] bits identify the byte pattern inserted into fixed byte columns of the synchronous payload envelope.

FIXBYTE[1]	FIXBYTE[0]	BYTE
0	0	00H
0	1	55H
1	0	AAH
1	1	FFH

TXBYTEPRTY:

The transmit byte parity, TXBYTEPRTY, bit selects between byte parity and word parity mode for inputs TXPRTY[1:0]. When the TXBYTEPRTY bit is set to logic one, byte parity mode is selected; otherwise, word parity mode is selected. In byte parity mode, TXPRTY[1] is the parity bit for inputs TDAT[15:8], and TXPRTY[0] is the parity bit for inputs TDAT[7:0]. In word parity mode, TXPRTY[1] is the parity bit for inputs TDAT[15:0], and TXPRTY[0] is unused. Word parity mode can only be selected when the BUS8 input is low (i.e., the 16-bit FIFO interface is selected).

FSEN:

The FSEN bit determines the payload mapping of ATM cells when STS-1 (AU-3) mapping is selected. When FSEN is a logic one, the S/UNI-PLUS does not map ATM cells into columns 30 and 59 of the STS-1 SPE. When FSEN is a logic zero, the S/UNI-PLUS maps ATM cells into the entire STS-1 SPE. The FSEN bit is ignored in STS-3c (STM-1) modes.

TGFCE[3:0]:

The TGFCE[3:0] bits select the source of the GFC bits. When a TGFCE[3:0] bit is a logic one, the TGFC input is used to source the corresponding GFC[3:0] bit of transmit cell headers. If a TGFCE[3:0] bit is a logic zero, the corresponding GFC[3:0] bit of an idle/unassigned cell (as programmed in the TACP Idle/Unassigned Cell Header register) or the corresponding GFC[3:0] bit of a cell read from the FIFO is transmitted unaltered.

Register 0x68: SPTB Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SPTB.

LEN16:

The LEN16 bit selects the length of the path trace message to be 16 bytes or 64 bytes. When LEN16 is a logic one, a 16 byte path trace message is selected. When LEN16 is a logic zero, a 64 byte path trace message is selected.

NOSYNC:

The NOSYNC bit disables the writing of the path trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is a logic one and NOSYNC is a logic zero, the receive path trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 and NOSYNC are logic zero, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is a logic one, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

TNULL:

The TNULL bit controls the insertion of an all-zero path trace identifier message in the transmit stream. When TNULL is a logic one, the contents of the transmit buffer is ignored and all-zeros bytes are inserted. When TNULL is a logic zero, the contents of the transmit path trace buffer are inserted into

the J1 byte. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The PER5 bit controls the number of times a path trace identifier message must be received unchanged before being accepted. When PER5 is a logic one, a message is accepted when it is received unchanged five times consecutively. When PER5 is a logic zero, the message is accepted after three identical repetitions.

RTIMIE:

The RTIMIE bit controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state. When RTIMIE is a logic one, changes in match state activates the interrupt (INTB) output.

RTIUIE:

The RTIUIE bit controls the activation of the interrupt output when the receive identifier message changes state. When RTIUIE is a logic one, changes in the received path trace identifier message stable/unstable state activates the interrupt output.

RRAMACC:

The RRAMACC bit directs read and writes access to either the receive or transmit path trace buffer. When RRAMACC is a logic one, microprocessor accesses are directed to the receive path trace buffer. When RRAMACC is a logic zero, microprocessor accesses are directed to the transmit path trace buffer.

Register 0x69: SPTB Path Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RPTIUI	X
Bit 2	R	RPTIUV	X
Bit 1	R	RPTIMI	X
Bit 0	R	RPTIMV	X

This register reports the path trace identifier status of the SPTB.

RPTIMV:

The RPTIMV bit reports the match/mismatch status of the identifier message framer. RPTIMV is a logic one when the accepted identifier message differs from the expected message written by the microprocessor. RPTIMV is a logic zero when the accepted message matches the expected message.

RPTIMI:

The RPTIMI bit is a logic one when match/mismatch status of the trace identifier framer changes state. This bit is cleared when this register is read.

RPTIUV:

The RPTIUV bit reports the stable/unstable status of the identifier message framer. RPTIUV is a logic one when the current received path trace identifier message has not matched the previous message for eight consecutive messages. RPTIUV is a logic zero when the current message becomes the accepted message as determined by the PER5 bit in the SPTB Control register.

RPTIUI:

The RPTIUI bit is a logic one when the stable/unstable status of the trace identifier framer changes state. This bit is cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set to a logic one immediately upon writing to the SPTB Indirect Address register and stays high until the initiated access is completed (about 0.6 µs in STS-3 or 1.8 µs in STS-1). This register should be polled to determine when new data is available in the SPTB Indirect Data register.

Register 0x6A: SPTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into path trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) are used to address the path trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the captured message page while addresses 64 to 127 reference the expected message page of the receive path trace buffer. The captured message page contains the identifier bytes extracted from the receive stream. The expected message page contains the path trace message to which the captured message page is compared. When RRAMACC is set low, addresses 0 to 63 reference the transmit path trace buffer which contains the path trace message inserted in the transmit stream.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the selected path trace buffer (receive or transmit as determined by the RRAMACC bit). Writing to this register initiates an access to the selected path trace buffer. When RWB is a logic one, a read access is initiated. The addressed location's contents are placed in the SPTB Indirect Data register. When RWB is a logic zero, a write access is initiated. The data in the SPTB Indirect Data register is written to the addressed location in the selected buffer.

Register 0x6B: SPTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the path trace message buffer after a read operation or the data to be written into the buffer during a write operation.

D[7:0]:

The indirect data bits (D[7:0]) contains the data read from either the transmit or receive path trace buffer after an indirect read operation is completed. The data that is written to a buffer is set up in this register before initiating the indirect write operation.

Register 0x6C: SPTB Expected Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	EPSL7	0
Bit 6	R/W	EPSL6	0
Bit 5	R/W	EPSL5	0
Bit 4	R/W	EPSL4	0
Bit 3	R/W	EPSL3	0
Bit 2	R/W	EPSL2	0
Bit 1	R/W	EPSL1	0
Bit 0	R/W	EPSL0	0

This register contains the expected path signal label byte in the receive stream.

EPSL[7:0]:

The EPSL[7:0] bits contain the expected path signal label byte (C2). EPSL[7:0] is compared with the accepted path signal label extracted from the receive stream. A path signal label match or mismatch is declared based upon the following table:

Table 3 -

Expect	Receive	Action
00	00	Match
00	01	Mismatch
00	XX	Mismatch
01	00	Mismatch
01	01	Match
01	XX	Match
XX	00	Mismatch
XX	01	Match
XX	XX	Match
XX	YY	Mismatch

Register 0x6D: SPTB Path Signal Label Status

Bit	Type	Function	Default
Bit 7	R/W	RPSLUIE	0
Bit 6	R/W	RPSLMIE	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RPSLUI	X
Bit 2	R	RPSLUV	X
Bit 1	R	RPSLMI	X
Bit 0	R	RPSLMV	X

This register reports the path signal label status of the SPTB.

RPSLMV:

The RPSLMV bit reports the match/mismatch status between the expected and the accepted path signal label. RPSLMV is a logic one when the accepted PSL results in a mismatch with the expected PSL written by the microprocessor. RPSLMV is a logic zero when the accepted PSL results in a match with the expected PSL.

RPSLMI:

The RPSLMI bit is a logic one when the match/mismatch status between the accepted and the expected path signal label changes state. This bit is cleared when this register is read.

RPSLUV:

The RPSLUV reports the stable/unstable status of the path signal label in the receive stream. RPSLUV is a logic one when the current received C2 byte differs from the previous C2 byte for five consecutive frames. RPSLUV is a logic zero when the same PSL code is received for five consecutive frames.

RPSLUI:

The RPSLUI bit is a logic one when the stable/unstable status of the path signal label changes state. This bit is cleared when this register is read.

RPSLMIE:

The RPSLMIE bit is the interrupt enable for the path signal label match/mismatch status. When RPSLMIE is a logic one changes in the match state generate an interrupt.

RPSLUIE:

The RPSLUIE bit is the interrupt enable for the path signal label stable/unstable status. When RPSLUIE is a logic one, changes in the stable/unstable state generate an interrupt.

Register 0x70: BERM Control

Bit	Type	Function	Default
Bit 7	R/W	BERTEN	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	BERE	0

This register controls the automatic bit error rate alarm circuitry.

BERE:

The BERE bit is the interrupt enable for bit error rate threshold events. When BERE is a logic one, an interrupt is generated when the bit error rate threshold is exceeded.

BERTEN:

The BERTEN bit enables and disables automatic monitoring of line bit error rate threshold events. When BERTEN is a logic one, the S/UNI-PLUS continuously accumulates line BIP errors over a period defined in the BERM Line BIP Accumulation Period registers. If at any point the accumulated count exceeds the value defined in the BERM Line BIP Threshold registers, a bit error rate threshold event is generated. Both the BERM Line BIP Accumulation Period and BERM Line BIP Threshold registers should be set up before the monitoring is enabled. When BERTEN is a logic zero, the BIP accumulation logic is disabled.

Register 0x71: BERM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	BERI	X

This register indicates the bit error rate threshold events.

BERI:

The BERI bit indicates that the incoming bit error rate has exceeded the user programmed threshold. When BERI is a logic one, incoming B2 errors have exceeded the programmable threshold. This bit is cleared when this register is read.

Register 0x72: BERM Line BIP Accumulation Period LSB

Bit	Type	Function	Default
Bit 7	R/W	LB_AP[7]	0
Bit 6	R/W	LB_AP[6]	0
Bit 5	R/W	LB_AP[5]	0
Bit 4	R/W	LB_AP[4]	0
Bit 3	R/W	LB_AP[3]	0
Bit 2	R/W	LB_AP[2]	0
Bit 1	R/W	LB_AP[1]	0
Bit 0	R/W	LB_AP[0]	0

Register 0x73: BERM Line BIP Accumulation Period MSB

Bit	Type	Function	Default
Bit 7	R/W	LB_AP[15]	0
Bit 6	R/W	LB_AP[14]	0
Bit 5	R/W	LB_AP[13]	0
Bit 4	R/W	LB_AP[12]	0
Bit 3	R/W	LB_AP[11]	0
Bit 2	R/W	LB_AP[10]	0
Bit 1	R/W	LB_AP[9]	0
Bit 0	R/W	LB_AP[8]	0

LB_AP[15:0]:

The LB_AP[15:0] bits represent the number of 125 µs frames that define a line BIP accumulation period. Refer to the Operations section for the recommended settings.

Register 0x74: BERM Line BIP Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	LB_TH[7]	0
Bit 6	R/W	LB_TH[6]	0
Bit 5	R/W	LB_TH[5]	0
Bit 4	R/W	LB_TH[4]	0
Bit 3	R/W	LB_TH[3]	0
Bit 2	R/W	LB_TH[2]	0
Bit 1	R/W	LB_TH[1]	0
Bit 0	R/W	LB_TH[0]	0

Register 0x75: BERM Line BIP Threshold MSB

Bit	Type	Function	Default
Bit 7	R/W	LB_TH[15]	0
Bit 6	R/W	LB_TH[14]	0
Bit 5	R/W	LB_TH[13]	0
Bit 4	R/W	LB_TH[12]	0
Bit 3	R/W	LB_TH[11]	0
Bit 2	R/W	LB_TH[10]	0
Bit 1	R/W	LB_TH[9]	0
Bit 0	R/W	LB_TH[8]	0

LB_TH[15:0]:

The LB_TH[15:0] bits represent the allowable number of line BIP errors that can be accumulated during a line BIP accumulation period before an BER threshold event is asserted. Refer to the Operations section for the recommended settings.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-PLUS. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[7]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-PLUS are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-PLUS also supports a standard IEEE 1149.1 five signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port with the exception of the PECL pins and the analog pins.

11.1 Test Mode Register Memory Map

Address	Register
0x00-0x7F	Normal Mode Registers
0x80	Master Test
0x81	Analog Test Register 0
0x82-0x84	Reserved
0x85	CSU Test Register 0
0x86	CRU Test Register 0
0x87-0x8B	Reserved
0x8C	TTOP Test Register 0
0x8D-0x8F	Reserved
0x90	RSOP Test Register 0
0x91	RSOP Test Register 1
0x92	RSOP Test Register 2

Address	Register
0x93	RSOP Test Register 3
0x94	TSOP Test Register 0
0x95	TSOP Test Register 1
0x96	TSOP Test Register 2
0x97	TSOP Test Register 3
0x98	RLOP Test Register 0
0x99	RLOP Test Register 1
0x9A	RLOP Test Register 2
0x9B-0x9F	Reserved
0xA0	TLOP Test Register 0
0xA1	TLOP Test Register 1
0xA2	TLOP Test Register 2
0xA3	TLOP Test Register 3
0xA4-0xA7	Reserved
0xA8	SSTB Test Register 0
0xA9	SSTB Test Register 1
0xAA	SSTB Test Register 2
0xAB	SSTB Test Register 3
0xAC-0xAF	Reserved
0xB0	RPOP Test Register 0
0xB1	RPOP Test Register 1
0xB2	RPOP Test Register 2
0xB3-0xBF	Reserved
0xC0	TPOP Test Register 0
0xC1	TPOP Test Register 1
0xC2	TPOP Test Register 2
0xC3	TPOP Test Register 3

Address	Register
0xC4	TPOP Test Register 4
0xC5-0xCF	Reserved
0xD0	RACP Test Register 0
0xD1	RACP Test Register 1
0xD2	RACP Test Register 2
0xD3	RACP Test Register 3
0xD4	RACP Test Register 4
0xD5-0xDF	Reserved
0xE0	TACP Test Register 0
0xE1	TACP Test Register 1
0xE2	TACP Test Register 2
0xE3	TACP Test Register 3
0xE4-0xE7	Reserved
0xE8	SPTB Test Register 0
0xE9	SPTB Test Register 1
0xEA	SPTB Test Register 2
0xEB	SPTB Test Register 3
0xEC-0xEF	Reserved
0xF0	BERM Test Register 0
0xF1	BERM Test Register 1
0xF2-0xFF	Reserved

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x80: Master Test

Bit	Type	Function	Default
Bit 7	R/W	TT_BYP	0
Bit 6		Unused	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-PLUS test features. All bits, except PMCTST and PMCATST, are reset to zero by a reset of the S/UNI-PLUS.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-PLUS . While the HIZIO bit is a logic one, all output pins of the S/UNI-PLUS except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-PLUS for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-PLUS to

drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the digital portion of the S/UNI-PLUS for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-PLUS microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST:

The PMCATST bit is used to configure the analog portion of the S/UNI-PLUS for PMC's manufacturing tests. When PMCATST is set to logic one, the S/UNI-PLUS microprocessor port becomes the test access port used to run the PMC manufacturing analog test vectors. The PMCATST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

TT_BYP:

The TT_BYP bit is used to bypass the glue logic on the TTOH and TTOHEN input pins to permit direct access to the TTOP block. When TT_BYP is set to logic one, the glue logic is bypassed, and TTOH and TTOHEN feed directly into the TTOP block. When TT_BYP is set to logic zero, the glue logic is not bypassed, and TTOH and TTOHEN pass through the glue logic before entering the TTOP block.

11.2 Test Mode 0 Details

In test mode 0, the S/UNI-PLUS allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the Master Test register should be set to logic one.

To enable test mode 0, the IOTST bit in the Master Test register is set to logic one and the following addresses must be written with 00H: 91H, 95H, 99H, A1H, A5H, A7H, A9H, B1H, C1H, D1H, E1H, E9H, F1H. Clock edges must be provided on inputs TFCLK and RFCLK.

Reading the following address locations returns the values on the indicated inputs:

Table 5 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07H					PIP[3]	PIP[2]	PIP[1]	PIP[0]
0FH							TTOH	TTOHEN
94H	TSUC[1]	TSOW[1]	TSD			TLAIS		
A0H		TLOW	TLD	TLDRI[2]				TCLK
C0H				TPRDI[3]	TPAIS			
C3H							TPOH[4]	TPOHEN[5]
C4H								TFP
D0H					BUS8			
E0H				XOFF	TGFC			

The following inputs cannot be read using the IOTST feature: TDAT[15:0], TSOC, TXPRTY[1:0], TWRENB, TFCLK, RFCLK, TSEN, RRDENB, D[7:0], A[7:0], ALE, CSB, WRB, RDB, RSTB, TRSTB, TMS, TCK, and TDI.

1. TOWCLK must be toggled to a logic zero and then back to a logic one in order to capture the value on these inputs.

2. To read TLDRI, AUTOLRDI must be set to 0 in the Master Auto Alarm/Monitor Register.

3. To read TPRDI, AUTOPRDI must be set to 0 in the Master Auto Alarm/Monitor Register.

4. To read TPOH, TPOHEN must be set to a logic one.

5. To read TPOHEN, TPTBEN must be set to 0 in the Master Configuration Register.

Writing the following address locations forces the outputs to the value in the corresponding bit position (zeros should be written to all unused test register locations):

Table 6 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07H	POP[3]	POP[2]	POP[1]	POP[0]				
90H			LOF	OOF	LOS			
92H			RSOW		RSD	RSDCLK	RSUC	
94H					TSDCLK			
96H								TOHFP
98H				LRDI	LAIS	ROHFP[3]		
9AH					RLD	RLDCLK	RLOW	ROWCLK
9BH						RTOHFP[3]	RTOHCLK[3]	RTOH[3]
A0H				TOWCLK	TLDCLK			
B0H				PAIS				
B2H			LOP					
B3H					PRDI	RPOHFP	RPOH	RPOHCLK
C2H							TTOHCLK	TTOHFP
C3H					TPOHCLK	TPOHFP		
D0H				RCP	RGFC		LCD	
E0H							TCP	INT[1]

The following outputs can not be controlled using the IOTST feature: TCA, RSOC, RDAT[15:0], RXPRTY[1:0], RCA, D[7:0], and TDO.

1. INT corresponds to output INTB. INTB is an open drain output and should be pulled high for proper operation. Writing a logic one to the INT bit allows the S/UNI-PLUS to drive INTB low. Writing a logic zero to the INT bit tristates the INTB output.

2. To control these outputs, RMODE[1:0] should be set to binary '10' in the Master Configuration Register.

3. To control GTOCLK, TMODE[1:0] should be set to binary '11' in the Master Configuration Register.

11.3 JTAG Test Port

The S/UNI-PLUS JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and

boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device boundary scan path can be bypassed. For more details on the JTAG port, please refer to the Operation section.

12 OPERATION

This section presents PCB design recommendations, tutorial information on the SONET/SDH transmission convergence sublayer for ATM, the SCI-PHY™ compliant cell data structures, and operating details for the JTAG boundary scan feature.

12.1 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines *must* be followed in order to ensure proper operation.

1. Connect digital and analog grounds together at a point where the ground reference is clean and as free as possible of digital return currents. Typically, this means as close as possible to the PCB connector where ground is brought into the card.

2. Provide separate +5 volt analog transmit, +5 volt analog receive, and +5 volt digital supplies, but otherwise connect the supply voltages together at a point where the supply is clean and as free as possible of digitally induced switching noise. Typically, this means as close as possible to the PCB connector where +5 volts is brought into the card. In some systems separate regulation is required for the transmit and receive analog supplies.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistor does not lower the supply voltage below the recommended operating voltage.

4. Ferrite beads are recommended for TAVD1, TAVD2, RAVD1 and RAVD2.

5. Separate high-frequency decoupling capacitors are recommended for each analog power (TAVD1, TAVD2, RAVD1 and RAVD2) pin as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into the reference circuitry powered by TAVD1 and RAVD1.

6. The high speed serial streams (TXD+/- and RXD+/) must be routed with controlled impedance circuit board traces and must be terminated with a

matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device.

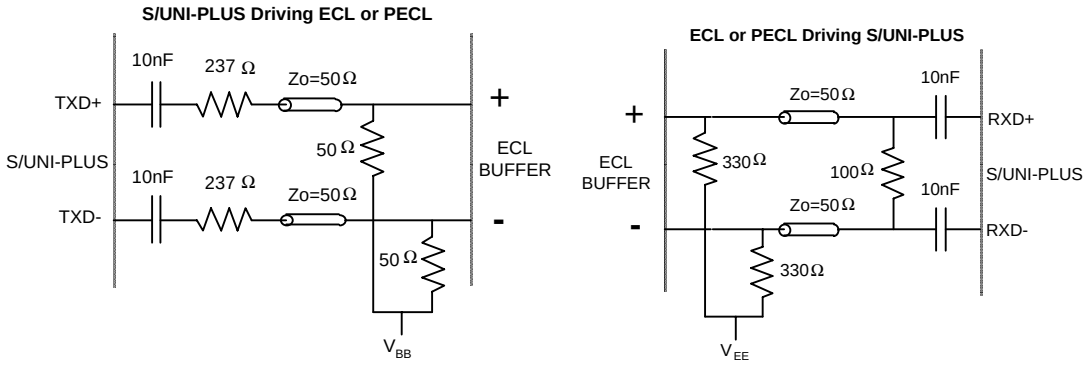
12.2 Interfacing to ECL or PECL Devices

Although the TXD+/- outputs are TTL compatible, only a few passive components are required to convert the signals to ECL (or PECL) logic levels. Figure 10 illustrates the recommended configuration. The capacitors AC couple the outputs so that the ECL inputs are free to swing around the ECL bias voltage (V_{BB}). The combination of the 237 Ω and 50 Ω resistors divide the voltage down to a nominally 800mV swing. The 50 Ω resistors also terminate the signals.

Similarly, the RXD+/- inputs to the S/UNI-PLUS are AC coupled as shown in Figure 10. The S/UNI-PLUS inputs are self-biasing to improve operating speed and waveform symmetry. For this reason, the DC blocking capacitors are always required, even when interfacing to PECL drivers. The only exception are the ALOS+/- inputs which must be DC coupled because of their low frequency content.

Ceramic coupling capacitors are recommended.

Figure 10 - Interfacing S/UNI-PLUS to ECL or PECL

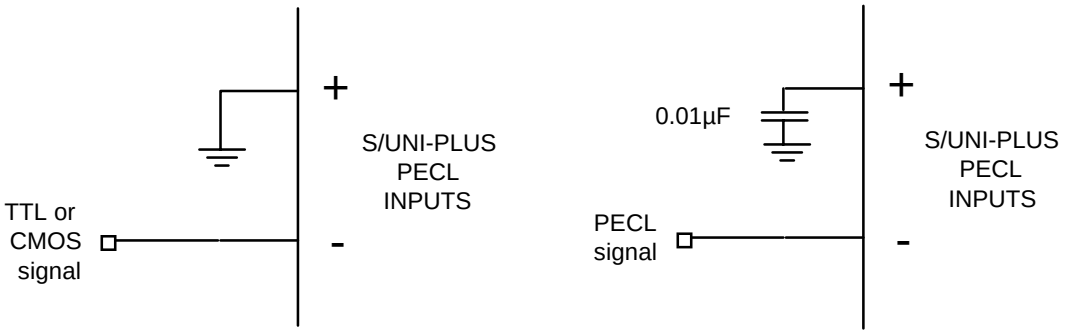


12.3 Driving Differential Inputs Single Ended

In some applications it may be more cost effective or technically desirable to drive the RRCLK+/-, TRCLK+/- or ALOS+/- inputs with a single ended PECL, TTL or CMOS signal. Figure 11 illustrates the suggested configuration to achieve this.

Note that the RXD+/- inputs do not support single ended operation and must always be driven by a differential source.

Figure 11 - Single Ended Driving Differential Inputs



For TTL or CMOS signals, the positive input must be grounded. The negative input should be connected directly to a TTL or CMOS signal. In the case where a single ended PECL source is to be used, the positive input should be decoupled to ground through a 0.01µF capacitor.

These configurations logically invert the input signal.

12.4 Clock Recovery

Figure 12 is an abstraction of the clock recovery phase lock loop illustrating the connections to external components. The figure illustrates the unity gain buffer loop filter application where the integral op-amp output is buffered through a unity gain amplifier to minimize the effect of its finite output impedance on the transfer function of the PLL. The unity gain buffer loop filter circuit typically exceeds SONET/SDH jitter tolerance and jitter transfer specifications and is recommended for all designs.

Figure 12 -

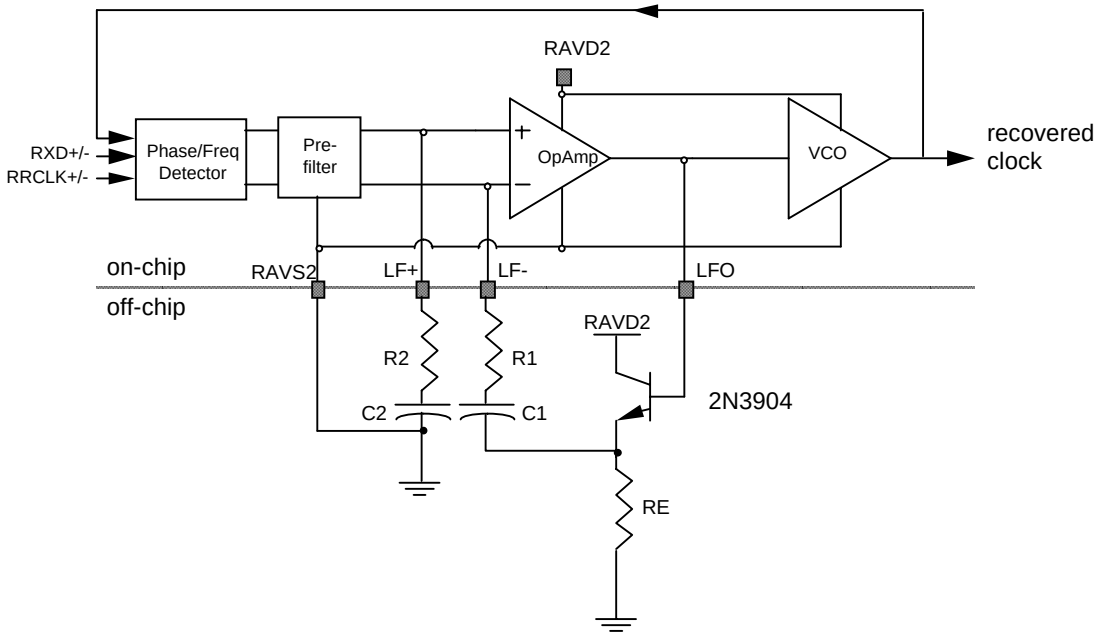


Table 7 -

Line Rate (Mbit/s)	R1 (Ω±1%)	R2 (Ω±1%)	C1, C2 min (µF)	RE (Ω±1%)
155.52	68.1	90.9	4.7	100
51.84	68.1	90.9	15	100

The capacitors (C1, C2) determine the amount of "peaking" in the jitter transfer curve. The capacitor values can be ±10%. The capacitors should be non-polarized because when the S/UNI-PLUS is held in reset, the capacitors are reverse-biased at approximately 2.0V. Also, for some process extremes, the capacitors may operate with a D.C. reverse-bias of up to 1.0V.

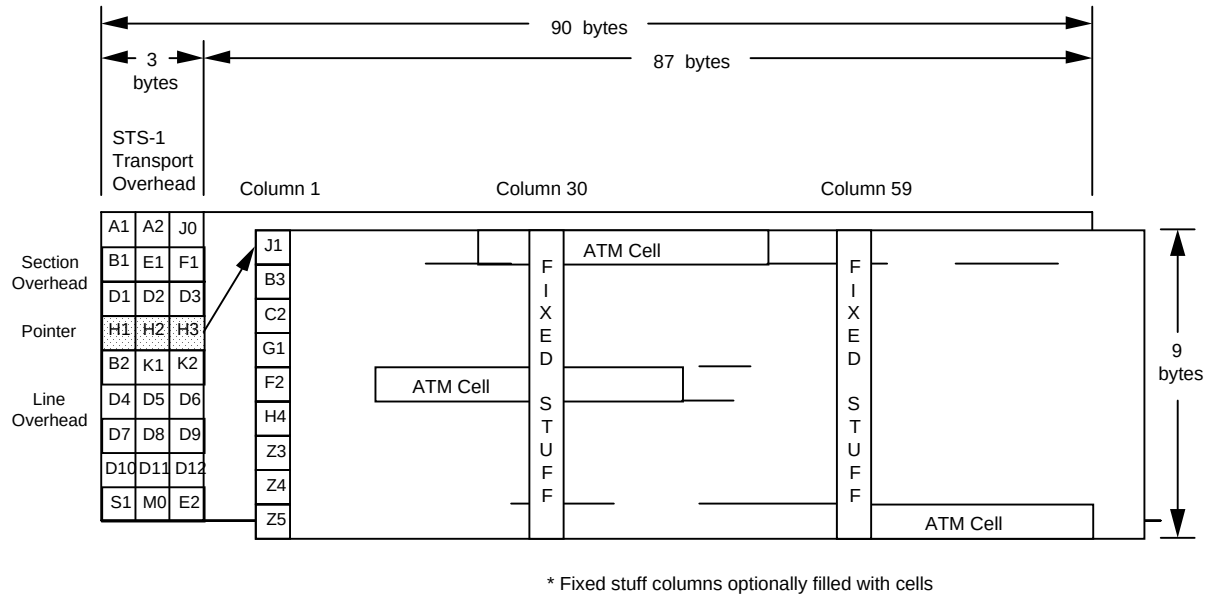
12.5 ATM Mapping and Overhead Byte Usage

The S/UNI-PLUS processes the ATM cell mappings for STS-3c (STM-1) and STS-1 as shown below in figures 12 and 13. The S/UNI-PLUS processes the transport and path overhead required to support ATM UNIs and NNIs. In addition, the S/UNI-PLUS provides support for the APS bytes, the data

communication channels and provides full external control and observability of the transport and path overhead bytes.

In Figure 13, the STS-1 mapping is displayed. The S/UNI-PLUS supports two STS-1 mappings, one with the indicated stuff columns containing fixed stuff bytes and the other with the indicated stuff columns used for ATM cells.

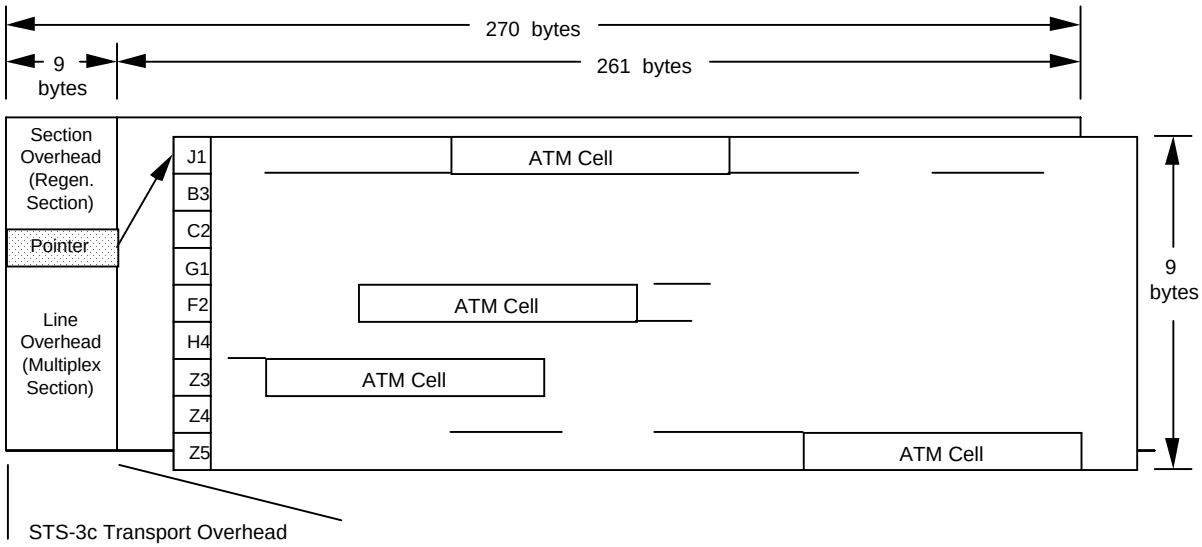
Figure 13 - STS-1 Mapping



* Fixed stuff columns optionally filled with cells

In Figure 14, the STS-3c (STM-1) mapping is shown. In this mapping, no stuff columns are included in the SPE. The entire SPE is used for ATM cells.

Figure 14 - STS-3c (STM-1) Mapping



STS-3c Transport Overhead
STM-1 Section Overhead

A1	A1	A1	A2	A2	A2	J0	Z0	Z0
B1			E1			F1		
D1			D2			D3		
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2	K1			K2		
D4			D5			D6		
D7			D8			D9		
D10			D11			D12		
S1	Z1	Z1	Z2	Z2	M1	E2		

Transport Overhead Bytes

A1, A2: The frame alignment bytes (A1, A2) locate the SONET frame in the STS-3c/1 (STM-1) serial stream.

J0 The J0 byte is currently defined as the STS-1/STM-1 section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler.

Z0: The Z0 bytes are currently defined as the STM-1 section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler.

B1:	The section bit interleaved parity byte provides a section error monitoring function.
E1:	The section orderwire byte provides a 64 kbit/s craftperson voice channel for network element to network element communication.
F1:	The section user channel byte provides a 64 kbit/s data channel for use by the network provider.
D1 - D3:	The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications.
H1, H2:	The pointer value bytes locate the path overhead column in the SONET/SDH frame.
H3:	The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.
B2:	The line bit interleaved parity bytes provide a line error monitoring function.
K1, K2:	The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.
D4 - D12:	The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications.
S1:	The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of the STS-3c/1 (STM-1) signal. Bits 1 through 4 are currently undefined.

Z1: The Z1 bytes are located in the second and third STS-1s of a STS-3c (STM-1) and are allocated for future growth.

M0: The M0 byte is defined only for STS-1, and bits 5 through 8 provide a line far end block error function for remote performance monitoring. Bits 1 through 4 are currently undefined.

M1: The M1 byte is located in the third STS-1 of a STS-3c (STM-1) and provides a line far end block error function for remote performance monitoring.

Z2: The Z2 bytes are located in the first and second STS-1s of a STS-3c (STM-1) and are allocated for future growth.

E2: The line orderwire byte provides a 64 kbit/s craftperson voice channel for network element to network element communication.

Path Overhead Bytes

J1: The Path Trace byte is used to repetitively transmit a 64-byte CLLI message (for SONET networks), or a 16-byte E.164 address (for SDH networks). When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00.

B3: The path bit interleaved parity byte provides a path error monitoring function.

C2: The path signal label indicator identifies the equipped payload type. For ATM payloads, the identification code is 0x13.

G1: The path status byte provides a path FEBE function, and a path remote defect indication function. Two bits are allocated for remote defect indications: bit 5 (the path RDI bit) and bit 6 (the auxiliary path RDI bit). Taken together these bits provide a four state path RDI code that can be used to categorize path defect indications.

F2: The path user channel byte provides a 64 kbit/s data channel for use by the network provider.

H4: The multiframe indicator byte is a payload specific byte, and is not used for ATM payloads. This byte is forced to 0x00 in the transmit direction, and is ignored in the receive direction.

Z3 - Z5: The path growth bytes provide three unused bytes for future use.

12.6 Cell Data Structure

ATM cells may be passed to/from the S/UNI-PLUS using a twenty-seven word data structure or a fifty-three word data structure. These data structures are shown in Figure 15 and Figure 16.

Figure 15 - 16-bit Wide, 27 Word Structure

	Bit 15 — Bit 8	Bit 7 — Bit 0
Word 1	**H1**	**H2**
Word 2	**H3**	**H4**
Word 3	**H5**	**HCS STATUS/CONTROL**
Word 4	**PAYLOAD1**	**PAYLOAD2**
Word 5	**PAYLOAD3**	**PAYLOAD4**
Word 6	**PAYLOAD5**	**PAYLOAD6**
⋮	⋮	⋮
Word 27	**PAYLOAD47**	**PAYLOAD48**

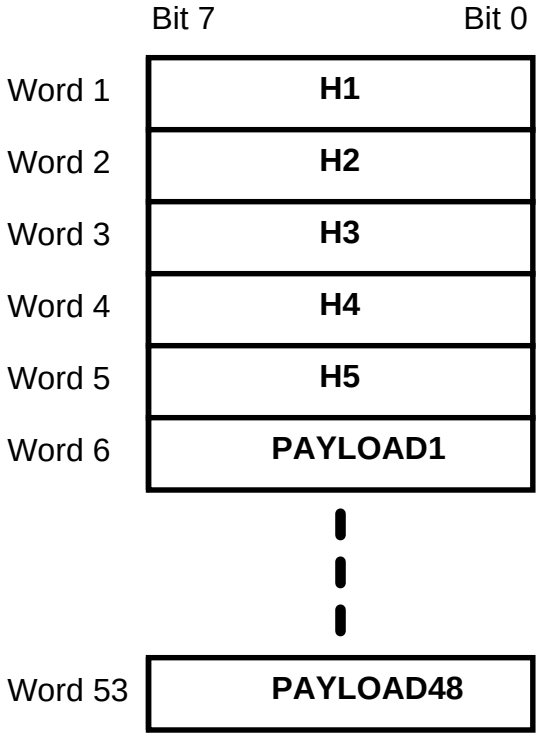
The 16-bit SCI-PHY compliant data structure is selected when the BUS8 input is tied low. Bit 15 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC

and RSOC) are coincident with Word 1 (containing the first two header octets). Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction, the lower 8 bits of Word 3 contain the HCS status octet. An all-zeros pattern in these 8 bits indicates that the associated header is error free. An all-ones pattern indicates that the header contains an uncorrectable error (if the HCSPASS bit in the RACP Control Register is set to logic zero, the all-ones pattern will never be passed in this structure). An alternating ones and zeros pattern (0xAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, the HCS bit in the TACP Control register determines whether the HCS is calculated internally or is inserted directly from the upper 8 bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position (for example a logic one in bit 7 causes the most significant bit of the HCS to be inverted).

Figure 16 - 8-bit Wide, 53 Word Structure



The 8-bit SCI-PHY compliant data structure is selected when the BUS8 input is tied high. Bit 7 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first cell header octet). Word 5 of this structure contains the HCS octet.

In the receive direction, cells containing "detected and uncorrected" header errors are dropped when the HCSPASS bit in the RACP Control/Status Register is set to logic zero. No HCS status information is passed within this data structure. Error free headers and "detected and corrected" headers are passed when HCSPASS is a logic zero. Error free headers, "detected and corrected" headers, and "detected and uncorrected" headers are passed when HCSPASS is a logic one.

In the transmit direction, the HCS bit in the TACP Control Register determines whether the HCS is calculated internally or is inserted directly from Word 5.

12.7 Bit Error Rate Monitor

The S/UNI-PLUS Bit Error Rate Monitor (BERM) block counts line BIP errors over programmable periods of time and monitors whether the accumulated count of line BIP errors exceeds a programmable threshold within that specific period. The BERM block can be used to trigger an interrupt when the bit error rate (BER) of the line is ±50% of the programmed rate. The following tables list the recommended contents of the BERM Line BIP Accumulation Period and BERM Line BIP Threshold Period registers to detect various BERs.

In STS-1 mode, the following register contents are recommended:

Table 8 -

BER	Accumulation Period LSB	Accumulation Period MSB	Threshold LSB	Threshold MSB
10^{-4}	0x87	0x01	0xCA	0x00
10^{-5}	0x19	0x0F	0xD9	0x00
10^{-6}	0xFA	0x9C	0xDB	0x00

In STS-3c mode, the following register contents are recommended:

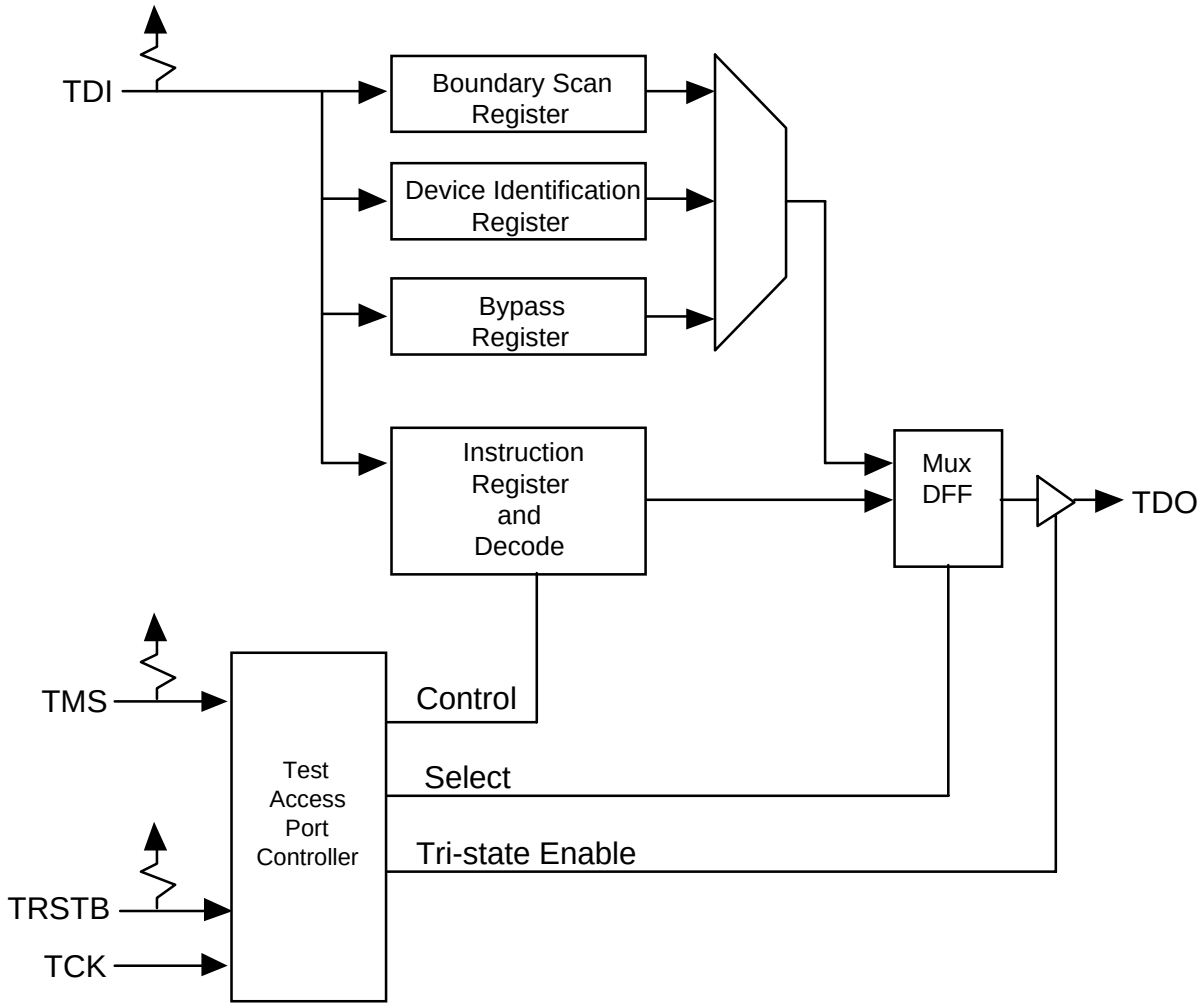
Table 9 -

BER	Accumulation Period LSB	Accumulation Period MSB	Threshold LSB	Threshold MSB
10^{-4}	0x85	0x00	0xCA	0x00
10^{-5}	0x08	0x05	0xD9	0x00
10^{-6}	0x53	0x34	0xDB	0x00

12.8 JTAG Support

The S/UNI-PLUS supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO, used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 17.

Figure 17 - Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output , TDO. The device identification register contains the device identification code.

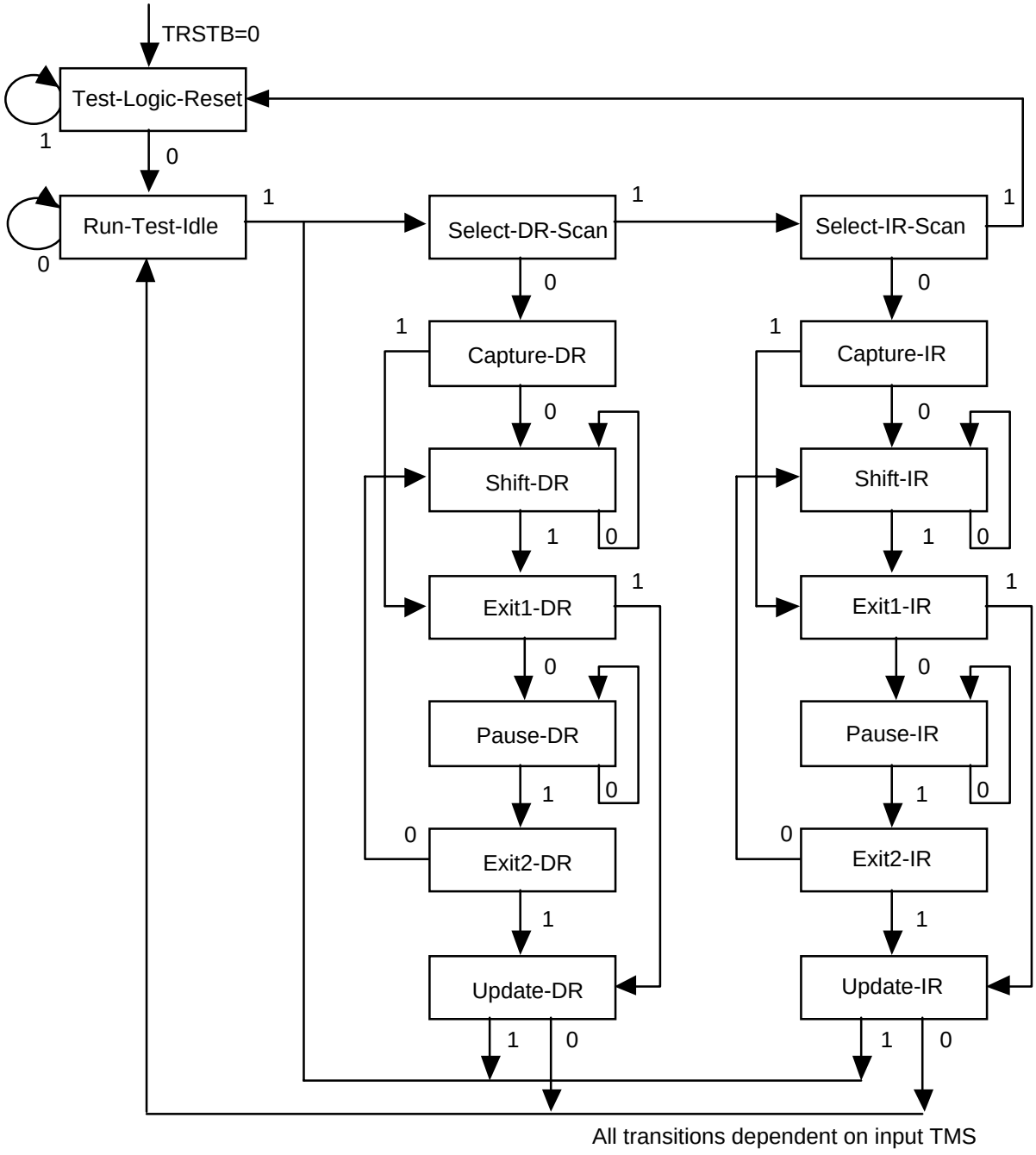
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device

inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described in Figure 18.

Figure 18 - TAP Controller Finite State Machine



Test-Logic-Reset: The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is

entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle: The run test/idle state is used to execute tests.

Capture-DR: The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR: The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR: The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR: The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR: The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR: The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

The TDO output is enabled during states Shift-DR and Shift-IR. Otherwise, it is tri-stated.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects an serial test data register path between input, TDI, and output, TDO.

BYPASS — The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST — The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input TDI and output TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE — The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE — The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST — The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan

register. The code can then be shifted out on output TDO using the Shift-DR state.

Table 10 - Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 0x0

Part Number - 0x5347

Manufacturer's identification code - 0x0CD

Device identification - 0x053470CD

Boundary Scan Register

The boundary scan register is made up of 139 boundary scan cells, divided into input observation (in_cell), output (out_cell), and bidirectional (io_cell) cells. These cells are detailed in the Figures 22, 23, 24 and 25. The first 32 cells form the ID code register, and carry the code 0x053470CD. The cells are arranged as follows:

Table 11 -

Pin/ Enable	Register Bit	Cell Type	I.D. Bit(s)	Pin/ Enable	Register Bit	Cell Type	I.D. Bit(s)
A[7:0][1]	138-131	IN_CELL	00000101	txcn	58	out_CELL	-
ALE	130	IN_CELL	0	txdp	57	OUT_CELL	-
CSB	129	IN_CELL	0	txdn	56	OUT_CELL	-
WRB	128	IN_CELL	1	tohfp	55	OUT_CELL	-
RDB	127	IN_CELL	1	tsdclk	54	out_CELL	-
RSTB	126	IN_CELL	0	tbyp	53	in_cell	-
D[7:0]	125-118	IO_CELL	10001110	rbyp	52	in_CELL	-
PIP[3:0]	117-114	IN_CELL	0001	rxdon	51	out_CELL	-
POP[3:0]	113-110	OUT_CELL	1001	rxdop	50	out_CELL	-
OENB[2]	109	OUT_CELL	1	los	49	OUT_CELL	-
INTB	108	OUT_CELL	0	rsow	48	out_CELL	-
HIZ[3]	107	OUT_CELL	1	rsuc	47	out_CELL	-
TDAT[15:0]	106-91	IN_CELL	-	lof	46	out_CELL	-
xoff	90	in_cell	-	rsdclk	45	OUT_CELL	-
tsoc	89	in_CELL	-	rsd	44	out_CELL	-
txprty[1:0]	88-87	in_CELL	-	lrdi	43	OUT_CELL	-
twrenb	86	in_CELL	-	rlow	42	out_CELL	-
tfclk	85	in_CELL	-	rowclk	41	OUT_CELL	-
bus8	84	in_CELL	-	rld	40	out_CELL	-
tgfc	83	IN_CELL	-	rldclk	39	OUT_CELL	-
tca	82	out_CELL	-	lais	38	out_CELL	-
tcp	81	out_CELL	-	rohfp	37	OUT_CELL	-
tpoh	80	In_CELL	-	groclk	36	out_CELL	
tpohen	79	in_CELL	-	rtohfp	35	OUT_CELL	-
tprdi	78	in_CELL	-	rtohclk	34	out_CELL	-
tpais	77	in_CELL	-	rtoh	33	OUT_CELL	-
tfp	76	IN_CELL	-	rpoh	32	OUT_CELL	-
tpohfp	75	out_cell	-	rpohfp	31	OUT_CELL	-
tpohclk	74	out_celL	-	rpohclk	30	out_cell	-
ttohen	73	in_cell	-	prdi	29	out_cell	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit(s)	Pin/ Enable	Register Bit	Cell Type	I.D. Bit(s)
ttoh	72	in_cell	-	pais	28	out_cell	-
ttohclk	71	out_cell	-	lop	27	out_cell	-
ttohfp	70	out_cell	-	RFCLK	26	in_cell	-
gtoclk	69	out_cell	-	RRDENB	25	in_cell	-
tld	68	in_cell	-	tsen	24	in_cell	-
tlow	67	in_cell	-	RGFC	23	out_cell	-
tsow	66	in_cell	-	RCP	22	out_cell	-
tsuc	65	in_cell	-	LCD	21	out_cell	-
tlrdi	64	in_cell	-	RSOC	20	out_cell	-
tlais	63	in_cell	-	rdat[15:0]	19-4	out_cell	-
TLDCLK	62	out_cell	-	rxprty[1:0]	3-2	out_cell	-
TOWCLK	61	out_cell	-	rdatenb[4]	1	out_cell	-
TsD	60	in_cell	-	rca	0	out_cell	-
TXcp	59	out_cell	-				

Notes:

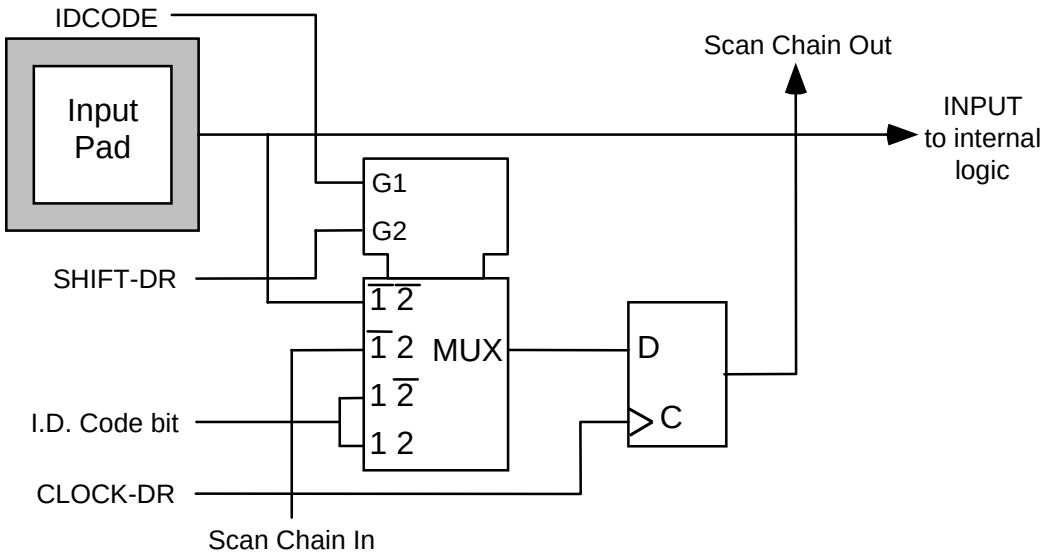
1. A[7] is the first bit of the boundary scan chain.

2. OENB signal will set the bidirectional D[7:0] pins to an output when set low.

3. When set high, TCA, TCP, TPOHFP, TPOHCLK, TTOHCLK, TTOHFP, GTOCLK, TLDCLK, TOWCLK, TXC+/-, TXD+/-, TOHFP, TSDCLK, RXDO+/-, LOS, RSOW, RSUC, LOF, RSDCLK, RSD, LRDI, RLOW, ROWCLK, RLD, RLDCLK, LAIS, ROHFP, GROCLK, RTOHFP, RTOHCLK, RTOH, RPOH, RPOHFP, RPOHCLK, PRDI, PAIS, LOP, RGFC, RCP, LCD, RCA, POP[3:0] and INTB will be set to high impedance.

4. When set high, RDAT[15:0], RXPRTY[1:0] and RSOC will be set to high impedance.

Figure 19 - Input Observation Cell (IN_CELL)



In this diagram and those that follow, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

Figure 20 - Output Cell (OUT_CELL)

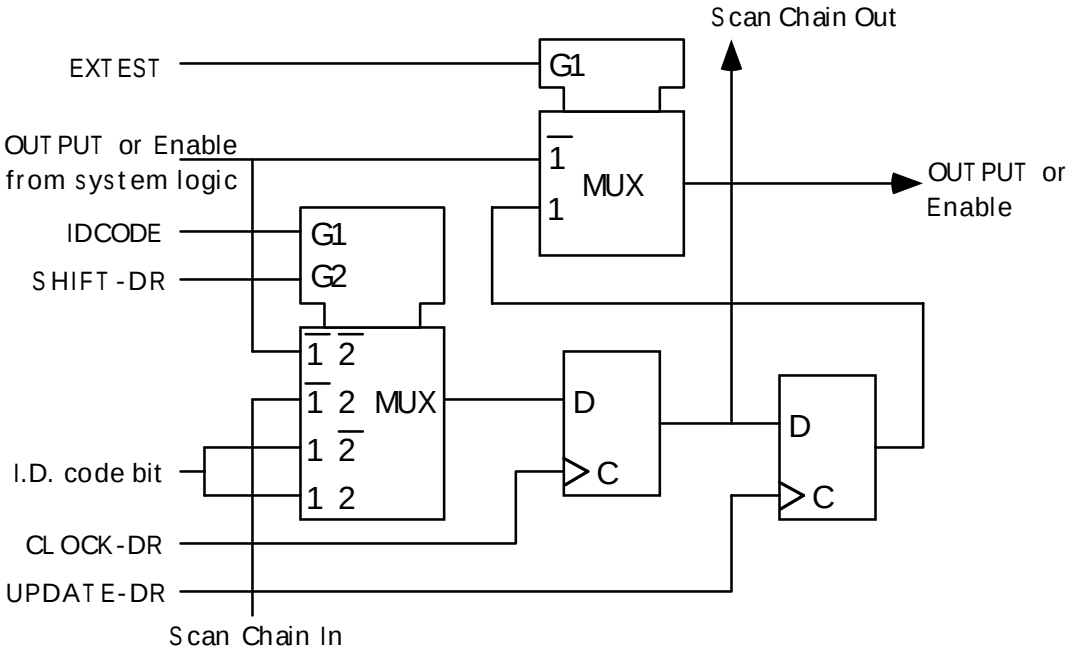
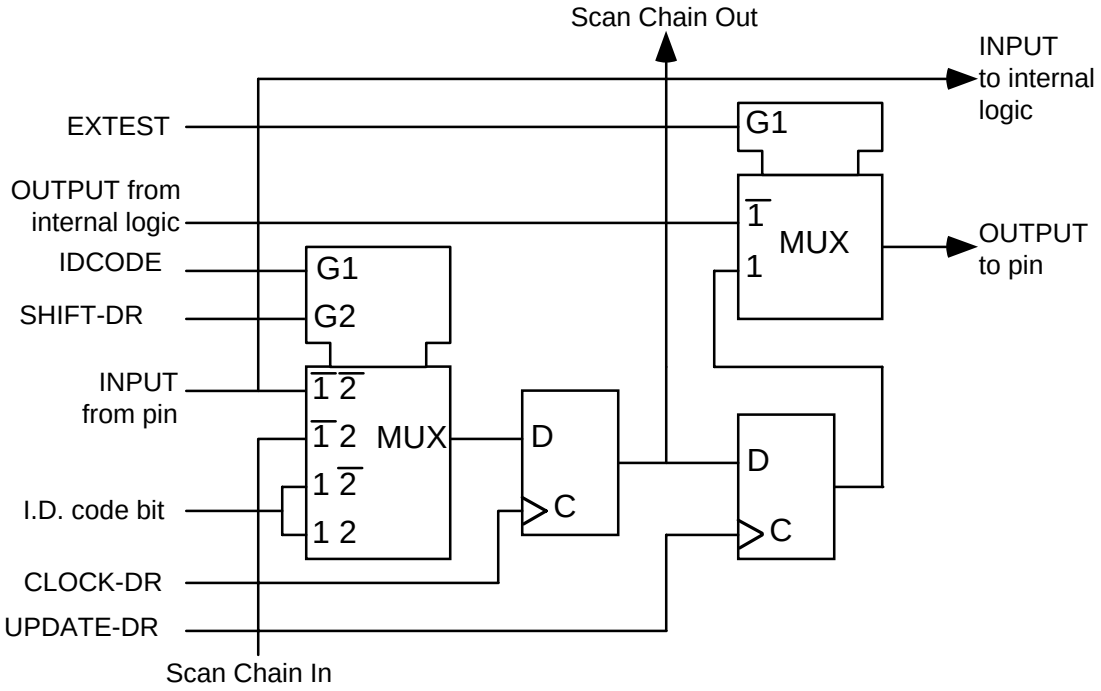


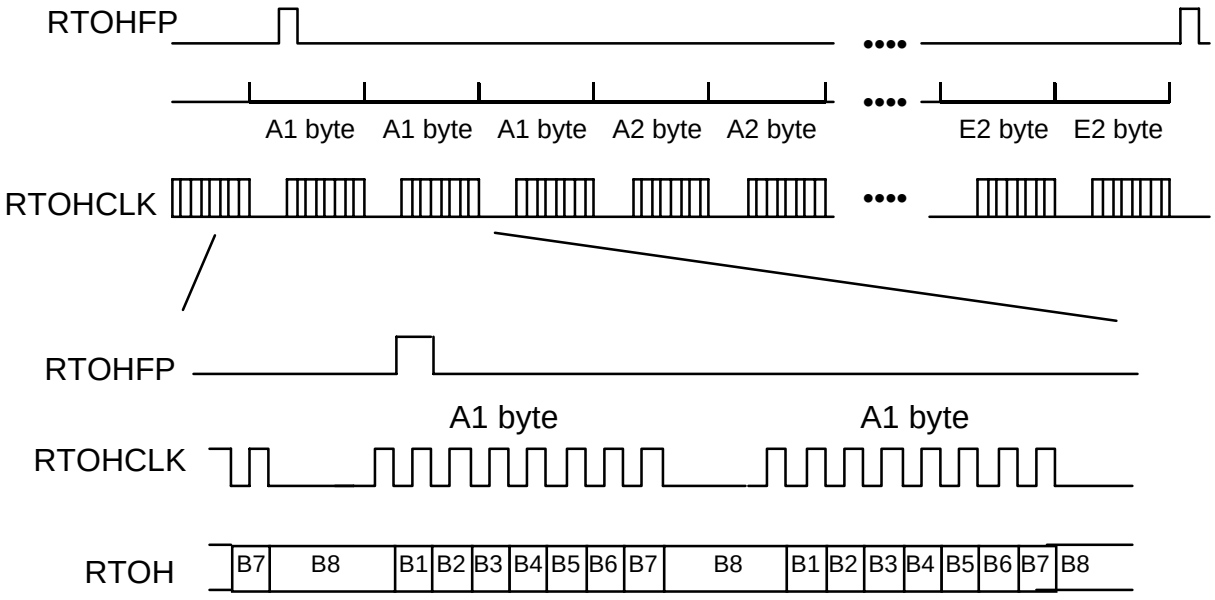
Figure 21 - Bidirectional Cell (IO_CELL)



13 FUNCTIONAL TIMING

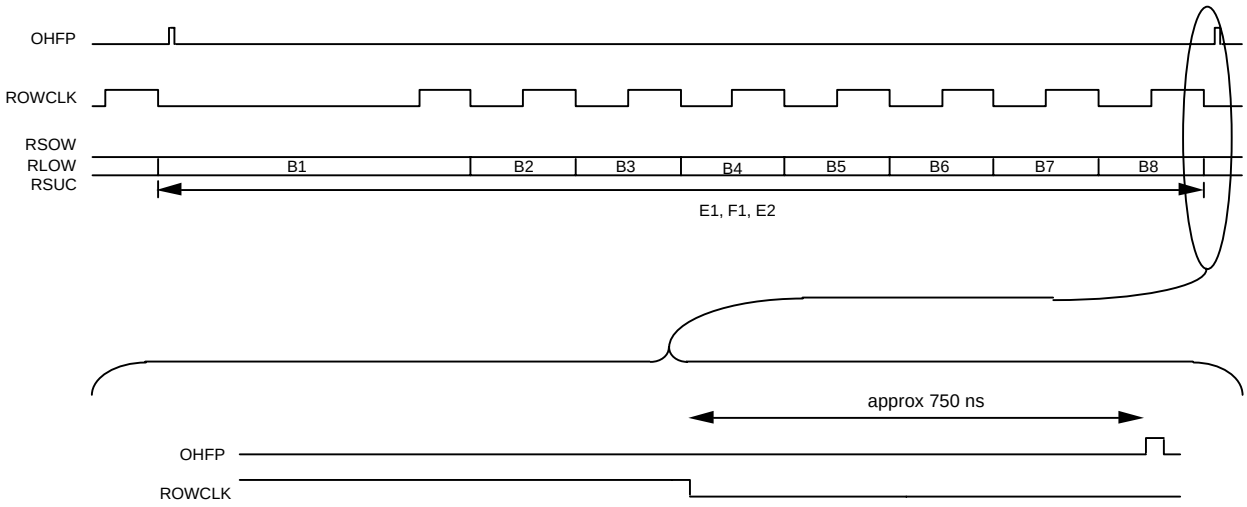
13.1 Overhead Access

Figure 22 - Transport Overhead Extraction



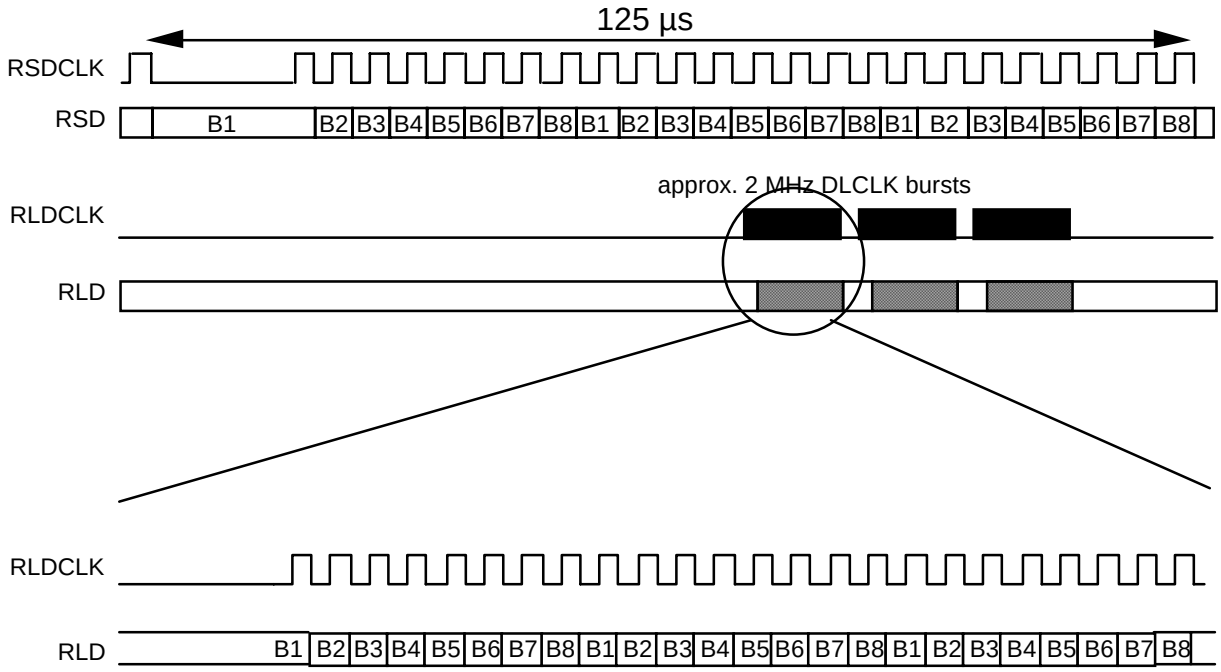
The Transport Overhead Extraction timing diagram (Figure 22) illustrates the transport overhead extraction interface. The transport overhead extraction clock, RTOHCLK is nominally a 5.184 MHz (1.728 MHz for an STS-1 stream) clock and is derived from the recovered line clock, GROCLK. The entire 9 row by 9 (or 3) column transport overhead structure is extracted and serialized on RTOH over a frame period (125 µs).

Figure 23 - Transport Overhead Orderwire and User Channel Extraction



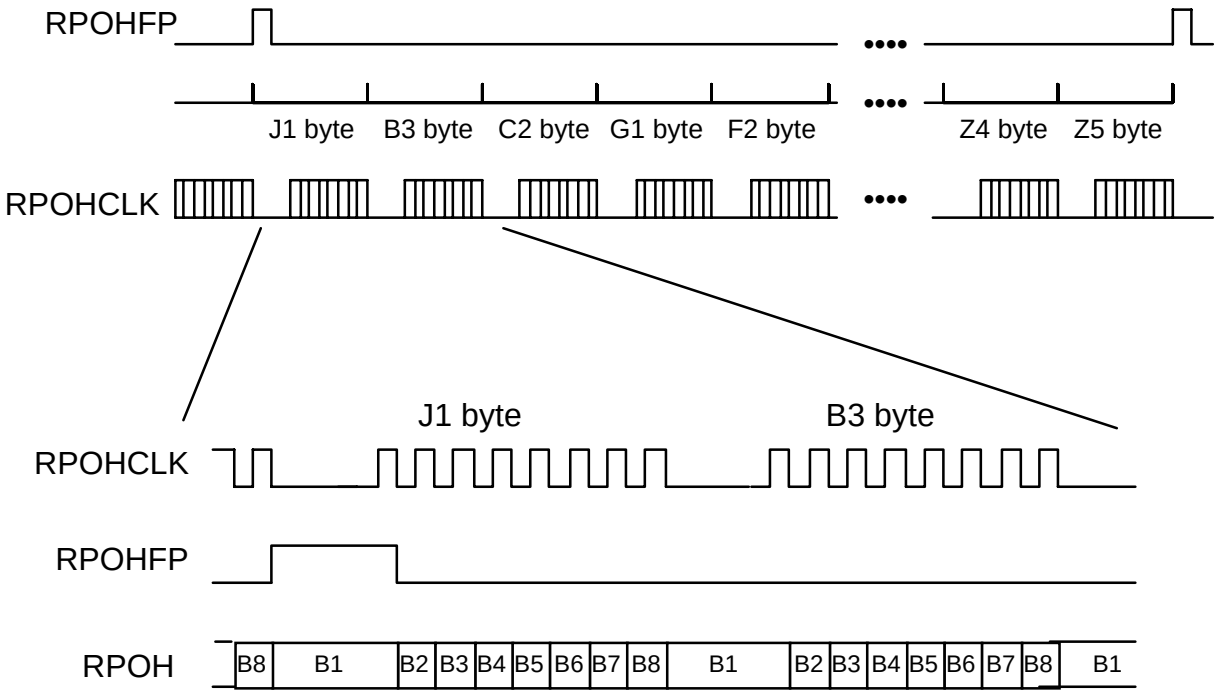
The Transport Overhead Orderwire and User Channel Extraction diagram (Figure 23) shows the relationship between the RSOW, RSUC and RLOW serial data outputs and their associated clock, ROWCLK. ROWCLK is a 72 kHz 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate and is aligned as shown in the timing diagram. The E1, F1 and E2 bytes shifted out of the S/UNI-PLUS on RSOW, RSUC and RLOW in the frame shown are extracted from the corresponding transport overhead channels in the previous frame.

Figure 24 - Transport Overhead Data Link Clock and Data Extraction



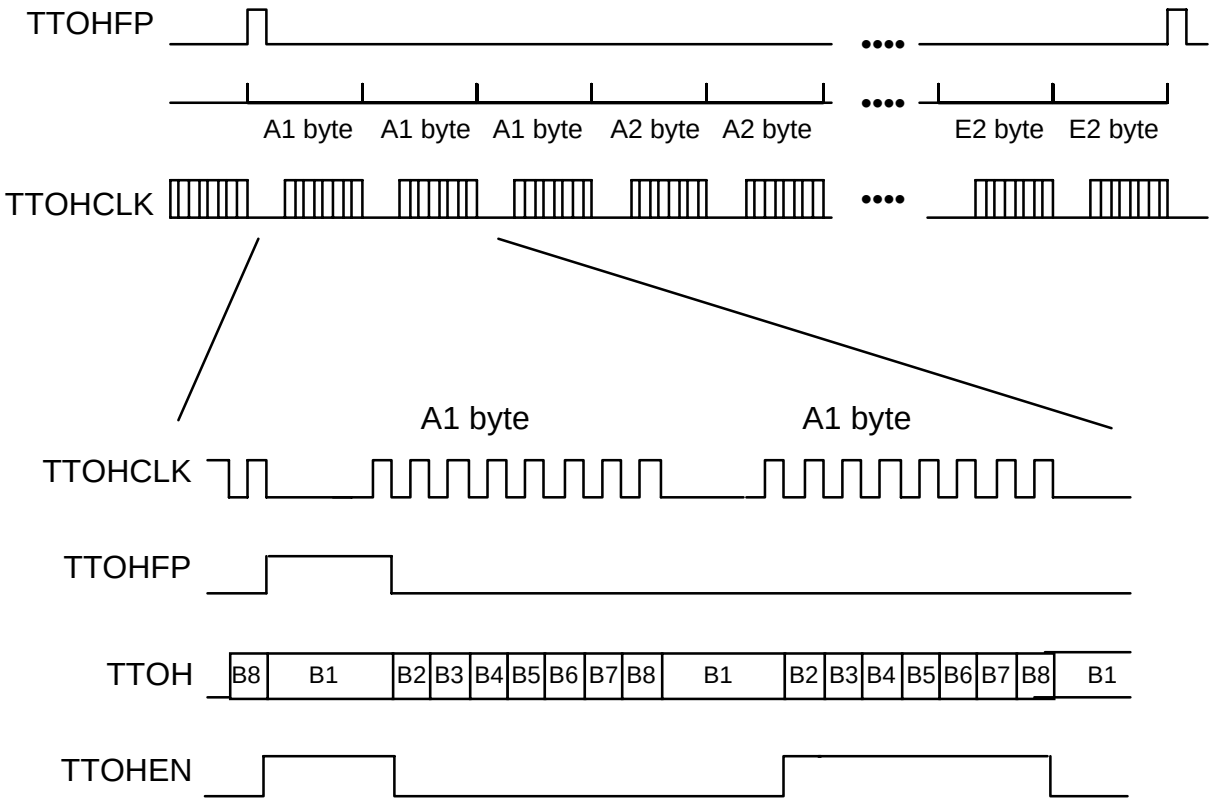
The Transport Overhead Data Link Clock and Data Extraction timing diagram (Figure 24) shows the relationship between the RSD, and RLD serial data outputs, and their associated clocks, RSDCLK and RLDCLK. RSDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate. RLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate. RSD (RLD) is updated on the falling RSDCLK (RLDCLK) edge. The D1-D3, and D4-D12 bytes shifted out of the S/UNI-PLUS in the frame shown are extracted from the corresponding receive line overhead channels in the previous frame.

Figure 25 - Path Overhead Extraction



The Path Overhead Extraction Timing Diagram (Figure 25) illustrates the path overhead extraction interface. The path overhead extraction clock, RPOHCLK is nominally a 576 kHz clock, and is derived from the recovered line clock, GROCLK. The entire path overhead (the complete 9 byte structure) is extracted, serialized and output on RPOH over a frame time.

Figure 26 - Transport Overhead Insertion

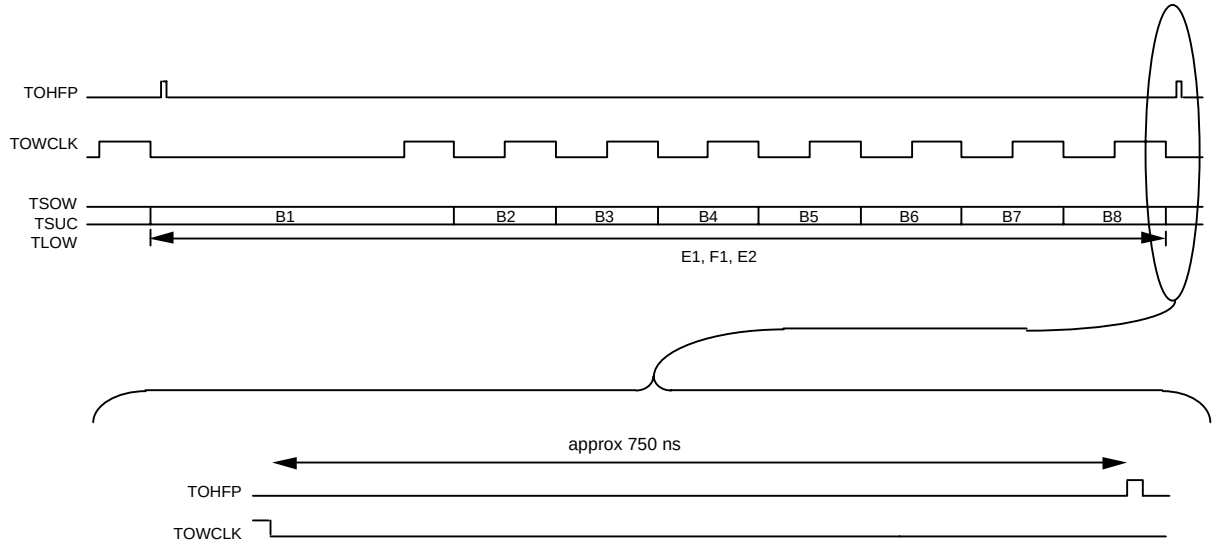


The transport overhead insertion timing diagram (Figure 26) illustrates the transport overhead insertion interface. Output TTOHCLK is nominally a 5.184 MHz clock (1.728 MHz for an STS-1 stream) and is used to update output TTOHFP, and to sample inputs TTOH and TTOHEN. The value sampled on TTOHEN during the first overhead bit position of a given set of overhead bytes determines whether the values sampled on TTOH are inserted in the transmit stream. TTOHEN is held high during the bit 1 position of the first A1 byte in the TTOH stream. The eight bit values sampled on input TTOH during the first A1 byte period are inserted in the first A1 byte position in the transmit stream. Similarly, TTOHEN is held low during the bit 1 position of the second A1 byte. The default value (F6H) is inserted in the second A1 byte position in the transmit stream.

An error insertion feature is also provided for the B1, H1, H2, and B2 byte positions. When TTOH is held high during any of the bit positions corresponding to these bytes, the corresponding bit is inverted before being inserted in the

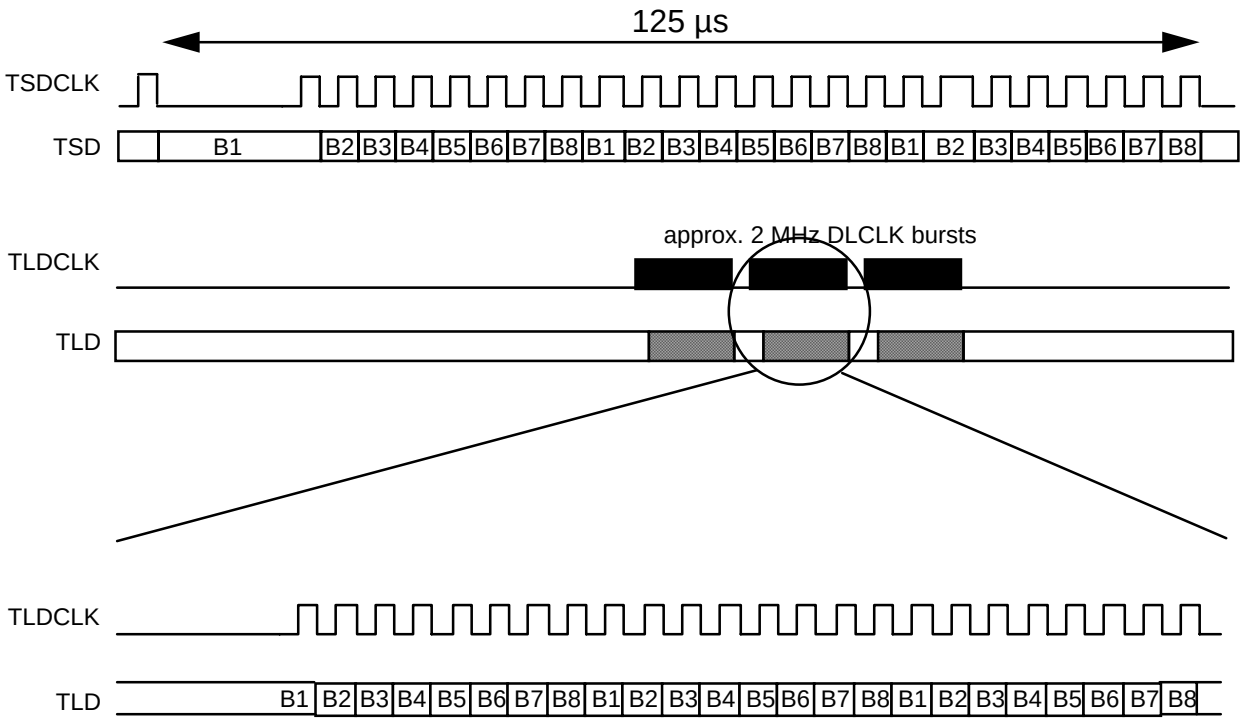
transmit stream (TTOHEN must be sampled high during the first bit position to enable the error insertion mask).

Figure 27 - Transport Overhead Orderwire and User Channel Insertion



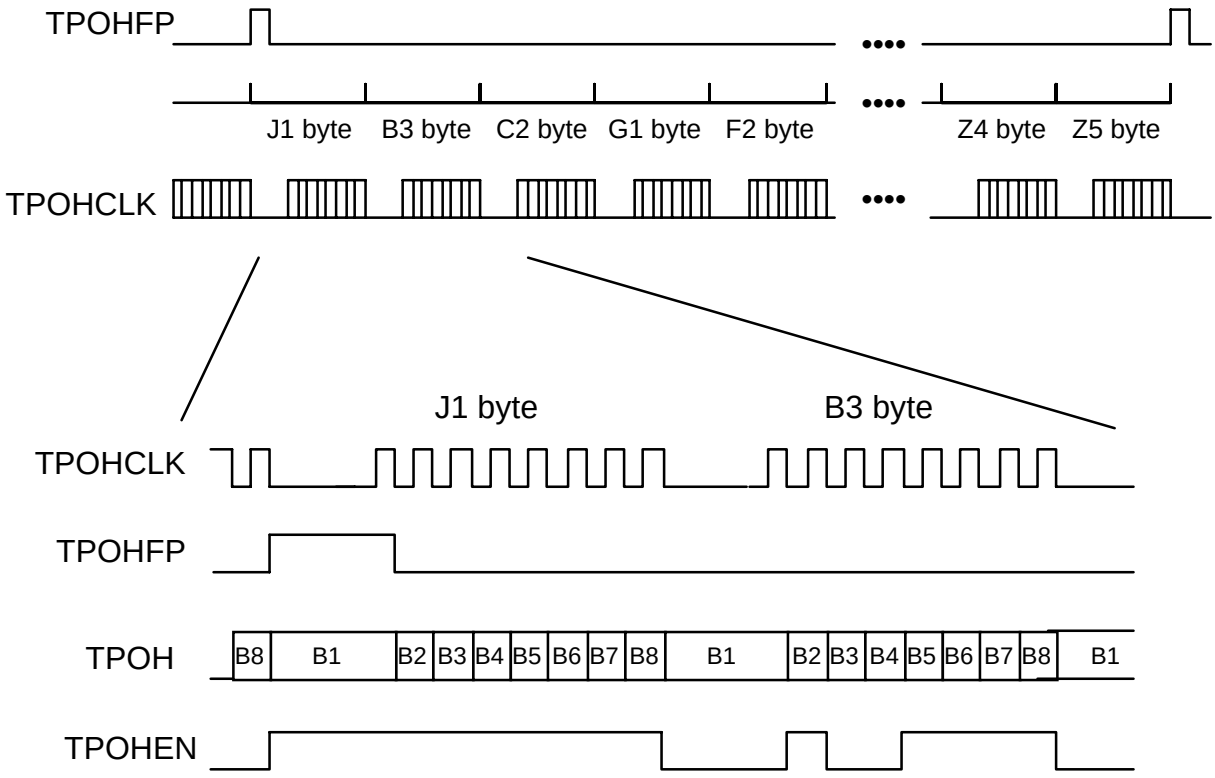
The Transport Overhead Orderwire and User Channel Insertion diagram (Figure 27) shows the relationship between the TSOW, TLOW and TSUC serial data inputs and their associated clock TOWCLK. TOWCLK is a 72 kHz 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate and is aligned as shown in the timing diagram. The E1, E2 and F1 bytes shifted into the S/UNI-PLUS on TSOW, TLOW and TSUC in the frame shown are inserted in the corresponding transport overhead channels in the next frame.

Figure 28 - Transport Overhead Data Link Clock and Data Insertion



The Transport Overhead Data Link Clock and Data Insertion timing diagram (Figure 28) shows the relationship between the TSD, and TLD serial data inputs, and their associated clocks, TSDCLK and TLDCLK respectively. TSDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate. TLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate. TSD (TLD) is sampled on the rising TSDCLK (TLDCLK) edge. The D1-D3, and D4-D12 bytes shifted into the S/UNI-PLUS in the frame shown are inserted in the corresponding transport overhead channels in the following frame.

Figure 29 - Path Overhead Insertion

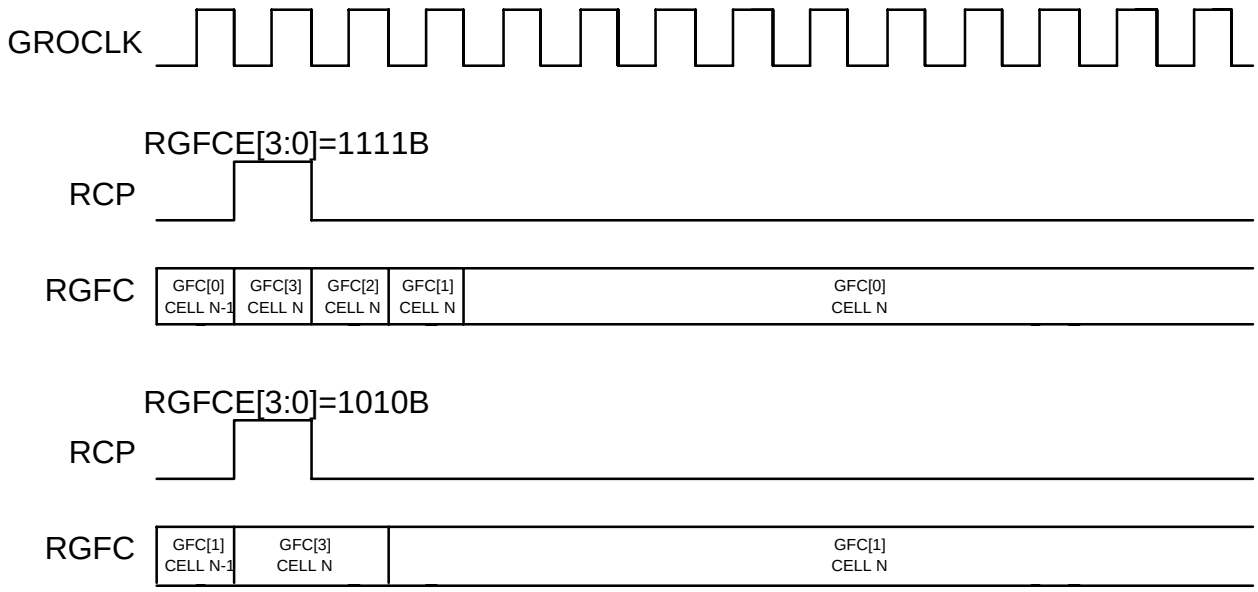


The Path Overhead Insertion Timing Diagram (Figure 29) illustrates the path overhead insertion interface. Output TPOHCLK is nominally a 576 kHz clock, and is used to update output TPOHFP, and to sample inputs TPOH and TPOHEN. In the figure, TPOHEN is held high throughout the eight bit positions of the J1 byte. The eight bit values sampled on input TPOH are inserted in the J1 byte position in the transmit stream. If TPOHEN was low during any of the 8 bit locations, the internally generated bit values of the corresponding bit positions would be inserted in the J1 byte.

For the B3 byte position, an error insertion feature is provided. TPOHEN is held high during bit positions 2, 5, 6, 7, and 8 of the B3 byte. The values sampled on input TPOH are used as an error mask in the corresponding bit positions (2, 5, 6, 7, and 8) of the B3 byte in the transmit stream. If TPOH and TPOHEN are high during a bit location, the corresponding bit of the internally generated B3 byte is inverted before transmission.

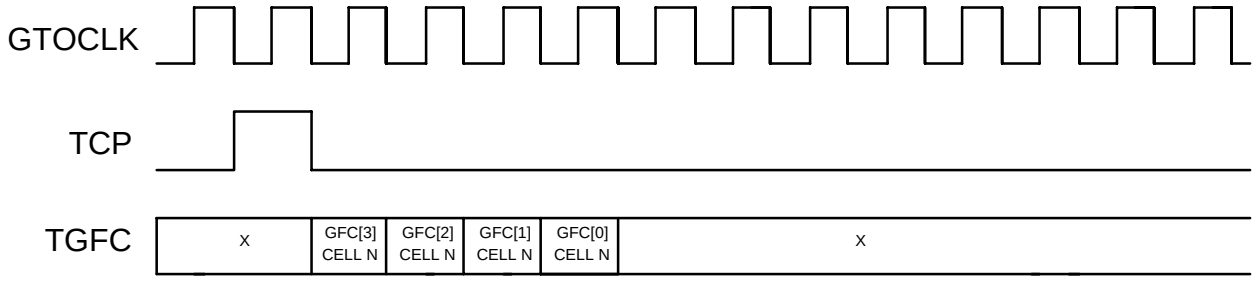
13.2 GFC Access

Figure 30 - GFC Extraction Port



The GFC Extraction Port Diagram (Figure 30) illustrates the relationship between the receive cell pulse, RCP signal and the receive serial GFC output. The RCP signal identifies the most significant GFC bit in the GFC field of a cell header. Whether a GFC bit is output or not is control by the RGFCE[3:0] bits in the RACP GFC Control register.

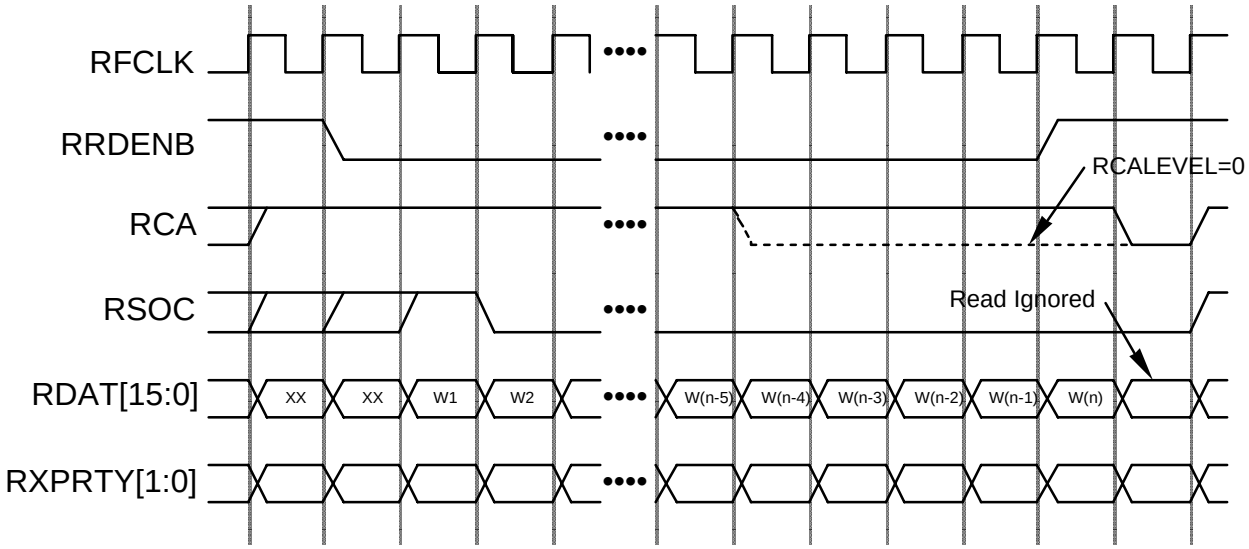
Figure 31 - GFC Insertion Port



The GFC Insertion Port Diagram (Figure 31) illustrates the relationship between the transmit cell pulse, TCP output and the transmit generic flow control, TGFC input. The MSB (GFC[3]) of the four bit GFC code on the TGFC input is identified using the TCP output. The S/UNI-PLUS accumulates the code and transmits the code in the next transmit cell. If the next transmit cell is an idle/unassigned cell, the GFC code provided in the Idle/Unassigned Cell Header Pattern register is overwritten. If the next transmit cell is read from the FIFO, the GFC code passed through the FIFO is overwritten.

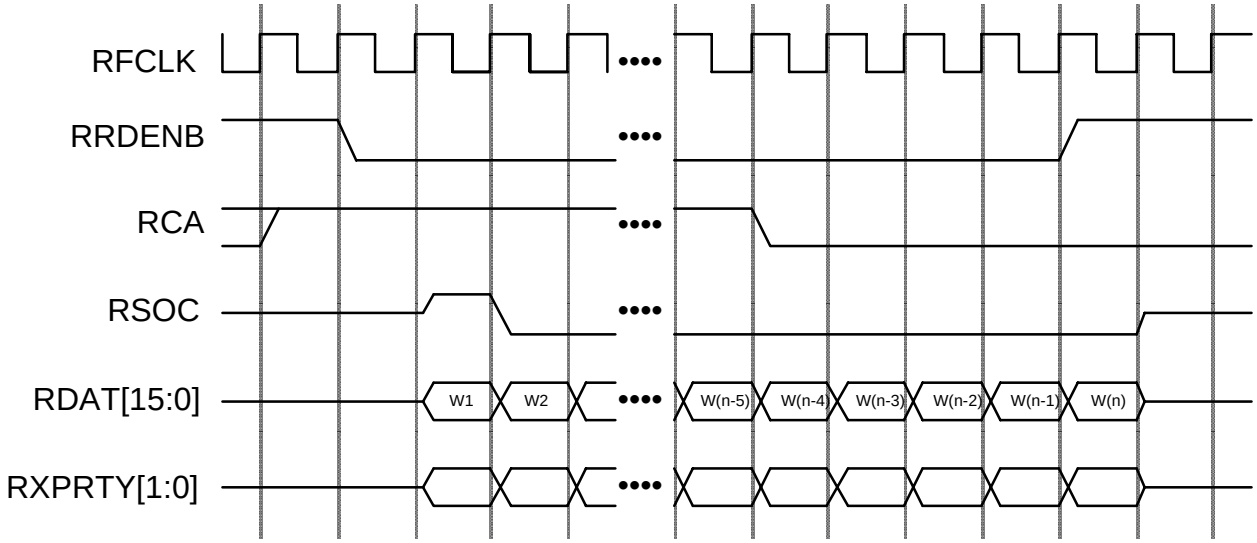
13.3 Drop Side Receive Interface

Figure 32 - Receive Synchronous FIFO, TSEN=0



The Receive Synchronous FIFO Timing, TSEN=0 Diagram (Figure 32) illustrates the operation of the drop side receive interface with tristating disabled. The S/UNI-PLUS indicates a cell is available by asserting the receive cell available output, RCA. RCA remains high until the receive FIFO is near empty (four words remaining), empty or if an error condition is detected. Selection of empty and near empty is made using the RCALEVEL0 bit in the RACP Interrupt Enable/Control register. For the near empty option, RCA transitions low four words before the last word of the last cell is read from the FIFO. RCA remains low for a minimum of one RFCLK clock cycle and then can transition high to indicate that there are additional cells available in the FIFO.

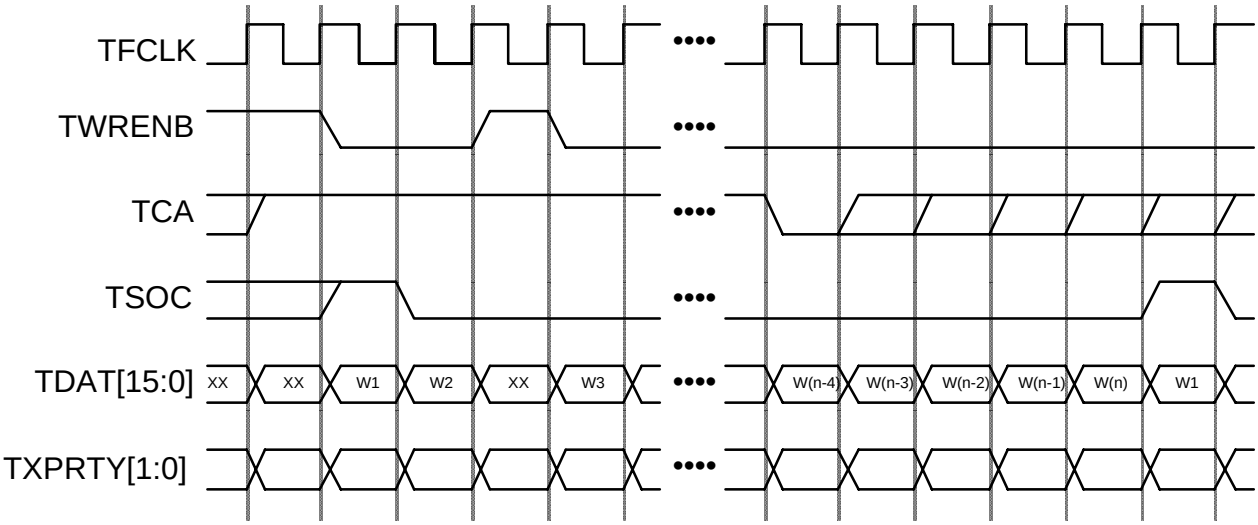
Figure 33 - Receive Synchronous FIFO, TSEN=1



The Receive Synchronous FIFO Timing, TSEN=1 Diagram (Figure 33) illustrates the operation of the drop side receive interface with tristating enabled.

13.4 Drop Side Transmit Interface

Figure 34 - Transmit Synchronous FIFO



The Transmit Synchronous FIFO Timing Diagram (Figure 34) illustrates the operation of the drop side transmit interface. The S/UNI-PLUS indicates that there is space available in the transmit FIFO by asserting the transmit cell available output, TCA. TCA remains high until the transmit FIFO is almost full, full or if an error condition is detected. Almost full implies that the transmit FIFO can accept at most an additional four writes. Selection between almost full and full is made using the TACP FIFO Control register. If TCA is asserted high and the downstream is ready to write a word, the downstream device should assert TWRENB low. At anytime, if the downstream does not have a word to write, it can deassert TWRENB.

14 ABSOLUTE MAXIMUM RATINGS

Table 12 - S/UNI-PLUS Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

15 D.C. CHARACTERISTICS

T_C = -40°C to +85°C, V_{DD} = 5 V ±5%

(Typical Conditions: T_C = 25°C, V_{DD} = 5 V)

Table 13 - S/UNI-PLUS D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	4.75	5	5.25	Volts	
A_{VD}	Power Supply	4.75	5	5.25	Volts	
V_{IL}	Input Low Voltage (TTL Only)	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{PIL}	Input Low Voltage (PECL Only)	A_{VD} - 1.8		A_{VD} - 1.6	Volts	Input LOW Voltage referenced to TAVD3, RAVD3, or RAVD4
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{PIH}	Input High Voltage (PECL Only)	A_{VD} - 1.0		A_{VD} - 0.8	Volts	Input HIGH Voltage referenced to TAVD3, RAVD3, or RAVD4
V_{PSWG}	Input Voltage Swing (RXD+/-, RRCLK+/-, TRCLK+/- Only)	600			mV	$\lvert V_{PIH} - V_{PIL} \rvert$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OL}	Output or Bidirectional Low Voltage		0.1	0.4	Volts	I_{OL} = -6 mA for outputs TXD+/-, TXC+/-. I_{OL} = -4 mA for outputs GTOCLK, GROCLK, RDAT[15:0], RSOC, RCA, TCA, and RXPRTY[1:0]. I_{OL} = -2 mA for all others, Note 3
V_{OH}	Output or Bidirectional High Voltage	V_{DD} - 1.0	4.7		Volts	I_{OH} = 6 mA for outputs TXD+/-, TXC+/-. I_{OH} = 4 mA for outputs GTOCLK, GROCLK, RDAT[15:0], RSOC, RCA, TCA, and RXPRTY[1:0]. I_{OH} = 2 mA for all others, Note 3
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.6	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	
I_{ILPU}	Input Low Current	100	450	525	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
I_{DDOP}	Operating Current Processing Cells (RFCLK = TFCLK = 51.84 MHz)		175 100	220 170	mA mA	V_{DD} = 5.25 V, Outputs Unloaded, TXD+/- = RXD+/- = 155.52 Mbit/s TXD+/- = RXD+/- = 51.84 Mbit/s

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Typical values are given as a design aid. The product is not tested to the typical values given in the data sheet.

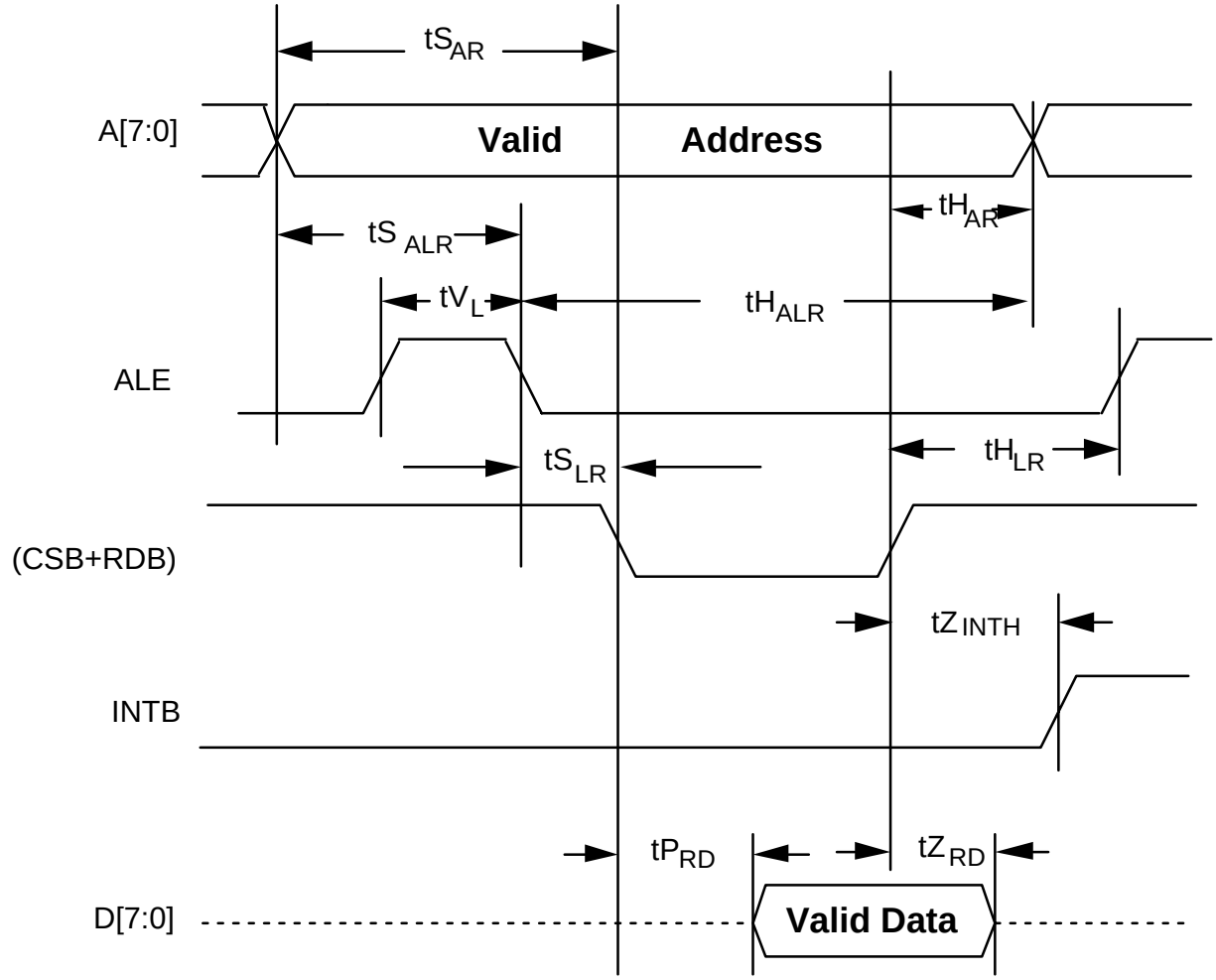
16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = 5 V ±5%)

Table 14 - Microprocessor Interface Read Access (Figure 35)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 35 - Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architecture's, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, tH_{LR} and tS_{LR} are not applicable.

6. Parameter tH_{AR} is not applicable if address latching is used.

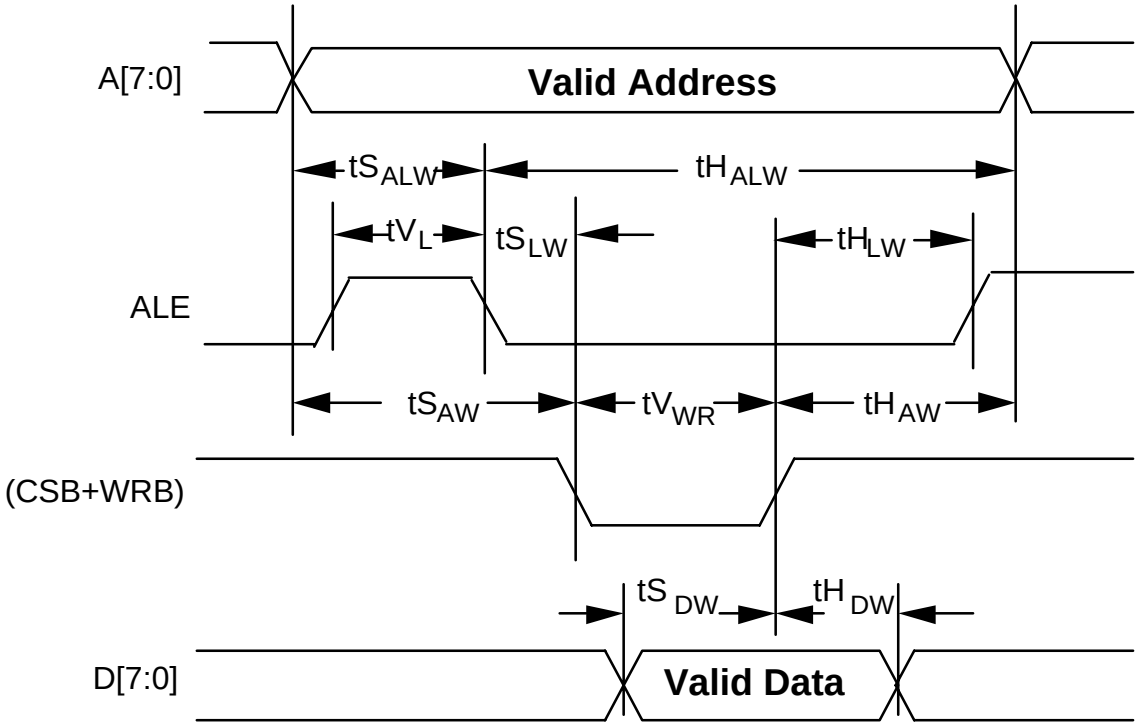
7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 15 - Microprocessor Interface Write Access (Figure 36)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 36 - Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architecture's, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, tH_{LW} and tS_{LW} are not applicable.

4. Parameter tH_{AW} is not applicable if address latching is used.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

17 S/UNI-PLUS TIMING CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = 5 V ±5%)

Table 16 - Line Side Receive Interface (Figure 37)

Symbol	Description	Min	Max	Units
	RRCLK+/RRCLK- Duty Cycle			
	51.84 or 155.52 MHz (RBYP high)	45	55	%
	19.44 or 6.48 MHz (RBYP low)	30	70	
	RXD+/RXD- Operating Frequency			
	STS-3c/STM-1 (RBYP high)		156	Mbit/s
	STS-3c/STM-1 (RBYP low)	155	156	Mbit/s
	STS-1 (RBYP high)		52	Mbit/s
	STS-1 (RBYP low)	51	52	Mbit/s
	RRCLK+/RRCLK- Frequency Tolerance†	-20	+20	ppm
tS_{RXD}	RXD+/RXD- Setup time to RRCLK+/RRCLK- (RBYP asserted high.)	1		ns
tH_{RXD}	RXD+/RXD- Hold time to RRCLK+/RRCLK- (RBYP asserted high.)	1.5		ns

† **Note:**

The specification may be relaxed to +/- 50 ppm if the S/UNI-PLUS is not loop timed, or for applications that do not require this timing accuracy. If loop timing is enabled, the tighter tolerance is required to meet the SONET free run accuracy specification under loss of signal conditions. Frequency tolerance is measured with respect to the receive stream on RXD+/- when clock recovery is enabled (RBYP is low).

Figure 37 - Line Side Receive Interface Timing

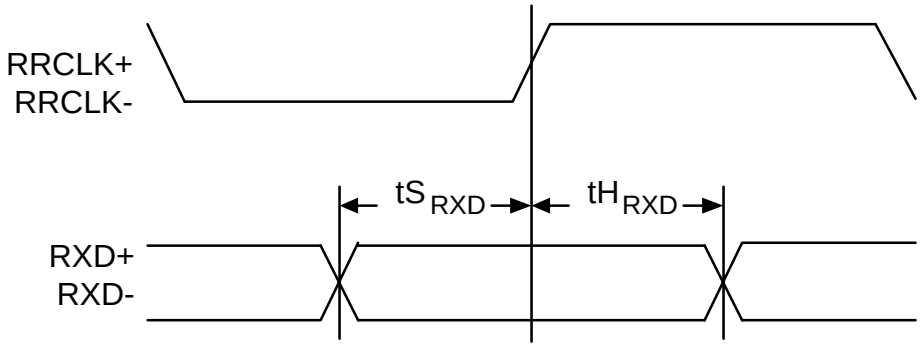


Table 17 - Receive Alarm Output (Figure 38)

Symbol	Description	Min	Max	Units
tP_{LOF}	GROCLK Low to LOF Valid	-5	15	ns
tP_{LOS}	GROCLK Low to LOS Valid	-5	15	ns
tP_{LAIS}	GROCLK Low to LAIS Valid	-5	15	ns
tP_{LRDI}	GROCLK Low to LRDI Valid	-5	15	ns
tP_{LOP}	GROCLK Low to LOP Valid	0	20	ns
tP_{PAIS}	GROCLK Low to PAIS Valid	0	20	ns
P_{PRDI}	GROCLK Low to PRDI Valid	0	20	ns
tP_{LCD}	GROCLK Low to LCD Valid	0	20	ns

Figure 38 - Receive Alarm Output Timing

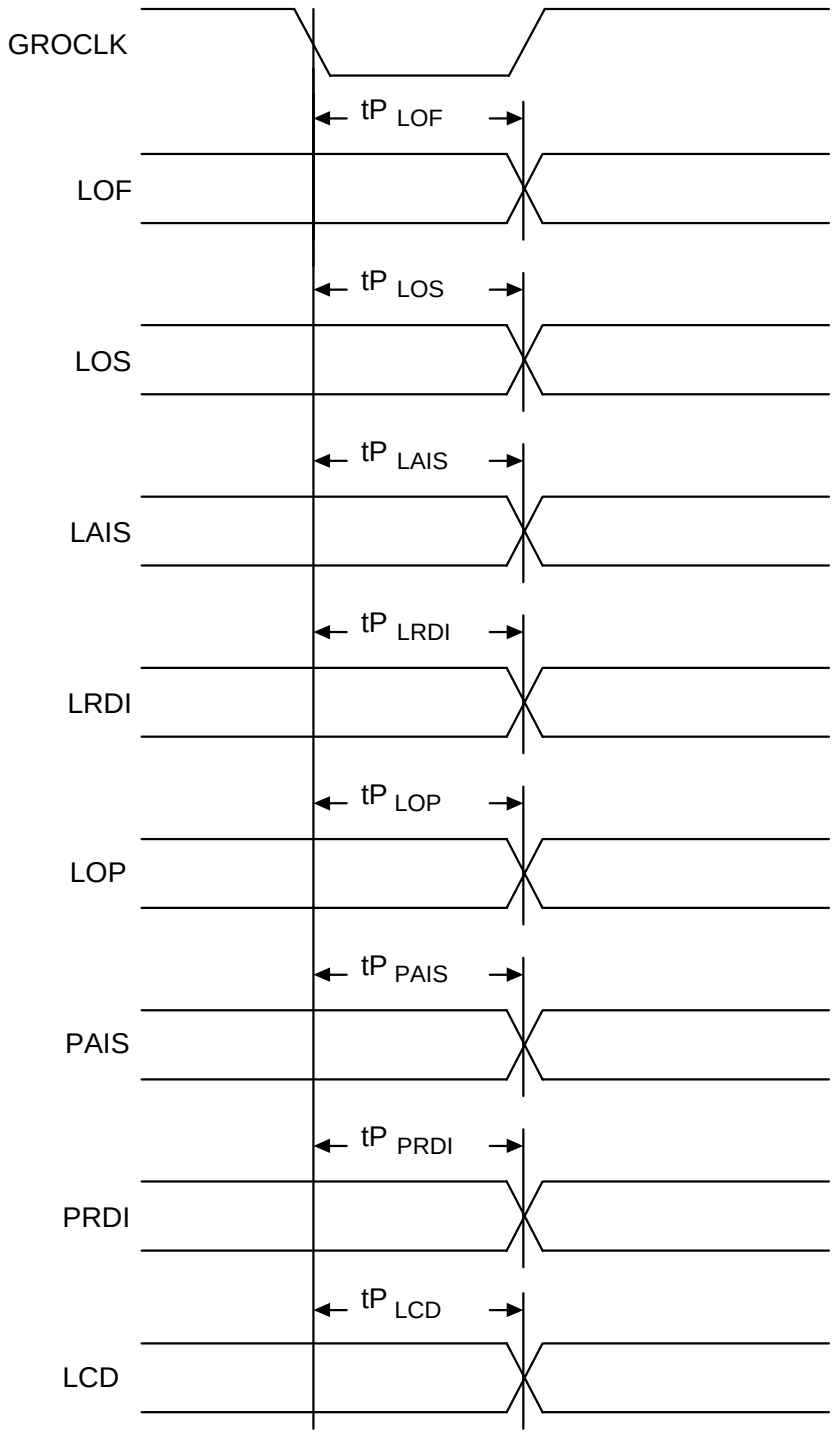
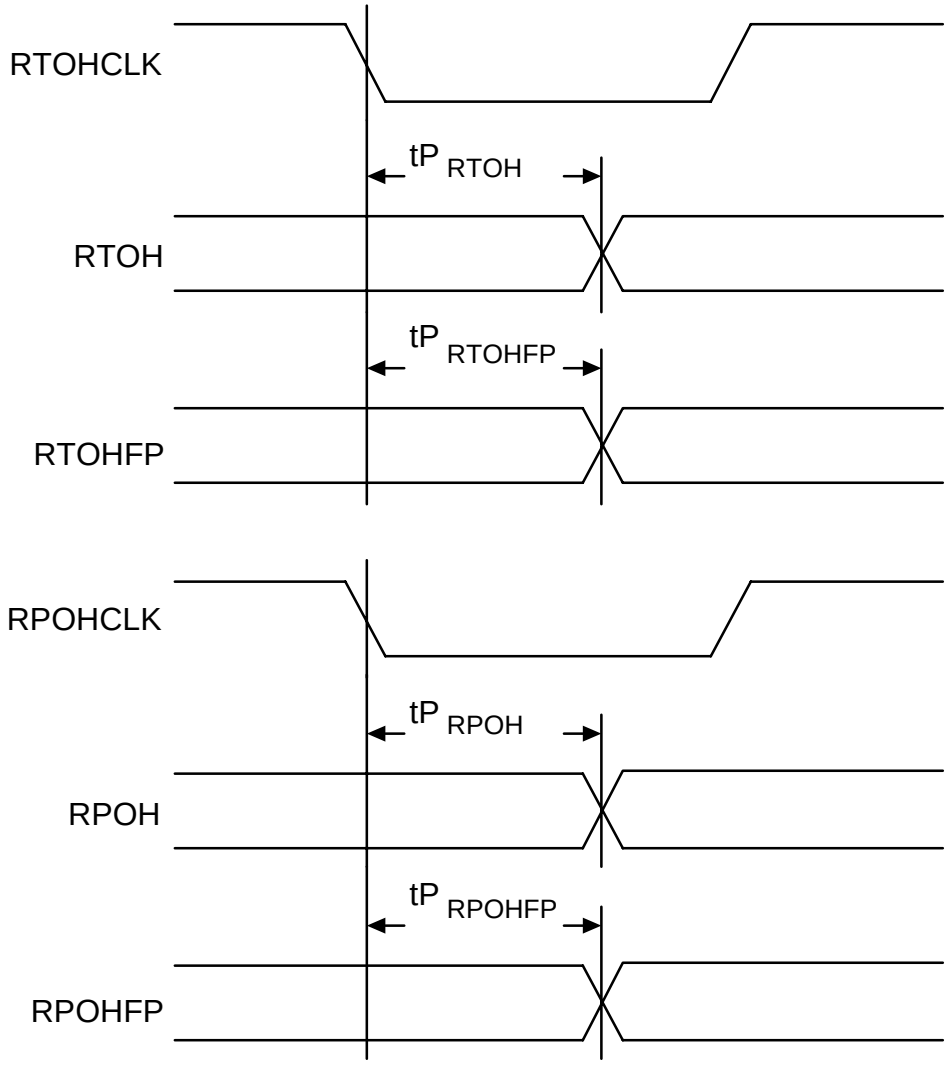


Table 18 - Receive Overhead Access (Figure 39)

Symbol	Description	Min	Max	Units
t_{PRTOH}	RTOHCLK Low to RTOH Valid	-15	5	ns
$t_{PRTOHFP}$	RTOHCLK Low to RTOHFP Valid	-15	5	ns
t_{PROW}	ROWCLK Low to RSOW, RSUC,			
	RLOW Valid Prop Delay	-10	10	ns
t_{PRSD}	RSDCLK Low to RSD Valid	-15	5	ns
t_{PRLD}	RLDCLK Low to RLD Valid	-15	5	ns
t_{PRPOH}	RPOHCLK Low to RPOH Valid	-15	5	ns
$t_{PRPOHFP}$	RPOHCLK Low to RPOHFP Valid	-15	5	ns

Figure 39 - Receive Overhead Access Timing



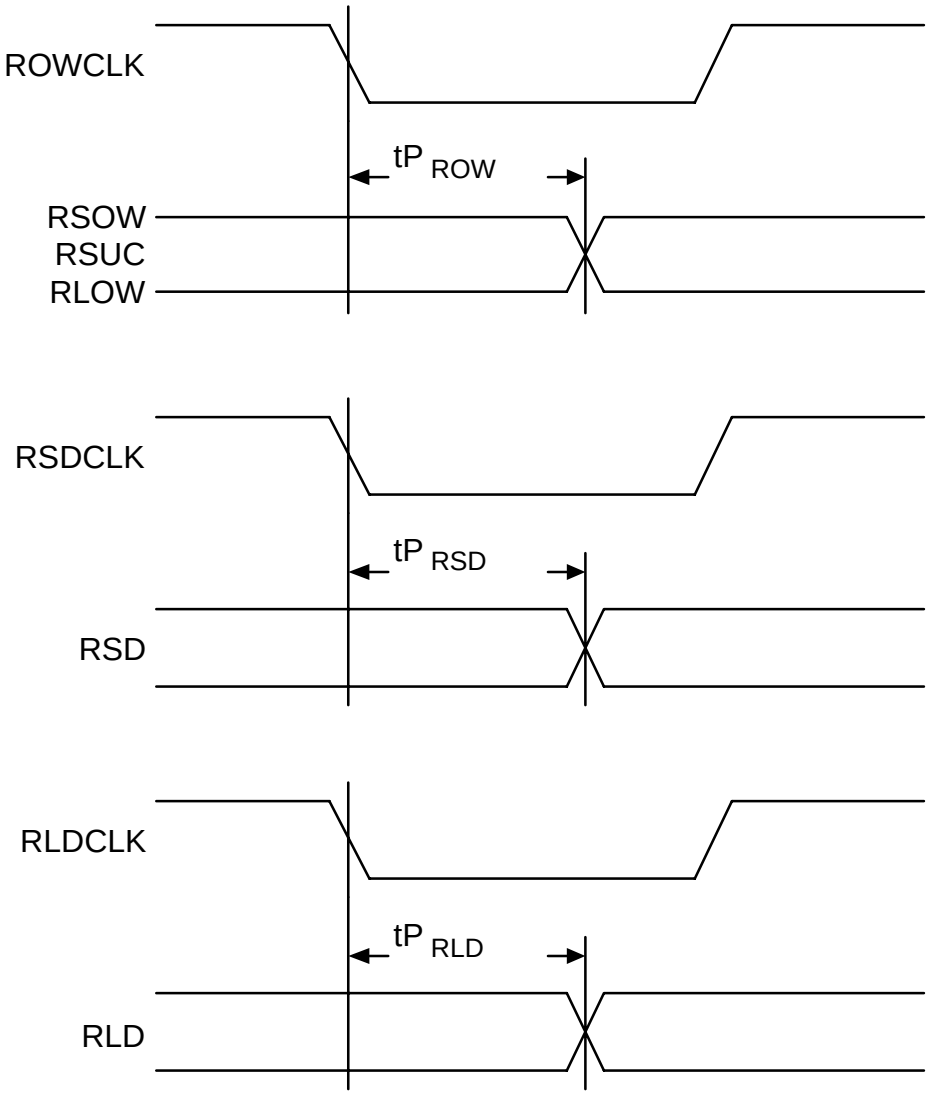

ROWCLK
tP ROW
RSOW
RSUC
RLOW
RSDCLK
tP RSD
RSD
RLDCLK
tP RLD
RLD

Table 19 - Receive GFC Access (Figure 40)

Symbol	Description	Min	Max	Units
tP_{RCP}	GROCLK Low to RCP Valid	1	20	ns
tP_{RGFC}	GROCLK Low to RGFC Valid	1	20	ns

Figure 40 - Receive GFC Access Timing

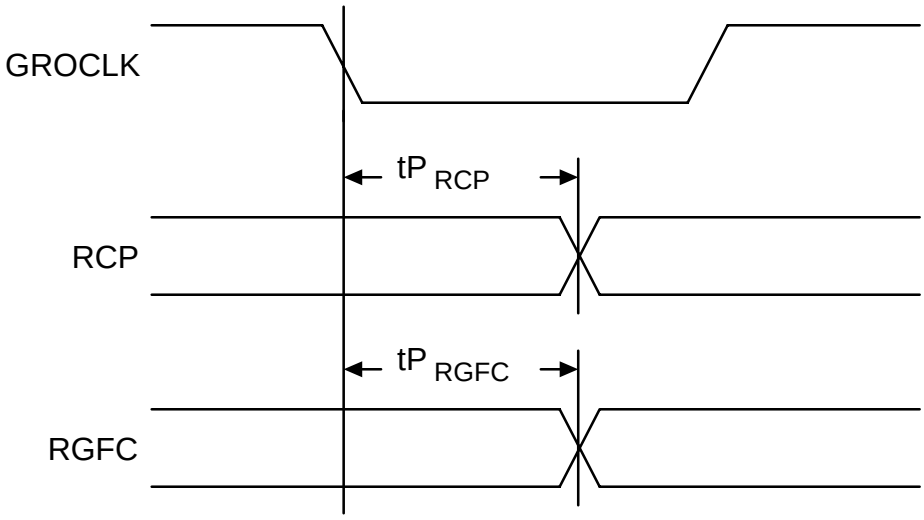


Table 20 - Line Side Transmit Interface (Figure 41)

Symbol	Description	Min	Max	Units
	TRCLK+/TRCLK- Duty Cycle			
	51.84 or 155.52 MHz (TBYP high)	45	55	%
	19.44 or 6.48 MHz (TBYP low)	30	70	
	TRCLK+/TRCLK- Operating Frequency			
	STS-3c/STM-1 (TBYP high)		156	MHz
	STS-1 (TBYP high)		52	MHz
	19.44 MHz Nominal (TBYP low)	19.375	19.5	MHz
	6.48 MHz Nominal (TBYP low)	6.375	6.5	MHz
	TRCLK+/TRCLK- Frequency Tolerance†	-20	+20	ppm
$tP_{TXDdiff}$	TXC+/TXC- Low to TXD+/TXD- Valid (STS-1 only)	-2	2	ns
tP_{TXDneg}	TXC+ Low to TXD+ Valid (STS-1 only)	-3	2	ns
tP_{TXDpos}	TXC- High to TXD+ Valid (STS-1 only)	-2	3	ns

†Note:

The specification may be relaxed to +/- 50 ppm for LAN applications that do not require this timing accuracy. The tighter tolerance is required to meet the SONET free run accuracy specification.

Figure 41 - Line Side Transmit Interface Timing

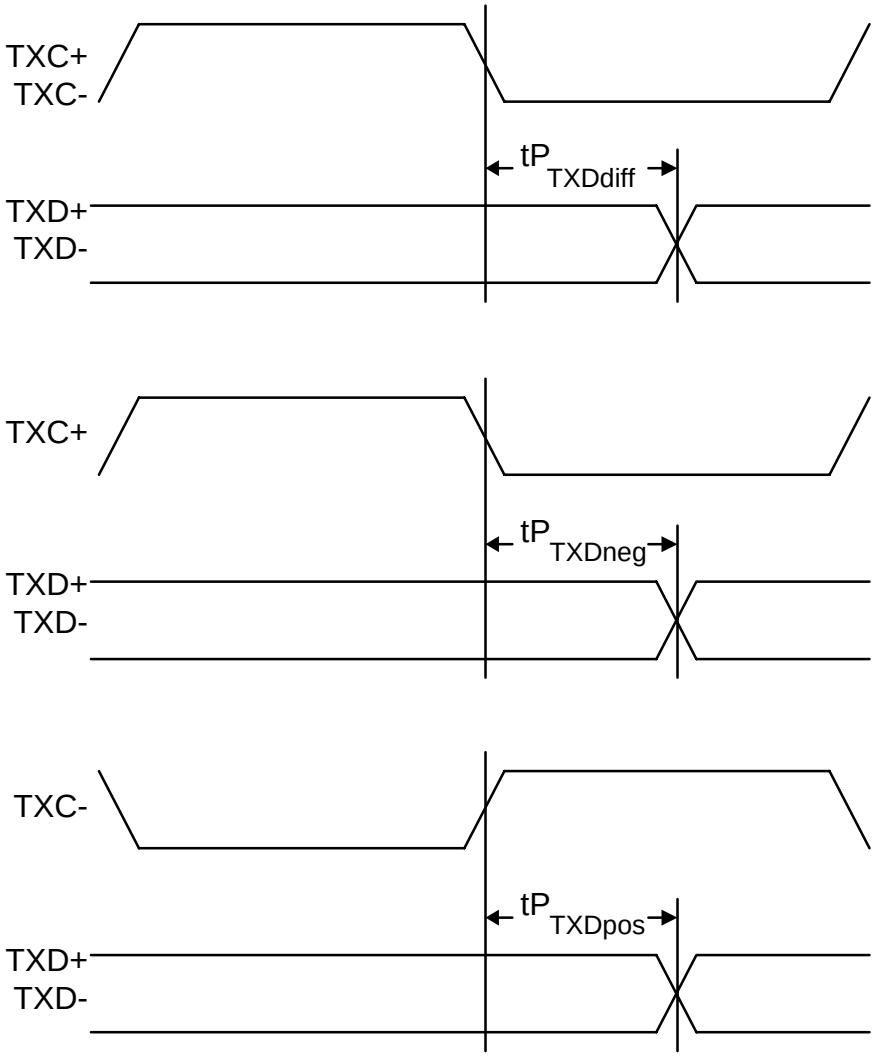


Table 21 - Transmit Alarm Input (Figure 42)

Symbol	Description	Min	Max	Units
tSTLAIS	TLAIS Set-up time to GTOCLK	10		ns
tHTLAIS	TLAIS Hold time to GTOCLK	5		ns
tSTLRDI	TLRDI Set-up time to GTOCLK	10		ns
tHTLRDI	TLRDI Hold time to GTOCLK	5		ns
tSTPAIS	TPAIS Set-up time to GTOCLK	10		ns
tHTPAIS	TPAIS Hold time to GTOCLK	5		ns
tSTPRDI	TPRDI Set-up time to GTOCLK	10		ns
tHTPRDI	TPRDI Hold time to GTOCLK	5		ns

Figure 42 - Transmit Alarm Input Timing

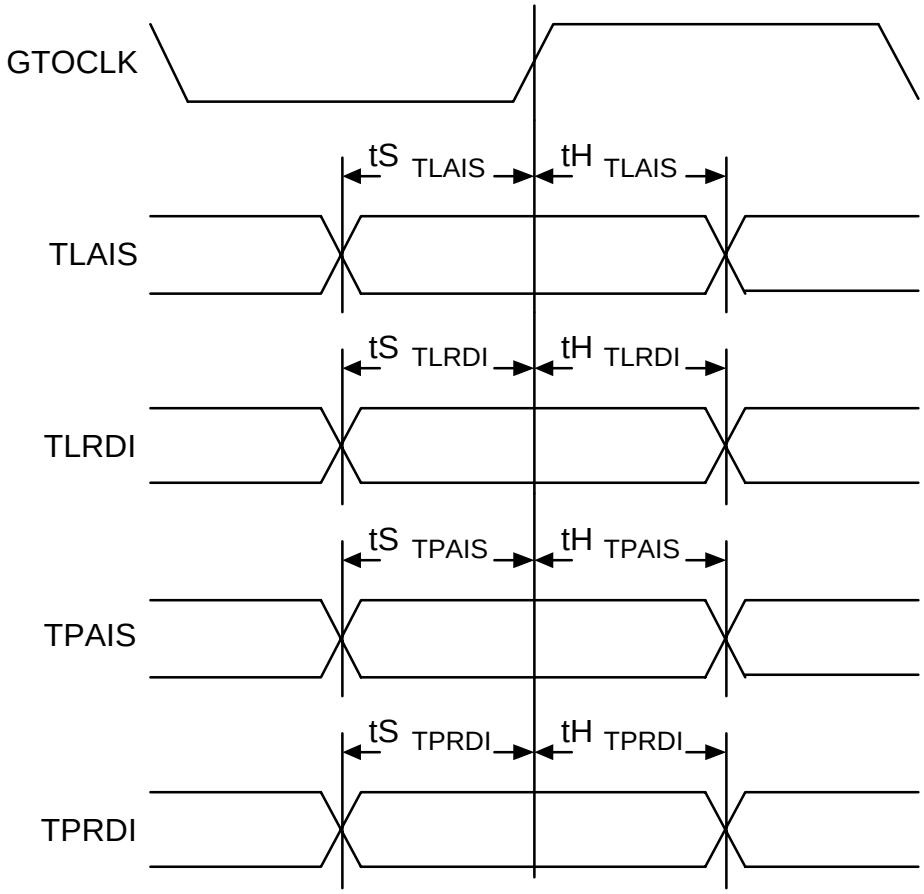
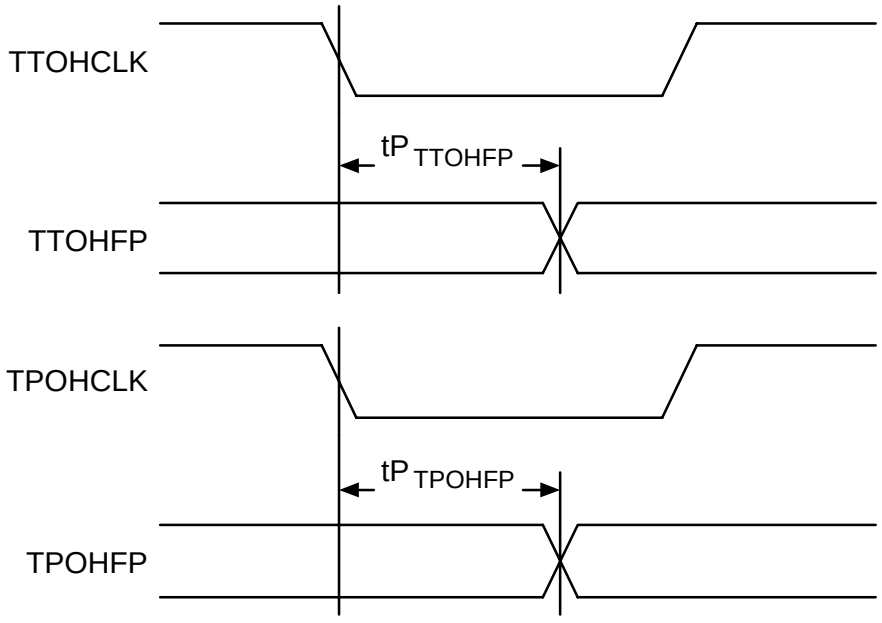


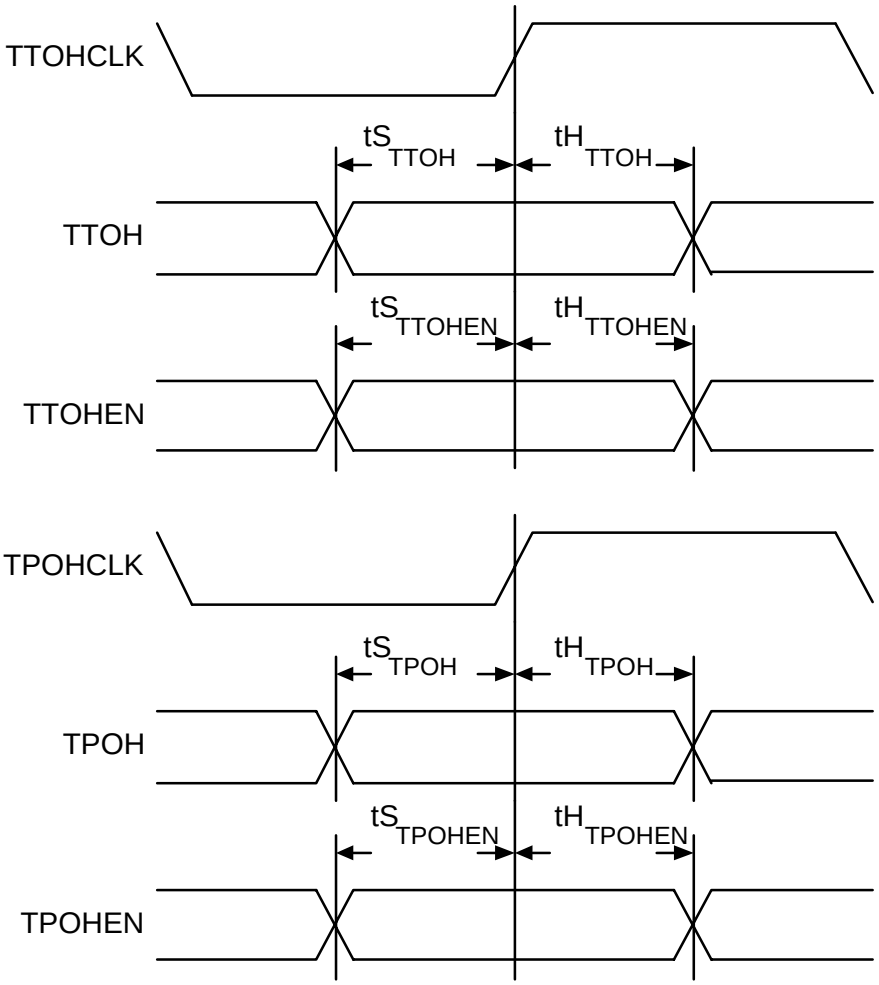
Table 22 - Transmit Overhead Access (Figure 43)

Symbol	Description	Min	Max	Units
$t_{PTTOHFP}$	TTOHCLK Low to TTOHFP Valid	-15	5	ns
$t_{PTPOHFP}$	TPOHCLK Low to TPOHFP Valid	-15	5	ns
t_{STTOH}	TTOH Set-up time to TTOHCLK	25		ns
t_{HTTOH}	TTOH Hold time to TTOHCLK	25		ns
$t_{STTOHEN}$	TTOHEN Set-up time to TTOHCLK	25		ns
$t_{HTTOHEN}$	TTOHEN Hold time to TTOHCLK	25		ns

Symbol	Description	Min	Max	Units
tS_{TOW}	TSOW, TSUC, TLOW Set-up Time to TOWCLK	25		ns
tH_{TOW}	TSOW, TSUC, TLOW Hold Time to TOWCLK	25		ns
tS_{TSD}	TSD Set-up Time to TSDCLK	25		ns
tH_{TSD}	TSD Hold Time to TSDCLK	25		ns
tS_{TLD}	TLD Set-up Time to TLDCLK	25		ns
tH_{TLD}	TLD Hold Time to TLDCLK	25		ns
tS_{TPOH}	TPOH Set-up time to TPOHCLK	25		ns
tH_{TPOH}	TPOH Hold time to TPOHCLK	25		ns
tS_{TPOHEN}	TPOHEN Set-up time to TPOHCLK	25		ns
tH_{TPOHEN}	TPOHEN Hold time to TPOHCLK	25		ns

Figure 43 - Transmit Overhead Access Timing




TTOHCLK
tS TTOH
tH TTOH
TTOH
tS TTOHEN
tH TTOHEN
TTOHEN
TPOHCLK
tS TPOH
tH TPOH
TPOH
tS TPOHEN
tH TPOHEN
TPOHEN

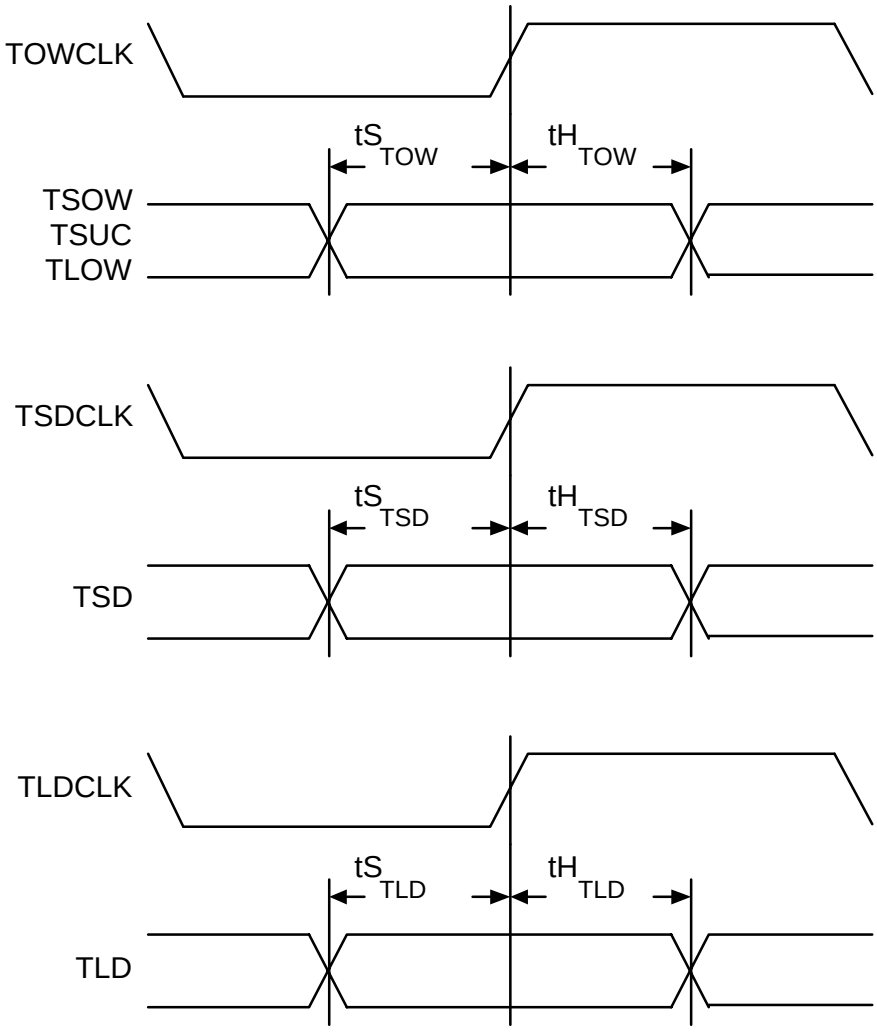

TOWCLK
tS TOW
tH TOW
TSOW
TSUC
TLOW
TSDCLK
tS TSD
tH TSD
TSD
TLDCLK
tS TLD
tH TLD
TLD

Table 23 - Transmit GFC Access (Figure 44)

Symbol	Description	Min	Max	Units
tP_{TCP}	GTOCLK Low to TCP Valid	1	20	ns
tS_{TGFC}	TGFC Set-up time to GTOCLK	10		ns
tH_{TGFC}	TGFC Hold time to GTOCLK	0		ns

Figure 44 - Transmit GFC Access Timing

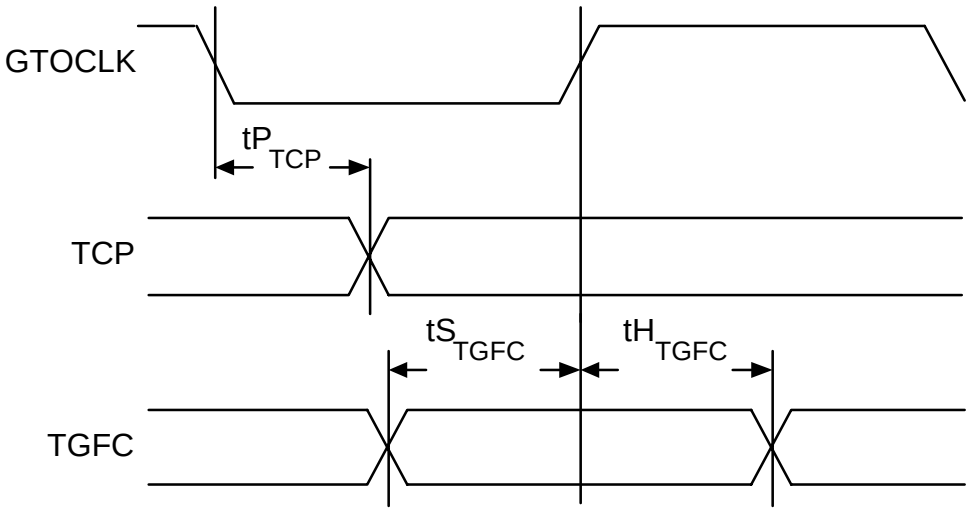


Table 24 - Drop Side Receive Interface (Figure 45, Figure 46)

Symbol	Description	Min	Max	Units
	RFCLK Frequency		50	MHz
	RFCLK Duty Cycle	40	60	%
tS_{RRDENB}	RRDENB Set-up time to RFCLK	4		ns
tH_{RRDENB}	RRDENB Hold time to RFCLK	1		ns
tP_{RCA}	RFCLK High to RCA Valid	1	14	ns
tP_{RSOC}	RFCLK High to RSOC Valid	1	14	ns

Symbol	Description	Min	Max	Units
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	1	14	ns
tP_{RXPRTY}	RFCLK High to RXPRTY[1:0] Valid	1	14	ns
tP_{RFCLK}	RFCLK High to Output Enable (TSEN high)	1	14	ns
tZ_{RFCLK}	RFCLK High to Output Tristate (TSEN high)	1	14	ns

Figure 45 - Drop Side Receive Interface Timing, TSEN = 0

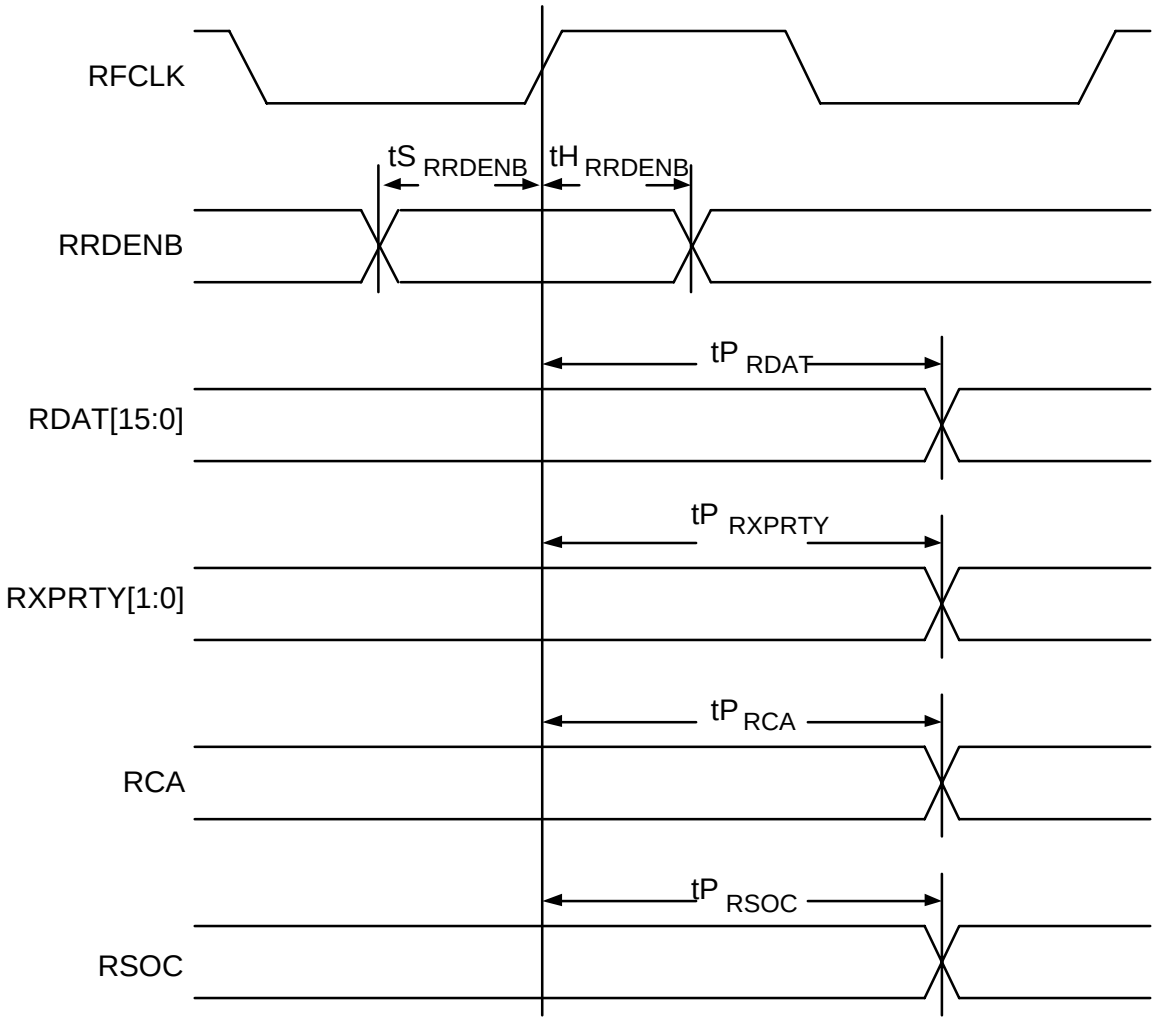


Figure 46 - Drop Side Receive Interface Timing, TSEN = 1

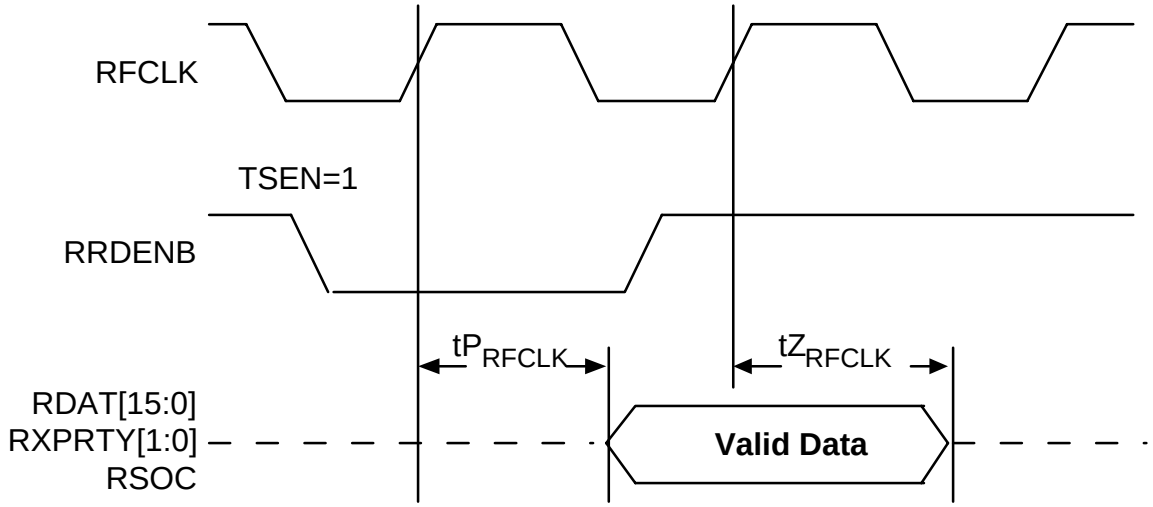


Table 25 - Drop Side Transmit Interface (Figure 47)

Symbol	Description	Min	Max	Units
	TFCLK Frequency		50	MHz
	TFCLK Duty Cycle	40	60	%
tS_{TWRENB}	TWRENB Set-up time to TFCLK	4		ns
tH_{TWRENB}	TWRENB Hold time to TFCLK	1		ns
tS_{TDAT}	TDAT[15:0] Set-up time to TFCLK	4		ns
tH_{TDAT}	TDAT[15:0] Hold time to TFCLK	1		ns
tS_{TXPRTY}	TXPRTY[1:0] Set-up time to TFCLK	4		ns
tH_{TXPRTY}	TXPRTY[1:0] Hold time to TFCLK	1		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	4		ns
tH_{TSOC}	TSOC Hold time to TFCLK	1		ns
tP_{TCA}	TFCLK High to TCA Valid	1	14	ns

Figure 47 - Drop Side Transmit Interface

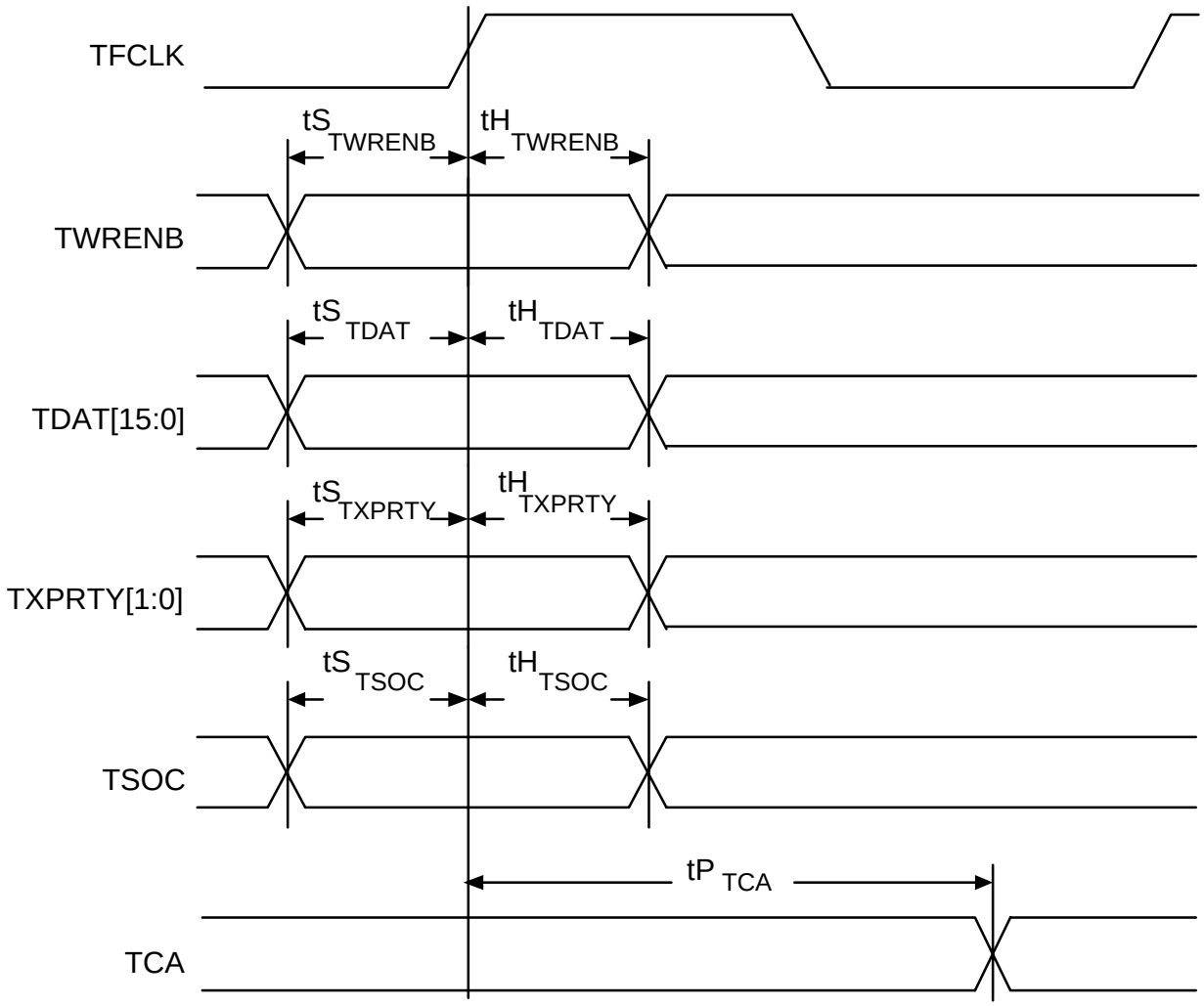
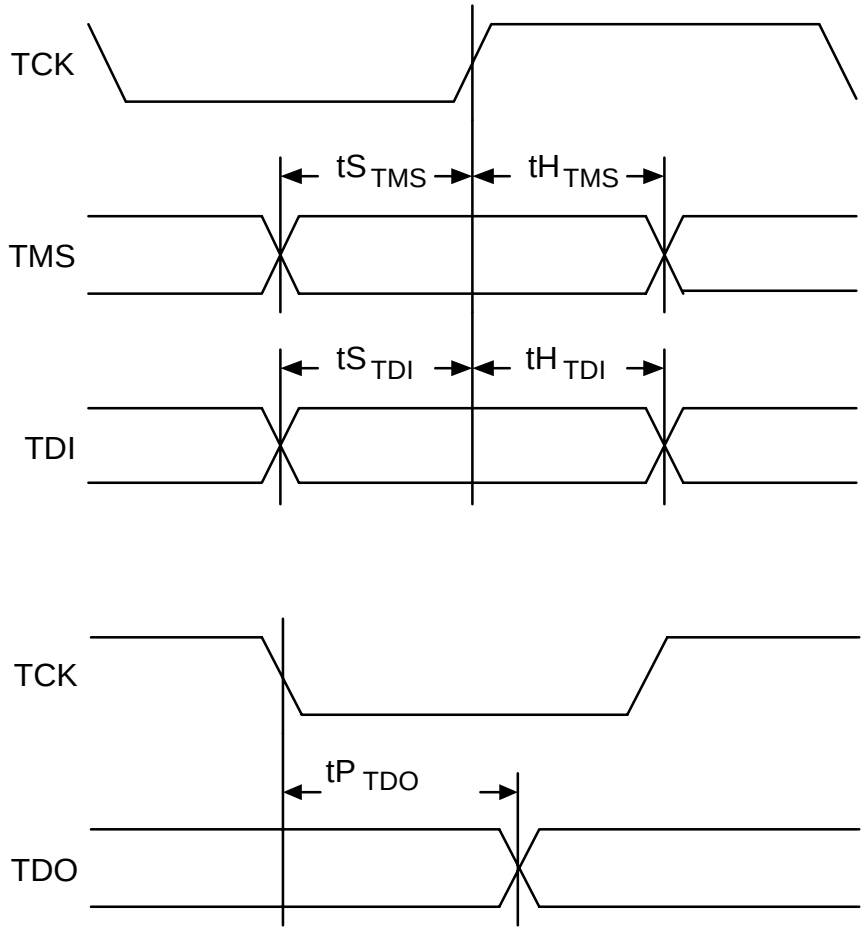


Table 26 - JTAG Port Interface (Figure 48)

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns

Figure 48 - JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. When a set-up time is specified between a PECL input and a PECL clock, the set-up time is the time in nanoseconds from the crossing point of the differential input to the crossing point of the differential clock.

4. When a hold time is specified between a PECL input and a PECL clock, the hold time is the time in nanoseconds from the crossing point of the differential clock to the crossing point of the differential input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are specified with a 50 pF load on the outputs, except for TXD+/- and TXC+/-. Maximum output propagation delays for TXD+/- and TXC+/- are specified with a 30 pF load.

3. Differential output propagation delay time is the time in nanoseconds from the crossing point of the reference signal to the crossing point of the output.

18 ORDERING AND THERMAL INFORMATION

Table 27 - S/UNI-PLUS Ordering Information

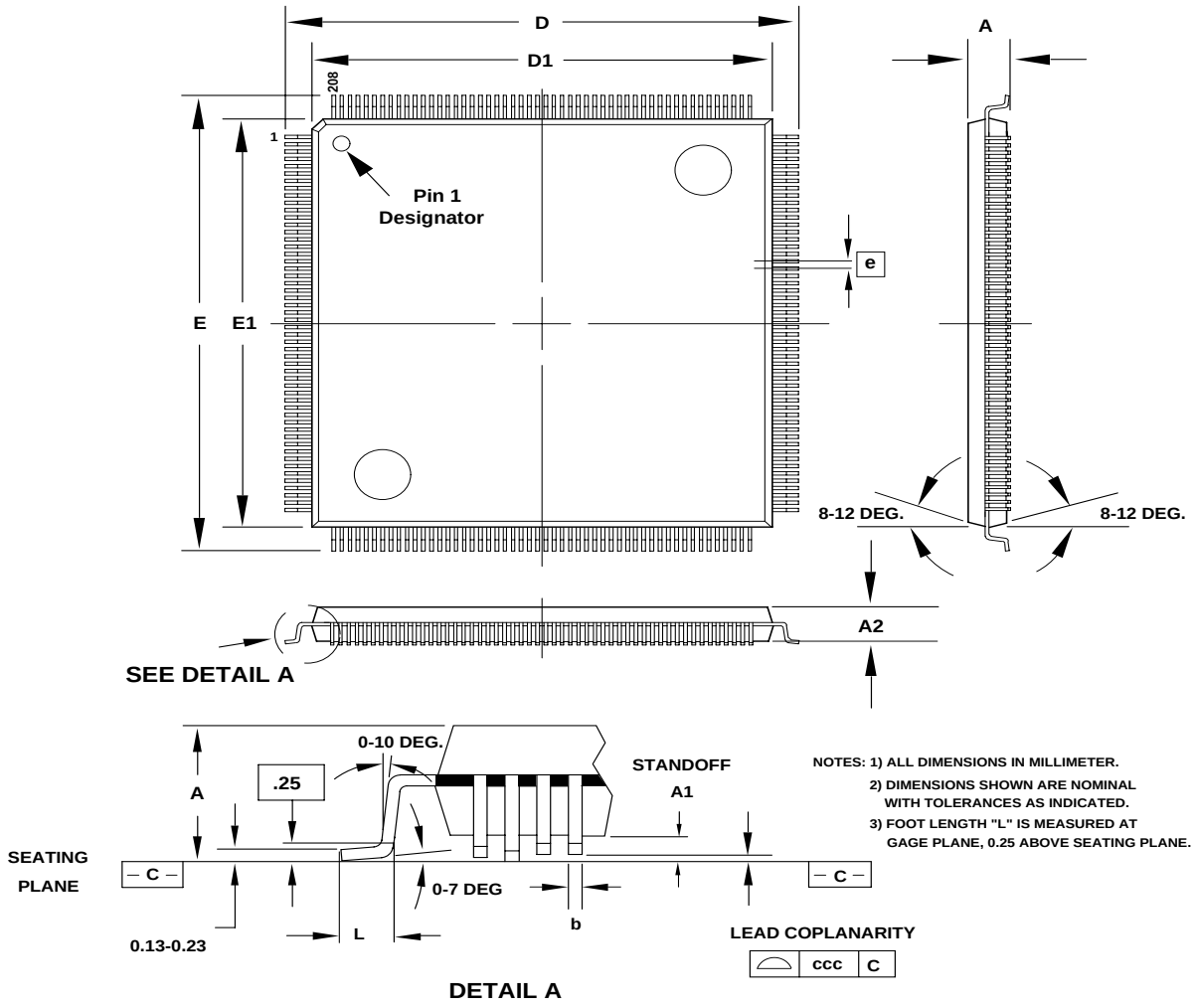
PART NO.	DESCRIPTION
PM5347-RI	208 Pin Plastic Quad Flat Pack (PQFP)

Table 28 - S/UNI-PLUS Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5347-RI	-40°C to 85°C	28 °C/W	10 °C/W

19 MECHANICAL INFORMATION

Figure 49 - 208 Pin Plastic Quad Flat Pack (R Suffix):



PACKAGE TYPE: 208 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 28 x 28 x 3.49 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	3.64	0.25	3.39	30.40	27.90	30.40	27.90	0.50		0.17	
Nom.			3.49	30.60	28.00	30.60	28.00	0.60	0.50	0.22	
Max.	4.07	0.48	3.59	30.80	28.10	30.80	28.10	0.75		0.27	0.10

NOTES

NOTES

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