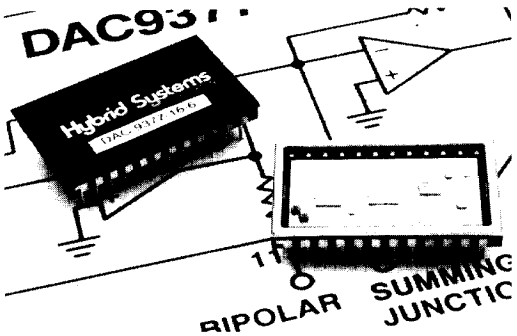
DAC9377-SERIES

COMPLETE BUFFERED 16-BIT DAC

FEATURES

- True 16-bit (0.0008%) linearity
- μP compatible
- Complete
- 24-pin package
- Low power — 450mW
- Low cost
- Binary or BCD code



DESCRIPTION

The DAC9377-16 is a complete, voltage output, 16-bit D/A converter with true 16-bit linearity. Complete with storage registers, internal reference and output amplifier, DAC9377-16 provides the user with exceptional performance and self-contained operation. The input storage register is composed of 16 parallel latches — a system compatible with 16-bit data bus interfaces. A single proprietary monolithic chip contains switches, storage registers and other electronics for high resolution and low linearity error. TTL and CMOS compatibility combined with low power dissipation in a ceramic 24-pin DIP, makes the DAC9377-16 unsurpassed in a high resolution data conversion device.

True 16-Bit Linearity — 16-bit (±0.0008%) linearity in a 24-pin DIP is unequaled. No other microcircuit converter does better. Additional versions with 15-and 14-bit linearity are also available.

Low Power — CMOS proprietary monolithic devices in a unique circuit configuration yield the lowest power dissipation (450 mW typ.) of any complete 16-bit converter available.

Complete — No external components are required for 16-bit conversion.

Input Storage Registers — Designed in one 16-bit segment, the input storage register provides data storage when latched, but is "transparent" when unlatched. The latch control is level-triggered for either static or dynamic operation.

Reliability — A proven performer, the DAC9377-16 is packaged in a 24-pin ceramic DIP for the utmost in reliability. Combined with our proprietary monolithic device and automatic wirebonding, we've made the DAC9377-16 the most reliable device to date. Reliability is further enhanced by batch-processed, precision laser-trimmed resistor networks fabricated in our own facility. Networks are functionally trimmed and glass passivated to assure reliability under adverse environmental conditions.

Advanced designs, proven processes and continuous monitoring during all production operations by our quality control organization are combined with rigorous AQL screening to provide the most dependable, low cost D/A converter possible.

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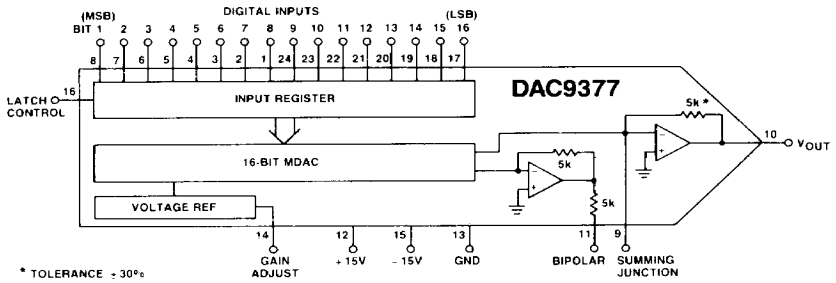
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C unipolar operation and nominal power supply, no load)

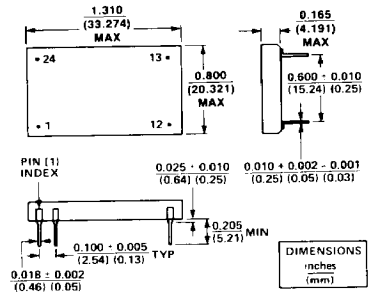
MODEL	DAC9377-16-6	DAC9377-16-5	DAC9377-16-4	DAC9377-4D
TYPE	Latched Inputs	*	*	*
DIGITAL INPUT				
Resolution	16-Bits	*	*	*
Unipolar Coding	Binary	*	*	BCD
Bipolar Coding	Offset Binary	*	*	N.A.
Logic Compatibility[1]	TTL, CMOS	*	*	*
Input Leakage Current	±1μA (max) 0.4V>V_{LOGIC}>3.2V	*	*	*
Latch Control Width	250nS (min)	*	*	*
Data Set-up Time[2]	500nS (min)	*	*	*
Data Hold Time[3]	0nS (min)	*	*	*
ANALOG OUTPUT				
Scale Factor[4]	0.1% F.S.R. (typ)	*	*	*
Initial Offset[4]	0.15% F.S.R. (max)			
Unipolar	±0.05% F.S.R. (max)	*	*	*
Bipolar	±0.10% F.S.R. (max)	*	*	N.A.
Voltage Range				
Unipolar	0 to +10V	*	*	*
Bipolar	±10V	*	*	N.A.
Current Compliance	±5mA	*	*	*
Output Impedance	<0.1Ω	*	*	*
Noise				
PP-noise (wideband)	±0.0005% F.S.R.	*	*	*
REFERENCE				
Voltage	−10V (internal)	*	*	*
Drift	5ppm/°C	*	*	*
Stability	1mV/yr	*	*	*
STATIC PERFORMANCE				
Integral Linearity[6]	±0.0008% F.S.R. (typ)	±0.0015% F.S.R. (typ)	±0.0015% F.S.R. (typ)	±0.002% F.S.R. (typ)
	±0.0015% F.S.R. (max)	±0.002% F.S.R. (max)	±0.003% F.S.R. (max)	±0.005% F.S.R. (max)
Differential Linearity[7]	±0.0004% F.S.R. (typ)	±0.0008% F.S.R. (typ)	±0.0015% F.S.R. (typ)	±0.005% F.S.R. (typ)
	±0.0015% F.S.R. (max)	±0.003% F.S.R. (max)	±0.006% F.S.R. (max)	±0.01% F.S.R. (max)
Monotonicity	Guaranteed to 16-bits	Guaranteed to 15-bits	Guaranteed to 14-bits	
DYNAMIC PERFORMANCE				
Major Carry Transition Settling to 0.006% F.S.R. (strobed)	20μS	*	*	*
Slew Rate	0.20V/μS	*	*	*
STABILITY[5] (Over Specified Temp. Range)				
Gain	8ppm/°C F.S.R. (max)	*	*	*
Linearity	1ppm/°C F.S.R. (max)	*	*	5ppm/°C
Differential Linearity	1ppm/°C F.S.R. (max)	*	*	5ppm/°C
Offset Drift				
Unipolar	3ppm/°C F.S.R.	*	*	*
Bipolar	5ppm/°C F.S.R.	*	*	*
POWER SUPPLY				
Requirements	+15V ±5% @ 15mA (max)	*	*	*
	−15V ±5% @ 20mA (max)	*	*	*
Rejection Ratio	0.0039%/% (max)	*	*	*
Power Dissipation	450mW, 600mW max	*	*	*
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	*	*
Storage	−25°C to +85°C	*	*	*
MECHANICAL				
Case Style	24 pin, double-DIP			
Case Dimensions				

NOTES:

* Same as DAC9377-16-6

1. Digital input voltage must not exceed supply voltage or go below −0.5V;
2. Time, data must be stable before latch control goes to "0".
3. Time, data must be stable after latch control goes to "0"
4. See APPLICATIONS INFORMATION for calibration procedure.
5. See APPLICATIONS NOTES.
6. Integral Linearity, for this product, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.
7. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.

Package Outline



Pin Connections

Unipolar Output: Ground pin 11 (No Connection for BCD)

Bipolar Output: Connect pin 11 to pin 9 (Binary Only)

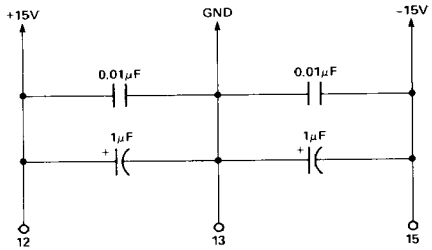
PIN DESIGNATIONS

PIN	FUNCTION		PIN	FUNCTION	
	Binary	BCD		Binary	BCD
1	2^{-8}	(100)	24	2^{-9}	(80)
2	2^{-7}	(200)	23	2^{-10}	(40)
3	2^{-6}	(400)	22	2^{-11}	(20)
4	2^{-5}	(800)	21	2^{-12}	(10)
5	2^{-4}	(1000)	20	2^{-13}	(8)
6	2^{-3}	(2000)	19	2^{-14}	(4)
7	2^{-2}	(4000)	18	2^{-15}	(2)
8	2^{-1}	(8000)	17	2^{-16}	(1)
9	SUMMING JUNCTION		16	LATCH CONTROL	
10	OUT		15	−15V	
11	BIPOLAR	N/C	14	GAIN ADJUST	
12	+15V		13	GND	

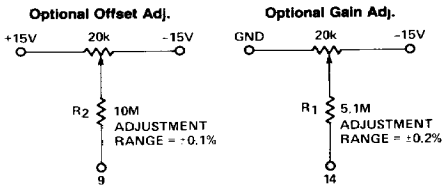
Note on BCD pin 11 must have no connection.

APPLICATIONS INFORMATION

RECOMMENDED BYPASS CIRCUIT



OPTIONAL GAIN & OFFSET ADJUSTMENT CIRCUIT



Values of R_1 & R_2 can be changed to increase or decrease the sensitivity of the adjustment. This adjustment should not be greater than ±1% around the nominal value for best performance.

CALIBRATION PROCEDURE
(for optional external Gain & Offset adjustment)

Unipolar operation:
1. Apply a 0 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 1 1 1 . . . 1 input code and set the GAIN ADJ pot for F.S. −1 LSB.

Bipolar operation:
1. Apply a 1 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 0 0 0 . . . 0 input code and set the GAIN ADJ pot for −F.S.

TRANSFER CHARACTERISTICS

Unipolar Operation

BINARY INPUT	ANALOG OUTPUT
111 . . 111	+F.S. −1 LSB
100 . . 000	+F.S./2
011 . . 111	+F.S./2 −1 LSB
000 . . 000	0V

Bipolar Operation

BINARY INPUT	ANALOG OUTPUT
111 . . 111	+F.S. −1 LSB
100 . . 000	0V
011 . . 111	−1 LSB
000 . . 000	−F.S.

BCD Operation

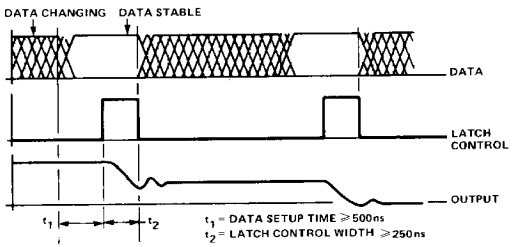
BCD INPUT	VOLTAGE OUTPUT
9 9 9 9	9.999 Volts
5 0 0 0	5.000 Volts
2 5 0 0	2.500 Volts
0 0 0 0	0.000 Volts

APPLICATION NOTES

TIMING DIAGRAM

LATCH CONTROL

Latch Strobe Input	Function
0	data latched (held)
1	data changing (transfer)



INTERNAL REFERENCE (NOTE4)

Buffered bootstrap design of the reference voltage is totally internal. A temperature compensated −6.2 volt planar-zener diode minimizes temperature drift. The voltage can be monitored with a high impedance digital voltmeter at pin 14 (GAIN ADJUST).

SETTLING TIME

The DAC9377-16 incorporates input buffering circuits whose propagation time introduces a skewing of the digital data reaching the bit switches. The skewing results in the bit switches not operating synchronously with each data change, producing an increase in the settling time (1 to 2 microseconds) and large "glitches". The dynamic performance of the DAC9377-16 can be greatly improved by using the internal latches which are available on these units. The latches are located after the input buffer circuits and just before the bit switches. When correctly strobed the latches present a data change to the bit switches in a synchronous manner. The latches should be closed while the input data is changing and propagating through the buffers. After the digital data has settled the latch is loaded and the "new" data is transferred to the switches synchronously. The latch is then closed and is ready for the next data update.

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APPLICATION NOTES

OUTPUT NOISE

Noticeable amounts of noise at both low and high input levels can be prevented through output noise filtering. Care must be taken in choosing an output filter network that will not slow down the operating speed beyond what is desired.

ADDITIONAL RECOMMENDATIONS

1. For optimum performance, DAC9377-16 should be allowed sufficient warmup time (5 min).
2. Due to the small bit weight (152μV), noise becomes a noticeable factor; therefore, high quality sockets are recommended, if sockets are used, to minimize contact resistance.
3. When changing output/gain range, a resistor (connected between pins 9 and 10) with a temperature coefficient between 0 and 10ppm/°C, is required to keep the DAC9377-16 within guaranteed specifications.
4. No digital input should be left floating as the unit will draw excessive current.
5. Power supplys should be applied before or at the same times as the digital input supply.

LONG TERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. Offset Drift. For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 200μV for the first 1000 hrs; and 100μV per 1000 hrs thereafter.

b. Reference Voltage Drift. The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. Output Amplifier Gain Change. Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs, which can be corrected using the gain circuitry.

d. Linearity Drift. Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm F.S.R./1000 hrs.

IMPORTANT NOTICE TO THE USER: When measuring the stability of the DAC9377-16, care should be taken so that the drift of the measurement instruments can be separated from the drift factors mentioned above and the measurements are taken at identical temperatures.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC9377-16-6	16-Bit DAC with 16-bit linearity
DAC9377-16-5	16-Bit DAC with 15-bit linearity
DAC9377-16-4	16-Bit DAC with 14-bit linearity
DAC9377-4D	16-Bit 4 Decade BCD

Specifications subject to change without notice.