CY7C361

Ultra High Speed State Machine EPLD

Features

- **High speed: 125-MHz state machine output generation**
  - **Token passing**
  - **Multiple, concurrent processes**
  - **Multiway branch or join**
- **One clock with programmable clock doubler**
- **Programmable miser bits for power savings**
- **8 to 12 inputs with input macrocells**
  - **Metastability hardened: 10-year MBTF**
  - **0, 1, or 2 input registers**
  - **3 programmable clock enables**
- **32 synchronous state macrocells**
- **10 to 14 outputs**
  - **Skew-controlled OR output array**
  - **Outputs are sum of states like PLA**
- **Security fuse**
- **Available in 28-pin slimline DIP and 28-pin HLCC**
- **UV-erasable and reprogrammable**
- **Programming and operation 100% testable**

Product Characteristics

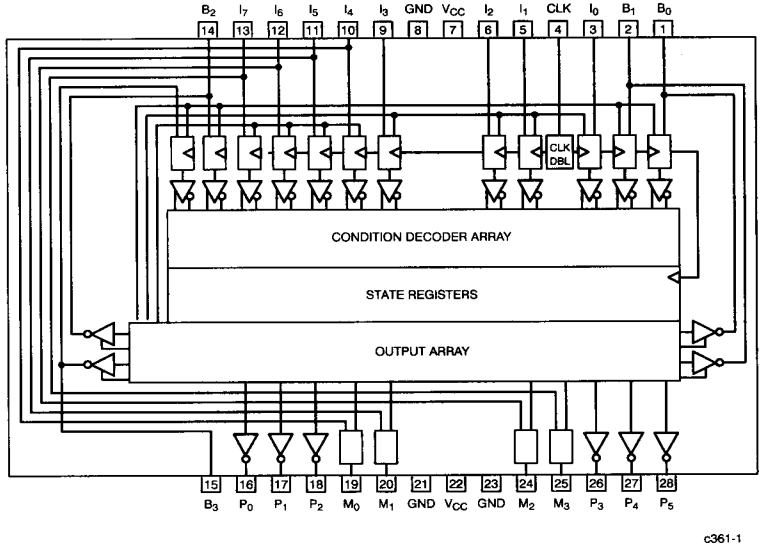
The CY7C361 is a CMOS erasable, programmable logic device (EPLD) with very high speed sequencing capabilities.

Applications include high-speed cache and I/O subsystems control, control of high-speed numeric processors, and high-speed arbitration between synchronous or asynchronous systems.

A programmable on-board clock doubler allows the device to operate at 125 MHz internally based on a 62.5-MHz input clock reference. The clock doubler is not a phase-locked loop. It produces an internal pulse on each edge of the external clock. The length of each internal pulse is determined by the intrinsic delays within the CY7C361. When the doubler is enabled, all macrocells in the CY7C361 are referenced to the doubled clock. If the clock doubler is disabled, a 125-MHz input clock can be connected to pin 4, and it will be used as a clock to all macrocells.

The CY7C361 has two arrays, similar to those in a PLA except that the registers are placed between the two arrays so that the long feedback path of the PLA is eliminated.

Logic Block Diagram



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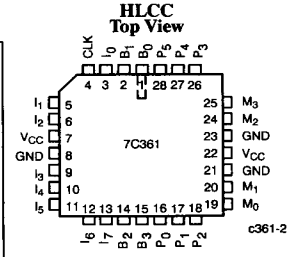
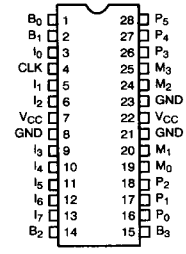
Pin Configurations

HLCC
Top View



c361-2

DIP
Top View



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Selection Guide

Generic Part Number	I_{CC} mA at f_{MAX}		f_{MAX} MHz		t_{IS} ns		t_{CO} ns	
	Com	Mil	Com	Mil	Com	Mil	Com	Mil
CY7C361-125	200		125.0		2		15	
CY7C361-100	200	200	100.0	100.0	3	3	19	19
CY7C361-83			83.3	83.3	5	5	23	23

Product Characteristics (continued)

In the CY7C361, the state information is contained in 32 state macrocells sandwiched between the input and output arrays. The current state information is fed back fast enough to achieve the 125-MHz operating frequency. These state macrocells also have serial connections that allow state machines to be built using a token-passing methodology similar to one hot encoding, but with the ability to support multiple active states at any given time.

The output array performs an OR function over the state macrocell outputs, allowing the control signals of the state machine to be produced directly. The signals from the output array are connected to the 14 device outputs (4 of which are bidirectional). In addition there are 3 sum terms that act as clock enables to the 3 groups of input macrocells. There are also 4 sum term output enables for the 4 bidirectional pins.

Input Macrocells

The CY7C361 has 12 input macrocells, shown in *Figure 1*. Each macrocell can be configured to have 0, 1, or 2 registers in the path of the input data. In the configuration where there is no input register, the set-up time required is the longest, because it includes the propagation delay through the input array plus the state register set-up time. In the single-registered configuration the set-up time is less than half of the unregistered case. The double-registered configuration is used to synchronize asynchronous inputs without causing metastable events.

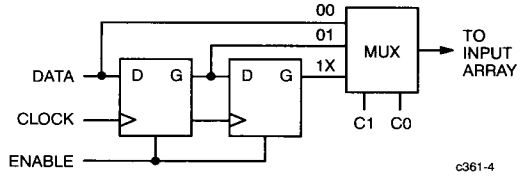


Figure 1. Input Macrocell

Input Register Enables

The input macrocells are divided into 3 groups of 4 macrocells each. Each of these groups has a register clock enable coming from the output array. The assignment of enable signal node numbers to input macrocells is as follows:

Input Nodes	Enable Node
3, 5, 6, 9	29
10, 11, 12, 13	30
1, 2, 14, 15	31

When the enable node is true, data is clocked into the registers of the input macrocells on the rising edge of the internal global clock.

Metastability Immunity

A high level of metastable immunity is afforded in the double-registered configuration. The CY7C361 registers are done in fast CMOS and they resolve inputs in a minimal amount of time. With all inputs switching at maximum frequency, one metastable event capable of violating the set-up time of a subsequent register occurs every 10 years. The probability of failure in a configured state machine is much lower than this calculation suggests, because there are more registers in the device and thus more decision time is allowed. No state machine failures due to metastable phenomena will be observed if the maximum frequency and double-registered operation frequency are used. This makes the CY7C361 ideally suited for constructing state machines requiring arbitration. For more information on metastability, refer to the "Are Your PLDs Metastable?" application note in the *Cypress Applications Handbook*.

Input Array

The input array is based on the condition decoder, shown in *Figure 2*. In a conventional PLA or PLD device, only PRODUCT1 would be present in the first array and the output and the feedback would be encoded by a second programmable or fixed or array. The speed of state machines is limited mainly by the feedback path.

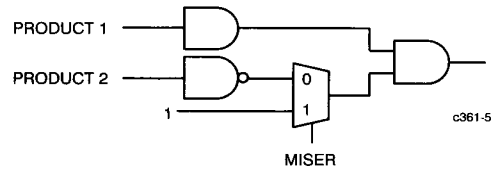


Figure 2. Condition Decoder

The condition decoder of the CY7C361 forms a product of a product and a sum over the input field. (The sum term is obtained by inverting the inputs to PRODUCT2.) Since there is immediate feedback information in the input field, multiway fork and join operations can be performed using this type of condition decoder. In other words, the condition decoder is used to control or gate the token being passed from macrocell to macrocell. In contrast, a traditional PLD or PLA requires more logic because the array is used to encode the states. In the CY7C361, state transitions can be made in half the time because there is no "state encoding" delay.

Each condition decoder has a miser bit in its sum term path. If the term is not used, the miser bit is automatically programmed. The miser bit completely disconnects the product term and replaces it with a logic HIGH. This results in a power savings.

The input array has 41 condition decoders: one global reset decoder, 8 local reset decoders, and 32 macrocell decoders. The array has 44 true/complement input pairs, 88 inputs total.

For speed reasons, the feedback signals are segmented. This means that for each group of 8 macrocells, 2 have global feedback, 2 have intermediate feedback to 16 of the 32 macrocells, and 4 have local feedback within their group of 8 macrocells only. Segmenting the feedback reduces the number of inputs per decoder to 56. Because the CY7C361 utilizes token passing, a large state machine will be effectively broken down into several smaller machines using 4 or less macrocells. The global and intermediate feedback is used to communicate between these smaller machines, and the local feedback is used within the smaller machines. For more information on the hot state encoding or token-passing design methodology, refer to the application notes titled "State Machine Design Considerations and Methodologies" and "Understanding the CY7C361" in the *Cypress Applications Handbook*.

State Machine Macrocells

The CY7C361 has 32 state macrocells. The state macrocells each have a single condition decode and share a common clock and global reset condition. The global reset is synchronous, and it lasts for two internal clock cycles. For each group of four state macrocells, there is a synchronous local reset condition.

All 32 of the macrocells are "daisy-chained." Each has a C_IN input that is connected to the C_OUT output of the previous macro-

cell, as shown in *Figure 3*. Configuration bit C2 is used in all state macrocells to select C_IN to be active (C2=0) or inactive (C2=1).

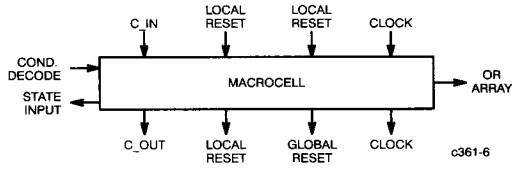
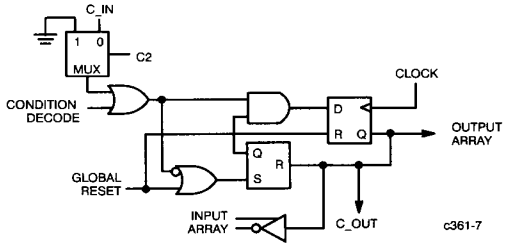


Figure 3. CY7C361 Macrocell

For the topmost macrocell (node 32), the C2 bit is used to specify a reset option. If the bit is 0, then the C_IN for this macrocell will be true (1). If the C2 bit is 1, then the C_IN for the macrocell will be false (0).

There are three state macrocell configurations: START, TOGGLE, and TERMINATE. The purpose of the START configuration is to create a "token" based on the condition decode. The TOGGLE configuration is used for building counters. The TERMINATE configuration is used to insert wait states in a process. It captures a token and holds it until a condition tells it to terminate the token.

Figure 4 shows a state macrocell in the START configuration. This configuration synchronously creates a token if C_IN or the condition decode is a logic HIGH. The token is represented by a true output on the macrocell register going to the output array and back as feedback to the input array. A machine implemented in the CY7C361 will consist of multiple machines or processes running concurrently, each with zero, one or more tokens active at any given time. Put another way, each state macrocell in the CY7C361 can be thought of as a line of microcode that can execute concurrently.



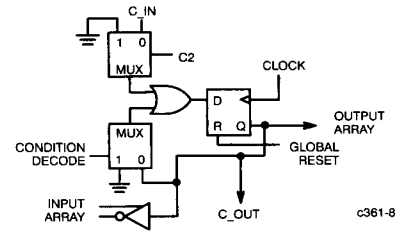
C1,C0 = 0,0: START

Figure 4. Start Configuration

In addition to the main register going to the array, there is an R-S latch in the feedback path that is used to convert the input condition to a pulse.

In operation, the START macrocell starts from a reset condition (output array input = FALSE). When a condition decode "fires" or a token is carried in (C_IN), the register output (Q going to the array) goes true for exactly one cycle. The OR of the condition decode and the C_IN must go FALSE before the START configuration can fire again. Local resets have no effect on this configuration.

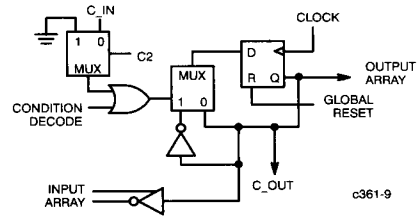
The TERMINATE macrocell (see *Figure 5*) captures a token via the C_IN path. The token is then held in the state register until the condition decoder fires, which causes the token to be terminated. Another way of saying this is that the TERMINATE macrocell is like a synchronous SR flip-flop. It is set by C_IN and reset by the condition decoder. Local resets have no effect on this configuration.



C1,C0 = 0,1: TERMINATE

Figure 5. Terminate Configuration

The TOGGLE macrocell (see *Figure 6*) operates like a T-type flip-flop. If C_IN or the condition decode is asserted, the state register will toggle on every rising edge of the internal clock. If neither the C_IN nor the condition decoder are asserted, the state register will retain its current state. The TOGGLE configuration is used to build counters. A local reset condition will synchronously reset the state register in this configuration.



C1,C0 = 1,0: TOGGLE

Figure 6. Toggle Configuration

The Output Array

The output array is an OR-based array. The array inputs are the LOW-asserted outputs of the 32 state macrocells. There are five types of array outputs. The first type is the three clock enables for the input macrocells. Each enable is a programmable OR of asserted state macrocells; when one of the connected macrocells is asserted, the clock is enabled. Next are the four output enables of the bidirectional I/O pins. Again, the output enables are a programmable OR of the connected asserted state macrocells; when one of the connected macrocells is asserted, the output is enabled. The third type of array output is the "pure" device output. These six outputs are a functional OR of the Low-asserted outputs of the state registers. Next is the output path of the four bidirectional I/O pins, which is identical to that of the "pure" outputs. The last type of array output is the Mealy output macrocell. The CY7C361 has four of these outputs; they can be used as a fast combinatorial out-

put. The three device outputs are pictured in *Figure 7*. Note that the Mealy output is the only one that is configurable.

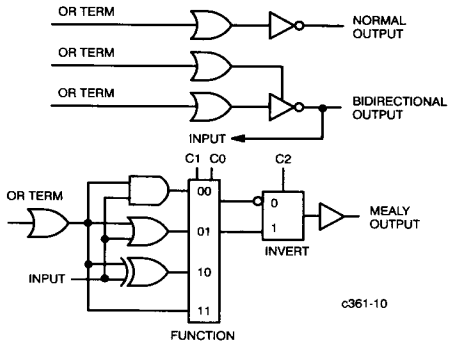


Figure 7. Output Configurations

In order to reduce output skew, the CY7C361 output array contains a set of self-timed latches in the output array path. These latches are controlled by an internal clock that has a delay equal to the worst-case path through the output array. While this delayed internal clock is LOW, the output array data is latched. When the delayed internal clock is HIGH, the latches become transparent, and the outputs change. These latches are the reason why the t_{CO} max is 15 ns with respect to the state registers, but the part can change its outputs every 7.5 ns. Since these latches cannot be accessed by the user, they have been left off of the block diagram.

The normal output signal from the device is a boolean sum of a subset of the state macrocell outputs. The subset selection is programmed into the output array. The number of state machines in the device, and the output mappings of each are determined by the user. The architecture is thus "horizontally divisible" and offers advantages in coding efficiency and event response time over the non-divisible architectures found in most PLA and sequencer implementations.

An output pin is normally LOW-asserted. The output gate performs an OR function over the flip-flop outputs of the state macrocells. The OR function includes only the outputs that are programmed to be connected to the OR line in the output array. When none of the connected state macrocell flip-flops are in the true or set condition, the output is HIGH, or deasserted. If any connected macrocell flip-flop is asserted (true) then the OR gate function is true and the output pin is LOW.

Forcing a false condition is easily accomplished by disconnecting all of the state macrocells from the OR line. To force a true condition, the OR line is connected only to node 73, which is labeled as V_{CC} in the block diagram. Any OR line connected to this node will be forced permanently true, which will cause any normal output to always be LOW.

The bidirectional outputs are I/O pins that may be used as either inputs or outputs. Under state machine control, these pins may be three-stated and used as inputs or outputs depending on how the OE term is programmed. If the OE is connected to node 73, the pin will always function as an output.

The Mealy outputs are designed to implement the fastest possible path between a device input and an output. Functions are available that combine the OR term and a specific input signal. These functions, XOR, AND, and OR, coupled with output polarity control are useful for data strobes and semaphore operations where signaling occurs based on the current state, but independent of a signal transition.

The AND and OR functions can be used to gate data strobe signals by the state. The XOR function can be used to implement two-cycle signaling, which is used in self-timed systems to minimize signaling delays. If these functions are not needed, then the Mealy outputs can be configured as normal outputs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (DIP Pins 7 or 22 to Pins 8, 21, or 23) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs During Programming ..... 0.0V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Programming Voltage 13.0V

Output Current into Outputs (LOW) ..... 8 mA

UV Exposure ..... 7258 Wsec/cm^2

Latch-Up Current ..... >200 mA

Static Discharge Voltage ..... >1500V (per MIL−STD−883, Method 3015)

Operating Range

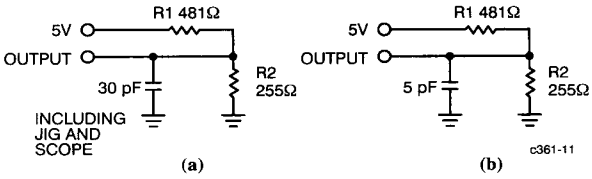
Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

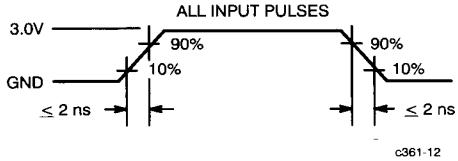
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Level	Guaranteed HIGH Input, All Inputs[1]		2.2		V
V_{IL}	Input LOW Level	Guaranteed LOW Input, All Inputs[1]			0.8	V
I_{IX}	Input Leakage Current	V_{SS} < V_{IN} < V_{CC}, V_{CC} = Max.		−10	+10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{SS} < V_{OUT} < V_{CC}		−40	+40	μA
I_{SC}[2]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]		−30	−110	mA
I_{CC}[2, 4]	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open, Operating at f = f_{MAX}	Commercial		200	mA
			Military			

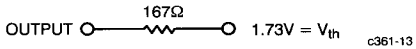
Notes:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Tested initially and after any design or process changes that may affect this parameter.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested with device programmed as an 8-bit counter.

AC Test Loads and Waveforms

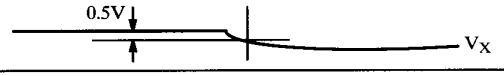
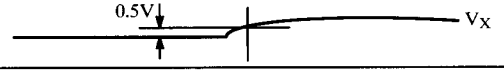
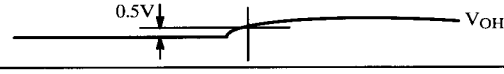
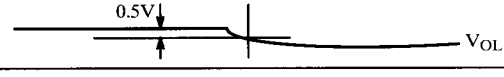




Equivalent to: THÉVENIN EQUIVALENT



Test Waveforms

Parameter	V_X	Output Waveform—Measurement Level
$t_{CER(-)}$	0.0V	
$t_{CER(+)}$	2.6V	
$t_{CEA(+)}$	V_{th}	
$t_{CEA(-)}$	V_{th}	

Commercial Switching Characteristics Over the Operating Range[5, 6]

Parameter	Description	−125		−100		−83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Mealy Output Delay	2	9	2	11	2	12	ns
t_{CO}[7]	Clock to Output Delay		15		19		23	ns
t_{CM}[7]	Clock to Mealy Output Delay		17		20		25	ns
t_{OH}	Output Stable Time	5		5		5		ns
t_{IS}	Input Register Input Set-Up Time	2		3		5		ns
t_{IH}	Input Register Input Hold Time	3		4		5		ns
t_S[8]	State Register Input Set-Up Time	7		9		12		ns
t_H[8]	State Register Input Hold Time	0		0		0		ns
t_{DWH}[2, 9, 10]	Input Clock Pulse Width HIGH (Doubler Enabled)	6		7		9		ns
t_{DWL}[2, 9, 10]	Input Clock Pulse Width LOW (Doubler Enabled)	6		7		9		ns
t_{DP}[2, 10]	Input Clock Period (Doubler Enabled)	15		20		24		ns
t_{WH}[2, 9, 11]	Input Clock Pulse Width HIGH	2		3		4		ns
t_{WL}[2, 9, 11]	Input Clock Pulse Width LOW	2		3		4		ns
t_P[2, 11]	Input Clock Period	7.5		10		12		ns
t_{SO}[12]	Output Skew		2		2		2	ns
t_{SM}[13]	Mealy Output Skew		3		3		3	ns
f_{MAXI}[2, 11]	Input Maximum Frequency (Doubler Enabled)	62.5		50.0		41.7		MHz
f_{MAX}[2, 4]	Output Maximum Frequency	125.0		100.0		83.3		MHz
t_{CER}[2, 6]	Clock to Output Disable Delay		16		20		22	ns
t_{CEA}[2, 14, 15]	Clock to Output Enable Delay		16		20		22	ns

Notes:

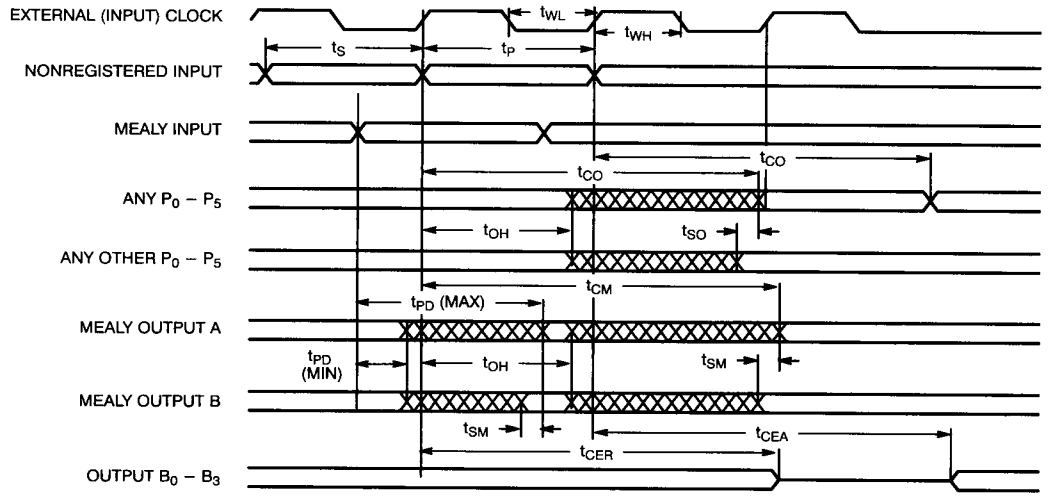
5. Output reference point on AC measurements is 1.5V, except as noted in Test Waveforms:
   $t_{CER(-)}$ negative going is measured at V_{OH} − 0.5V.
   $t_{CER(+)}$ positive going is measured at V_{OL} + 0.5V
6. Part (a) of AC Test Loads and Waveforms is used for all parameters except t_{CEA} and t_{CER}. Part (b) of AC Test Loads and Waveforms is used for t_{CEA} and t_{CER}.
7. This specification is guaranteed for the worst-case programmed pattern for which all device outputs are changing state on a given access or clock cycle.
8. Input register bypassed.
9. The clock input is tested to accommodate a 60/40 duty cycle waveform at the maximum frequency.
10. This applies to the input clock when the doubler is enabled.
11. This applies to the input clock when the doubler is disabled.
12. This parameter specifies the maximum allowable t_{CO} clock to output delay difference, or skew, between any two outputs on the same device triggered by the same clock edge with all other device outputs changing state within the same clock cycle.
13. This parameter specifies the maximum allowable t_{PD} difference between any two Mealy outputs on the same device triggered by the same or simultaneous input signals with all other device outputs changing state within the same access or clock cycle.
14. R1 is disconnected for $t_{CEA(+)}$ positive going (open circuited). See part (b) of AC Test Loads and Waveforms.
15. R2 is disconnected for $t_{CEA(-)}$ negative going (open circuited). See part (b) of AC Test Loads and Waveforms.

Military Switching Characteristics Over the Operating Range[5, 6]

Parameter	Description	Military				Unit
		−100		−83		
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Mealy Output Delay	1.5	11	1.5	13	ns
t_{CO}[7]	Clock to Output Delay		19		23	ns
t_{CM}[7]	Clock to Mealy Output Delay		21		25	ns
t_{OH}	Output Stable Time	5		5		ns
t_{IS}	Input Register Input Set-Up Time	3		5		ns
t_{IH}	Input Register Input Hold Time	4		5		ns
t_S[8]	State Register Input Set-Up Time	9		12		ns
t_H[8]	State Register Input Hold Time	0		0		ns
t_{DWH}[2, 9, 10]	Input Clock Pulse Width HIGH (Doubler Enabled)	7		9		ns
t_{DWL}[2, 9, 10]	Input Clock Pulse Width LOW (Doubler Enabled)	7		9		ns
t_{DP}[2, 10]	Input Clock Period (Doubler Enabled)	20		24		ns
t_{WH}[2, 9, 11]	Input Clock Pulse Width HIGH	3		4		ns
t_{WL}[2, 9, 11]	Input Clock Pulse Width LOW	3		4		ns
t_P[2, 11]	Input Clock Period	10		12		ns
t_{SO}[12]	Output Skew		3		3	ns
t_{SM}[13]	Mealy Output Skew		4		4	ns
f_{MAXI}[2, 11]	Input Maximum Frequency (Doubler Enabled)	50		41.7		MHz
f_{MAX}[2, 4]	Output Maximum Frequency	100.0		83.3		MHz
t_{CER}[6]	Clock to Output Disable Delay		20		22	ns
t_{CEA}[2, 14, 15]	Clock to Output Enable Delay		20		22	ns

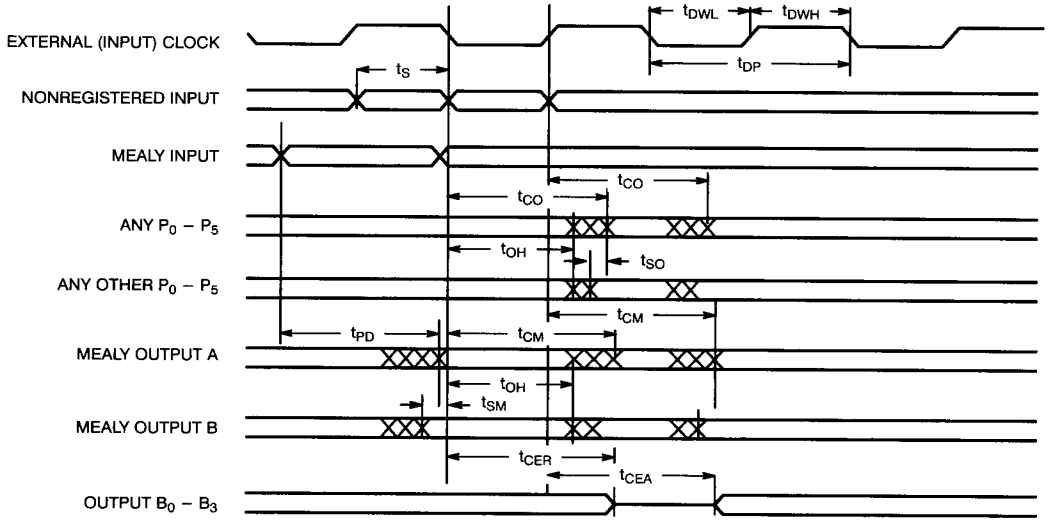
Switching Waveforms

Clock Doubler Inactive (Virgin State).
Nonregistered Input (Virgin State – C1,C0 = 0,0).



c361-18

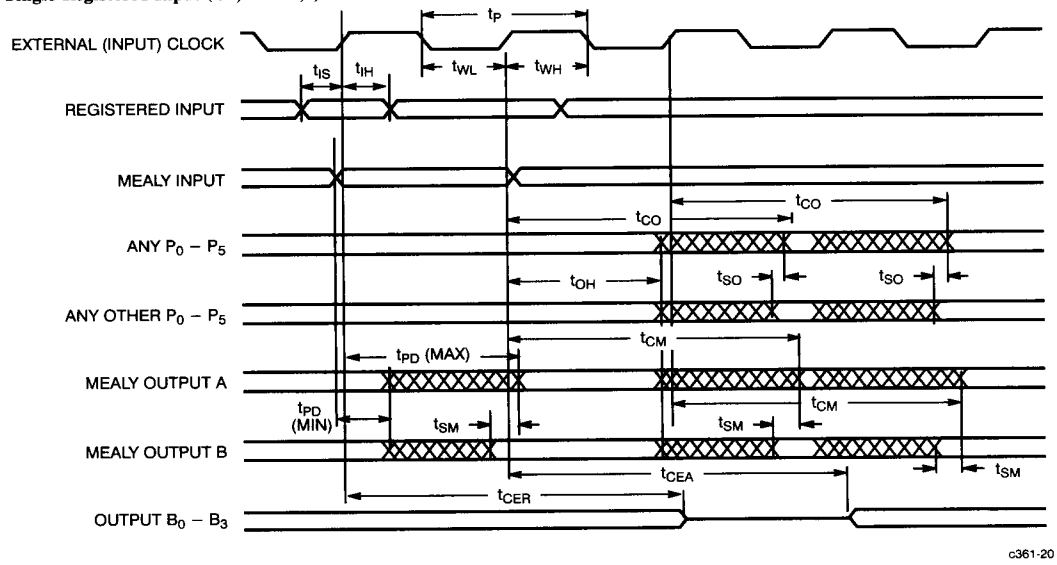
Clock Doubler Enabled (C0 = 1)
Nonregistered Input (Virgin State – C1,C0 = 0,0)



c361-19

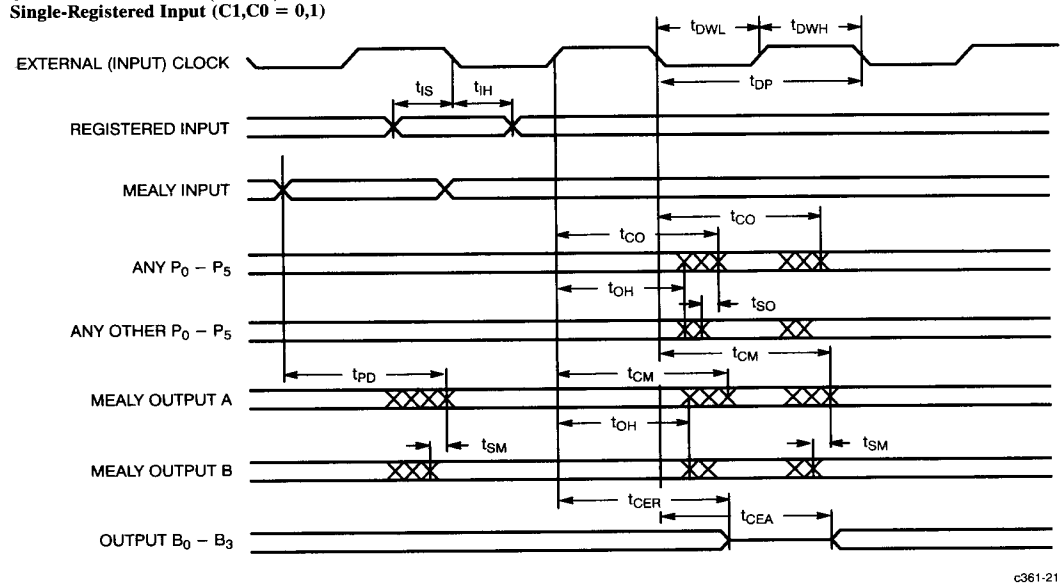
Switching Waveforms (continued)

Clock Doubler Inactive (Virgin State).
Single-Registered Input (C1,C0 = 0,1).



c361-20

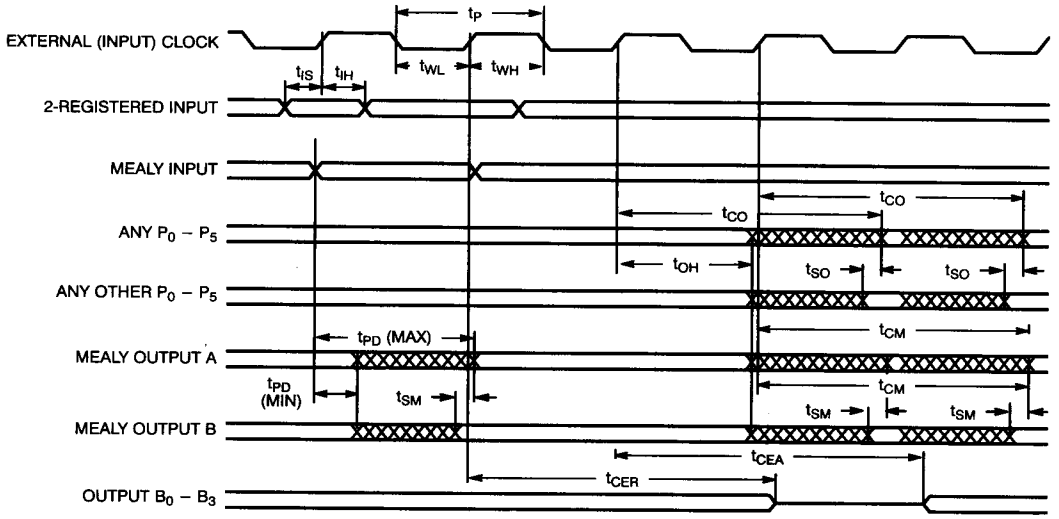
Clock Doubler Enabled (C0 = 1)
Single-Registered Input (C1,C0 = 0,1)



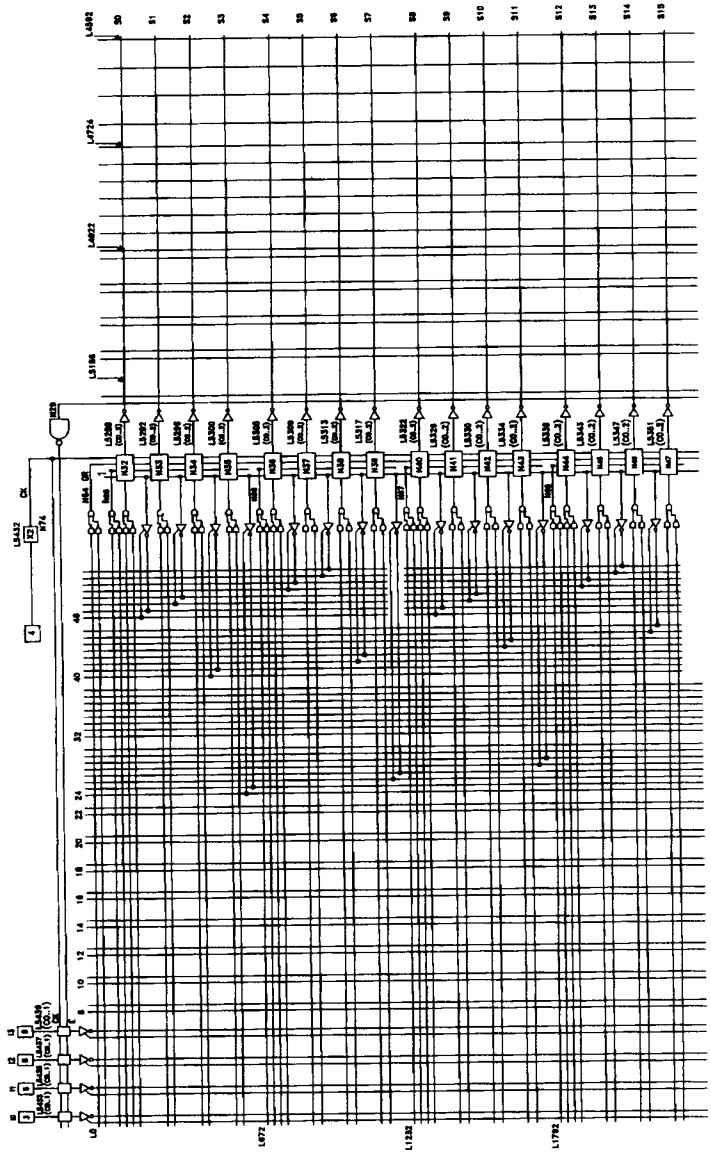
c361-21

Switching Waveforms (continued)

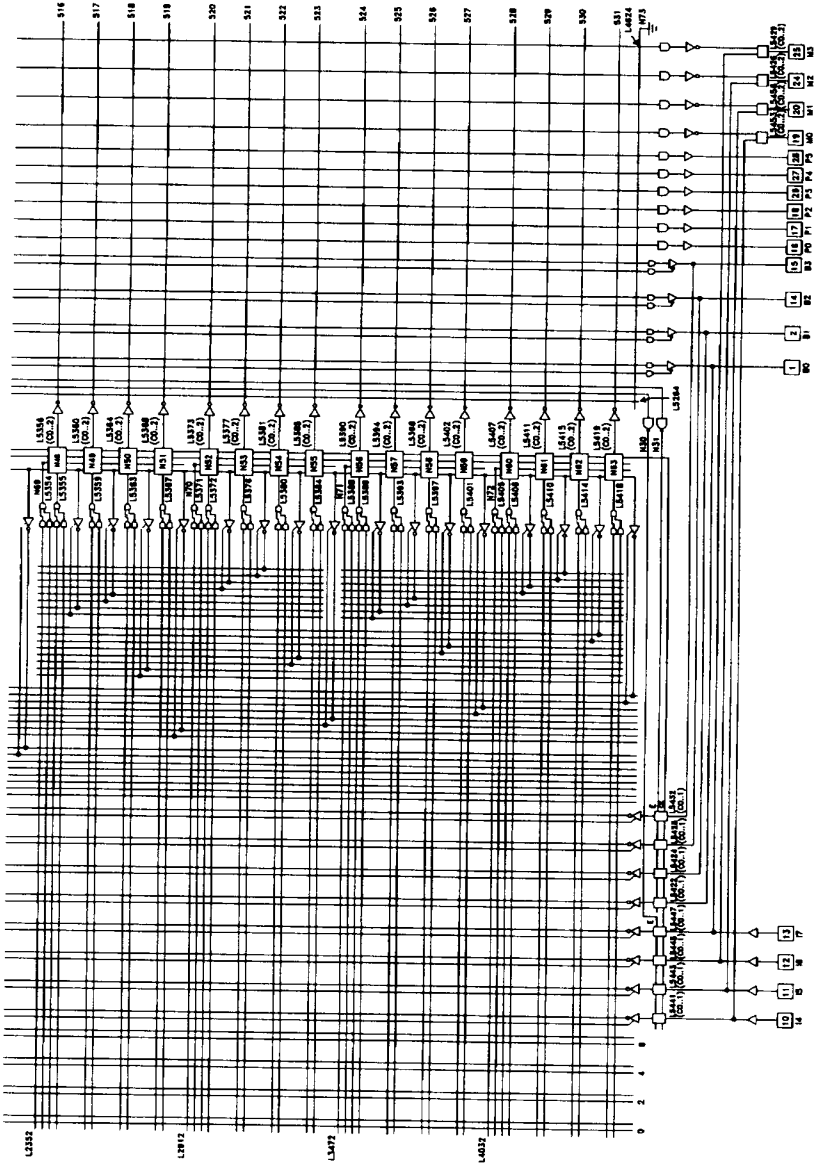
Clock Doubler Inactive (Virgin State)
Double-Registered Input (C_1, C_0 = 1,X)



CY7C361 Block Diagram (Upper Half)



CY7C361 Block Diagram (Lower Half)



Ordering Information

I_{CC} mA	f_{MAX} MHz	Ordering Code	Package Name	Package Type	Operating Range
200	125.0	CY7C361–125HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C361–125WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	100.0	CY7C361–100HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C361–100WC	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C361–100HMB	H64	28-Pin Windowed Leaded Chip Carrier	Military
		CY7C361–100QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C361–100WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
	83.3	CY7C361–83HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C361–83WC	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C361–83HMB	H64	28-Pin Windowed Leaded Chip Carrier	Military
		CY7C361–83QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C361–83WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{CM}	7, 8, 9, 10, 11
t_{OH}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{S}	7, 8, 9, 10, 11
t_{H}	7, 8, 9, 10, 11

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