AP-645

APPLICATION NOTE

3 Volt and 5 Volt FlashFile™ Memory Migration Guide

December 1998

NOTE: This document formerly known as *Word-Wide FlashFile™ Memory (28F160S3, 28F320S3, 28F160S5, 28F320S5) Migration Guide.*

Order Number: 292203-003

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
06/09/97	-001	Original version
12/02/97	-002	Updated all references to 28F160S3/S5 to include 28F320S3/S5. Updated Section 1.0 *Introduction* to clarify descriptive text. Updated Section 3.1 *Pinout.* Added Table 3 and adjusted all subsequent table numbers. Corrected documentation error in Table 5. Added Figure 1 and adjusted all subsequent figure numbers. Corrected documentation error in Table 7. Updated Section 4.4.3 *Enhanced Suspend Operations* to clarify descriptive text. Updated Section 4.4.8 *Commands Not Supported on the S3/S5* to clarify descriptive text. Removed Section on Specification Differences. Updated Figure 2 and Figure 3 and all associated references. Updated Section 6.0 *Conclusion* to clarify descriptive text. Moved Rev -001 Section 6.0 *Conversion Checklist* to Section 2.0. Updated Rev -001 Table 19 *Checklist*, split it into two tables, and moved it to Table 1 and Table 2. Adjusted all subsequent section numbers and table numbers. Updated Appendix A document references.
12/01/98	-003	Name of document changed from *Word-Wide FlashFile™ Memory (28F160S3, 28F320S3, 28F160S5, 28F320S5) Migration Guide*

1.0 INTRODUCTION

This application note discusses design migration from 28F016SA/SV FlashFile™ memories to 3 Volt and 5 Volt FlashFile memories (28F160S3, 28F320S3, 28F160S5, 28F320S5). The remainder of this application note will refer to 28F016SA/SV devices as SA/SV and 28F160S3, 28F320S3, 28F160S5, and 28F320S5 devices as S3/S5.

The S3/S5 memory devices provide enhancements which reduce cost, increase performance and ease upgrades:

- Multiple Voltage Options
- Common Flash Interface (CFI) Support
- Scaleable Command Set (SCS) Support
- Enhanced Suspend Operations
- Two 32-Byte Buffers
- New Status Register Structure

In addition, S3/S5 are manufactured on Intel's 0.4 micron ETOX™ V process technology. SA/SV are manufactured on Intel's 0.6 micron ETOX IV process technology. The Intel 0.4 micron ETOX V process technology reduces manufacturing costs.

This application note focuses on three topics:

- hardware compatibility
- software compatibility
- design for forward-compatibility

The first two sections highlight specific differences between SA/SV and S3/S5. The last section will discuss how to design in a SA/SV device today for upgrade to a S3/S5 in the future.

This documentation is meant for use with the *3 Volt-FlashFile™ Memory 28F160S3, 28F320S3* datasheet and/or *5 Volt- FlashFile™ Memory 28F160S5, 28F320S5* datasheets. Please refer to the documentation listed in Appendix A of this application note for a full description of all flash memory components discussed in this application note.

2.0 CONVERSION CHECKLIST

Table 1 and Table 2 provide a brief overview of the hardware and software changes required to migrate from SA/SV to S3/S5.

Table 1 is a checklist of hardware changes and Table 2 is a checklist of software changes that need to be considered when converting to S3/S5 or when designing in an upgrade path to S3/S5.

Table 1. Hardware Checklist for SA/SV Migration to S3/S5

Migrating from SA/SV	Migrating to S3/S5	Changes Required	Refer to Section
Three pinout differences:			3.1
3/5#	3/5# pin becomes NC	NC may be driven or floated	
RY/BY#	RY/BY# pin becomes STS	Be aware of operational differences between RY/BY# and STS pins. STS in default mode is the same as RY/BY in default mode	
A_{21}	A_{21} pin on 32-Mb device	Connect A_{21} on 32-Mb device	
Uses 12 V V_{PP}	12 V V_{PP} Not Available	For 28F160/320S3: Connect V_{PP} to 2.7 V, 3.3 V or 5 V (away from 12 V V_{PP}) For 28F160/320S5: Connect V_{PP} to 5 V (away from 12 V V_{PP})	3.2 and 5.1.3
Uses 3.3 V or 5 V V_{CC} (2.7 V V_{CC} is not available on the SA/SV)	2.7 V V_{CC} is available on 28F160/320S3	Connect V_{CC} to 2.7 V if desired (away from 5 V is required or away from 3.3 V if desired)	3.2 and 5.1.2
Uses 5 V or 12 V V_{PP} (2.7 V and 3.3 V V_{PP} is not available on SA/SV)	2.7 V and 3.3 V V_{PP} is available on 28F160/320S3	Connect V_{PP} to 2.7 V or 3.3 V if desired (away from 12 V V_{PP} is required or away from 5 V if desired)	3.2 and 5.1.3
28F016SA is Write Protected when $V_{PP} = V_{CC}$	Device is Write Protected when $V_{PP} \leq V_{PPLK}$, not when $V_{PP} = V_{CC}$	Provide a means to switch V_{PP} to GND	3.3 and 5.1.4
65 ns access time available on 28F160SV	No 65 ns access time available on S3/S5	28F160S5 has 70 ns access time	Datasheet
Some DC and AC Characteristics on the SA/SV change	Some DC and AC Characteristics on the S3/S5 differ	Change design as necessary	Datasheet
SA/SV are available in TSOP and SSOP packages.	28F160S3/S5 are available in TSOP and SSOP packages. 28F320S3/S5 are available in SSOP packages.	Consider packages available	Datasheet

Table 2. Software Checklist for the SA/SV Migration to the S3/S5

Migrating from SA/SV	Migrating to S3/S5	Solution	Refer to Section
SA/SV use the 28F008SA Compatible Command Set and Performance-Enhancement Command Set	S3/S5 use the CFI-SCS Compatible Command Set	Create new software or update existing software for commands listed in Table 6. Use device identification method described in Section 5.2.2.	4.1, 4.2, 4.3, 4.4 and 5.2
Command queuing available on SA/SV	No command queuing available on S3/S5	Designs incorporating command queuing will need to update software by polling for WSM ready or create new software	4.5
Status register bits arranged differently on SA/SV	Status register bits arranged differently on S3/S5	Refer to Table 9 to make sure correct bit is being polled in software	4.6

3.0 HARDWARE COMPATIBILITY

3.1 Pinout

There are three pinout differences between the S3/S5 and SA/SV memories. These difference are summarized in Table 3.

The 3/5# pin on the SA/SV, which is used to configure internal circuits for operation at either 3.3 V or 5 V V_{CC}, has become a No Connect (NC) pin on the S3/S5. The 28F160/320S3 operates at 2.7 V or 3.3 V V_{CC} and the 28F160/320S5 operates at 5 V V_{CC}. The No Connect pin is not internally connected and may be driven or floated.

Second, the RY/BY# pin on the SA/SV has become the STS pin on the S3/S5. Both the RY/BY# pin (on the SA/SV) and STS pin (on the S3/S5) operate in the same way at device power-up. They both default to a "level-mode RY/BY#" configuration at device power-up. In this configuration, the device pulls the RY/BY# or STS pin low whenever the Write State Machine (WSM) is busy performing an operation. Both pins can be configured in software. See Section 4.4.7 for further information.

The last pinout difference is an extra address pin (A_{21}) on the 32-Mbit device (28F320S3/S5). This pin is a No Connect (NC) on the 16-Mbit devices.

Table 3. 3 Volt/5 Volt FlashFile™ Memory Pinout Differences

Migrating from SA/SV	to 28F160S3/S5	to 28F320S3/S5
3/5#	NC	NC
RY/BY#	STS	STS
NC	NC	A_{21}

NOTE:
The DC Characteristics have changed somewhat between the devices. Some pins may handle different voltages or currents on the S3/S5 than they did on the SA/SV. Refer to the datasheets for further information.

3.2 Multiple Voltage Options

The S3/S5 devices incorporates both fast programming and low-power operation. This voltage flexibility allows designers to incorporate different voltage combinations in their applications. Fast program and erase performance can be realized at 5 V V_{PP} on both the 28F160/320S3 and 28F160/320S5. Low-power operation occurs at 2.7 V or 3.3 V V_{PP} on the 28F160/320S3 and 5 V V_{PP} on the 28F160S3/S5 and 28F320S3/S5.

Table 4. 28F160/320S5: Voltage Combinations

V_{CC} Voltage	V_{PP} Voltage
5.0 V	5.0 V

Table 5. 28F160/320S3: Voltage Combinations

V_{CC} Voltage	V_{PP} Voltage
2.7 V	2.7 V, 3.3 V and 5.0 V
3.3 V	3.3 V and 5.0 V

There is **no 12 V V_{PP} available** on the S3/S5. Applying 12 **V** V_{PP} to the S3/S5 could damage the device. The S3/S5 provides faster programming at 5 V V_{PP} than the SA/SV at 12 V V_{PP}.

3.3 Write Protection Using V_{PPLK}

As a write protection method, some 28F016SA applications may pull V_{PP} voltage to V_{CC} when not in use. However, the S3/S5's V_{CC} voltage is not low enough to lockout program and erase operations. On these devices, V_{PP} should be pulled below V_{PPLK} to protect data. An external pulldown resistor can be used to pull V_{PP} to GND when not in use. Other write protection alternatives like RP# and WP# should also be used.

4.0 SOFTWARE COMPATIBILITY

This application note is intended to give an operational overview of the differences between the SA/SV and the S3/S5 memory devices. For complete information on command sets, refer to the datasheets.

Figure 1 shows that the Intel Basic Command Set (BCS) is a subset of the Intel Scaleable Command Set (SCS).

4.1 Common Flash Interface (CFI)

The S3/S5 supports CFI. This specification allows for compatibility between the S3/S5 and future CFI-compliant devices. By incorporating CFI, software can be standardized for long-term compatibility. For more information on CFI, refer to AP-646, *Common Flash Interface and Command Sets* or the CFI Specification.

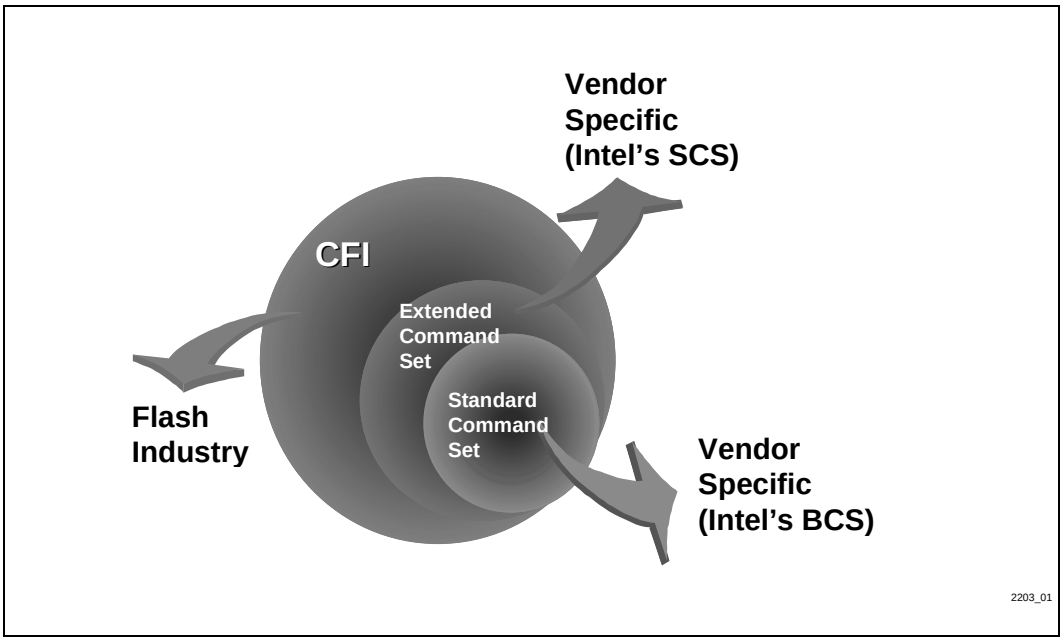

Figure 1. BCS, SCS, and CFI

4.2 Scaleable Command Set (SCS)

The S3/S5's SCS command definitions are similar in function to the Performance-Enhancement Commands on the SA/SV. However, the command codes are different. Software changes may be required to migrate from the SA/SV to the S3/S5 devices. For more information on SCS, refer to *AP-646, Common Flash Interface and Command Sets*.

4.3 Intel Basic Command Set (BCS)

The Intel BCS, formerly the 28F008SA Compatible Command Set, is the same between the S3/S5 and the SA/SV. If your software makes use of only the commands contained in the Intel BCS, minimal software updates are required. In this case, note that the Intelligent Identifier and Suspend commands have been enhanced. See Sections 4.4.2 and 4.4.3 for further information.

4.4 Command Superset

Commands summarized in Table 6 show which commands on the S3/S5 have been enhanced, added, and deleted in comparison to the SA/SV. Commands labeled "Enhanced on S3/S5" have the same command codes between the S3/S5 and the SA/SV, but have been improved in some way. Commands labeled "New on S3/S5" have new command codes that were not available on the SA/SV. Some commands, labeled "Not Supported on S3/S5" are replaced by new S3/S5 commands. Commands not supported on S3/S5 and their new replacement commands have been grouped in the table. Other unsupported commands are not replaced by any S3/S5 command. Commands not listed in Table 6 operate exactly the same between the devices.

Table 6. Summary of Command Changes Between the SA/SV and the S3/S5

Command Function	Command Code	Enhanced on S3/S5	New on S3/S5	Not Supported on S3/S5	Notes
Intelligent Identifier	90H	✔			
Suspend	B0H	✔			
Lock Block / Confirm	77H/D0H			✔	
Set Block Lock-Bit / Confirm	60H/01H		✔		
Clear Block Lock-Bits / Confirm	60H/D0H		✔		2
Single Load to Page Buffer	74H			✔	
Sequential Load to Page Buffer	E0H			✔	
Page Buffer Write to Flash	0CH			✔	
Write to Buffer / Confirm	E8H/D0H		✔		
Erase All Unlocked Blocks / Confirm	A7H/D0H			✔	
Full Chip Erase / Confirm	30H/D0H		✔		
Device Configuration	96H/CC			✔	3
STS Configuration	B8H/CC		✔		3

Table 6. Summary of Command Changes Between the SA/SV and the S3/S5 (Continued)

Command Function	Command Code	Enhanced on S3/S5	New on S3/S5	Not Supported on S3/S5	Notes
Read Query	98H		✔		
Read Extended Status Register	71H			✔	1
Read Page Buffer	75H			✔	
Page Buffer Swap	72H			✔	
Two-Byte Program	FBH			✔	
Upload Status Bits	97H			✔	
Upload Device Information	99H			✔	
Sleep	F0H			✔	
Abort	80H			✔	

NOTES:

1. The status registers differ between the SA/SV and the S3/S5. Please see Section 4.6 for more information.
2. The SA/SV parts unlock blocks by performing an erase on a locked block with WP# at logic high.
3. CC = Configuration Code. See Section 4.4.7 for more information.

4.4.1 READ QUERY MODE COMMAND

The Read Query command (98H) allows reading of the Common Flash Interface (CFI) Query structure. The CFI specification allows for future compatibility. System software should parse this structure to gain critical information about flash writes, block erases, and other flash component characteristics. The query is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI. For more information on CFI and its use in this device see the datasheets, application note *AP-646, Common Flash Interface and Command Sets*, or the CFI Specification.

4.4.2 ENHANCED INTELLIGENT IDENTIFIER OPERATION

The Intelligent Identifier command (90H) has been renamed the Read Identifier Codes command (90H) on the S3/S5. It continues to output the manufacturer code and device code. In addition, it has been enhanced to supply each block's lock configuration code. See the S3/S5 datasheets for the device identifier memory map.

The manufacturer and device identifier codes are different between the SA/SV and the S3/S5. Table 7 compares Identifier Codes. For the complete Identifier Codes description for the S3/S5, see the datasheets.

Table 7. Identifier Code Comparison

Device	Manufacturer Code	Device Code
28F016SA	89H	A0H
28F016SV	89H	A0H
28F160S3/S5	B0H	D0H
28F320S3/S5	B0H	D4H

4.4.3 ENHANCED SUSPEND OPERATIONS

The SA/SV supports the Erase Suspend to Read command (B0H). The S3/S5 enhances the following suspend capabilities:

- Erase Suspend to Read
- Erase Suspend to Program
- Program Suspend to Read

The Erase Suspend command (B0H) interrupts a block erase so that another block can be read or programmed. status register bit SR.6 reflects the erase suspend status. Any programming operation that is initiated during a suspended block erase can be suspended using the Program Suspend command.

The Program Suspend command (B0H) suspends byte/word programming as well as buffered programming so that another byte/word can be read. status register bit SR.2 reflects the program suspend status. Refer to Section 4.6 for more status register information.

All three suspend operations are continued by issuing the Resume command (D0H), the same as on the SA/SV. Note that a block erase cannot resume until program operations initiated during block erase suspend have completed.

4.4.4 BLOCK LOCKING AND BLOCK STATUS OPERATIONS

The block locking capability of the S3/S5 is similar to that of the SA/SV. The blocks are individually locked using a combination of hardware and software. Like the SA/SV, a block lock-bit is configured in software and hardware enabled by the WP# pin. Note that the S3/S5's command code to lock blocks is different from the SA/SV. See the datasheets for the write protection alternatives available on the S3/S5.

Within the S3/S5, a block lock-bit is assigned to each block. With WP# high, this block lock-bit can be set in software with the Set Block Lock-Bit command (60H/01H). This is a two-step sequence which ensures that block lock-bits are not accidentally set.

When WP# is low, all blocks with their block lock-bit set are locked. Locked blocks cannot be programmed, erased, or have their block lock-bit configured. Attempting to perform these operations on a locked block will result in status register bits SR.4 and SR.5 being set to "1," indicating an improper command sequence. A Full Chip Erase command (30H/D0H) with WP# active will erase only those blocks which are not locked.

The Clear Block Lock-Bits command (60H/D0H) simultaneously clears all of the block lock-bits. This is also a two-step sequence to protect against accidental clearing of block lock-bits. Similarly, this command will only clear the lock-bits when WP# is high.

The status of the block lock-bit can be found in one of two ways. The Read Identifier Codes command can be used to access the block lock configuration codes (See Section 4.4.2). Alternatively, the Read Query Command can be used to access the Block Status Register (See Section 4.4.1).

4.4.5 WRITING TO THE BUFFER

The architecture of the S3/S5 incorporates two 32-byte write buffers. This reduction in capacity from the 256-byte buffers found in the SA/SV lowers the cost of the S3/S5 without sacrificing performance. Using the Write to Buffer command (E8H) allows for writes at 2.0 µs/byte effective on the 28F160/320S5, and 2.7 µs/byte effective on the 28F160/320S3.

The functionality of the page buffers is similar between the SA/SV and S3/S5, but the commands used to operate the page buffers differ. The SA/SV's Single Load to Page Buffer, Sequential Load to Page buffer and Page Buffer Write to Flash commands have all been replaced by the Write to Buffer and Confirm commands on the S3/S5.

4.4.6 FULL CHIP ERASE

The S3/S5 incorporates a Full Chip Erase command (30H/D0H) which replaces the Erase All Unlocked Blocks command on the SA/SV. The Full Chip Erase command, followed by a confirm command, will erase all unlocked blocks when WP# is low, and will erase the entire chip when WP# is high. The Full Chip Erase command can be suspended to read from locked blocks when WP# is low.

4.4.7 STS CONFIGURATION

The STS pin on the S3/S5 can be configured to four different pulse modes. This capability is similar to the SA/SV's RY/BY# pin configuration. Table 8 shows each part's configuration options.

The S3/S5's STS pin is configured using a two bus cycle command set, including the STS Configuration command (B8H) and the Configuration Code (CC). Refer to the S3/S5 datasheets for the Configuration Coding Definitions.

4.4.8 COMMANDS NOT SUPPORTED ON THE S3/S5

The Read eXtended Status Registers (XSR's), Read Page Buffer, Page Buffer Swap, Two-Byte Program, Upload Status Bits, Upload Device Information, Sleep, and Abort commands are not directly replaced in the S3/S5's Scaleable Command Set. Some commands are now performed automatically by the device, and others are not used.

The status register structure is different between the SA/SV and S3/S5. Because of this change, some commands are no longer used on the S3/S5. The Read eXtended Status Registers command (71H) has been deleted. However, an eXtended Status Register (XSR) and Block Status Register (BSR) do exist. The XSR is automatically polled by the S3/S5 when a Write to Buffer command is issued. The BSR can be read from address 02H within each block by using the Read Query command. In addition, the Upload Status Bits command (97H), which was used to update status in the SA/SV's BSR and GSR, is no longer necessary. See Section 4.6 for more information on status registers.

The Read Page Buffer (75H) and Page Buffer Swap (72H) commands are not available on the S3/S5. The page buffer cannot be read on the S3/S5, and there is no manual page buffer swap. The SA/SV's Single Load to Page Buffer, Sequential Load to Page buffer and Page Buffer Write to Flash commands have all been replaced by the Write to Buffer and Confirm commands on the S3/S5.

In addition, the Upload Device Information command (99H) on the SA/SV wrote information into the page buffers including the Device Revision Number (28F016SA and 28F016SV), Device Proliferation Code (28F016SV only), and Device Configuration Code (28F016SV only). This command is not available on the S3/S5, however, similar types of information can be found in the query database. See Section 4.4.1 and the datasheets for more information on the query database.

The Two-Byte Program command (FBH) is not available on the S3/S5.

The Abort command (80H) does not exist on the S3/S5. A Write to Buffer command can be aborted by issuing an address outside of the current block address. Other operations can be aborted by bringing RP# low.

The Sleep command (F0H) is not supported on the S3/S5. The device does not have a sleep mode like the SA/SV.

4.5 Command Queuing

There is no command queuing on the S3/S5. However, CFI supports command queuing, and the Block Erase flowchart in the S3/S5 datasheet contains the steps necessary to incorporate command queuing on future devices. Applications which use command queuing on the SA/SV will have to use software to account for the lack of command queuing on the S3/S5. Software which previously took advantage of the command queuing capability of the SA/SV can be updated by polling for SR.7 = 1 (WSM ready) before issuing any new commands to the Command User Interface (CUI). An alternative is to create new software which does not incorporate command queuing.

4.6 Status Registers

The SA/SV devices have a Compatible Status Register (CSR), Global Status Register (GSR) and 32 Block Status Registers (BSRs). Most of the information reflected in these three status registers has been compressed into a single status register (SR) on the S3/S5. The 28F160/320, S3/S5 status register has the same structure as the 28F008/016, S3/S5 status register.

The S3/S5 has two additional status registers: the Block Status Register (BSR) and the eXtended Status Register (XSR). The S3/S5's BSR, unlike the SA/SV's BSR, is included in the CFI information and can be accessed by using the Read Query command. The S3/S5's XSR is accessed when a Write to Buffer command is issued. Devices which incorporate CFI erase queuing access the XSR during queued erase operations. The device accesses the XSR automatically in both cases.

Table 8. STS and RY/BY# Configurations

Configuration	S3/S5 (STS)	28F016SA (RY/BY#)	28F016SV (RY/BY#)
Level Mode RY/BY# (default mode)	✔	✔	✔
Pulse on Erase Complete	✔	✔	✔
Pulse on Program Complete	✔	✔	✔
Pulse on Erase or Program Complete	✔		✔
Disable		✔	✔

The status register on the S3/S5 can be read at any time by issuing a Read Status Register command (70H). status register data is also available to be read after the completion of a program, block erase, set lock-bit or clear lock-bits command sequence. Bits which are masked in the SA/SV CSR should not be masked when reading the S3/S5 status register.

For the full S3/S5 status register descriptions, see the S3/S5 datasheets. Table 9 gives a cross-reference for the various status register bits from the SA/SV to the S3/S5.

5.0 DESIGN FOR FORWARD-COMPATIBILITY

Manufacturers that use the SA/SV and plan to move to the S3/S5 in the future for cost reduction, CFI-SCS compliance, or other reasons should keep these design considerations in mind.

5.1 Hardware

5.1.1 PINOUT

To create a footprint which can accommodate both a SA/SV and S3/S5 pinout, the following procedures should be followed:

1. Connect the SA/SV's 3/5# pin to the correct level for its operation. This voltage level does not have to change when converting to the S3/S5 since the pin becomes a No Connect.
2. The STS and RY/BY# pins have the same function in hardware. However, the STS pin cannot be disabled like the RY/BY# pin. As long as these two pins are configured to the same mode in software, there are no hardware changes required.
3. Connect the A_{21} pin when using a 28F320S3/S5 device.

Pinout changes are discussed in Section 3.1. Refer to Sections 5.1.2 and 5.1.3 for information on V_{CC} and V_{PP}.

Table 9. Status Register Bit Cross Reference: SA/SV to S3/S5

Status	S3/S5	SA/SV CSR	SA/SV GSR	SA/SV BSR	Notes
Write State Machine Status	SR.7	CSR.7	GSR.7		
Erase-Suspend Status	SR.6	CSR.6			
Program-Suspend Status	SR.2	N/A			1
Operation Suspend Status	SR.6 or SR.2		GSR.6		1
Erase Status	SR.5	CSR.5			2
Data-Write Status	SR.4	CSR.4			2
Device Operation Status	SR.5 or SR.4		GSR.5		2
Improper Command Sequence	SR.5 and SR.4	CSR.5 and CSR.4			
Device Sleep Status	N/A		GSR.4		3
Block Status	SR.1			BSR.7	5
Block Lock Status	BSR.0			BSR.6	4
Block Operation Status	BSR.1, SR.5 or SR.4			BSR.5	4,5
Block Operation Abort Status	N/A			BSR.4	6
Queue Status	N/A (XSR.7)		GSR.3	BSR.3	7
V_{PP} Status	SR.3	CSR.3		BSR.2	
V_{PP} Level (28F016SV only)	N/A			BSR.1	6
Page Buffer Available Status	XSR.7		GSR.2		
Page Buffer Status	N/A		GSR.1		6
Page Buffer Select Status	N/A		GSR.0		6
Reserved	XSR.0–6 BSR.2–7 SR.0	CSR.2–0		BSR.0	

NOTES:

1. The S3/S5's SR.6 gives erase suspend information and SR.2 gives program suspend information.
2. The S3/S5's SR.4 and SR.5 also give set block lock-bit status and clear lock-bits status, respectively.
3. The S3/S5 does not have a sleep mode.
4. The S3/S5's BSR.0 and BSR.1 can be read using the Read Query command. See Section 4.4.7.
5. The S3/S5's SR.1, SR.5 and SR.4 give overall device information and are not block specific.
6. There are no status register bits in the S3/S5 which reflect this information.
7. The S3/S5 does not support command queuing. CFI-SCS compliant software that supports command queuing should poll XSR.7 for queue status.

5.1.2 V_{CC} VOLTAGE

V_{CC} voltage options differ slightly between the devices (refer to Table 10).

Table 10. V_{CC} Voltage Comparison

			28F160 28F320	
V_{CC} Voltage	**16SA**	**16SV**	**S3**	**S5**
5.0 V	✔	✔		✔
3.3 V	✔	✔	✔	
2.7 V			✔	

One migration path between the SA/SV and the S3/S5 is to use the same V_{CC} value on both devices. The SA/SV and 28F160S5 are capable of using 5 V V_{CC}. The SA/SV and 28F160S3 are capable of using 3.3 V V_{CC}. However, it should be noted there are some AC Characteristic differences between the parts at the same V_{CC} values (see the datasheets for further information). Applications that wish to take advantage of the 2.7 V V_{CC} operation of the S3/S5 can implement a jumper, as shown in Figure 2 The $V_{CC(original)}$ (3.3 ± 0.3 V) can be supplied from a converter and later removed after the conversion to S3/S5 has taken place

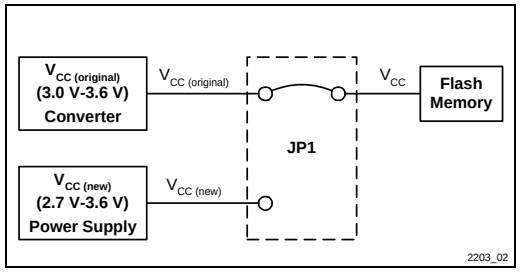

Figure 2. V_{CC} Jumper Selection

The S3/S5's V_{CC} maximum standby current is less than the 28F016SV and the same as the 28F016SA. However, for the V_{CC} read current, the current values are tested at separate frequencies between the three devices. Refer to the datasheets for DC Specification differences.

Conversion of SA/SV to the S3/S5 will most likely involve V_{PP} conversion from 12 V or 5 V to 2.7 V, 3.3 V, or 5 V. Because of this conversion, power supply current calculations should take into account the initial V_{CC} value, as well as an additional V_{PP} connection that may be present upon conversion.

5.1.3 V_{PP} VOLTAGE

V_{PP} voltage options differ between the devices. Table 11 shows a V_{PP} voltage comparison. It is possible to get the same or better write timings on the 28F160/320S5 at 5 V V_{PP} as on the 28F016SV at 12 V V_{PP}.

Table 11. V_{PP} Voltage Comparison

			28F160 28F320	
V_{PP} Voltage	**16SA**	**16SV**	**S3**	**S5**
12.0 V	✔	✔		
5.0 V		✔	✔	✔
3.3 V			✔	
2.7 V			✔	

To design in a 28F016SA today for migration to a S3/S5 in the future, it will be necessary to provide a jumper from 12 V V_{PP} to 2.7 V, 3.3 V, or 5 V V_{PP} as shown in Figure 3. In this case, $V_{PP\ (original)}$ is 12 V, supplied from a converter. $V_{PP(new)}$ will be 2.7 V, 3.3 V, or 5 V. Once conversion has taken place, the 12 V converter can be removed. DC and AC Characteristic differences should be taken into account as well (refer to the datasheets).

To design in a 28F016SV for migration to the S3/S5 in the future, 5 V V_{PP} can be used for both devices. There are some DC Specifications that differ in this case (refer to the datasheets). Some AC write timings differ between the devices (refer to the datasheets). Designs requiring fast programming should use 12 V V_{PP} on the 28F016SV and later convert to 5 V V_{PP} on the S3/S5. A jumper, such as the one shown in Figure 3, can be used. Designs requiring low power may want to use 2.7 V or 3.3 V V_{PP} after conversion to the 28F160/320S3. This operation can be accomplished by a jumper as well.

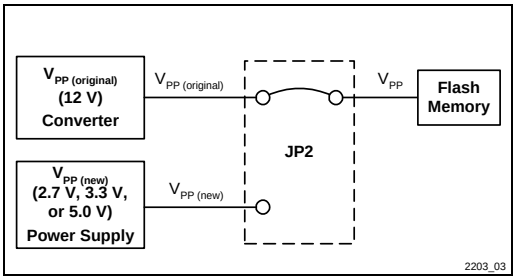

Figure 3. V_{PP} Jumper Selection

5.1.4 WRITE PROTECTION VIA V_{PPLK}

Switching V_{PP} "off" when not in use is a common write protection technique. It is necessary to switch V_{PP} below V_{PPLK} to ensure write protection on the 28F016SV and S3/S5. See Section 3.3 for further information.

5.1.5 READ/WRITE PERFORMANCE

Conversion to the S3/S5 may also be driven by its higher write performance. Component identification to determine whether the 28F016SA, 28F016SV or S3/S5 is in system can be accomplished via software methods (see Section 5.2.2). Depending on which component resides in the system, the state machine within the interface logic and/or system software can modify the program time of the flash memory space to take advantage of the S3/S5's higher write performance capability.

5.2 Software

5.2.1 COMMAND SET COMPATIBILITY

Applications using only the Intel Basic Command Set (BCS) can use the same software for the SA/SV and the S3/S5. Applications using the SA/SV Performance-Enhancement Commands should create one branch of software for the SA/SV and one branch of software for the S3/S5. Identifying whether the 28F016SA, 28F016SV or S3/S5 is in a system can be accomplished via software methods (see Section 5.2.2).

5.2.2 SOFTWARE IDENTIFICATION OF 28F016SA, 28F016SV OR 28F160S3/S5

The S3/S5 can be identified using the Read Query command (98H). After sending this command, a return of the ASCII "QRY" will indicate the presence of a CFI-compliant device. If a CFI-compliant device is found, reading of the CFI database will allow software to identify the device as the S3/S5 or another CFI-compliant device.

If the "QRY" data is not found, the read identifiers code command (90H) should be issued to the device to read the intelligent identifier codes of the SA/SV. For more information, refer to *AP-646, Common Flash Interface and Command Sets*.

6.0 CONCLUSION

This application note has summarized migration and compatibility considerations between the SA/SV and the S3/S5. The major differences that need to be considered for migrations are:

- Three Pinout Differences
- Input Voltage Differences
- AC and DC Specification Differences
- Software Differences

Refer to the documentation listed in Appendix A for more information on compatibility and device capabilities. Please contact your local Intel sales office, distribution sales office, or visit Intel's World Wide Web home page at http://www.intel.com for additional technical documentation and tools.

APPENDIX A
ADDITIONAL INFORMATION

Order Number	Document/Tool
290609	*5 Volt FlashFile™ Memory; 28F160S5 and 28F320S5* datasheet
290608	*3 Volt FlashFile™ Memory; Family 28F160S3 and 28F320S3* datasheet
292204	*AP-646 Common Flash Interface and Command Sets*
292163	*AP-610 Flash Memory In-System Code and Data Update Techniques*
292144	*AP-393 28F016SV Compatibility with 28F016SA*
292124	*AP-375 Upgrade Considerations from the 28F008SA to the 28F016SA*
292123	*AP-374 Flash Memory Write Protection Techniques*
292092	*AP-357 Power Supply Solutions for Flash Memory*
Note 3	*28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory* datasheet
Note 3	*28F016SA 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory* datasheet
www.mcif.org	*Common Flash Interface Specification*
Contact Intel/Distribution Sales Office	CFI - Common Flash Interface Reference Code

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. These documents can be located at the Intel World Wide Web support site, http://www.intel.com/support/flash/memory