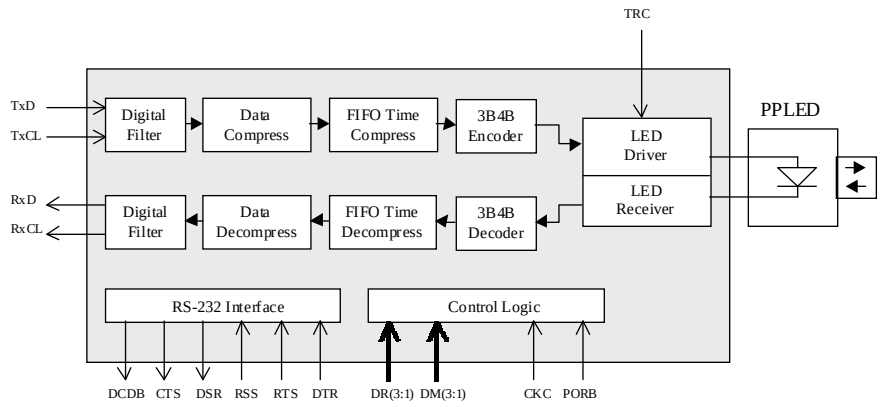
100 SERIES

ACS101A Revision 1.2 October 1999

Acapella Optical Modem IC

ACS101A Main Features:

* Full duplex serial transmission over one fiber.
* Link lengths up to 5km.
* Supports asynchronous data rates from DC to 76.8kbps.
* Supports synchronous data rates up to 512kbps.
* Full diagnostic modes - Remote and Local loopback.
* Uses a single Ping Pong LED (PPLED) to both receive and transmit data for single fiber operation.
* Supports two additional low frequency asynchronous channels or the RS-232 handshake signals.
* Digital mode for non fiber applications - RF.
* Bit Error Rate (BER) < 10^{-9}
* Available in 44 pin PLCC package.



Equivalent Block Diagram of ACS101A

General Description:

The ACS101A is a complete controller, driver and receiver IC, supporting full-duplex asynchronous transmission from DC to 76.8kbps and synchronous data rates up to 512kbps over one optical fiber. The ACS101A also supports two additional low frequency asynchronous channels or RS-232 handshake signals, RTS, CTS, DTR and DSR.

The ACS101A employs data compression and time compression techniques, affording high launch power in short bursts, leading to a low average power consumption. The advantage of this approach is that high link budgets can be achieved with inexpensive optical components.

Communicating optical modems automatically maintain synchronisation with each other such that the receive phase of one modem is lined-up with the transmit phase of the other, compensating for the propagation delay presented by the link. Link lengths from zero to maximum distance are catered for automatically. In 'standard' mode, the fiber may be up to 2.5km long, or up to 5km in 'double' mode.

Synchronous or Asynchronous Single Fiber Modem

Inter-IC Encoding Technique

The 3B4B encoding method is used for communication between ACS101A, thus ensuring that there is no DC component in the signal. The encoding and decoding is transparent to the user.

Transmitter and Receiver Functions

The TxD input data of the transmitting modem is compressed, filtered, and 3B4B encoded. In the receiving modem, 3B4B encoding ensures easy extraction of the bit-clock. The received data is filtered, decoded, then stored in an output memory. The memory provides time expansion, de-jittering and frequency compensation. Finally, the data is filtered again to improve BER then directed to the RxD output pin.

Transmit Current

The transmit current to the LED can be defined by the Transmit Current pin (TRC). The current is set to the maximum value (~100mA) when TRC is unconnected. The current is set to the minimum value (~10mA) when TRC is connected directly to ground. To obtain current values between minimum and maximum TRC is connected to ground through a resistor. The resistor value R is given by:

LED current drive (mA) = $\frac{100 * (110+R)}{(1100+R)}$

Data-rate Selection DR1 to DR4

Modes for Asynchronous Data :

DR4	DR3	DR2	DR1	XTAL freq (MHz)	Data-rate (kbps)	Distance
0	1	1	0	9.216	DC - 19.2	Double
1	1	1	0	9.216	DC - 38.4	Standard
1	1	1	0	18.432	DC - 76.8	Short

Modes for Synchronous Data :

DR4	DR3	DR2	DR1	XTAL freq (MHz)	Data-rate (kbps)	Distance
0	0	0	1	9.216	9.6	Double
0	0	1	0	9.216	19.2	Double
0	0	1	1	9.216	38.4	Double
0	1	0	0	9.216	48.0	Double
0	1	1	1	9.216	64.0	Double
1	0	0	0	9.216	2.4	Standard
1	0	0	1	9.216	9.6	Standard
1	0	1	0	9.216	19.2	Standard
1	0	1	1	9.216	38.4	Standard
1	1	0	0	9.216	48.0	Standard
1	1	0	1	9.216	56.0	Standard
1	1	1	1	9.216	64.0	Standard
0	1	0	1	9.216	192.0	Standard
0	0	0	0	9.216	256.0	Standard
0	0	0	0	18.432	512.0	Short

Standard' mode of operation is up to 2.5km, 'double' mode is up to 5km and 'short' is up to 1.25km. Other non-standard data-rates may be generated by using different crystal frequencies as long as the 5 - 19MHz crystal range is observed.

For data-rates of 9.6, 19.2, 33.4, 48 and 64kbps the data-rate selection pins DR1-DR3 are common to standard and double modes of operation, with DR4 selecting the distance mode.

Modem Control Signals

RSS.

RTS, CTS, DTR and DSR signals may be used in either of two modes, depending on the RSS setting:

RSS = Low; data transmission mode

RSS = High; modem handshake mode

RSS Low - Data Transmission Mode.

In data transmission mode the inputs RTS and DTR are sampled continuously at (crystal freq.) / 1536, 6.0kHz with a crystal of 9.216MHz. The outputs appear at CTS and DSR respectively.

RSS High - Modem Handshake Mode.

In modem handshake mode the control signals are used as conventional handshake signals between the DTE (terminal) and the DCE (modem):

DSR (Data Set Ready) DCE → DTE.

The DCE is powered up and asserts a Low (active level) on DSR. The DTE is informed that it is connected to a “live” DCE.

DTR (Data Terminal Ready) DTE → DCE.

The DTE is powered-up and asserts a Low (active level) on DTR. The DCE is informed that it is connected to a “live” DTE. If DTR is set High, the DCE responds by asserting DCDB High.

RTS (Request to Send) DTE → DCE.

The DTE recognises that synchronisation has been achieved (DCDB active) and asserts a Low (active level) on RTS. This constitutes a request by the DTE to send data to the far-end modem.

CTS (Clear to Send) DCE → DTE.

The DCE recognises the active RTS signal and responds by asserting a Low (active level) on CTS. If RTS is set High the DCE responds by bringing CTS High.

DCDB (Data Carrier Detect) DCE → DTE.

When synchronisation is achieved between DCEs the DCDB signal is set Low (active level). If synchronisation is lost the DCE sets DCDB and CTS High.

Crystal Clock

A crystal may be connected between the pins XLI and XLO. Alternatively, XLI may be driven directly by an external clock. The operational frequency range is 5MHz to 19MHz, though communicating devices must be driven at the same nominal frequency with a tolerance of 100ppm. In synchronous mode the frequency should be 9.216MHz, resulting in the standard range of synchronous communication frequencies selected by DR1-DR4.

For asynchronous operation, the choice of clock frequency dictates the sample rate of the asynchronous data appearing at the input TxD, and consequently the jitter on the output RxD. The sample frequency is always 1/36 of the chosen clock frequency in 'standard' mode and 1/72 in 'double' mode.

Integrating Capacitor

The ACS101A requires the use of an integrating ceramic capacitor of value 10nF - 33nF between pins CNT and GND for a crystal oscillator frequency range from 18MHz to 5MHz respectively.

PORB

The PORB pin is a single-pin alternative to the reset combination DM3 = 0, DM2 = 0, and DM1 = 1. If left unconnected the input pulls High to the operational state. Selecting reset using DM1-DM3 or holding PORB Low turns off the LED and most of the digital logic. The device has been designed to power-up correctly and operate without the aid of PORB.

Transmission Clock TxCL

The ACS101A gives a choice between internally and externally generated transmission clocks (see Figure 3. Timing diagrams for set-up and hold specifications).

When the CKC pin is held Low, TxCL is configured as an output producing a clock at the frequency defined by DR1-DR4. Data is clocked into the device on the rising edge of the internally supplied clock.

When the CKC pin is held High, TxCL is configured as an input, and will accept an externally produced transmission clock with a tolerance of up to 500ppm with respect to the transmission rate determined by DR1-DR4.

The ACS101A performance is at its best when external changes on input pins are synchronised with internal clocks. Therefore, superior performance is likely when using the internally generated data transmission clock. If however, the externally generated transmission clock is used, then TxCL and TxD are generally asynchronous to the ACS101A internal clocks, performance in this case will be enhanced by limiting the edge speed of the TxCL and TxD signals so that they are greater than 150 ns. The modem has been designed to cope with very slow edges on inputs, without fear of metastability problems.

Receive Clock RxCL

In synchronous mode data is valid on the rising edge of RxCL clock (see Figure 3. Timing diagrams). To ensure that the average receive frequency is the same as the transmitted frequency RxCL is generated from a Digital Phase-Lock Loop (DPLL) system. The DPLL makes periodic corrections to the output RxCL clock to compensate for differences in the crystal values, and in the case of an externally supplied transmission clock, TxCL, compensation is also made for differences in frequency between this supplied data clock and the selected clock rate (DR1-DR4). The DPLL is adaptive and will minimise the frequency of correction and jitter when the crystal values and transmission clocks are tightly toleranced.

If the ACS101A receive FIFO empties (e.g. transmissions at far-end are halted) the RxCL clock stops, therefore rising edges of the RxCL clock always correspond to valid received data bits. This enables the system designer to use the ACS101A for the transmission of packets of data with blank periods between packets. The minimum quanta of data that can be sent over the link is three bits.

In asynchronous mode the RxCL clock is turned off.

Diagnostic/Operational Modes

The diagnostic/operational modes input pins DM1-DM3 may be changed asynchronously within a window of (crystal clock period) * 1536. The diagnostic mode signals are sampled 1536 * (crystal clock period) after a change is detected on any of the DM inputs. The sampled value is taken as the valid diagnostic mode.

Diagnostic Mode	Lock	DM3	DM2	DM1
Full-duplex	drift	0	0	0
Reset		0	0	1
Remote loopback	active	0	1	0
Full-duplex	random	0	1	1
Local loopback	drift	1	0	0
Full-duplex slave	active	1	0	1
Full-duplex master	drift	1	1	0
Full-duplex	active	1	1	1

Full-Duplex

In full-duplex configuration the RxCL clock of both devices tracks the average frequency of the TxCL clock of the opposing end of the link. The receiving Digital Phase-Lock Loop (DPLL) system makes periodic adjustments to the RxCL clock to ensure that the average frequency is exactly the same as the far-end TxCL clock. In this mode each TxCL is an independent master clock and each RxCL a slave clock.

Full-Duplex Slave

In slave mode the TxCL and the RxCL clock is derived from the TxCL clock of the opposing side of the link, such that the average frequency is exactly the same. It is therefore essential that only one modem is configured in slave mode at a time. The CKC pin is overridden such that TxCL is always configured as an output.

Full-Duplex Master

In master mode, the local RxCL clock is internally generated from the local TxCL clock. The local TxCL clock may be internally or externally generated. Master mode is only valid if the far-end device is configured in slave mode or if the far-end TxCL clock is derived from the far-end RxCL clock. Only one modem within a communicating pair may be configured as a master.

Local Loopback

In local loopback mode data is looped back inside the near-end modem and is output at its own RxD output. The data is also sent to the far-end modem; synchronisation between the modems is maintained. In local loopback mode data received from the far-end device is ignored, except to maintain lock. When local loopback is activated the DCDB signal assumes the logic High state. If concurrent requests occur for local and remote loopback, local loopback is selected.

When RSS = 0, RTS and DTR are looped back to CTS and DSR respectively.

Remote Loopback

In remote loopback mode the near-end modem sends a request to the far-end modem to loopback its received data, thus returning the data. The far-end modem also outputs the received data at its RxD. Both modems are exercised completely, as well as the LEDs and the fiber optic link. Once remote loopback is established, the DCDB of the near-end (initiating) modem is Low, and DCDB on the far-end modem is set High. Any data appearing on the TxD input of the far-end modem is ignored.

When RSS = 0, RTS and DTR are looped back to CTS and DSR respectively.

Drift Lock

Communicating modems attain a stable state where the 'transmit window' of one modem coincides with the 'receive window' of the other allowing for delay through the optical link. Adjustments to machine cycles are made automatically during operation to compensate for differences in crystal frequencies which cause loss of synchronisation.

Using drift lock, synchronisation described above depends on a difference in the crystal frequencies at each end of the link, the greater the difference the faster the locking. Therefore, if the difference between crystal frequencies is very small (a few ppm), automatic locking may take tens of seconds.

Active Lock Mode

Active lock mode may be used to accelerate synchronisation of a pair of communicating modems. This mode synchronises the modems with less than 250 ms delay, by adjusting the machine cycles of the modem. Active lock reduces the machine cycle of the device by 0.5 % ensuring rapid lock. After synchronisation the machine cycle reverts to normal.

Note that only one device can be configured in active lock at any one time, and thus the DM pins must not be permanently wired High on both devices in a production system. Active lock mode is usually invoked on power-up.

One common way of temporarily invoking active lock is to adopt the standard RC time-constant method. This is achieved on the ACS101A by connecting DM1, DM2 and DM3 together, and attaching that node to an RC arrangement, i.e. with the capacitor to 5V and the resistor to ground. This creates a 5V → 0V ramp on power-up. The RC time-constant should be Ca. 1 second.

Random Lock

This is a new mode of operation (over the ACS100), both ends of a link can be permanently configured in this mode (i.e. with hard-wired DM1-DM3 pins), which will achieve lock in typically 1 second, and worst case 5 seconds.

Like active lock, random lock will operate even when both ends of the link are driven by identical clock frequencies (0ppm difference). Random lock mode is compatible with drift lock available on the ACS100.

Mixing Lock modes

It is possible to mix all combinations of locking modes once the modems are locked, however, prior to synchronisation two modems configured in active lock will not operate. Normally, random lock will be the preferred mode. The effect of mixing locking modes on locking speed is tabulated below:

Device A Mode	Device B Mode	Locking Speed
Drift	Drift	Drift
Drift	Active	Active
Drift	Random	Random
Active	Active	Not allowed
Active	Random	Random
Random	Random	Random

LIN (Lock Indicator)

LIN goes High when synchronisation or “lock” is achieved. Lock is normally an invert of DCDB. But unlike DCDB is not affected by the status of RTS and DTR, or the selected diagnostic mode.

ERD (Error Detector)

This signal can be used to give an indication of the quality of the optical link. Even when a DC signal is applied to the TxD and TxCL inputs, the ACS101A transmits approximately 256 kbps over the link in each direction. This control data is used to maintain the timing and the relative positioning of transmit and receive windows. The transmit data and the control data is constantly monitored to make sure it is compatible with the 3B4B coding rules. If an infringement of the rules is detected then ERD will go High and will remain High until reset. ERD may be initialised by applying reset (DM1-DM3) or PORB, or by removing the fiber-optic cable from one side of the link thereby forcing the device temporarily out of lock. ERD is only an indication and should not be considered as a substitute for Bit Error Rate (BER) tests.

LED Considerations

Since LEDs from different suppliers may emit different wavelengths, it is recommended that the LEDs in a communicating pair of modems are obtained from the same supplier. The emission spectrum of an LED is a function of temperature, so a temperature difference between the ends of a link reduces the responsivity of the receiving diode. This results in a reduction in the link budget. Information is given in the LED suppliers’ data sheets. The following manufacturers have LEDs that have been successfully tested with the ACS101A, and Acapella will be glad to assist with contact names and addresses on request:

Suppliers

MITEL	(e.g. 1A-212-*connector*)
Acapella	(e.g. A-*connector*)
Optek Technology	(e.g. OPF372, OPF322)

Most suppliers support the standard range of fiber *connectors*, e.g. ST, SMA & FC.

Power Supply Decoupling

The ACS101A contains a highly sensitive amplifier, capable of responding to extremely low current levels. To exploit this sensitivity it is important to reduce external noise to a low level compared to the input signal from the LED. The modem should have an independent power trace to the point where power enters the board.

Figure 4. shows the recommended power supply decoupling. The LED should be sited very close to the LDN and LDP pins. A generous ground plane should be provided, especially around the sensitive LDN and LDP pins. The modem should be protected from EMI/RFI sources in the standard ways.

Link Budgets

The link budget is the difference between the power coupled to the fiber via the transmit LED and the power required to realise a current of 500 nA (minimum amplifier sensitivity) via the receive LED. The link budget is normally specified in dB or dBm, and represents the maximum attenuation allowed between communicating LEDs. The budget is utilised in terms of the cable length, cable connectors and splices. It usually includes an operating margin to allow for degradation in LED performance.

The power coupled to the cable is a function of the efficiency of the LED, the current applied to the LED and the diameter of the fiber optic cable. The larger the cable diameter the greater the power coupled. The conversion current produced by the receive diode is a function of the LED efficiency and the cable diameter. The conversion efficiency is measured in terms of its ability to convert the available power to current, known as the responsivity, given by (A/W). Some examples of link budgets are given in Note 7: Link Budget Examples. High quality LEDs can offer > 12dB link budget on 50µm fiber.

Maximum Link Length

The internal timing chain within the ACS101A supports a maximum link length of 5km, with 2 modes giving provision for the link length to 2.5km ('standard' mode) and 5km ('double' mode) with a crystal frequency of 9.216MHz. However, the maximum link length as determined by the ACS101A timing chain is inversely proportional to the crystal frequency. Hence with a 18.4MHz crystal the range is decreased to 1.25km. The maximum link length of 5km in 'double' mode is subject to the optical link budget that is available.

TxD Inputs

There is a choice of pins for TxD, pins 8 and 27. Only one input should be used. The other input will pull-up to VDD via an internal resistor. Pin 8 is the recommended choice since it is further away from the sensitive analogue pins. However, pin 27 is available for designers wishing to maintain compatibility with the ACS100.

Digital Mode

The ACS101A may be used as a controller and data buffer, with external analogue circuitry for data transmission and reception. This external circuitry could be used to create a higher-performance fiber link, or allow the ACS101A to be used in non-fiber applications such as wire or RF interfaces.

The digital interface mode is selected by connecting pins 5 (DP2) and pin 6 (DP3) to ground and pin 2 (DP1) to VD+. In this mode the data to be sent over the link is produced on pin 17 and the received data from the link is input on pin 18, instead of using the LDN and LDP pins. A simple digital connection is also possible with pin 17 of the first I.C. driving into pin 18 of the second I.C. and pin 17 of the second I.C. driving into pin 18 of the first I.C.

In addition, in digital mode, to aid data reception with external amplifiers or AGCs, pin 26 produces a signal which indicates the data reception time of the data burst over the link. After the data burst is sent, the data output on pin 17 goes high.

Figure 5 shows the inter IC wiring connections for a simple digital communications link using the digital interface mode. This example shows a single wire connection between the two ICs (two including ground) for data to and from each IC. This only demonstrates how a simple single medium interface can be used, because each IC transmits it's data at different times, automatically interleaving it's transmitted data with the data from the other IC. Any other medium for connecting the ICs could be used, such as RF, twisted pair or mains power carrier for example.

Pin Descriptions

Pin	Sym	IO	Name	Description
1	DR1	I	Data Rate Select	The DR1-DR4 inputs select the Data Rates.
2	DP1	-	Digital Preset	Leave unconnected, for normal fibre applications. Set high to select special digital interface mode (see p5).
3	DM1	I	Diagnostic Modes	DM1-DM3 inpust select the Diagnostic Modes such as local loopback and remote loopback.
4	RxD	O	Received Data	Received data.
5 6	DP2 DP3	-	Digital Preset	Leave unconnected, for normal fibre applications. Set low to select special digital interface mode (see p5).
7	RTS	I	Request To Send / Data Channel 2 input	Modem control signal or additional low frequency data channel input
8	TxD	I	Transmit Data	Transmitted data
9 10	XLI XLO	I O	Oscillator Crystal	Connection to fundamental parallel resonance crystal with padding capacitors to GND
11	CKC	I	Clock Control	Configures the TxCL pin for either internally or externally generated clocks
12	TxCL	IO	Transmit Data Clock	Transmit Data Clock, frequency set by DR1-DR4, input or output depending on CKC.
13	RxCL	O	Receive Data Clock	Receive Data Clock, turned off in asynchronous mode
14 15	DM2 DM3	I	Diagnostic Modes	Diagnostic modes select see DM1 pin and main text
16	DTR	I	Data Terminal Ready / Data channel 3 i/p	Modem contrrol signal or additional low frequency data channel input
17	ERD / DO	O	Error Detector / Digital mode data output	In normal fibre applications indicates quality of link. If a coding infringement is detected, ERD goes High. Data output in special digital interface mode.
18	DI	I	Digital mode data input	Data input in special digittal interface mode. Not used in normal fibre applications, can be left disconnected.
19	PORB	I	Power-on-Reset	Will initiate the device when PORB=0. PORB is normally connected to a capacitor to gnd so that a POR is automatically invoked on power-up.
20	CTS	O	Clear To Send / Data Channel 2 output	Modem control signal or additional low frequency data channel output
21	DSR	O	Data Set Ready / Data Channel 3 output	Modem control signal or additional low frequency data channel output
22	DCDB	O	Data Carrier Detect	Goes low when modems locked and ready for data transmission

Pin	Sym	IO	Name	Description
23	GND	-	Ground	Ground Supply
24	VD+	-	+ve power supply	Power Supply, 4.75-5.25 Volts
25	RSS	I	RS232 handshake or data channels select	Modem control signal, Low = data transmission mode, High = modem handshake mode
26	LIN / RW	O	Lock Indicator / Receive Window	In normal fibre mode indicates modem lock, high when both modems locked together. In digital interface mode indicates the receiving window, high when the data burst being received.
27	TxD	I	Transmit Data	Normally unconnected as main data is input on Pin8, but is used to maintain compatibilty with ACS100
28	IC	-	Internally connected	Should not be connected to, only used for test access.
29	NC	-	Not connected	Can be connected to or not.
30	GND	-	Ground	Ground Supply
31	CNT	IO	Capacitor Integration	Integrating capacitor is placed between CNT and GND of value 10nF-33nF with an XTAL of 19MHz to 5MHz
32	GND	-	Ground	Ground Supply
33	LDN	IO	LED Cathode	Connection to LED used for transmission and receiption
34	NC	-	Not connected	Can be connected to or not.
35	LDP	IO	LED Anode	Connection to LED used for transmission and receiption
36	GND	-	Ground	Ground Supply
37	VA+	-	+ve power supply	Power supply, 4.75-5.25 Volts
38	VG	-	Guard ring & mode select	Can be left unconnected or connected to VA+. Pulled high internally.
39	NC	-	Not connected	Can be connected to or not.
40	DR4	I	Data Rate Select	Data rate select, see DR1
41	TRC	I	Transmit Current	Defines transmit current to the LED. Set by connecting TRC to GND via a resistor, value R defined by equation on page 2
42	DR2	I	Data Rate Select	Data rate select, see DR1
43	GND	-	Ground	Ground Supply
44	DR3	I	Data Rate Select	Data rate select, see DR1

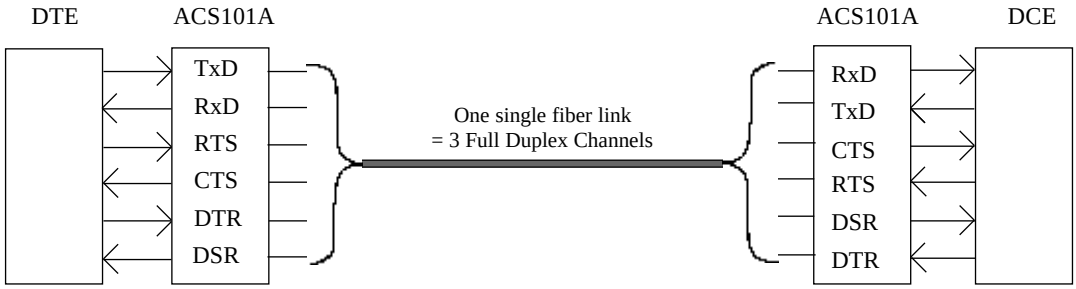


Figure 1. Data Flow Representation showing data and handshake signals transmitted over a single fiber

Figure 2. Top view of 44 PLCC package

NC = Not Connected IC = Internally Connected

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power supply VD+ and VA+ (VDD = VD+ or VA+)	VDD	-0.3	6.0	V
Input voltage (non-supply pins)	Vin	GND - 0.3	VDD + 0.3	V
Input current (except LDN,LDP,CNT,VG)	Iin	-	10.0	mA
Input current (LDN,LDP,CNT)	Iin	-	1.0	mA
Storage temperature	Tstor	-50	160	ºC

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power supply (VA+ and VD+)	V+	4.75	5.0	5.25	V
Ambient temperature range	TA	-40	-	85	ºC

Static Digital Input Characteristics (for specified operating conditions)

Input pins: DR1/2/3/4, DP1/2/3, DM1/2/3, CKC, RSS, TxD, RTS, DTR, XTI, DI, PORB, TxCL(input).

Parameter	Symbol	Min	Typ	Max	Units
Vin High	Vih	2.0	-	-	V
Vin Low	Vil	-	-	0.8	V
Vin High (PORB, XTI)	Vih	0.8 * VD+	-	-	V
Vin Low (PORB, XTI)	Vil	-	-	0.2 * VD+	V
Pull-up resistor (except XTI and TxCL)	PU	50k	125k	340k	Ω
Input current (Note 1)	Iin	-	-	100	µA

Note 1: Input current is mainly attributed to pull-up resistor, so it applies when input is low. The high input current is < +/-10 µA.

Static Digital Output Characteristics (for specified operating conditions)

Output pins: RxD, CTS, DSR, DCDB, LIN, ERD, XLO, RxCL, TxCL(output).

Parameter	Symbol	Min	Typ	Max	Units
Vout Low (Iout = 4mA)	Vol	0	-	0.5	V
Vout High (Iout = 4mA)	Voh	VDD-0.5	-	-	V
Max load capcitance	Cl	-	-	50	pF
XLO (Note 2)	-	-	-	-	pF

Note 2: XLO does not have a drive capability other than that of the load presented by a parallel resonant crystal and appropriate padding capacitor.

Dynamic Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Crystal frequency (XTI, XTO)	frc	5	9.216	19	MHz
External clock (XTI) High or Low time	fcl	40	-	60	%
RxD and TxD data rate Synchronous Short range: Standard: Double: Asynchronous Short range: Standard: Double:	fckc	 4.8 2.4 9.6 DC DC DC	-	 512 256 64 76.8 38.4 19.2	kbps
RxCL and TxCL duty cycle (with TxCL = output)	twh twl	-	50	-	%
Frequency deviation at TxCL from selected value (with TxCL = input)	Fd	-	-	500	ppm
TxD to TxCL set-up time	tsut	300	-	-	ns
TxD to TxCL hold time	tht	25	-	-	s
RxD to RxCL set-up time	tsur	-	0.5 *1/RxCL	-	ns
RxD to RxCL hold time	thr	-	0.5 *1/RxCL	-	ns
Digital output - fall time	tf	-	-	100	ns
Digital output - rise time	tr	-	-	100	ns
Power consumption: TRC floating (or 100kOhm) TRC tied to GND (Note 3)	Pc	-	 155 85	 230 120	mW

Note 3: Power consumption assumes that digital outputs drive CMOS loads. includes LED.

Matching Characteristics (for specified operating conditions)

Parameter	Symbol	Min	Typ	Max	Units
Crystal tolerance use parallel resonant crystal and recommended padding capacitors	Ct	-100	0	100	ppm
Amplifier sensitivity input current	Irec	500	-	-	nA
Maximum amplifier input current	Imax	1	2	-	mA
Rtrc placed between TRC and GND	Rtrc	0	-	-	Ω
LED current with TRC floating peak current: average curent: (Note 4)	Icur	 70 14	 - -	 130 26	mA
LED capacitance with Vr = 0 Volts (Note 5)	Cled	-	-	100	pF
LED leakage current Vr = 1.8 Volts	Cl	-	1	100	nA
LED reverse bias (Note 6)	Vr	-	0	-	V

Note 4: The LED is switched on for approximately 1/5th of the time, with a cycle of 160 µs at 9.216MHz.

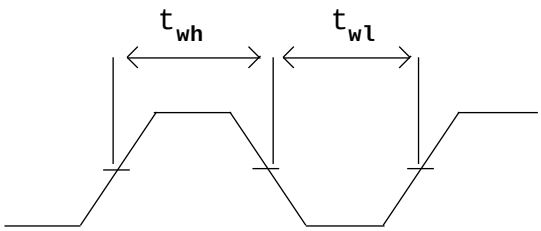
Note 5: The ACS101A is at its best with low capacitance LEDs - Acapella is able to supply LEDs with lower than 20pF capacitance.

Note 6: The ACS101A incorporates a differential receiver front end. Single ended reception, compatible with the ACS101 is still selectable by connecting VG, pin 38, low, in which case the LED reverse bias will be as specified for the ACS101, 1.3 to 1.8v.

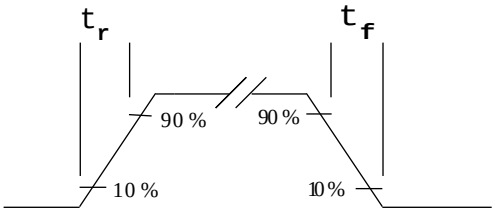
Link Budget Examples

Cable	200 micron	100 micron	62.5 micron	50 micron
Typical transmit couple power to fiber (µW)	1200	260	100	40
Minimum LED responsivity (A/W)	0.05	0.06	0.1	0.12
Available current (µA)	60	15.6	10	4.8
Minimum ACS101A sensitivity (nA)	500	500	500	500
Link budget (dB)	20	15	13	10

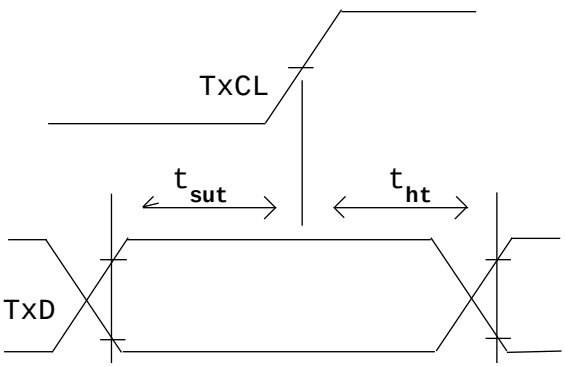
Note 7: Link Budget Calculations for a typical 1A-212 LED from MITEL Semiconductor.



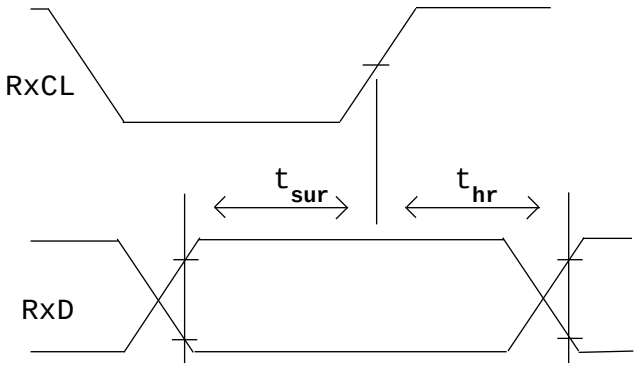
TxCL and RxCL clock pulse widths



Digital Outputs rise and fall times



Transmit set-up and hold times



Receive set-up and hold times

Figure 3. Timing diagrams

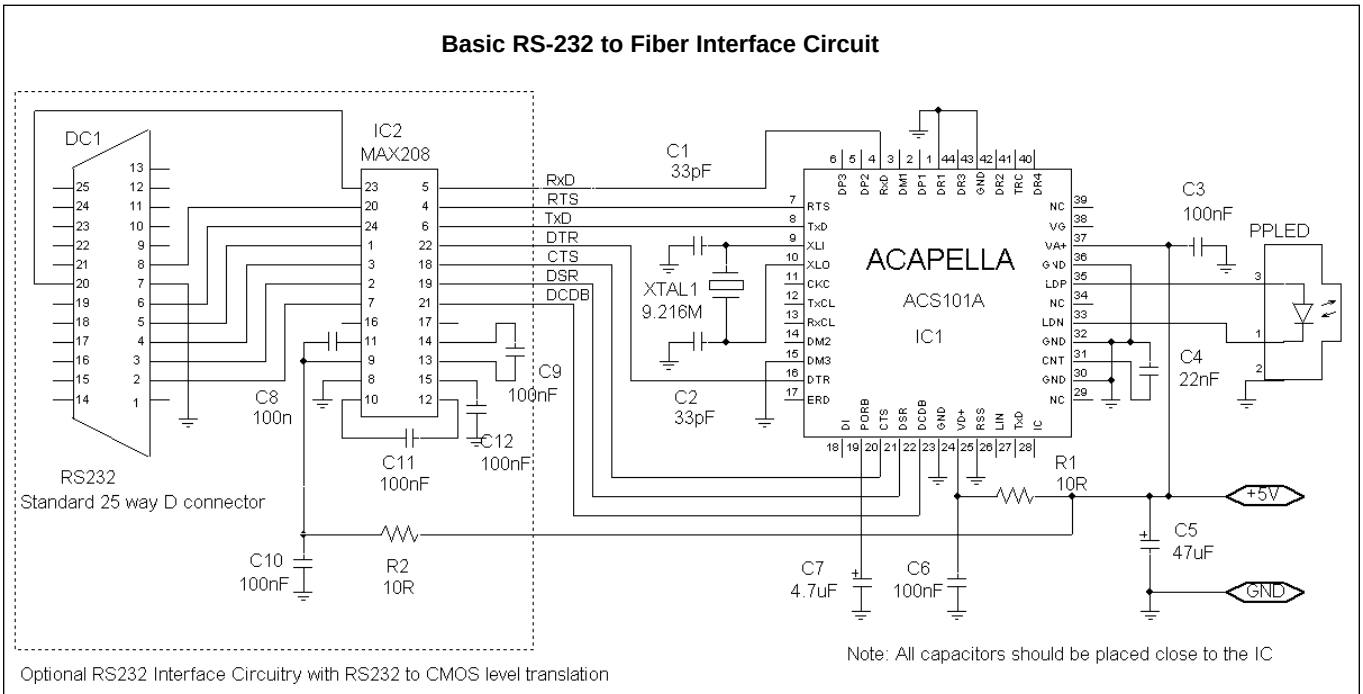


Figure 4. Typical application circuit for linking two PCs via a Single Fiber Optic Cable

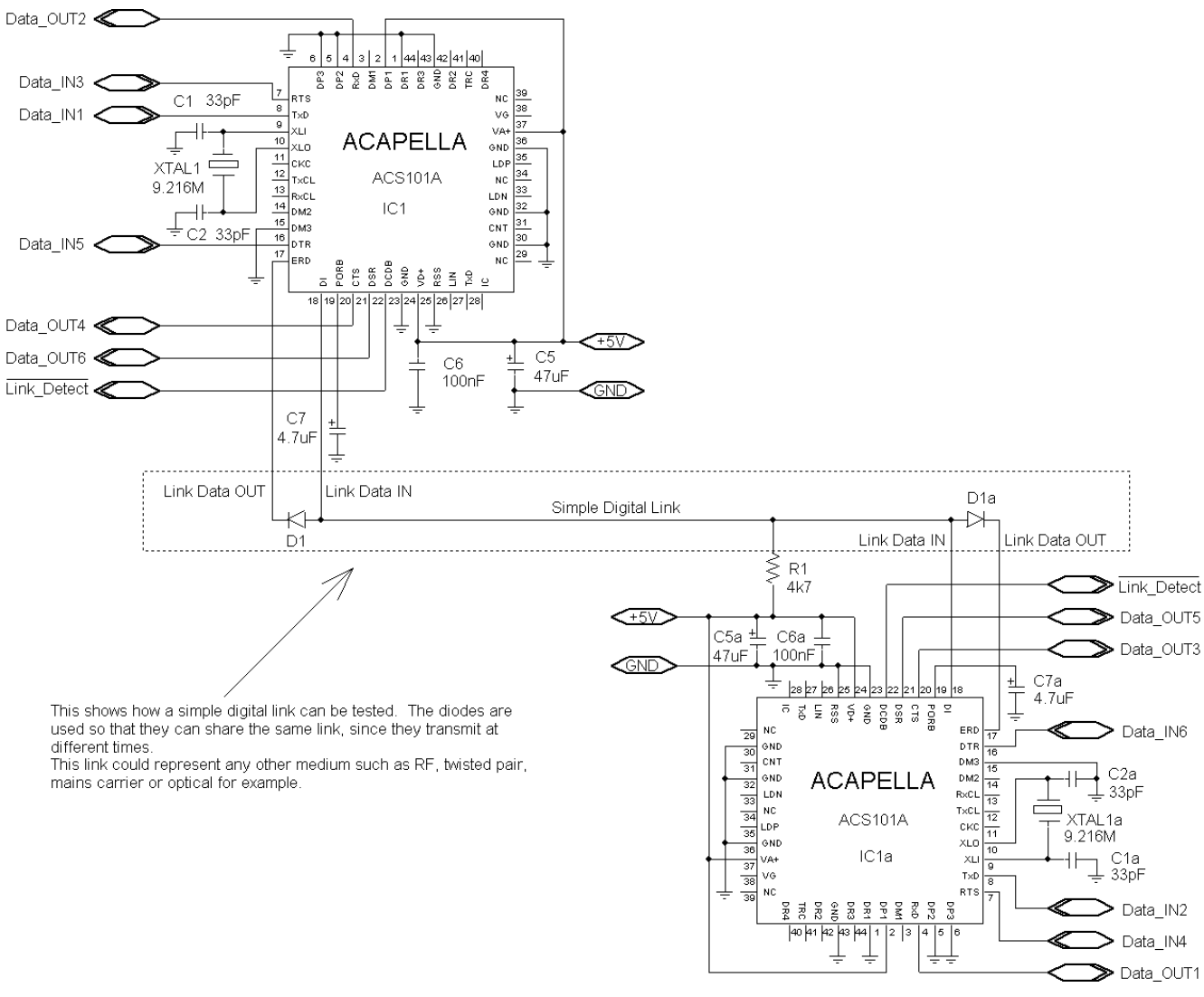
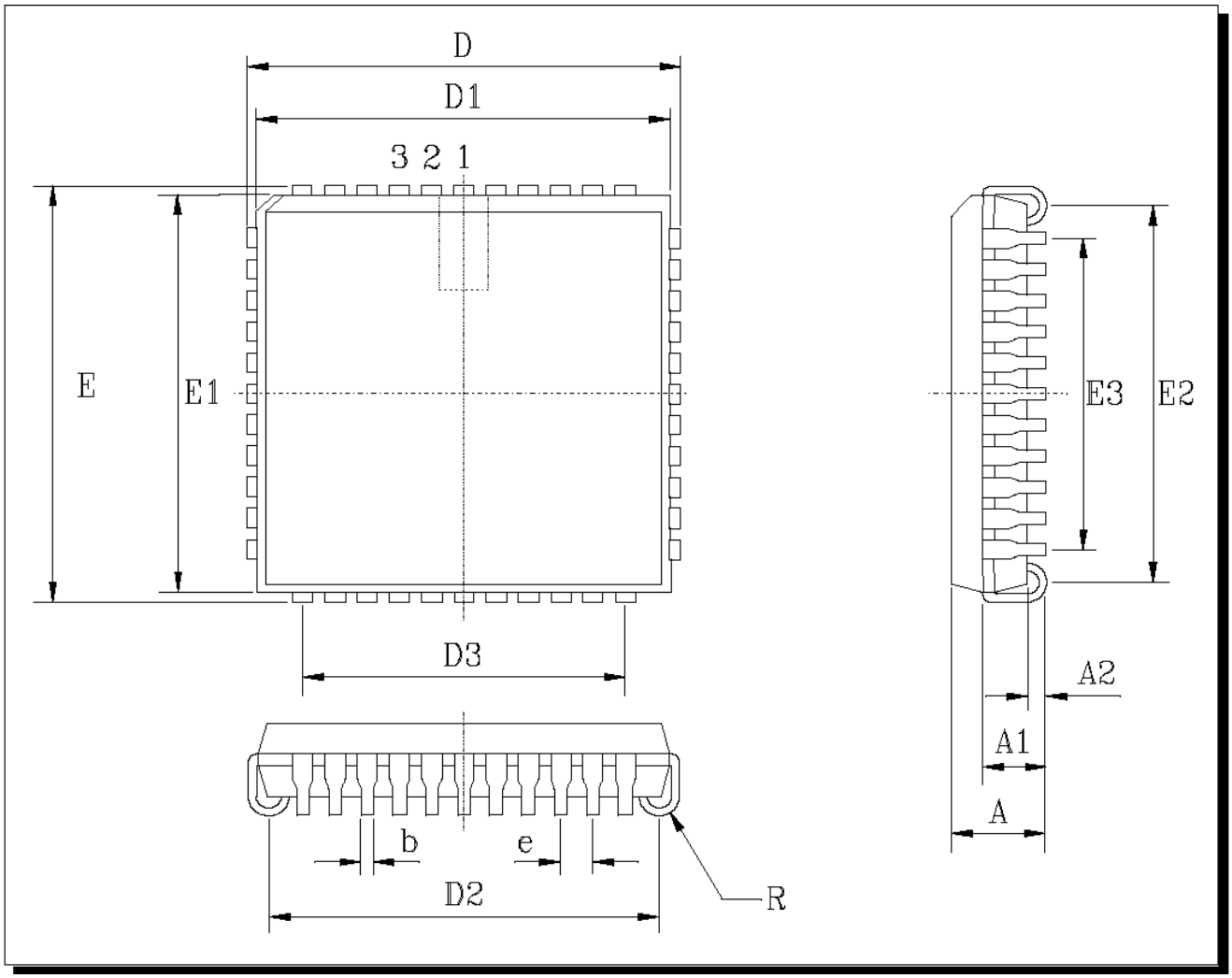


Figure 5. Test Circuit to demonstrate a simple Single medium link in digital interface mode



PLCC44	D/E	D1/E1	D2/E2	D3/E3	A	A1	A2	e	b	R	Copl.
min	17.40	16.51	14.99		4.20	2.29	0.51		0.33	0.64	
Dimensions in mm				12.70				1.27			
max	17.65	16.66	16.00		4.57	3.04			0.53	1.14	0.10

Figure 6. Package Dimensions, PLCC44

Acapella Ltd.
Delta House
Chilworth Research Centre
Southampton S016 7NS
United Kingdom

UK Tel. 023 80 769 008
UK Fax. 023 80 768 612

Intn'l. Tel. +44 23 80 769 008
Intn'l. Fax. +44 23 80 768 612

Email: sales@acapella.co.uk
Web: www.acapella.co.uk

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