NEC

MOS INTEGRATED CIRCUIT
μ**PD72042**

LSI DEVICES FOR Inter Equipment Bus™ (IEBus™) PROTOCOL CONTROL

The μPD72042 is a microcomputer peripheral LSI device for IEBus protocol control.

The μPD72042 performs all the processing required for layers 1 and 2 of the IEBus. The devices incorporate large transmission and reception buffers, allowing the microcomputer to perform IEBus operations without interruption. They also contain an IEBus driver and receiver, allowing them to directly connected to the bus directly.

FEATURES

○ Control of layers 1 and 2 of the IEBus protocol
- Support of a multi-master scheme
- Broadcast function
- Two communication modes having different transmission speeds can be selected.

	Transmission speed
Mode 0	Approx. 3.9 Kbps
Mode 1	Approx. 17 Kbps

○ Built-in IEBus driver and receiver
○ Transmission and reception buffers
  Transmission buffer : 33 bytes, FIFO
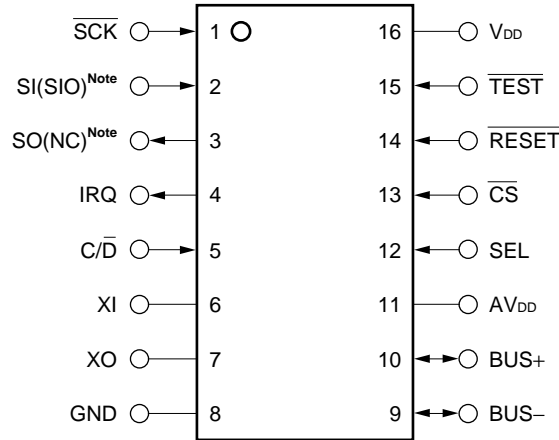 Reception buffer   : 40 bytes, FIFO (capable of holding more than one frame of reception data.)

○ Microcomputer interface
  Three-/two-wire serial I/O,
  Transfer starting with MSB
○ Program crashes can be detected by means of a watchdog timer.
○ Low power consumption (standby mode):
  50 μA (max)
○ Oscillator frequency (f_X): 6 MHz
  - frequency accuracy: ±1.5%
○ Operating voltage: 5 V ±10%

ORDERING INFORMATION

Part number	Package
μPD72042GT	16-pin plastic SOP (9.53 mm (375))

PIN CONFIGURATION (TOP VIEW)

- **16-pin plastic SOP (9.53 mm (375))**
  μPD72042GT

```
       SCK  O──►│ 1 O        16 │──── O VDD
  SI(SIO)Note O──►│ 2          15 │◄── O TEST
  SO(NC)Note  O◄──│ 3          14 │◄── O RESET
        IRQ  O◄──│ 4          13 │◄── O CS
        C/D  O──►│ 5          12 │◄── O SEL
         XI  O───│ 6          11 │──── O AVDD
         XO  O───│ 7          10 │◄──►O BUS+
        GND  O───│ 8           9 │◄──►O BUS─
```

Note Parentheses indicate the state corresponding to two-wire serial I/O mode.

AVDD	: Main power supply for IEBus (connected to the VDD pin)
BUS─, BUS+	: IEBus I/O
C/$\overline{D}$	: Command/data switch input
$\overline{CS}$	: Chip select input
GND	: Ground
IRQ	: Interrupt request output
NC	: No connection
$\overline{RESET}$	: Reset input
$\overline{SCK}$	: Serial clock input
SEL	: Serial mode selection
SI	: Serial data input
SIO	: Serial data I/O
SO	: Serial data output
$\overline{TEST}$	: Test input (connected to the VDD pin)
VDD	: Main power supply
XI, XO	: System clock

BLOCK DIAGRAM
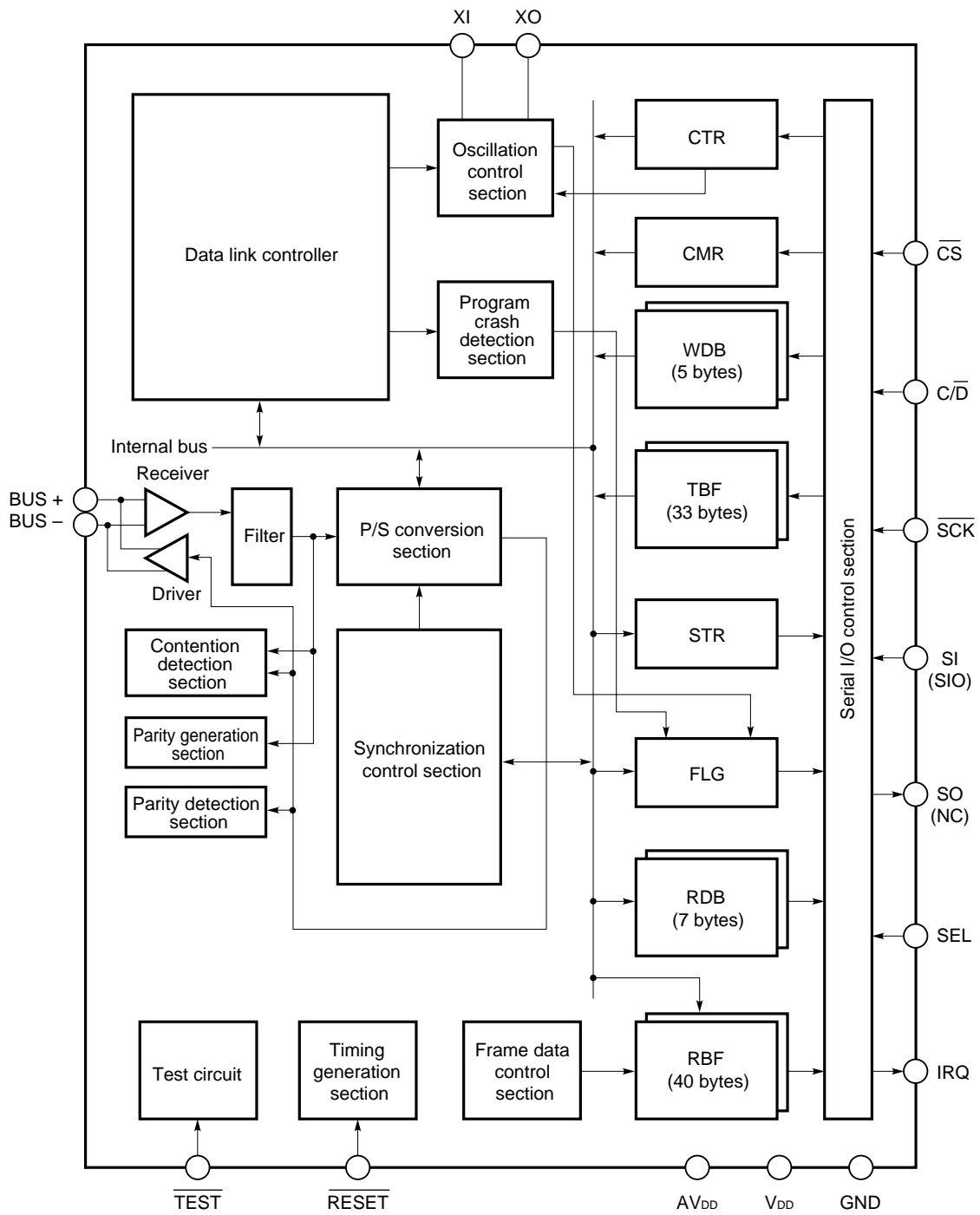
Remark The pin names in parentheses are used when two-wire serial I/O is selected.

CONTENTS

1. PIN FUNCTIONS

1.1 PIN FUNCTIONS

Pin No.	Pin**Note**	I/O**Note**	Function	I/O format**Note**	When reset [for both hardware and software]
1	$\overline{\text{SCK}}$	Input	Serial clock input pin for CPU interface	CMOS input	Input
2	SI (SIO)	Input (I/O)	Serial data pin for CPU interface. (This pin functions as an input pin when 3-wire serial I/O mode is selected, or as an I/O pin when 2-wire serial I/O mode is selected.)	CMOS input (CMOS I/O)	Input
3	SO (NC)	Output (none)	Serial data output pin for CPU interface. (The pin functions as an output when 3-wire serial I/O mode is selected. When 2-wire serial I/O mode is selected, the pin is left open.)	CMOS output (none)	High-impedance
4	IRQ	Output	Output pin for making an interrupt request to the CPU. When a return code or a program crash is detected, a high-level signal is output on this pin for at least 8 μs.	CMOS output	Low level
5	C/$\overline{\text{D}}$	Input	Input pin used to select control mode or data read/write mode. When this pin is driven high, internal register address setting and data read/write are enabled. When the mode changes, the serial clock counter is reset.	CMOS input	Input
6 7	XI XO	–	Pins for connecting a system clock resonator. A 6-MHz crystal or ceramic resonator must be used. The accuracy of the frequency is as follows; Mode 0, 1: $\pm$1.5%	–	When reset by hardware (Oscillation stopped) XI = GND XO = High level When reset by software (Oscillation continued)
8	GND	–	Ground pin	–	–
9 10	BUS– BUS+	I/O	I/O pins connected to the IEBus bus	–	High-impedance
11	AV$_{DD}$	–	Main power supply pin for the IEBus bus driver/receiver. When used, this pin must be tied to V$_{DD}$.	–	–
12	SEL	Input	Input pin used to select either 3- or 2-wire serial I/O mode. A high-level signal on this pin selects 3-wire serial I/O mode. A low-level signal on this pin selects 2-wire serial I/O mode.	CMOS input	Input
13	$\overline{\text{CS}}$	Input	Chip select pin. When this pin is driven low, the serial interface is enabled. When this pin is driven high, the SO pin becomes high-impedance, and the serial clock counter is reset.	CMOS input	Input

Note Parentheses indicate the state corresponding to two-wire serial I/O mode.

Pin No.	Pin	I/O	Function	I/O format	When reset [for both hardware and software]
14	$\overline{\text{RESET}}$	Input	Serial reset signal input pin. A low input causes a reset. Whenever the power is turned on, a low-level signal must be applied to this pin. During normal operation, a high level is applied.	CMOS input	Input
15	$\overline{\text{TEST}}$	Input	IC test pin. When used, this pin must be tied to the V_{DD} pin directly.	CMOS input	–
16	V_{DD}	–	Main power supply input pin	–	–

2. IEBus OPERATION

2.1 OVERVIEW

The μPD72042 is a CMOS LSI device for the IEBus interface.

The IEBus is designed to enable the data transmission between devices in a small-scale digital data transmission system.

The μPD72042 is connected to a microcomputer built into a device. A serial interface ($\overline{\text{SCK}}$, SO, and SI pins) is used for connection. The host controller (microcomputer) sets the commands and data needed for data transmission via this serial interface.

When data is transmitted, the host controller sets the data in the μPD72042 via the serial interface. Then, signals are output on the BUS pins (BUS+, BUS–). When data is received from the BUS pins, the host controller can read it via the serial interface.

2.2 IEBus COMMUNICATION PROTOCOL

The IEBus is outlined below.

- Communication method: Half duplex asynchronous communication

- Multi-master method
  All units connected to the IEBus can transmit data to every other connected unit.

- Broadcast function (one-unit-to-multiple-units communication)
  Group broadcast   : Broadcast to a specific group of units
  General broadcast   : Broadcast to all units

- Two modes, each offering different transmission speeds, can be selected.

	Transmission speed	Maximum number of bytes transmitted (bytes/frame)
Mode 0	Approx. 3.9 Kbps	16
Mode 1	Approx. 17 Kbps	32

- Access control: Carrier Sense Multiple Access with Collision Detection (CSMA/CD)
  Bus mastership priority is as follows:

  ① Broadcast takes priority over ordinary communication (one-unit-to-one-unit communication).
  ② Units having lower master addresses have a higher priority.

- Communication scale
  Number of units   : 50 max
  Cable length   : 150 m max (when twisted-pair cable is used <resistance 0.1 Ω/m or less>)
  Load capacity   : 7000 pF max <between BUS+ and BUS–>
  Terminating resistance   : 120 Ω

2.2.1 Bus Mastership Determination (Arbitration)

Before devices connected to the IEBus can control other devices, they must first acquire the bus. This operation is called arbitration.

When more than one unit starts transmission at the same time, arbitration determines which of those units is allowed to use the bus.

When arbitration results in only one device being granted bus mastership, the following bus mastership priority conditions are used:

Remark Those devices that are defeated in arbitration can automatically enter retransmission mode. (For the μPD72042, the number of retransmissions can be set by specifying a value between 0 and 7 in the MCR register.)

(1) Priority by communication type

Broadcast (one-unit-to-multiple-units communication) takes priority over ordinary communication (one-unit-to-one-unit communication).

(2) Priority by master address

If the communication type is the same, the smallest master address value has the highest priority.

Example Each master address consists of 12 bits. A unit having master address 000H has the highest priority, while a unit having master address FFFH has the lowest priority.

2.2.2 Communication Mode

The IEBus supports two communication modes, each having a different transmission speed. Table 2-1 lists the transmission speed for each communication mode and the maximum number of bytes transmitted within one communication frame.

Table 2-1 Transmission Speed and Maximum Number of Transmission Bytes in Each Communication Mode

Communication mode	Maximum number of transmission bytes (bytes/frame)	Effective transmission speed[Note] (Kbps)
0	16	Approx. 3.9
1	32	Approx. 17

Note Effective transmission speed at which the maximum transfer rate is achieved

Caution Before devices connected to the IEBus can perform communication, an appropriate communication mode must be set. Note that if a master unit and an associated unit (slave unit) have different communication modes, they will not be able to communicate properly.

2.2.3 Communication Address

With the IEBus, each device is assigned a unique 12-bit communication address. The communication address consists of the following parts:

High-order 4 bits   : Group number (number identifying the group to which a device belongs)
Low-order 8 bits   : Unit number (number identifying a device in a group)

2.2.4 Broadcast

In ordinary communication, transmission and reception are performed between one master unit and one associated slave unit. Broadcast can also be done between one master unit and more than one slave unit. In this case master unit transmits data to an arbitrary number of slave units. In this case, the slave units do not return on acknowledge signal to the master unit.

Whether the communication to be performed is broadcast or ordinary communication is determined by the setting of the broadcast bit. (For details of the broadcast bit, see **(1)** ② in **Section 2.3**.)

There are two types of broadcast.

(1) Group broadcast

Broadcast is performed to the devices in a particular group. These devices all have the same group number, as indicated by the high-order 4 bits of each communication address.

(2) General broadcast

Broadcast is performed to all devices, regardless of their group numbers.
These two types of broadcast are distinguished by the slave address. (For details of the slave address, see **(3)** in **Section 2.3**.)

2.3   TRANSMISSION PROTOCOL

Fig. 2-1 shows the IEBus transmission signal format.

Communication data is transmitted as a sequence of signals called a communication frame. The transmission speed and the maximum amount of data that can be transmitted in one communication frame depend on the communication mode.

Fig. 2-1   Transmission Signal Format

Field name	Header		Master address field		Slave address field			Control field			Data-length field			Data field						
Number of bits	1	1	12	1	12	1	1	4	1	1	8	1	1	8	1	1	8	1	1
	Start bit	Broad-cast bit	Master address	P	Slave address	P	A	Control bits	P	A	Data-length bits	P	A	Data bits	P	A	Data bits	P	A

Transmission time		
Mode 0	Approx. 7330 μs	Approx. 1590 $\times$ N μs
Mode 1	Approx. 2090 μs	Approx. 410 $\times$ N μs

P : Parity bit (1 bit)

A : Acknowledge bit (1 bit)

When A = 0: ACK

When A = 1: NAK

N : Number of data bytes

Remark   For broadcast, the value of the acknowledge bit is ignored.

(1) Header

The header consists of a start bit and a broadcast bit. These are explained below.

① **Start bit**

The start bit is a signal used to notify the other units of the beginning of data transmission.

Before a unit starts data transmission, it outputs a low-level signal (start bit) for a specified duration, then outputs the broadcast bit.

When the unit attempts to output the start bit, another unit may have already output the start bit. In such a case, the unit does not output the start bit, and instead waits for the other unit to stop outputting the start bit. Then, synchronized with the completion of start bit output by the other unit, the unit starts output of the broadcast bit.

All units, except that unit which started the transmission, detect the start bit and become ready for reception.

② **Broadcast bit**

The broadcast bit is used to distinguish between broadcast and ordinary communication.

If the broadcast bit is 0, broadcast is indicated. If the broadcast bit is 1, ordinary communication is indicated. There are two types of broadcast: group broadcast and general broadcast. These types are distinguished by the slave address. (For details of the slave address, see **(3)**.)

For broadcast, more than one slave unit can exist as an associated communication station. Therefore, the acknowledge bits for the master address field and subsequent fields are not returned.

When more than one unit starts sending a communication frame at the same time, broadcast takes precedence over ordinary communication and wins arbitration.

(2) Master address field

The master address field is used to transmit the local unit address (master address) to other units.

The master address field consists of master address bits and a parity bit.

A master address consists of 12 bits. It is output starting with the MSB.

When more than one unit starts transmitting the same broadcast bit value at the same time, arbitration determination is performed by the master address field.

Each time a unit transmits one bit of the master address field, the unit compares its output data with the data on the bus. If the comparison indicates that the master address output by the unit differs from the data on the bus, the unit determines that it has lost an arbitration. The unit stops transmission, and readies itself for reception. The IEBus is organized by wired AND. When arbitration is performed between units (arbitration masters), the unit having the smallest master address value wins the arbitration.

After the 12-bit master address has been output, only one unit is finally determined as being the master unit, such that that unit remains in the transmission state.

Next, the master unit outputs a parity bit[Note] to post the master address to other units. Then, the master unit proceeds to the slave address field.

Note Even parity is used. When the number of 1's in the master address bits is odd, the parity bit is set to 1.

(3) Slave address field

The slave address field is used to transmit the address (slave address) of a unit (slave unit) with which the master unit wants to communicate.

The slave address field consists of slave address bits, a parity bit, and an acknowledge bit.

A slave address consists of 12 bits. It is output starting with the MSB. After a 12-bit slave address has been transmitted, a parity bit is output to prevent the slave address from being received incorrectly. Then, the master unit attempts to detect the acknowledge signal from a slave unit to confirm that the slave unit exists on the bus. When the acknowledge signal is detected, the master unit outputs a control field. Note, however, that when performing broadcast, the master unit outputs the control field without attempting to detect the acknowledge bit. The slave unit outputs an acknowledge signal when the slave unit recognizes a match between the slave unit's address and the slave address transmitted by the master unit match, and that both the master address and slave address have even parity. If the slave unit detects odd parity, it does not recognize the addresses as matching, so does not output an acknowledge signal. In this case, the master unit is placed in the standby (monitor) state, and communication terminates.

For broadcast, the slave address is used to distinguish between group broadcast or general broadcast, as follows:

When the slave address is FFFH : General broadcast
When the slave address is other than FFFH : Group broadcast

Remark For group broadcast, the number of a target group is indicated by the high-order 4 bits of the slave address.

(4) Control field

The control field indicates the type and direction of the next data field.

The control field consists of control bits, a parity bit, and an acknowledge bit.

The four control bits are output starting with the MSB.

Following the control bits, a parity bit is output. If even parity is detected, and the function requested by the master unit can be performed by the slave unit, the slave unit outputs an acknowledge signal. Then, the slave unit proceeds to the data-length field. If the slave unit cannot perform the processing requested by the master unit, even when even parity is detected, or if odd parity is detected, the slave unit does not output an acknowledge signal, and it enters the standby (monitor) state again.

After detecting the acknowledge signal, the master unit proceeds to the data-length field.

If an acknowledge signal is not detected, the master unit enters the standby state, terminating communication. For broadcast, however, the master unit proceeds to the next data-length field without attempting to detect the acknowledge signal.

Table 2-3 lists the meanings of the control bits.

(5) Data-length field

The data-length field specifies the communication data length, in bytes.

The data-length field consists of the data-length bits, a parity bit, and an acknowledge bit.

The eight data-length bits are output starting with the MSB. The data-length bits indicate the communication data length, in bytes, as shown in Table 2-2.

Table 2-2   Values of the Data-Length Bits and Their Meanings

Data-length bit (hexadecimal)	Transmission data length, in bytes
01H	1
02H	2
:	:
:	:
FFH	255
00H	256

Remark If the data length set in the data-length bits exceeds the maximum number of transmission bytes, the latter varying with the communication mode, more than one frame is transmitted. In the second and subsequent frames, the data-length bits indicate the remaining communication data length, in bytes.

The operation performed for this field differs depending on whether master transmission (when bit 3 of the control bits is 1) or master reception (when bit 3 of the control bits is 0) is performed.

① **Master transmission**

The data-length bits and parity bit are output by the master unit. When the slave unit detects even parity, the slave unit outputs an acknowledge signal, then proceeds to the data field. For broadcast, however, the slave unit does not output an acknowledge signal.

If the slave unit detects odd parity, the slave unit does not output an acknowledge signal, regarding the received data-length bits as being incorrect. Then, the slave unit enters the standby (monitor) state again. At this time, the master unit also enters the standby state again, and communication terminates.

  ② **Master reception**

The data-length bits and parity bit are output by the slave unit. When the master unit detects even parity, the master unit outputs the acknowledge signal.

If the master unit detects odd parity, the master unit does not output an acknowledge signal, regarding the received data-length bits as being incorrect. Then, the master unit enters the standby state again. At this time, the slave unit also enters the standby state again, and communication terminates.

(6) Data field

The data field is used for data transmission and reception to and from a slave unit.

The master unit uses the data field to transmit data to the slave unit, or to receive data from the slave unit.

The data field consists of data bits, a parity bit, and an acknowledge bit.

The eight data bits are output, starting with the MSB.

After the data bits have been output, the parity bit and acknowledge bit are output from the master unit and slave unit, respectively.

Broadcast is performed only when the master unit transmits data. At this time, any acknowledge signal is ignored.

The operations related to master transmission and master reception are explained below.

  ① **Master transmission**

When the master unit performs a write to a slave unit, the master unit transmits the data bits and a parity bit to the slave unit. The slave unit receives the data bits and parity bit, then outputs an acknowledge signal if even parity is detected and the reception buffer is empty. If odd parity is detected, or if the reception buffer is not empty, the slave unit rejects the corresponding data, and does not output an acknowledge signal. If no acknowledge signal is received from the slave unit, the master unit transmits the same data again. The master unit repeats this operation until it receives an acknowledge signal from the slave unit, or until the data exceeds the maximum number of transmission bytes.

When even parity is detected, and an acknowledge signal is received from the slave unit, the master unit transmits the subsequent data, if any, and provided the maximum number of transmission bytes is not reached.

For broadcast, an acknowledge signal is not output by any slave unit. The master unit transfers data one byte at a time.

  ② **Master reception**

When the master unit reads data from a slave unit, the master unit outputs a synchronization signal for each bit as it is read.

The slave unit outputs data and a parity bit to the bus according to the synchronization signal output by the master unit.

The master unit reads the data and parity bit output by the slave unit, and checks the parity.

If the master unit detects odd parity, or if the reception buffer is not empty, the master unit rejects the data, and does not output an acknowledge signal. The master unit repeats the read operation for the same data provided the maximum allowable number of transmission bytes per communication frame has not been reached.

If the master unit confirms even parity, and the reception buffer is empty, the master unit accepts the data, and returns an acknowledge signal to the slave unit. Then, the master unit reads the next data, provided the maximum allowable number of transmission bytes per frame has not been reached.

(7) Parity bit

A parity bit is used to check for errors in the transmission data.

A parity bit is added to the master address bits, slave address bits, control bits, data-length bits, and data bits. Even parity is used. If the number of 1's in the data is odd, the parity bit is set to 1. If the number of 1's in the data is even, the parity bit is set to 0.

(8) Acknowledge bit

In ordinary communication (one-unit-to-one-unit communication), an acknowledge bit is added in the following positions to confirm that data has been received correctly:

- At the end of the slave address field
- At the end of the control field
- At the end of the data-length field
- At the end of the data field

The acknowledge bit is defined as follows:

- 0: Indicates that transmission data has been recognized. (ACK)
- 1: Indicates that no transmission data has been recognized. (NAK)

For broadcast, the acknowledge bit is ignored.

① **Acknowledge bit at the end of the slave address field**

If any of the following is detected, the acknowledge bit at the end of the slave address field is set to NAK, and transmission is stopped:

- The parity of the master address bits or slave address bits is incorrect.
- A timing error occurred (bit format error).
- No slave unit is found.

② **Acknowledge bit at the end of the control field**

If any of the following is detected, the acknowledge bit at the end of the control field is set to NAK, and transmission is stopped:

- The parity of the control bits is incorrect.
- Although the slave reception buffer**Note** is not empty, bit 3 of the control bits is 1 (write operation).
- Although the slave transmission buffer**Note** is empty, the control bits indicate data read (3H, 7H).
- For a locked unit, a unit other than the unit that specified the lock makes a request by using control bits indicating 3H, 6H, 7H, AH, BH, EH, or FH.
- Although no lock has been set, control bits indicating lock address read (4H) are set.
- A timing error occurred.
- An undefined control bit setting has been made.

Note   See **(1)** in **Section 2.4**.

③ **Acknowledge bit at the end of the data-length field**
If any of the following is detected, the acknowledge bit at the end of the data-length field is set to NAK, and transmission is stopped:

- The parity of the data-length bits is incorrect.
- A timing error occurred.

④ **Acknowledge bit at the end of the data field**
If any of the following is detected, the acknowledge bit at the end of the data field is set to NAK, and transmission is stopped:

- The parity of the data bits is incorrect[Note].
- A timing error occurred after the previous acknowledge bit.
- The reception buffer is full, such that no more data can be accepted[Note].

Note In this case, if the maximum allowable number of transmission bytes per frame has not yet been reached, the transmitter retries transmission of the data field until the maximum number of transmission bytes is reached.

2.4 TRANSMISSION DATA (CONTENTS OF THE DATA FIELD)

The contents of the data field are indicated by the control bits.

Table 2-3   Meanings of the Control Bits

	Bit 3**Note 1**	Bit 2	Bit 1	Bit 0	Function**Note 2**
0H	0	0	0	0	Read slave status (SSR)
1H	0	0	0	1	Undefined
2H	0	0	1	0	Undefined
3H	0	0	1	1	Read data and locking
4H	0	1	0	0	Read lock address (low-order 8 bits)
5H	0	1	0	1	Read lock address (high-order 4 bits)
6H	0	1	1	0	Read slave status (SSR) and unlocking
7H	0	1	1	1	Read data
8H	1	0	0	0	Undefined
9H	1	0	0	1	Undefined
AH	1	0	1	0	Write command and locking
BH	1	0	1	1	Write data and locking
CH	1	1	0	0	Undefined
DH	1	1	0	1	Undefined
EH	1	1	1	0	Write command
FH	1	1	1	1	Write data

Notes 1. The transfer direction of the data-length bits of the subsequent data-length field and data in the data field changes according to the value of bit 3 (MSB).

When bit 3 is 1: Transfer from the master unit to the slave unit

When bit 3 is 0: Transfer from the slave unit to the master unit

2. The values of control bits 3H, 6H, AH, and BH specify locking and unlocking. When an undefined value, 1H, 2H, 8H, 9H, CH, or DH, is transmitted, no acknowledge signal is returned.

Once a unit has been locked by a master unit, the locked unit rejects the control bits received from other than the master unit that requested the lock, unless the value of the control bits is one of the values listed in Table 2-4. Then, the unit does not output the acknowledge bit.

Table 2-4   Control Field Acceptable to a Locked Slave Unit

	Bit 3	Bit 2	Bit 1	Bit 0	Function
0H	0	0	0	0	Read slave status
4H	0	1	0	0	Read lock address (low-order 8 bits)
5H	0	1	0	1	Read lock address (high-order 4 bits)

(1) Reading the slave status (SSR) (control bits: 0H, 6H)

A master unit can read the slave status (0H, 6H) to determine why the slave unit did not return the acknowledge bit (ACK).

The slave status is determined from the result of the communication last performed by the slave unit.

All slave units can provide slave status information.

Table 2-5 lists the slave status meanings.
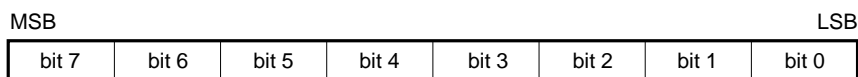
Fig. 2-2   Slave Status (SSR) Bit Format

MSB   LSB

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Table 2-5   Slave Status Meanings

Bit	Value	Meaning	
Bit 0[Note 1]	0	The slave transmission buffer is empty.	
	1	The slave transmission buffer is not empty.	
Bit 1[Note 2]	0	The slave reception buffer is empty.	
	1	The slave reception buffer is not empty.	
Bit 2	0	The unit is not locked.	
	1	The unit is locked.	
Bit 3	0	Fixed at 0	
Bit 4[Note 3]	0	Slave transmission disabled	
	1	Slave transmission enabled	
Bit 5	0	Fixed at 0	Indicates the highest mode supported by the unit[Note 4].
Bit 7	00	Mode 0	
Bit 6	01	Mode 1	
	10	Reserved for future expansion	
	11		

Notes 1. The slave transmission buffer is accessed during a data read operation (control bits: 3H, 7H). For the μPD72042, this buffer corresponds to the TBF available when STRQ of the FLG register is set to 1.

2. The slave reception buffer is accessed during a data write operation (control bits: 8H, AH, BH, EH, FH). For the μPD72042, this buffer corresponds to the RBF available when SLRE of the FLG register is set to 1.

3. The value of bit 4 can be selected by using the UAR1 register.

4. Bits 7 and 6 are currently fixed to 10 in the hardware of the μPD72042.

(2) Data/command transfer (control bits: Read (3H, 7H), write (AH, BH, EH, FH))

When data read (3H, 7H) is set, the data in the data buffer of the slave unit is read into the master unit.

When data write (BH, FH) or command write (AH, EH) is set, the data received by the slave unit is processed according to the operation specifications for the slave unit.

Remarks 1. The user can select data and commands as necessary according to the system.

2. 3H, AH, and BH may cause locking, depending on the communication conditions and status.

(3) Reading a lock address (control bits: 4H, 5H)

When a lock address read operation (4H, 5H) is specified, the address (12 bits) of the master unit that issued the lock instruction is read in one-byte form, as shown below.

Fig. 2-3 Lock Address Format

MSB   LSB

Control bits : 4H | Low-order 8 bits |

Control bits : 5H | Undefined | High-order 4 bits |

(4) Locking and unlocking (control bits: Locking (3H, AH, BH), unlocking (6H))

The lock function is used to enable the transfer a message using more than one communication frame.

When locked, a unit cannot receive data from other than the unit that requested the lock.

Locking and unlocking are performed as follows:

① **Locking**

The master unit can lock the slave unit by specifying the lock with the corresponding control bits (3H, AH, BH). In this case, when the transmission or reception of acknowledge bit 0 for the data-length field has been completed, but the communication frame is then terminated before transmission or reception of as many data bytes as are specified by the data-length bits is completed, the slave unit is locked. At this time, the bit indicating the lock status (bit 2) in the slave status byte is set to 1.

② **Unlocking**

The master unit can unlock a locked slave unit when the control bits specify locking (3H, AH, or BH) or unlocking (6H). The slave unit is unlocked once as many data bytes as are specified by the data-length bits have been transmitted or received within one communication frame. At this time, the bit indicating the lock status (bit 2) in the slave status byte is reset to 0.

For broadcast, locking or unlocking is not performed.

Caution When a locked unit is to be unlocked by the unit itself, hardware reset or software reset must be performed. (The lock status can be checked by referring to the contents of the LOR2 register.)

2.5 BIT FORMAT

Fig. 2-4 illustrates the bits that constitute an IEBus communication frame.

Fig. 2-4   IEBus Bit Format (Concept)
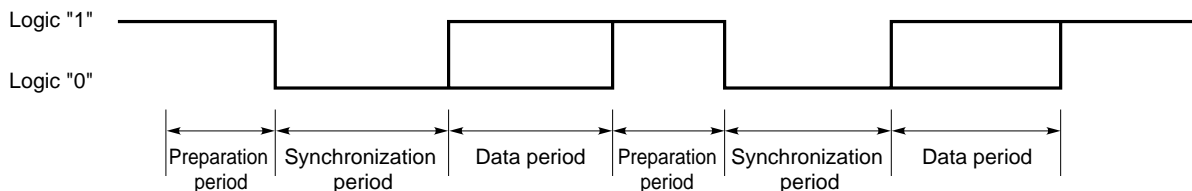
Logic 1: The potential difference between the bus lines (the BUS+ and BUS- pins) is 20 mV or less (low level).
Logic 0: The potential difference between the bus lines (the BUS+ and BUS- pins) is 120 mV or more (high level).

Preparation period   : First and subsequent low-level (logic 1) periods
Synchronization period   : Next high-level (logic 0) period
Data period   : Period in which a bit value is indicated (logic 1 = low level, logic 0 = high level)

The synchronization and data periods are almost equal in duration.

For the IEBus, synchronization is established for each bit. The specifications of the total time required for a bit and the duration of each period allotted within the bit vary depending on the type of the transmission bits, and whether the unit is a master or slave.

3. MICROCOMPUTER INTERFACE

3.1 TRANSFER METHOD

Either of two microcomputer interface modes can be selected: three-wire serial I/O mode or two-wire serial I/O mode.

Whether three-wire serial I/O mode or two-wire serial I/O mode is selected depends on the input level of the SEL pin (pin 12). (See **Section 3.3** for details.)

SEL ← 1: Three-wire serial I/O
SEL ← 0: Two-wire serial I/O

(1) Three-wire serial I/O (SEL ← 1)

Three wires are used to read and write data. The three wires are the serial clock input ($\overline{\text{SCK}}$), serial data input (SI**Note 1**), and serial data output (SO**Note 2**).

(a) Read operation

Data is output to the SO pin upon detecting the falling edge of the $\overline{\text{SCK}}$ pin.

(b) Write operation

Data is input via the SI pin upon detecting the rising edge of the $\overline{\text{SCK}}$ pin. At this time, 1 is output on the SO pin.

(2) Two-wire serial I/O (SEL ← 0)

Two wires are used to read and write data. The two wires are the serial clock input ($\overline{\text{SCK}}$) and serial data I/O (SIO**Note 1**).

(a) Read operation

The SIO pin is placed in the output state, and data is output upon detecting the falling edge of the $\overline{\text{SCK}}$ pin.

(b) Write operation

The SIO pin is placed in the input state, and data is input upon detecting the rising edge of the $\overline{\text{SCK}}$ pin.

Notes 1. The SI pin for three-wire serial I/O mode is also used as the SIO pin for two-wire serial I/O mode.
2. The impedance of the SO pin for three-wire serial I/O mode goes high in two-wire serial I/O mode. So, connect the SO pin to GND or V$_{DD}$.

Table 3-1   I/O States of the SIO (SI) and SO Pins

$\overline{\text{RESET}}$	$\overline{\text{CS}}$	SEL	C/$\overline{\text{D}}$	SI (SIO)	SO	State	
						Three-wire/two-wire	Operating mode
0	×	×	×	I	Hi-Z	–	Reset state
1	1	×	×	I	Hi-Z	–	Chip nonselected state
1	0	1	1	I	O*	Three-wire	Control mode
			0				Data write mode
					O		Data read mode
		0	1	I	Hi-Z	Two-wire	Control mode
			0				Data write mode
				O			Data read mode

I   : Input state   Hi-Z : High-impedance state
O   : Output state   ×   : Don't care
O* : State in which 1 is output

3.2   DATA TRANSFER FORMAT

3.2.1   Three-Wire Data Transfer (SEL = 1)

(1) Control mode
   When the C/$\overline{\text{D}}$ input is set high, control mode is set to control data transfer. Data transfer control involves the
   following processing.
   ① Register address setting
   ② Register read/write selection
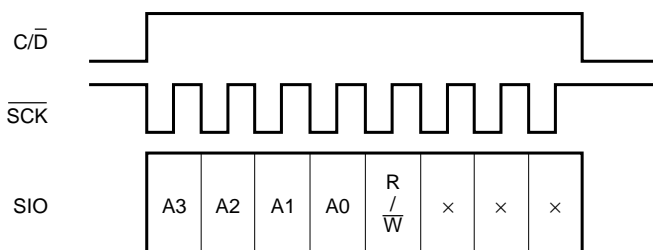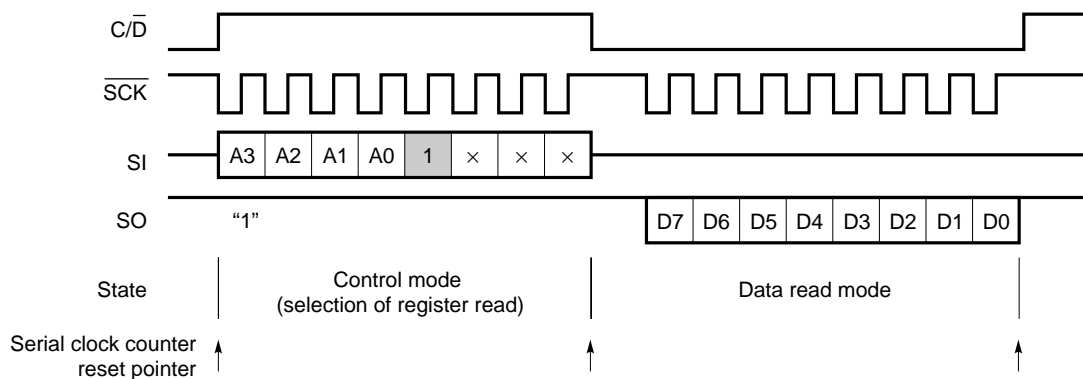

Remark After reset ($\overline{\text{RESET}}$) cancellation, the state enabling writing to the register at address 0000B is set.

**Caution In control mode, each data item is read every eighth clock pulse. (Data of less than eight clock
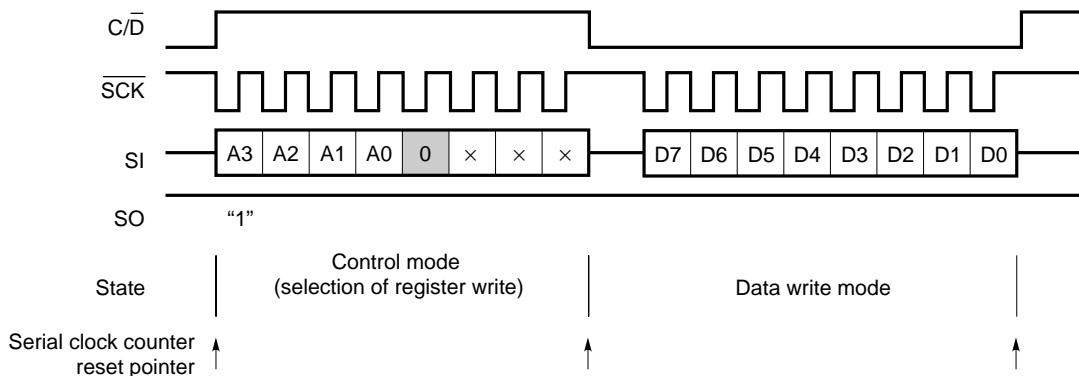   periods is ignored.)**

(2) Data read mode

When the C/$\overline{\text{D}}$ pin is set low after register read is selected in control mode, the data read mode is set. In data read mode, the data in a read register is read on the SO pin upon detecting the falling edge of the $\overline{\text{SCK}}$ pin.

C/$\overline{\text{D}}$

$\overline{\text{SCK}}$

SI: | A3 | A2 | A1 | A0 | 1 | × | × | × |

SO: "1" | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

State: Control mode (selection of register read) | Data read mode

Serial clock counter reset pointer

Caution **When the C/$\overline{\text{D}}$ pin is set high in data read mode, the serial clock counter is reset. Therefore, the remaining bits of the byte cannot be read; at the next falling edge, read is performed starting from the next byte in the case of RBF, or from the first bit for other registers.**

(3) Data write mode

When the C/$\overline{\text{D}}$ pin is set low after register write has been selected in control mode, data write mode is set. In data write mode, data for a write register is applied to the SI pin at the rising edge of the $\overline{\text{SCK}}$ pin.

C/$\overline{\text{D}}$

$\overline{\text{SCK}}$

SI: | A3 | A2 | A1 | A0 | 0 | × | × | × | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

SO: "1"

State: Control mode (selection of register write) | Data write mode

Serial clock counter reset pointer

Caution **Register overwrite is started immediately after the eighth clock rising edge. All registers other than TBF are overwritten on the eighth clock rising edge. (Data of less than eight clock periods is ignored.)**

3.2.2   Two-Wire Data Transfer (SEL = 0)

(1)   Control mode

When the C/$\overline{\text{D}}$ input is set high, control mode is set to control data transfer. Data transfer control involves the following processing.
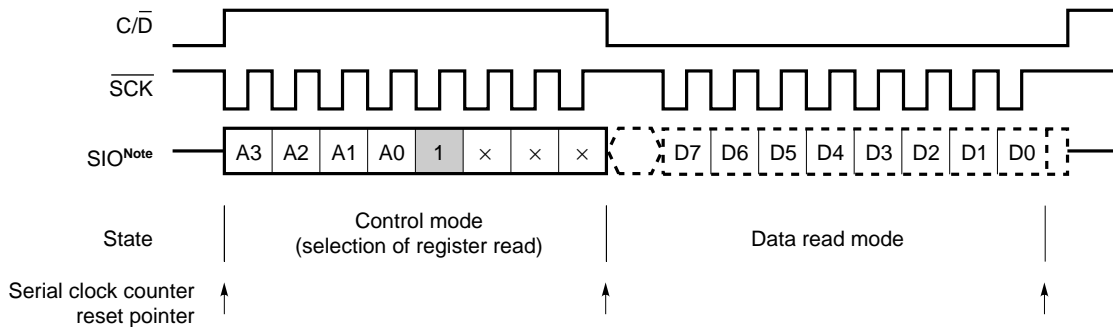
① Register address setting
② Register read/write selection
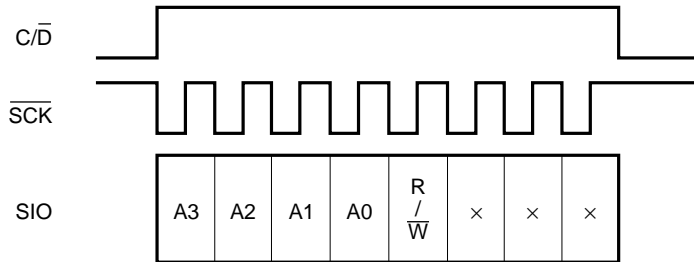
Remark   After reset ($\overline{\text{RESET}}$) cancellation, the state enabling writing to the register at address 0000B is set.

Caution   In control mode, each data item is read every eighth clock pulse. (Data of less than eight clock periods is ignored.)

(2)   Data read mode

Note ——— SIO pin input state
         - - - - - SIO pin output state

Cautions 1. When the C/$\overline{\text{D}}$ pin is set high in data read mode, the serial clock counter is reset. Therefore, the remaining bits of the byte cannot be read; at the next falling edge, a read operation is performed starting from the next byte in the case of RBF, or from the first bit for other registers.

2. The SIO pin is a CMOS I/O pin. So, be careful to avoid an output collision between the SIO pin and the microcomputer. Further, a pull-up resistor is required when N-ch open-drain output of the microcomputer is used. Note that if the last output level is low upon the termination of read mode, current will flow constantly.
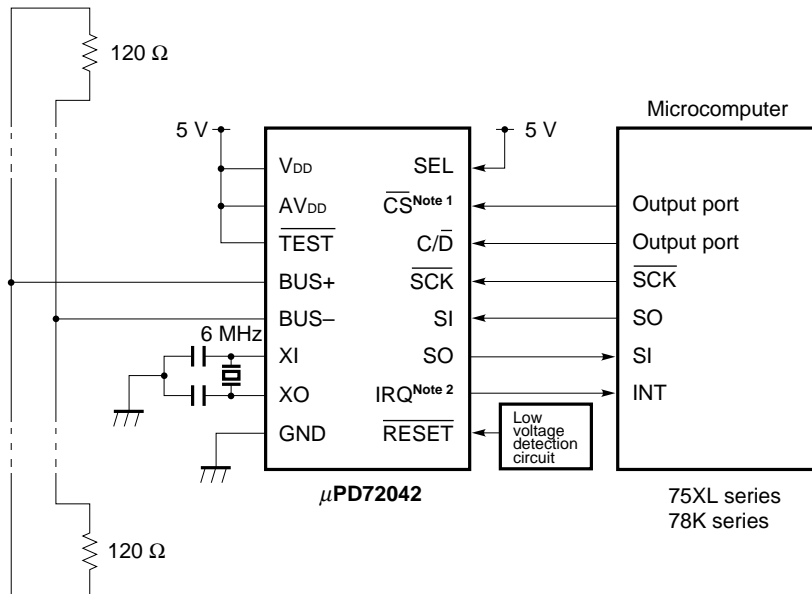
(3) Data write mode
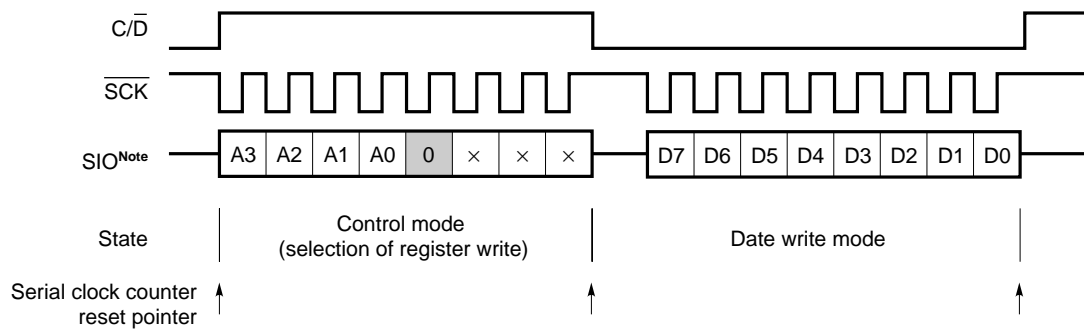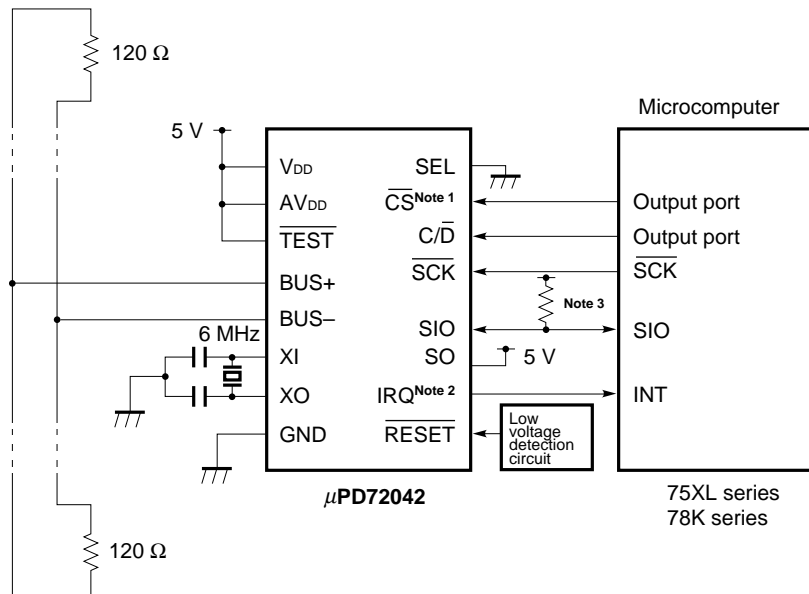

Note ————— SIO pin input state

Caution Register overwrite is started immediately after the eighth clock rising edge. All registers other than TBF are overwritten at the eighth clock rising edge. (Data of less than eight clock periods is ignored.)

3.3 CONNECTION TO A MICROCOMPUTER

(1) Three-wire serial I/O

(2) Two-wire serial I/O

Notes 1. When only the μPD72042 is to be controlled from a microcomputer via a serial I/O interface, the $\overline{CS}$ pin must be tied low (by connecting it to GND).

2. When an interrupt is detected by polling (in FLG register read), IRQ may be left open. When high-volume or high-speed data transfer is required, however, the system described above is recommended to ensure reliable data transfer.

3. Required when the microcomputer's N-ch open-drain output is used. The SIO pin of the μPD72042 is a CMOS I/O pin.

3.4 STANDBY MODE SETTING AND CANCELLATION

Standby mode can be set by setting STREQ of the CTR register to 1. The XI pin for oscillation is tied to GND, and the impedance of the XO pin goes high.

In standby mode (with the STM flag of the FLG register set to 1), only the following registers can be accessed:

Writable register   : CTR (address 0000B)
Readable register   : FLG (address 0001B)

Standby mode can be cancelled by setting STREQ of the CTR register to 0.

Caution Do not read any data from internal registers via the serial I/O during the period from when a microcomputer sets the STREQ flag to 1 to when the μPD72042 enters the standby mode. This period is one-communication frame at maximum.

3.5 RESET MODE SETTING AND CANCELLATION

For hardware reset, the registers are initialized and standby mode is set. (During this period, oscillation is stopped.)
For software reset, the registers are initialized, and operation is started.

4. REGISTERS

A microcomputer controls IEBus communication by reading from and writing to the internal registers of the μPD72042.

Registers are classified into write registers and read registers. The total size of the write registers is 40 bytes; the transmission buffer uses 33 of the 40 bytes. The total size of the read registers is 49 bytes; the reception buffer uses 40 of the 49 bytes.

Table 4-1 lists the registers.

Table 4-1   μPD72042 Registers

(a) Write registers

	Address	Name	High-order 4 bits				Low-order 4 bits				Note	Reference page
0H	0000	CTR	–	–	–	REEN	SRST	–	–	STREQ	A	p. 31
1H	0001	CMR	0	LOCK	BUFC		COMC				C	p. 32
			1	0	0	0	0	IRS	MFC	DERC		
2H	0010	UAR1	Local station address (low-order 4 bits)				Condition code				B	p. 34
3H	0011	UAR2	Local station address (high-order 8 bits)								B	p. 34
4H	0100	SAR1	Slave address (low-order 4 bits)				0	0	0	0	D	p. 35
5H	0101	SAR2	Slave address (high-order 8 bits)								D	p. 35
6H	0110	MCR	Broadcast bits		Number of arbitrations		Control bits				D	p. 36
7H	0111	–	–								–	–
8H	1000	–	–								–	–
EH	1110	TBF	Number of bytes of transmission data, transmission data								F	p. 38

(b) Read registers

	Address	Name	High-order 4 bits				Low-order 4 bits				Note	Reference page
0H	0000	STR	TFL	TEP	RFL	REP	–				A	p. 39
1H	0001	FLG	–	MARQ	STRQ	SLRE	CEX	RAW	STM	IRQ	A	p. 40
2H	0010	RDR1	Number of bytes of master reception data								A	p. 42
3H	0011	RDR2	Number of bytes of slave reception data or broadcast reception data								A	p. 42
4H	0100	LOR1	Lock address (low-order 8 bits)								H	p. 43
5H	0101	LOR2	Lock state				Lock address (high-order 4 bits)				H	p. 43
6H	0110	DAR1	Broadcast address (low-order 4 bits)				–				E	p. 44
7H	0111	DAR2	Broadcast address (high-order 8 bits)								E	p. 44
8H	1000	RCR	Return codes (MARC, SLRC)								A	p. 45
EH	1110	RBF	Transmitter address, reception data								G	p. 57

Note Writable and readable periods of the registers of the μPD72042
   A: Arbitrary
   B: After system reset cancellation
   C: While CEX of the FLG register (address 0001) is set to 0
   D: While MARQ of the FLG register (address 0001) is set to 0
   E: After SLRC of the RCR register (address 1000) is set to 1100 (broadcast reception error)
   F: While TFL of the STR register (address 0000) is set to 0
   G: While REP of the STR register (address 0000) is set to 0
   H: When CEX of the FLG register (address 0001) is set to 0 after LOCK of the CMR register (address 0001)
       is set to 1

Cautions 1. In standby mode (with STM of the FLG register set to 1), the user can only write to the CTR register (including standby mode cancellation) and read from the FLG register.
2. Never access a free address.
3. Slave status (SSR) can be read into RBF by setting the control bits to 0H or 6H from the master unit.

CTR							Address : 0000B (0H)
							Read/write : Write
Control register							When reset : ×××00××1B

CTR is a one-byte write register used to control μPD72042 operations.

b7	b6	b5	b4	b3	b2	b1	b0	
—	—	—	REEN	SRST	—	—	STREQ	CTR
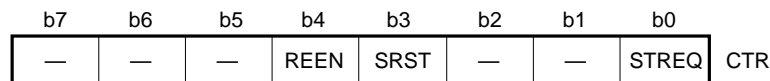
[REEN]
When REEN is set to 1, the SLRE flag of the FLG register is immediately set to 1 to enable both slave and broadcast reception.

[SRST]
When SRST is set to 1, the μPD72042 is immediately reset. (Note, however, that STREQ is set to a written value.)

[STREQ]
1: Requests standby mode.
0: Exits from standby mode.

• **Standby mode setting and cancellation**
The μPD72042 is requested to enter the standby mode by setting the STREQ flag to 1 from the microcomputer. The μPD72042 enters standby mode when the standby mode input enabled state (carrier sense state) is set. In this case, the impedance of the BUS+ and BUS– pins goes high (logic 1), and the STM flag of the FLG register is set to 1. In standby mode, oscillation is stopped, and all operations are stopped while preserving the internal data, thus minimizing power consumption.
When, in standby mode, the STREQ flag is set to 0 from the microcomputer, standby mode is cancelled after the period (about 20 ms) needed for oscillation to stabilize; the halted operations are resumed from the point at which standby mode was set. At this time, the STM flag of the FLG register changes to 0.
In standby mode, only writing to the CTR register (for standby mode cancellation) and reading from the FLG register can be performed from the microcomputer.

Cautions 1. When the SRST flag and STREQ flag are simultaneously set to 1, standby mode is set after software reset. (This state is the same as that set by hardware reset.) Note, however, that when the SRST flag is set to 1 in standby mode, a software reset is performed, but this is not reflected in the FLG register.
2. Do not read any data from internal registers via the serial I/O during the period from when a microcomputer sets the STREQ flag to 1 to when the μPD72042 enters the standby mode. This period is one-communication frame at maximum.

CMR	Address : 0001B (1H)
	Read/write : Write
Command register	When reset : 00000000B

CMR is a one-byte write register used to set a command for communication control, transmission/reception buffer control, or optional function setting.

When data is set in CMR from the microcomputer, CEX of the FLG register is set to 1. When the μPD72042 processes the data set in CMR, CEX is set to 0.

After the microcomputer checks that CEX of the FLG register is set to 0, new data can be set in CMR.

The following describes the data that is set in CMR.

(1) When bit 7 (MSB) of CMR is 0

b7	b6	b5	b4	b3			b0	
0	LOCK	BUFC		COMC				CMR
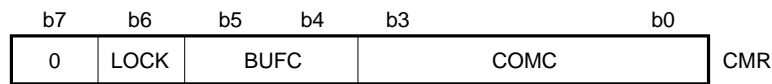
[LOCK]: Lock state setting command

1 : The value representing the lock state (0001 for locked or 0000 for not-locked) and lock address are output to LOR1 and LOR2. Note, however, that when 0000 (not-locked) is output, any lock address value is ignored.

0 : The contents of LOR1 and LOR2 remain as is.

[BUFC]: Transmission/reception buffer control command

00 : The transmission and reception buffers remain as is.

01 : The transmission buffer (TBF) is cleared.

10 : The reception buffer (RBF) is cleared.

11 : The data of the previous (latest) communication frame to be stored in the reception buffer (RBF) is cleared[Note 1].

[COMC]: Communication control command

0000: Communication operation remains as is.

0001: The locked state is cancelled.

1000: Master communication is requested[Note 2].

1001: Master communication is requested, with the previous master transmission state held[Note 3].

1010: Master communication is aborted.

1011: Slave data transmission is requested[Note 4].

1100: Slave data transmission is requested, with the previous slave data transmission state held[Note 5].

1101: Slave data transmission is aborted.

1111: Slave reception and broadcast reception are disabled.

Notes 1. If the microcomputer has already read the data for the previous (latest) communication frame from RBF, or optional function setting in CMR is selected and MFC = 0, clear RBF with BUFC = 10.

Notes 2. When the MSB of the control bits set in MCR is 1 (for master transmission), set the number of bytes of transmission data, and at least one byte of transmission data in TBF before command setting.

     3. When the MSB of the control bits set in MCR is 1 (for master transmission), set at least one byte of transmission data before command setting. This operation is not required if all transmission data has already been set in TBF.

     4. Set the number of bytes of transmission data, and at least one byte of transmission data in TBF before command setting.

     5. Set at least one byte of transmission data in TBF before command setting. This operation is not required if all transmission data has already been set in TBF.

(2) When bit 7 (MSB) of CMR is 1
An optional function is set.

b7	b6	b5	b4	b3	b2	b1	b0	
1	0	0	0	0	IRS	MFC	DERC	CMR

[MFC]: Selection of one frame/multiple frames
   1 : Data for multiple frames is stored in RBF.
   0 : Data for only one frame is stored in RBF.

[DERC]: Broadcast reception selection
   1 : The issue of return code 1100 (broadcast reception error) for SLRC of the RCR register is enabled.
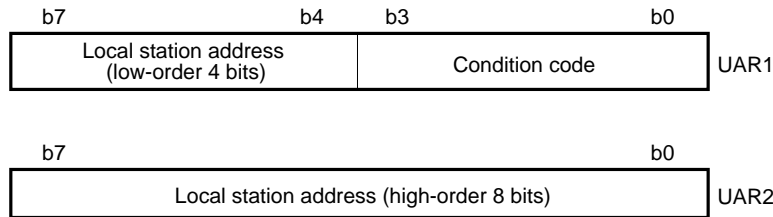   0 : The issue of return code 1100 (broadcast reception error) for SLRC of the RCR register is disabled.

[IRS]: Interrupt generation condition selection
   0 : An interrupt is requested when the data of the RCR register changes.
   1 : An interrupt is requested when the data of the RCR register changes to other than the following:
      MARC = 0000B (start of master transmission)
      MARC = 0100B (start of master reception)
      SLRC = 0000B (start of slave data transmission)
      SLRC = 0100B (start of slave reception)
      SLRC = 1000B (start of broadcast reception)

Caution Set an optional function in initialization processing after reset cancellation for the *μ*PD72042. Until an optional function has been set, the *μ*PD72042 will not accept IEBus communication.

UAR1	Address : 0010B (2H) (UAR1)
UAR2	0011B (3H) (UAR2)
	Read/write : Write
Local station unit address register	When reset : Undefined (with the previous data held)

UAR1 and UAR2 are registers used to set a local station unit address (12 bits) and condition code.
Set UAR1 and UAR2 after reset cancellation.

```
b7                    b4   b3                    b0
┌──────────────────────┬────────────────────────┐
│  Local station address│     Condition code     │  UAR1
│  (low-order 4 bits)   │                        │
└──────────────────────┴────────────────────────┘

b7                                              b0
┌─────────────────────────────────────────────┐
│     Local station address (high-order 8 bits) │  UAR2
└─────────────────────────────────────────────┘
```

[Local station address]

   A local station address is used as a master address when the local station performs communication as the master unit. A local station address is used as a slave address when the local station performs communication as a slave.

[Condition code]

Bit position	Condition code	Condition setting
b3, b2	00	Communication is performed in mode 0.
	01	Communication is performed in mode 1.
	10	Undefined
	11	
b0	0	The slave transmission section is disabled.
	1	The slave transmission section is enabled.

   Remark Bit 1 of a condition code is not used. (Set the bit to either 0 or 1.)

| SAR1	Address	: 0100B (4H) (SAR1)
SAR1	Address	: 0100B (4H) (SAR1)
SAR2		0101B (5H) (SAR2)
	Read/write	: Write
Slave address register	When reset	: Undefined (the previous data is held)

The SAR1 and SAR2 registers are used to set the address of a remote station (slave address) in master communication.

Set SAR1 and SAR2 while the value of MARQ of the FLG register is 0 (while master communication is not requested).

b7				b4	b3			b0	
Slave address (low-order 4 bits)					0	0	0	0	SAR1

b7	b0	
Slave address (high-order 8 bits)		SAR2
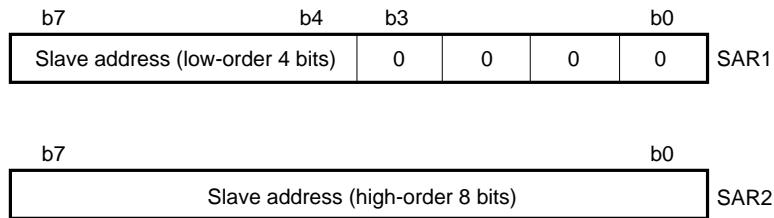
MCR **Master communication register**	Address : 0110B (6H) Read/write : Write When reset : Undefined (the pre- vious data is held)

The MCR register is used to set a master communication condition.

Set MCR while the value of MARQ of the FLG register is 0 (while master communication is not requested).

b7	b6	b4	b3	b0	
Broadcast bit	Number of arbitrations		Control bits		MCR
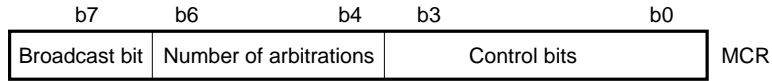
[Broadcast bit]

This bit is used to select broadcast or separate communication.

Bit 7 = 0: Broadcast

Bit 7 = 1: Separate communication

[Number of arbitrations] (Number of retries)

This field is used to set the maximum number of retry operations to be performed if arbitration is lost in master communication. The *µ*PD72042 automatically retries communication as many times as the number set in this field.

b6	b5	b4	Number of retries
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

[Control bits]

This control field is used to set the control bits (four bits).

• **Contents of control bits**

	Bit 3**Note 1**	Bit 2	Bit 1	Bit 0	Function**Note 2**
0H	0	0	0	0	Slave status (SSR) read
1H	0	0	0	1	Undefined
2H	0	0	1	0	Undefined
3H	0	0	1	1	Data read and lock
4H	0	1	0	0	Lock address read (low-order 8 bits)
5H	0	1	0	1	Lock address read (high-order 4 bits)
6H	0	1	1	0	Slave status (SSR) read and unlock
7H	0	1	1	1	Data read
8H	1	0	0	0	Undefined
9H	1	0	0	1	Undefined
AH	1	0	1	0	Command write and lock
BH	1	0	1	1	Data write and lock
CH	1	1	0	0	Undefined
DH	1	1	0	1	Undefined
EH	1	1	1	0	Command write
FH	1	1	1	1	Data write

Notes 1. The value of bit 3 (MSB) determines the transfer direction of the subsequent data-length field data and data field data.

When bit 3 is set to 1: Data is transferred from the master unit to a slave unit.

When bit 3 is set to 0: Data is transferred from a slave unit to the master unit.

2. 3H, 6H, AH, and BH are control bits used for lock setting and cancellation.

When an undefined value of 1H, 2H, 8H, 9H, CH, or DH is sent, no acknowledgement is returned.

TBF	Address : 1110B (EH)
	Read/write : Write
Transmission buffer	When reset : Empty

TBF is a 33-byte FIFO buffer used to hold the number of bytes of transmission data and transmission data for master transmission and slave data transmission.

TBF can be written from the microcomputer when the TFL flag of the STR register is set to 0 (indicating that TBF is not full).

In master transmission and slave data transmission, the following format is used to load data into TBF from the microcomputer.

TBF

Byte 1	Number of bytes of transmission data
Byte 2	First byte of transmission data
Byte 3	Second byte of transmission data
⋮	⋮
Byte 33	⋮

[Byte 1]: Number of bytes of transmission data
Between 1 and 256 bytes can be set.

Number of bytes of transmission data	Data set in byte 1 of TBF
1	01H
2	02H
⋮	⋮
255	FFH
256	00H

[Bytes 2 and up]: Transmission data
As much transmission data as is set in byte 1 is set in byte 2 and subsequent bytes.

STR	Address : 0000B (0H)
	Read/write : Read
Status register	When reset : 0101$\times\times\times\times$B

STR is a one-byte read register used to indicate the states of TBF and RBF.

b7	b6	b5	b4	b3	b2	b1	b0	
TFL	TEP	RFL	REP	—	—	—	—	STR
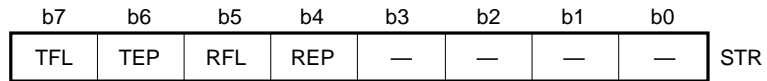
[TFL]

   1 : TBF is full.

   0 : TBF is not full. The microcomputer can load data into TBF.

[TEP]

   1 : TBF is empty. The microcomputer can load initial data into TBF.

   0 : TBF is not empty.

[RFL]

   1 : RBF is full.

   0 : RBF is not full.

[REP]

   1 : RBF is empty.

   0 : RBF is not empty. The microcomputer can read data from RBF.

FLG	Address	: 0001B (1H)
	Read/write	: Read
Flag register	When reset	: 00000010B

FLG is a one-byte read register used to indicate statuses such as the communication state, command execution state, and interrupt state.

b7	b6	b5	b4	b3	b2	b1	b0	
—	MARQ	STRQ	SLRE	CEX	RAW	STM	IRQ	FLG
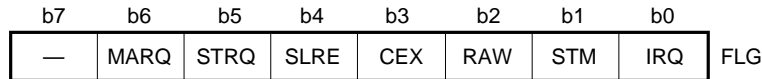
[MARQ]

    1 : A request for communication as the master unit is being made.

    0 : No request for communication as the master unit is being made. Data can be written to the SAR1, SAR2, and
        MCR registers.

The MARQ flag is set and reset as described below.

    • Set   : When the CEX flag of the FLG register is set to 0 after 1000 or 1001 is set in COMC of the CMR register

    • Reset : When master communication is terminated

[STRQ]

    1 : A request for slave unit data transmission is being made.

    0 : No request for slave unit data transmission is being made.

The STRQ flag is set and reset as described below.

    • Set   : When the CEX flag of the FLG register is set to 0 after 1011 or 1100 is set in COMC of the CMR register

    • Reset : When slave data transmission is terminated

[SLRE]

    1 : Slave reception or broadcast is allowed.

    0 : Slave reception and broadcast are not allowed.

The SLRE flag is set and reset as described below.

    • Set   : When REEN of the CTR register is set to 1

    • Reset : When slave reception or broadcast reception is terminated normally or suspended, or when CEX of
                the FLG register is set to 0 after 1111 is set in COMC of the CMR register

When SLRE = 0, bit 1 of the slave status is set to 1 regardless of the state of RBF; communication frame reception based on the AH, BH, EH, and FH control bits, received from the master station, is not performed.

[CEX]

    1 : A command is currently being executed.

    0 : Execution of a command has terminated. A command code can be set in CMR.

The CEX flag is set and reset as described below.

- Set   : When a command code is set in CMR
- Reset : When μPD72042 command processing is terminated

[RAW]

    1 : The μPD72042 is running away.

    0 : The μPD72042 is not running away.

The RAW flag is used to indicate a microprogram crash in the μPD72042, as detected by a watchdog timer.

When the RAW flag is set to 1, a request to interrupt the microcomputer is issued. An interrupt pulse signal is output on the IRQ pin, and the IRQ flag of the FLG register is set. At this time. The microcomputer must reset the μPD72042 by driving the $\overline{\text{RESET}}$ pin of the μPD72042 low or by setting the SRST flag of the CTR register to 1.

[STM]

    1 : Standby mode is set.

    0 : Standby mode is not set.

[IRQ]

    1 : An interrupt request was made.

    0 : No interrupt request is made.

The IRQ flag is set when a return code including the code in the RCR register is changed[Note], or when the RAW flag changes from 0 to 1 (crash). When the FLG register is read with the IRQ flag set to 1, the IRQ flag is reset.

For details of the return codes, see the description of the RCR register.

    Note   IRQ flag setting depends on the IRS value of the CMR register.

RDR1	Address	: 0010B (2H) (RDR1)
RDR2		0011B (3H) (RDR2)
	Read/write	: Read
Reception data register	When reset	: 00H

The RDR1 and RDR2 registers are used to hold the number of bytes of reception data stored in RBF for each frame received during master, slave, or broadcast reception.

b7   b0

Number of bytes of master reception data	RDR1

b7   b0

Number of bytes of slave or broadcast reception data	RDR2
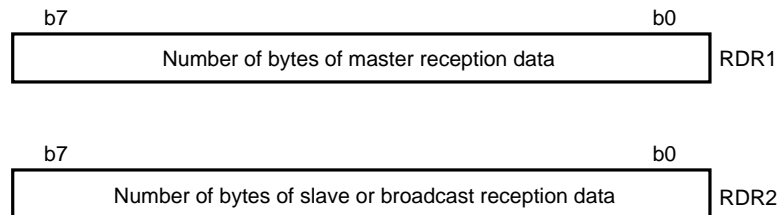
[RDR1]

RDR1 indicates the number of bytes of data set in RBF by a communication frame during master reception. One of the following values is set in RDR1:

- When master communication is requested (COMC = 1000 or 1001)   : RDR1 = 0
- When master reception is started (MARC = 0100)   : RDR1 = 3
- Each time one byte of data is received   : RDR1 is incremented by 1.

[RDR2]

RDR2 indicates the number of bytes of data set in RBF by a communication frame in slave reception or broadcast reception. One of the following values is set in RDR2:

- When slave reception is started (SLRC = 0100)   : RDR2 = 3
- When broadcast reception is started (SLRC = 1000)   : RDR2 = 3
- Each time one byte of data is received   : RDR2 is incremented by 1.

- **Example of RDR2 setting**

Control bits	P	A	Data-length bits	P	A	Data	P	A	Data	P	A
F	0	0	10	1	0	01	1	0	02	1	0

Communication frame

RDR2: $N^{Note} + 3$ 3   4   5
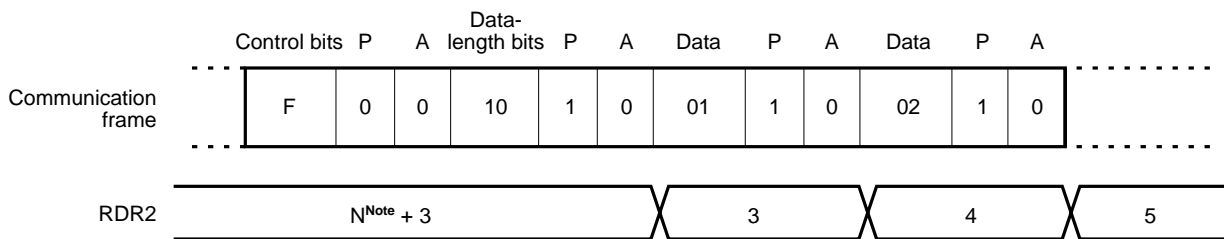
Note N: Number of bytes of data received with the previous communication frame

LOR1	Address	: 0100B (4H) (LOR1)
LOR2		0101B (5H) (LOR2)
	Read/write	: Read
Lock register	When reset	: 0×H (LOR2)
		LOR1 is undefined.

The LOR1 and LOR2 registers are used to hold a lock state.

LOR1 and LOR2 set a lock state and lock address after the lock state setting command is set in the CMR register (LOCK = 1), then executed.

b7		b0	
	Lock address (low-order 8 bits)		LOR1

b7	b4	b3	b0	
Lock state		Lock address (high-order 4 bits)		LOR2
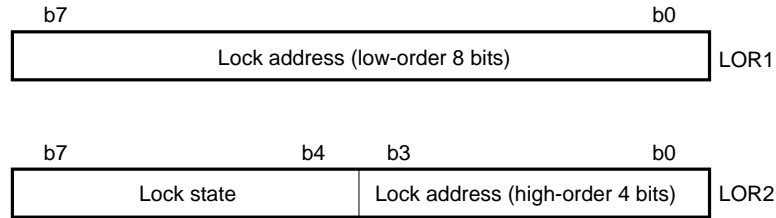
[Lock state]

0000: Not locked

0001: Locked

Remark When 0000 (not locked) is set in the lock state bits, any lock address value is ignored.

DAR1	Address	: 0110B (6H) (DAR1) High-order 4 bits
DAR2		0111B (7H) (DAR2)
	Read/write	: Read
Broadcast address register	When reset	: Undefined

The DAR1 and DAR2 registers are used to hold a broadcast address (master address) involved when a broadcast reception error occurs.

DAR1 and DAR2 are updated each time a broadcast reception error occurs (SLRC of the RCR register is set to 1100). So, ensure that when a broadcast reception error occurs, the contents of DAR1 and DAR2 are read by the microcomputer within the time indicated below.

| b7 | b4 | b3 | b0 | |
| Broadcast address (low-order 4 bits) | | — | | DAR1 |

| b7 | b0 | |
| Broadcast address (high-order 8 bits) | | DAR2 |
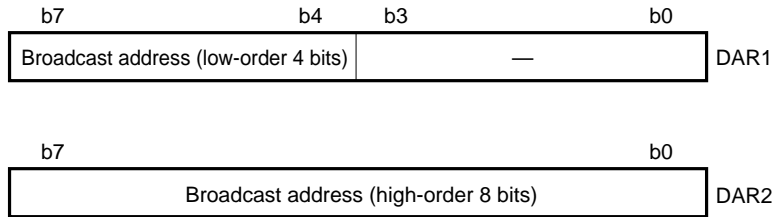
- **Maximum allowable DAR1 and DAR2 read time:**
  Approx. 5420 μs (mode 0)
  Approx. 1490 μs (mode 1)
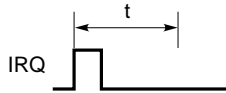
Cautions 1. **If the microcomputer cannot read the data in DAR1 and DAR2 within the times indicated above, DAR1 and DAR2 may be updated by the occurrence of another broadcast reception error, and the subsequently updated broadcast address may be read.**

2. **A broadcast address is stored in DAR1 and DAR2 when DERC (broadcast reception selection) of the CMR register is set to 1.**

RCR	Address : 1000B (8H)
	Read/write : Read
Return code register	When reset : 11111111B

RCR is a one-byte read register used to indicate the IEBus communication status (return code).

RCR consists of two return codes: MARC and SLRC. MARC indicates the communication status in master transmission or master reception. SLRC indicates the communication status in slave data transmission, slave reception, or broadcast reception. When the contents of RCR change, an interrupt request is sent to the microcomputer according to the setting of the IRS flag of the CMR register.

The MARC and SLRC flags are set independently, such that the microcomputer can simultaneously read the master communication status and slave communication status.

```
b7              b4  b3              b0
┌───────────────────┬───────────────────┐
│       MARC        │       SLRC        │  RCR
└───────────────────┴───────────────────┘
```
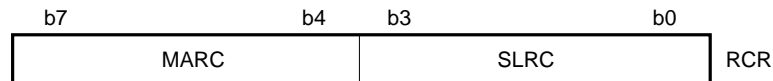
Caution   When IRQ is set as a result of a program crash, the previous value of RCR is preserved.

[MARC]

MARC represents a return code issued during master transmission or master reception.

(a) Master transmission

Master transmission is performed when the microcomputer performs the setting explained below.

• **Master transmission setting**

① In the low-order 4 bits of the MCR register, control bits (1010, 1011, 1110, or 1111) are set for master-to-slave data transfer.

② In COMC of the CMR register, a command (1000 or 1001) for requesting master communication is set.

Table 4-2 lists the MARC return codes for master transmission.

Table 4-2   MARC Return Codes for Master Transmission

MARC	Description
0000	1. **Meaning**: Master transmission is started.
	2. **Occurrence condition**: This return code is issued when the master address field in a communication frame has been transmitted, and the unit has won the arbitration to become the master unit.
0001	1. **Meaning**: Master transmission data is not available.
	2. **Occurrence condition**: This return code is issued if the next transmission data is not set in TBF during master transmission.
	3. **Microcomputer processing**: If data consisting of one or more bytes is not set in TBF within the time below, transmission may be terminated prior to its completion. • Transmission data setting time: Approx. 1570 μs (mode 0) Approx. 390 μs (mode 1)
0010	1. **Meaning**: Master transmission was terminated normally.
	2. **Occurrence condition**: This return code is issued when as much data as the amount specified in the data-length field has been transmitted normally. In this case, the MARQ flag of the FLG register changes from 1 to 0.
0011	1. **Meaning**: Master transmission was aborted.
	2. **Occurrence condition**: This return code is issued in any of the following cases. In each case, the MARQ flag of the FLG register changes from 1 to 0. • When the unit has lost the arbitration to become the master unit. • When a transmission is stopped because the NAK is returned from the slave unit at the end of the slave address field, the control field, or the data-length field of a communication frame (excluding the broadcast). • When a communication is terminated prior to the transmission of as much data as the amount specified in the data-length field of a communication frame.

(b) Master reception

Master reception is performed when the microcomputer performs the setting below.

• **Master reception setting**

① In the low-order 4 bits of the MCR register, control bits (0000, 0011, 0100, 0101, 0110, or 0111) are set for slave-to-master data transfer.

② In COMC of the CMR register, a command (1000 or 1001) for requesting master communication is set.

Table 4-3 indicates the MARC return codes for master reception.

Table 4-3   MARC Return Codes for Master Communication

MARC	Description
0100	**1. Meaning**: Master reception has started.
	2. Occurrence condition: ① The unit has won the arbitration to become the master unit, and a communication frame up to the data-length field was transferred successfully. ② When the control field is received, RBF becomes ready for reception**Note**. After the data-length field, 0000 is set in MARC, and three-byte data consisting of a slave address, control bits, and data-length bits is set in RBF. If RBF becomes full when this three-byte data is set, 0001 is set in MARC.
	3. Microcomputer processing: Three-byte data consisting of a slave address, control bits, and data-length bits can be read from RBF.
0101	**1. Meaning**: The master reception buffer is full.
	2. Occurrence condition: This return code is issued when RBF becomes full during data reception as the master unit, and reception data cannot be set in RBF.
	3. Microcomputer processing: If data consisting of one or more bytes is not read from RBF within the time below, the one-byte data cannot be received, and the μPD72042 returns an NAK. • Reception data read time: Approx. 1570 μs (mode 0) Approx. 390 μs (mode 1)
0110	**1. Meaning**: Master reception was terminated normally.
	2. Occurrence condition: This return code is issued when as much data as the amount specified in the data-length field has been received normally in a communication frame. In this case, the MARQ flag of the FLG register changes from 1 to 0.
	3. Microcomputer processing: Reception data can be read from RBF, and the number of bytes of master reception data can be read from RDR1.
0111	**1. Meaning**: Master reception was aborted.
	2. Occurrence condition: This return code is issued in any of the following cases. In each case, the MARQ flag of the FLG register changes from 1 to 0. • When the unit has lost the arbitration to become the master unit. • When a transmission is stopped because the NAK is returned from the slave unit at the end of the slave address field or the control field of a communication frame or because the NAK is sent to the slave unit at the end of the data-length field of a communication frame (excluding the broadcast). • When a communication is terminated prior to the reception of as much data as the amount specified in the data-length field of a communication frame.
	3. Microcomputer processing: Reception data can be read from RBF, and the number of bytes of master reception data can be read from RDR1.

Note   See **Note** of Table 4-9.

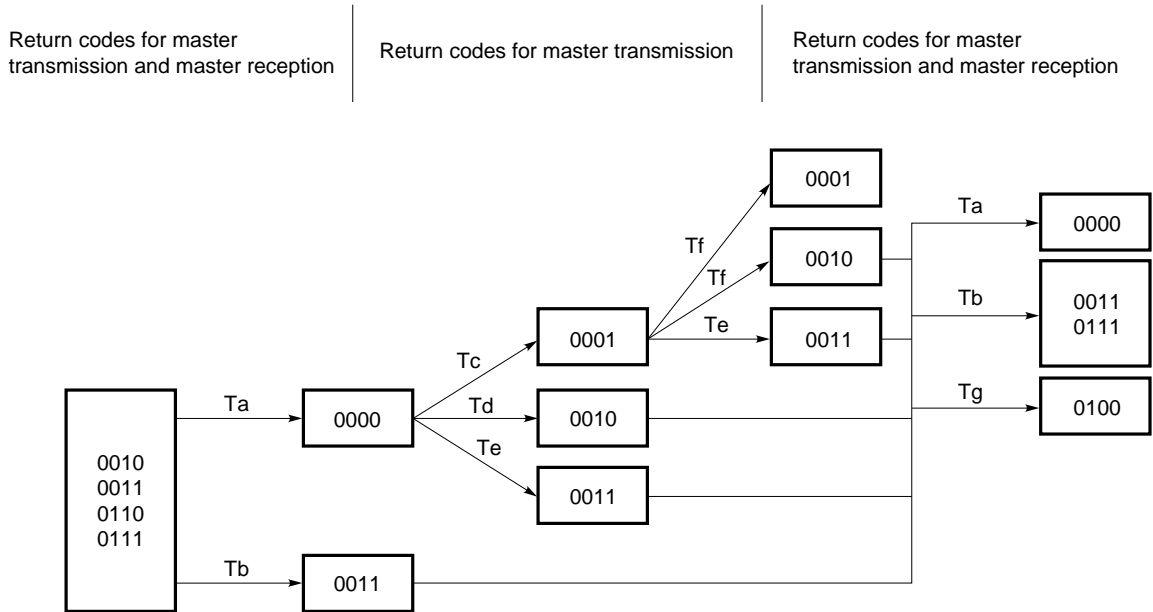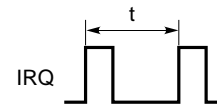**[MARC occurrence interval]**

(a) When master transmission is performed

Return codes for master transmission and master reception | Return codes for master transmission | Return codes for master transmission and master reception

Table 4-4 Minimum Return Code Occurrence Interval for Master Transmission

Interval	Mode 0	Mode 1
Ta	Approx. 2430 μs	Approx. 740 μs
Tb	Approx. 90 μs	Approx. 90 μs
Tc	Approx. 4710 μs	Approx. 1170 μs
Td	Approx. 6290 μs	Approx. 1570 μs
Te	Approx. 20 μs	Approx. 20 μs
Tf	Approx. 1570 μs	Approx. 390 μs
Tg	Approx. 7150 μs	Approx. 1920 μs

(b) When master reception is performed

Return codes for master transmission and master reception | Return codes for master reception | Return codes for master transmission and master reception
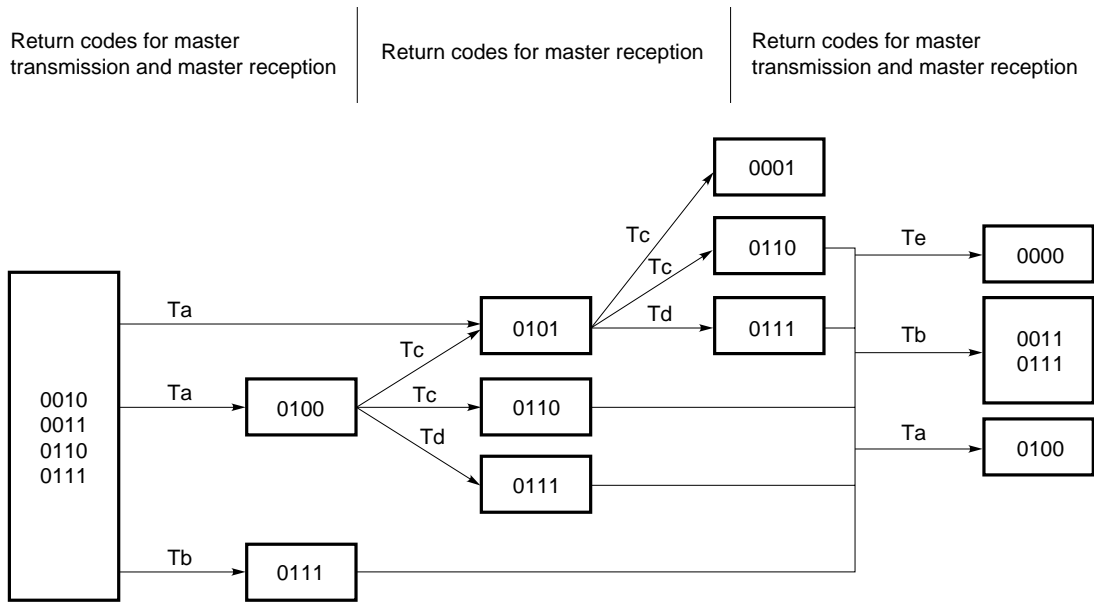
Table 4-5 Minimum Return Code Occurrence Interval for Master Reception

Interval	Mode 0	Mode 1
Ta	Approx. 7150 μs	Approx. 1920 μs
Tb	Approx. 90 μs	Approx. 90 μs
Tc	Approx. 1570 μs	Approx. 390 μs
Td	Approx. 20 μs	Approx. 20 μs
Te	Approx. 2430 μs	Approx. 740 μs

IRQ
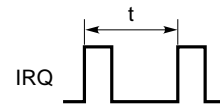
[SLRC]

SLRC indicates the communication status for slave data transmission, slave reception, or broadcast reception.

(a) Slave data transmission

Slave data transmission is performed when the microcomputer makes the setting described below.

• **Slave data transmission setting**

In COMC of the CMR register, a command (1011 or 1100) for requesting slave data transmission is set from the microcomputer.

Table 4-6   SLRC Return Codes in Slave Data Transmission

SLRC	Description
0000	1. **Meaning**: Slave data transmission has been started.
	2. **Occurrence condition**: This return code is issued when the control bits (0011 or 0111) requesting data transmission are received from the master unit.
0001	1. **Meaning**: Slave transmission data is not available.
	2. **Occurrence condition**: This return code is issued when the next transmission data is not set in TBF during slave data transmission.
	3. **Microcomputer processing**: If data consisting of one or more bytes is not set in TBF within the time below, transmission may be terminated prior to its completion. • **Transmission data setting time**: Approx. 1570 μs (mode 0) Approx. 390 μs (mode 1)
0010	1. **Meaning**: Slave data transmission was terminated normally.
	2. **Occurrence condition**: This return code is issued when as much data as the amount specified in the data-length field has been transmitted normally. In this case, the STRQ flag of the FLG register changes from 1 to 0.
0011	1. **Meaning**: Slave data transmission was aborted.
	2. **Occurrence condition**: This return code is issued when communication is terminated prior to the transmission of as much data as the amount specified in the data-length field in a communication frame. In this case, the STRQ flag of the FLG register changes from 1 to 0.

(b) Slave reception

Slave reception is performed when the broadcast bit is set to 1, and a communication frame with the local station address specified in the slave address field is received.

Table 4-7 indicates the SLRC return codes for slave reception.

Table 4-7   SLRC Return Codes for Slave Reception

SLRC	Description
0100	**1. Meaning**: Slave reception is started.
	2. Occurrence condition: ① A separate communication frame up to the data-length field was received normally from the master unit. ② Once the control field has been received, RBF is ready for reception**Note**. After the data-length field, 0100 is set in SLRC, and three-byte data consisting of a master address, control bits, and data-length bits is set in RBF.
	3. Microcomputer processing: Three-byte data consisting of a master address, control bits, and data-length bits can be read from RBF.
0101	**1. Meaning**: The slave reception buffer is full.
	2. Occurrence condition: This return code is issued when RBF becomes full during data reception as a slave unit, and reception data cannot be set in RBF.
	3. Microcomputer processing: If data consisting of one or more bytes is not read from RBF within the period indicated below, the one-byte data cannot be received, and the μPD72042 returns an NAK. • Reception data read time: Approx. 1570 μs (mode 0) Approx. 390 μs (mode 1)
0110	**1. Meaning**: Slave reception was terminated normally.
	2. Occurrence condition: This return code is issued when as much data as the amount specified in the data-length field has been received normally in a communication frame. In this case, the SLRE flag of the FLG register changes from 1 to 0.
	3. Microcomputer processing: Reception data can be read from RBF, and the number of bytes of slave reception data can be read from RDR2.
0111	**1. Meaning**: Slave reception was aborted.
	2. Occurrence condition: This return code is issued when reception is terminated prior to the reception of as much data as the amount specified in the data-length field of a communication frame. In this case, the SLRE flag of the FLG register changes from 1 to 0.
	3. Microcomputer processing: Reception data can be read from RBF, and the number of bytes of slave reception data can be read from RDR2.

Note   See **Note** of Table 4-9.

(c) Broadcast reception

Broadcast reception is performed when the broadcast bit is set to 0, and a communication frame with FFH (general broadcast) or the local station group address specified in the slave address field is received. Table 4-8 indicates the SLRC return codes for broadcast reception.

Table 4-8   SLRC Return Codes for Broadcast Reception

SLRC	Description
1000	1. **Meaning**: Broadcast reception is started.
	2. **Occurrence condition**: ① A broadcast frame up to the data-length field was received from the master unit normally. ② Once the control field has been received, RBF is ready for reception**Note**. After the data-length field, 1000 is set in SLRC, and three-byte data consisting of a master address, control bits, and data-length bits is set in RBF.
	3. **Microcomputer processing**: Three-byte data consisting of a master address, control bits, and data-length bits can be read from RBF.
1001	1. **Meaning**: The broadcast reception buffer is full.
	2. **Occurrence condition**: This return code is issued when RBF becomes full during data reception as a slave unit, preventing subsequent reception data from being set in RBF.
	3. **Microcomputer processing**: If data consisting of one or more bytes is not read from RBF within the time below, broadcast reception is aborted. • Reception data read time: Approx. 1570 μs (mode 0) Approx. 390 μs (mode 1)
1010	1. **Meaning**: Broadcast reception was terminated normally.
	2. **Occurrence condition**: This return code is issued when as much data as the amount specified in the data-length field has been received normally in a communication frame. In this case, the SLRE flag of the FLG register changes from 1 to 0.
	3. **Microcomputer processing**: Reception data can be read from RBF, and the number of bytes of broadcast reception data can be read from RDR2.
1011	1. **Meaning**: Broadcast reception was aborted.
	2. **Occurrence condition**: This return code is issued when reception is terminated prior to the reception of as much data as the amount specified in the data-length field in a communication frame. In this case, the SLRE flag of the FLG register changes from 1 to 0.
	3. **Microcomputer processing**: Reception data can be read from RBF, and the number of bytes of broadcast reception data can be read from RDR2.

Note   See **Note** of Table 4-9.

[SLRC occurrence interval]

(a) When slave data transmission is performed

Return codes for broadcast reception, slave data transmission, and slave reception | Return codes for slave data transmission | Return codes for broadcast reception, slave data transmission, and slave reception
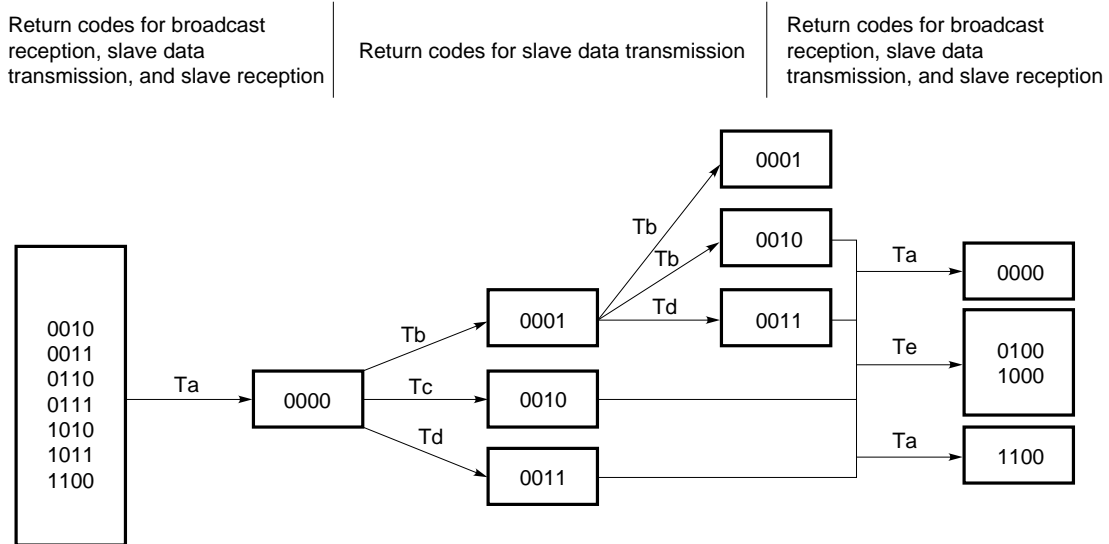
Table 4-10   Minimum Return Code Occurrence Interval for Slave Data Transmission

Interval	Mode 0	Mode 1
Ta	Approx. 5420 μs	Approx. 1490 μs
Tb	Approx. 1570 μs	Approx. 390 μs
Tc	Approx. 3140 μs	Approx. 780 μs
Td	Approx. 20 μs	Approx. 20 μs
Te	Approx. 7150 μs	Approx. 1920 μs

IRQ

(b) When slave reception is performed

Return codes for broadcast reception, slave data transmission, and slave reception

Return codes for slave reception

Return codes for broadcast reception, slave data transmission, and slave reception
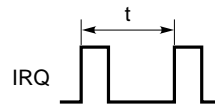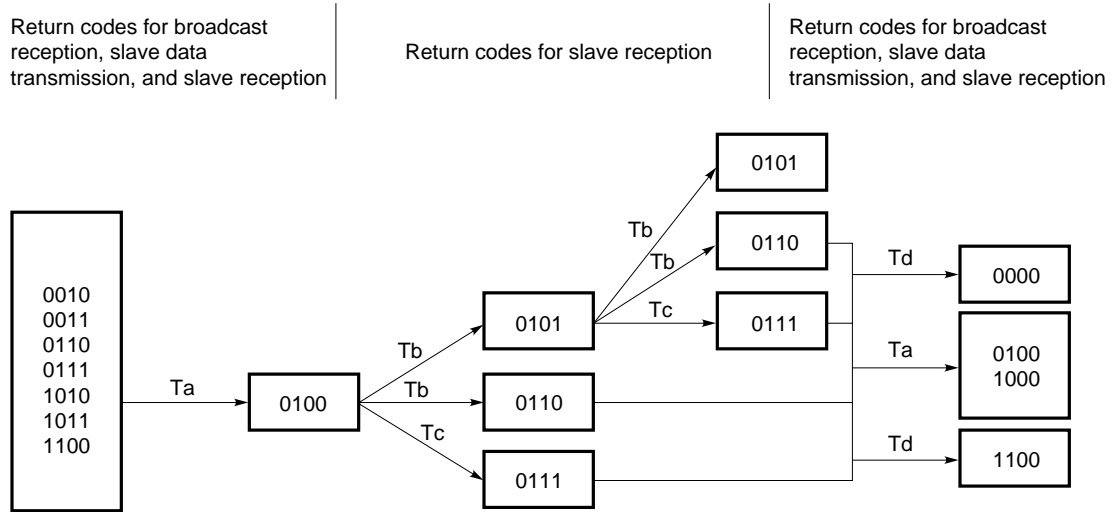
Table 4-11   Minimum Return Code Occurrence Interval for Slave Reception

Interval	Mode 0	Mode 1
Ta	Approx. 7150 μs	Approx. 1920 μs
Tb	Approx. 1570 μs	Approx. 390 μs
Tc	Approx. 20 μs	Approx. 20 μs
Td	Approx. 5420 μs	Approx. 1490 μs

(c) When broadcast reception is performed

Return codes for broadcast
reception, slave data
transmission, and slave reception │ Return codes for broadcast reception │ Return codes for broadcast
reception, slave data
transmission, and slave reception
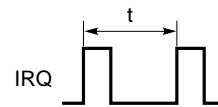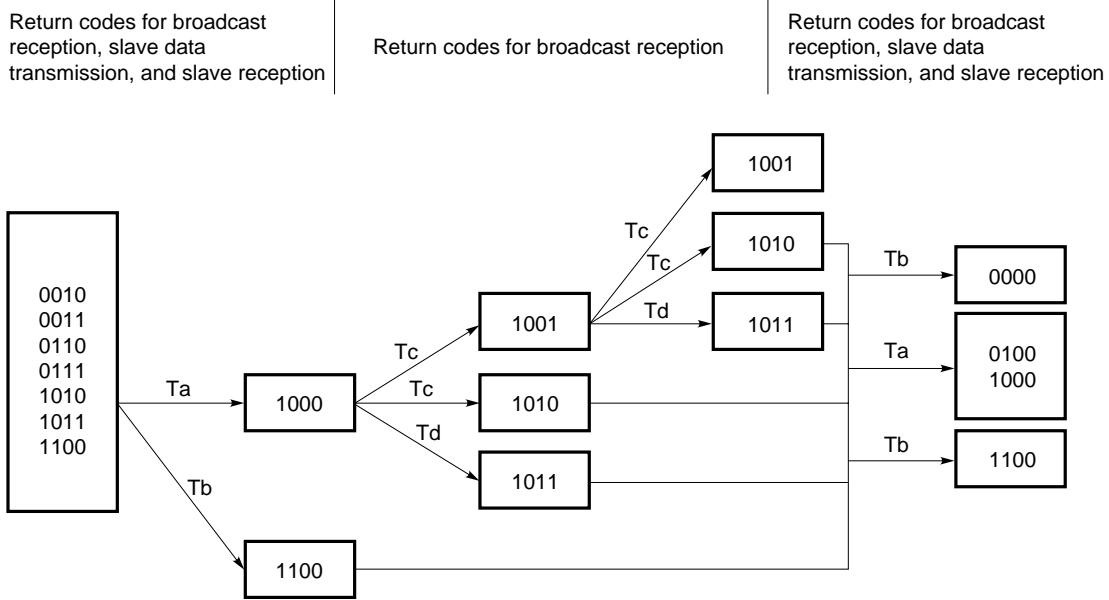
Table 4-12   Minimum Return Code Occurrence Interval for Broadcast Reception

Interval	Mode 0	Mode 1
Ta	Approx. 7150 μs	Approx. 1920 μs
Tb	Approx. 5420 μs	Approx. 1490 μs
Tc	Approx. 1570 μs	Approx. 390 μs
Td	Approx. 20 μs	Approx. 20 μs
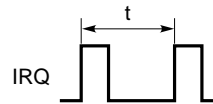
RBF	Address : 1110B (EH)
	Read/write : Read
Reception buffer	When reset : Undefined

RBF is a 40-byte FIFO buffer used to hold a transmitter address, control bits, data-length bits, and reception data for master reception, slave reception, or broadcast reception.

RBF can be read by the microcomputer when the REP flag of the STR register is 0 (indicating that RBF is not empty).

When an optional function is set in the CMR register with MFC = 1, multiple communication frames can be held in RBF until RBF becomes full.

In master reception, slave reception, and broadcast reception, the format below is used to transfer data from RBF to the microcomputer.

RBF

High-order 4 bits	Low-order 4 bits	
Byte 1	Transmitter address (high-order 8 bits)	
Byte 2	Transmitter address (low-order 4 bits)	Control bits
Byte 3	Data-length bits	
Byte 4	First byte of reception data	
Byte 5	Second byte of reception data	
⋮		Communication frame 1
Last reception data		
Transmitter address (high-order 8 bits)		
Transmitter address (low-order 4 bits)	Control bits	
Data-length bits		
First byte of reception data		
Second byte of reception data		
⋮		Communication frame 2
Last reception data		
⋮		
Byte 40		

[Byte 1, byte 2 (high-order 4 bits)]: Transmitter address

As indicated below, the transmitter address depends on whether the communication mode is master reception, slave reception, or broadcast reception.

- **Transmitter address**

Case	Transmitter address
Master reception	Slave address
Slave reception	Master address
Broadcast reception	

[Byte 2 (low-order 4 bits)] : Control bits

[Byte 3] : Data-length bits

[Byte 4 and up] : Reception data

The number of bytes of reception data is set in the RDR1 or RDR2 register, as described below.

RDR1: Number of bytes of reception data in master reception

RDR2: Number of bytes of reception data in slave reception or broadcast reception

The number of bytes of reception data indicates the number of bytes of data received normally within a communication frame. This means that the number of bytes of reception data will match the length set in the data-length field of a communication frame only when the data has been received normally.

5. EXAMPLE TIMINGS FOR COMMUNICATION

This chapter provides examples of the timings at which the contents of internal registers change during communication. The following seven examples are given:

(1) Master transmission timing example 1
Timing at which a return code is generated upon the start of master transmission and at the normal termination of transmission

(2) Master transmission timing example 2
Timing at which a return code is generated upon the start of master transmission, transmission data empty, and the suspension of transmission

(3) Slave data transmission timing example
Timing at which a return code is generated upon the start of slave data transmission and the normal termination of transmission

(4) Master reception timing example
Timing at which a return code is generated upon the start of master reception and the normal termination of reception

(5) Slave reception timing example 1
Timing at which a return code is generated upon the start of slave reception and the normal termination of reception
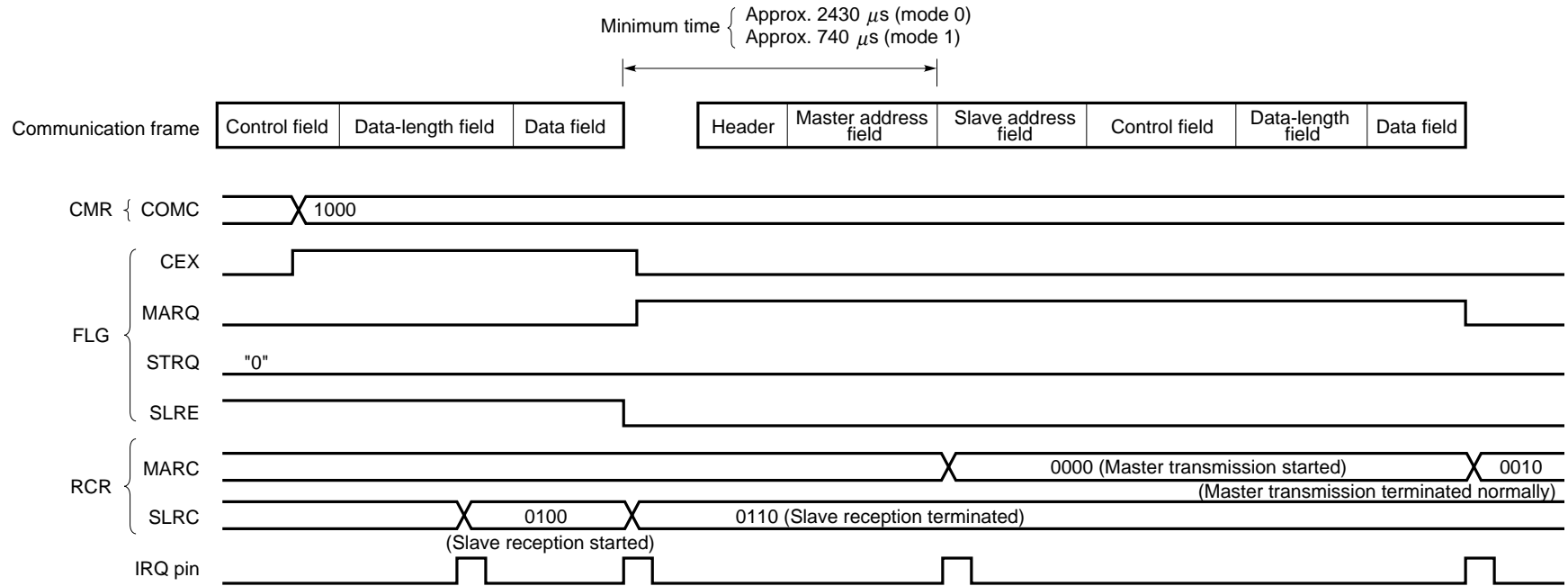
(6) Slave reception timing example 2
Timing at which a return code is generated upon the start of slave reception, reception buffer full, and the normal termination of reception
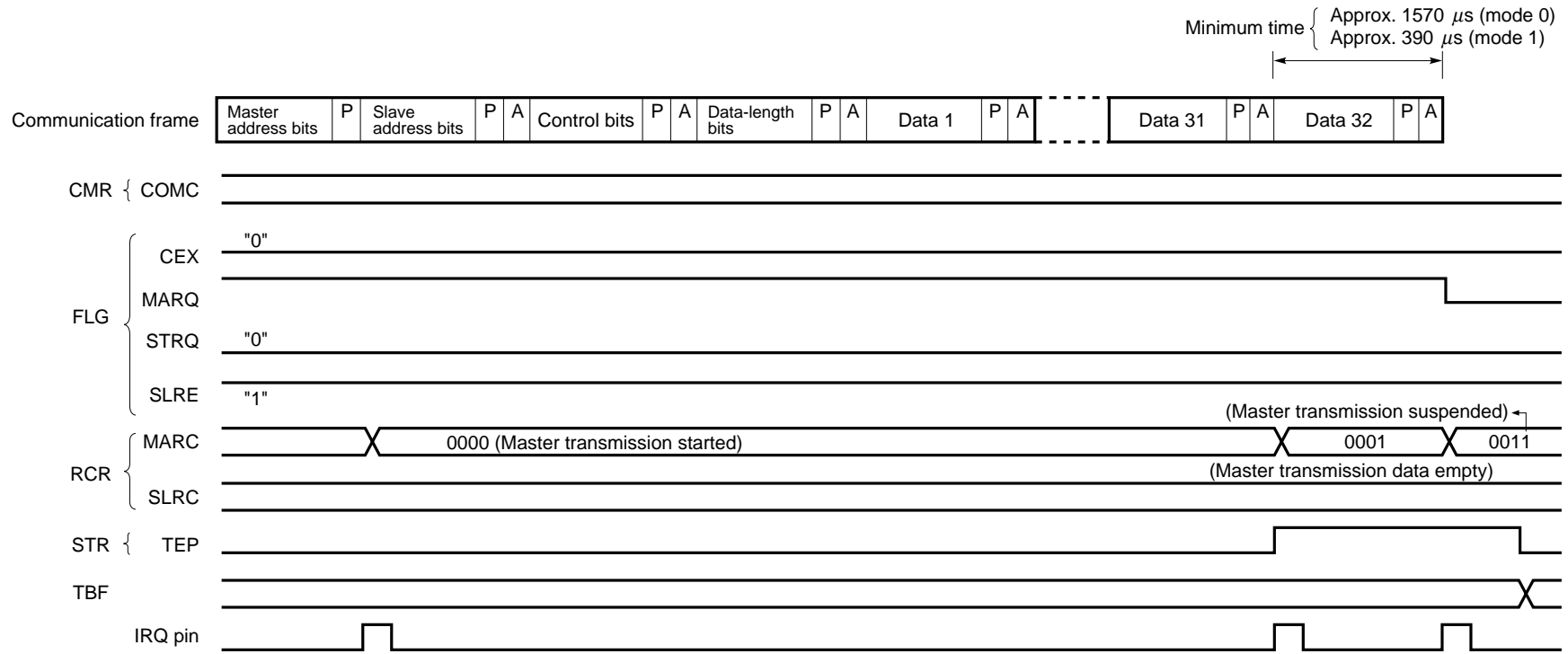
(7) Broadcast reception timing example
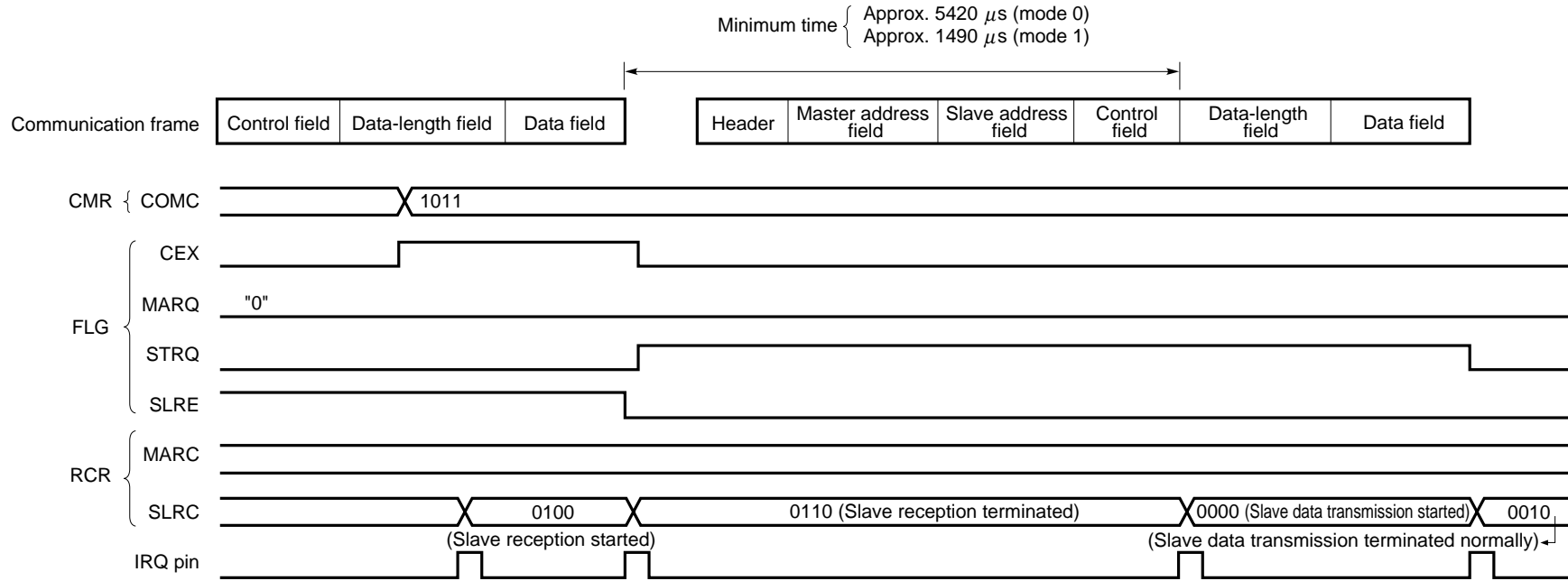Timing at which a return code is generated upon the occurrence of an error during broadcast reception

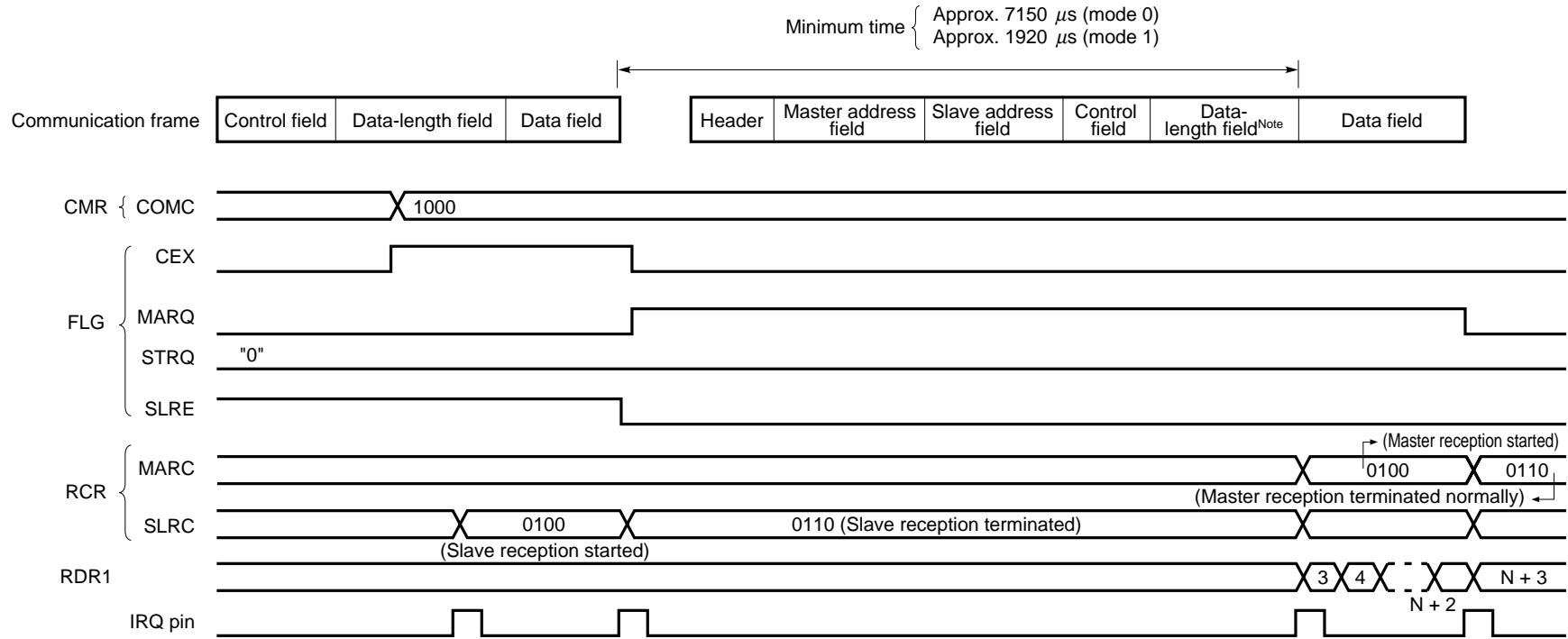**(1) Master transmission timing example 1**

(2) Master transmission timing example 2

Minimum time $\left\{\begin{array}{l}\text{Approx. 1570 }\mu\text{s (mode 0)}\\\text{Approx. 390 }\mu\text{s (mode 1)}\end{array}\right.$

Communication frame

| Master address bits | P | Slave address bits | P | A | Control bits | P | A | Data-length bits | P | A | Data 1 | P | A | | Data 31 | P | A | Data 32 | P | A |

CMR $\{$ COMC

FLG $\{$
- CEX "0"
- MARQ
- STRQ "0"
- SLRE "1"

RCR $\{$
- MARC 0000 (Master transmission started) 0001 0011
- SLRC

(Master transmission suspended)
(Master transmission data empty)

STR $\{$ TEP

TBF

IRQ pin

(3) Slave data transmission timing example

Minimum time { Approx. 5420 µs (mode 0) / Approx. 1490 µs (mode 1)

Communication frame:

| Control field | Data-length field | Data field | | Header | Master address field | Slave address field | Control field | Data-length field | Data field |

CMR { COMC   1011

FLG {

CEX

MARQ   "0"

STRQ

SLRE

RCR {

MARC

SLRC   0100 (Slave reception started)   0110 (Slave reception terminated)   0000 (Slave data transmission started)   0010

IRQ pin   (Slave reception started)   (Slave data transmission terminated normally)

(4) Master reception timing example

Minimum time { Approx. 7150 μs (mode 0) / Approx. 1920 μs (mode 1)

Note Data-length bit: N

(5) Slave reception timing example 1

Minimum time { Approx. 5260 μs (mode 0) / Approx. 1450 μs (mode 1)

Communication frame

| Control field | Data-length field | Data field |

| Header | Master address field | Slave address field | Control field | Data-length field | Data field |

Separate frame (data-length bits: N1)

Broadcast frame (data-length bits: N2)

CTR { REEN

FLG {
CEX "0"
MARQ "0"
STRQ "0"
SLRE

RCR {
MARC
SLRC   1000   1010 (Broadcast reception terminated normally)   0100   0110
(Slave reception started)

RDR2
(Broadcast reception started)
3 4 N1 + 3
N1 + 2
(Slave reception terminated normally)
3 4 N2 + 3
N2 + 2

IRQ pin

(6) Slave reception timing example 2

Minimum time { Approx. 1570 μs (mode 0) / Approx. 390 μs (mode 1) }

Communication frame: Data-length bits: 24 | P | A 0 | Data 1 | P | A 0 | ... | Data 22 | P | A 0 | Data 23 | P | A 1 | Data 23 | P | A 0 | Data 24 (last) | P | A 0

ACK — ACK — ACK — NAK — ACK — ACK

CMR { LOCK

CEX

FLG { MARQ "0", STRQ "0", SLRE

RCR { MARC, SLRC — 0100 (Slave reception started) — 0101 (Slave reception buffer full) — 0110 (Slave reception terminated normally)

STR { RFL

LOR1, LOR2 — Lock address

RBF

IRQ pin

(7) Broadcast reception timing example

Minimum time
{ Approx. 5420 μs (mode 0)
Approx. 1490 μs (mode 1) }

Communication frame

| Control field | Data-length field | Data field | | Header | Master address field | Slave address field | Control field |

Separate frame

Broadcast frame

CTR { REEN   "0"

FLG {
CEX   "0"
MARQ   "0"
STRQ   "0"
SLRE
}

RCR {
MARC
SLRC   0100   0110 (Slave reception terminated normally)   1100 (Broadcast reception error)
(Slave reception started)
}

STR { RFL

DAR1, DAR2   Master address

IRQ pin

6. EXAMPLE MICROCOMPUTER PROCESSING FLOW

This chapter provides an example of the processing flow for controlling the μPD72042 from the microcomputer. The main parts of this example processing flow are the following two routines:

• **Main routine**

Performs processing based on the communication flags set by the interrupt routine.

• **Interrupt routine**

Sets the communication flags by reading the statuses of the μPD72042 upon the issue of an interrupt request.

6.1 COMMUNICATION FLAGS

Table 6-1 lists the communication flags used in the main and interrupt routines, excluding those flags assigned to the registers of the μPD72042.

Table 6-1 Communication Flags

Name	Description
RAWF	Program crash detection flag (1: Detected, 0: Not detected)
TRRQ	Transmission processing request flag (1: Requested, 0: Not requested)
TRCF	Transmission status (TRC stored)
I	Number of bytes in transmission data set in TBF
RERQ**Note**	Reception processing request flag (1: Requested, 0: Not requested)
RECF**Note**	Reception status (REC stored)
SIZE**Note**	Number of bytes in reception data which can be read from RBF (RDR1/RDR2 stored)
PW**Note**	Write pointer for RERQ, RECF, and SIZE
PR**Note**	Read pointer for RERQ, RECF, and SIZE
J	Number of bytes in reception data which has actually been read from RBF
MCRQ	Master communication processing request flag (1: Requested, 0: Not requested)
SDRQ	Slave data transmission processing request flag (1: Requested, 0: Not requested)
CORQ	Command processing request flag (1: Requested, 0: Not requested)
MTRQF	Master transmission request flag (1: Requested, 0: Not requested)
MRRQF	Master reception request flag (1: Requested, 0: Not requested)
STRQF	Slave data transmission request flag (1: Requested, 0: Not requested)
SLREF	Slave broadcast reception enable flag (1: Enabled, 0: Disabled)

Note RERQ, RECF, and SIZE are stored in a buffer pair pointed to by PW and PR.

- **Buffer configuration**

Pointer	RERQ	RECF	SIZE
0			
1			
⋮			

Remark Buffers pointed to by the write pointer (PW) : RERQ$_W$, RECF$_W$, and SIZE$_W$
Buffers pointed to by the read pointer (PR) : RERQ$_R$, RECF$_R$, and SIZE$_R$

6.2 MAIN ROUTINE

Fig. 6-1 shows the processing flow of the main routine.

Fig. 6-1   Processing Flow of Main Routine
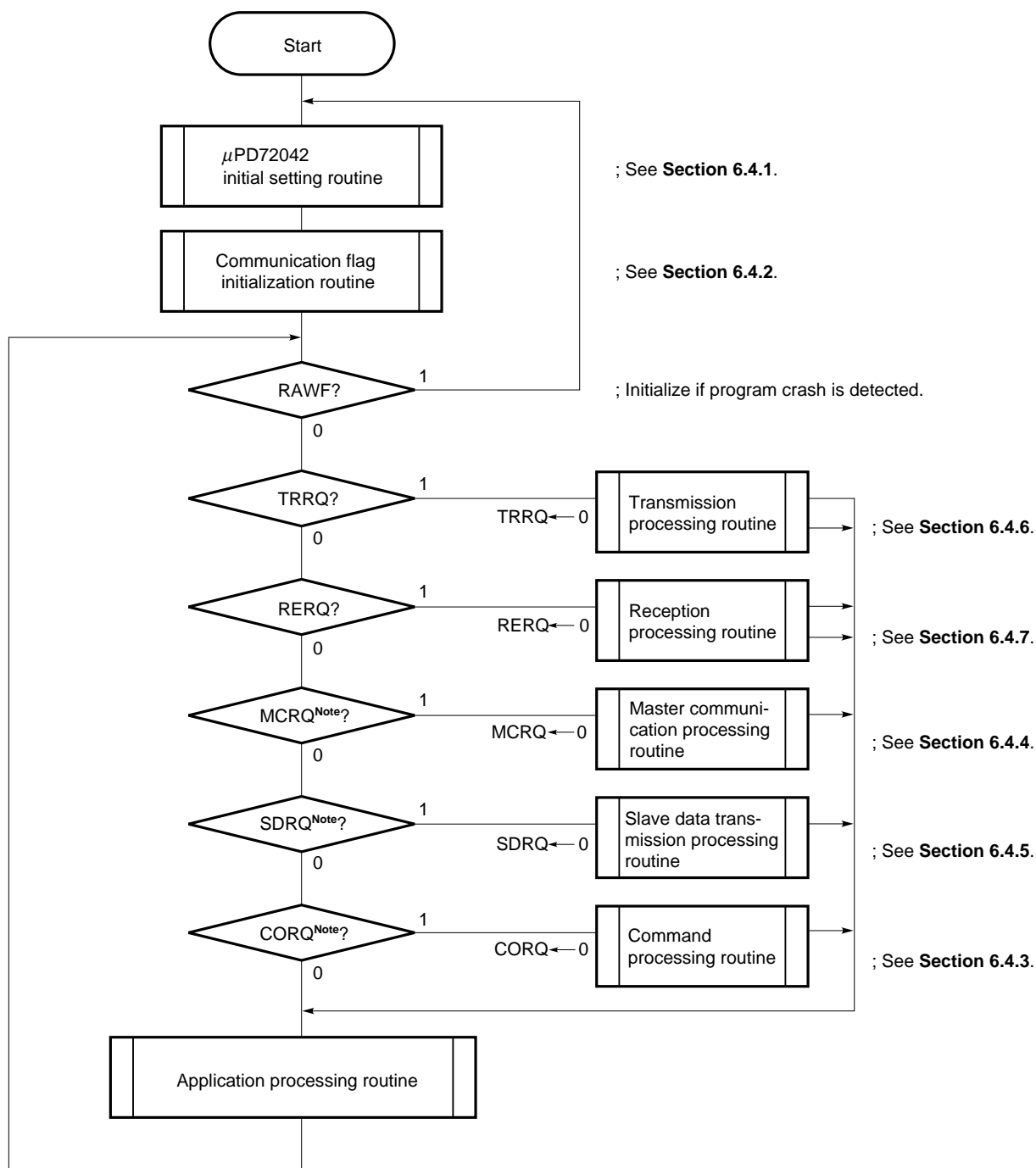
Note   Communication flags MCRQ, SDRQ, and CORQ are set to 1 by the application processing routine.

6.3   INTERRUPT ROUTINE

The interrupt routine performs the required processing when an interrupt request is issued from the µPD72042.

The interrupt routine disables the interrupts received from the µPD72042, reads the statuses (FLG and RCR registers) of the µPD72042, and sets the communication flags to be used by the main routine.

To enable the handling of an interrupt request which may occur while the interrupts from the µPD72042 are disabled, do not clear the interrupt flags such that such a request can be detected upon the completion of the interrupt routine processing (see **Fig. 6-2**).

Fig. 6-2   Operation when an Interrupt Occurs during Execution of Interrupt Routine
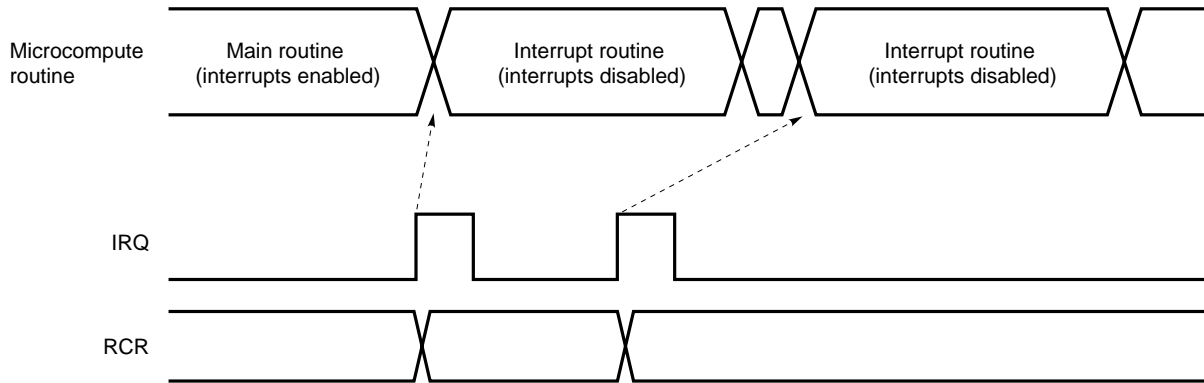
Fig. 6-3   Flow of Interrupt Routine

Start

Disable interrupts from
μPD72042

Read FLG

RAW?   ; Program crash?
1
0

RAWF ← 1

Read RCR

Is return code in MARC enabled?   ; See **Note 1**.
N
Y

MARC?   ; Classify MARC.
00×× | 010× | 011×

TRCF ← MARC
TRRQ ← 1

RERQw ← 1
SIZEw ← RDR1
RECFw ← MARC

RERQw ← 1
SIZEw ← RDR1
RECFw ← MARC

Increment PW
RERQw ← 0   ; Initialize RERQ.
SIZEw ← 0   ; Initialize SIZE.

Is return code in SLRC enabled?   ; See **Note 2**.
N
Y

SLRC?   ; Classify SLRC.
00×× | 010×, 100× | 011×, 101×

TRCF ← SLRC
TRRQ ← 1

RERQw ← 1
SIZEw ← RDR2
RECFw ← SLRC

RERQw ← 1
SIZEw ← RDR2
RECFw ← SLRC

REEN ← 1

Increment PW
RERQw ← 0   ; Initialize RERQ.
SIZEw ← 0   ; Initialize SIZE.

Enable interrupts from
μPD72042

RETI

End

Notes 1. The return code in MARC is enabled when any of conditions, ①, ②, or ③, below, is satisfied:
　　① MARC has been changed**Note 3**.
　　② MTRQF = 1 and MARQ = 0
　　③ MRRQF = 1 and MARQ = 0
2. The return code in SLRC is enabled when any of conditions, ①, ②, or ③, below, is satisfied:
　　① SLRC has been changed**Note 3**.
　　② STRQF = 1 and STRQ = 0
　　③ SLREF = 1 and SLRE = 0
3. When MARC is 0001 or 0101, the same value may be generated consecutively, such that MARC is set to 1111 to enable the detection of a change in MARC the next time it is generated. When SLRC is 0001, 0101, or 1001, it is again set to 1111 for the same reason.

6.4 PROCESSING ROUTINES

This section describes the processing routines called from the main routine.

6.4.1 μPD72042 Initial Setting Routine

This routine is executed when the μPD72042 is first started or upon the detection of a program crash (RAW = 1).

Fig. 6-4 shows the flow of the μPD72042 initial setting routine.

Fig. 6-4 μPD72042 Initial Setting Routine
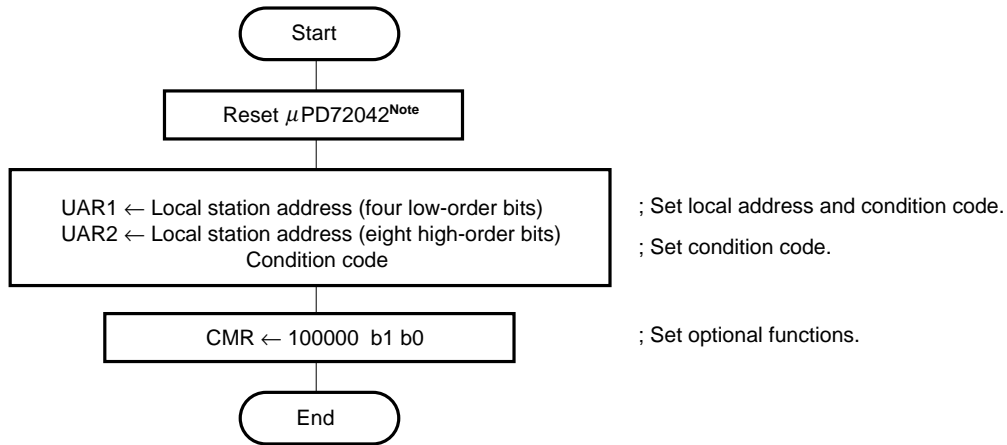
Note There are two methods of performing reset, as follows:
  ① Set the $\overline{\text{RESET}}$ pin to low.
  ② Set SRST in CTR to 1.
  Type ① reset causes the μPD72042 to enter standby mode, thus requiring the subsequent release of standby mode.

Caution   To enable normal IEBus communication, always perform the above initial setting.

6.4.2 Communication Flag Initialization Routine

This routine initializes the communication flags listed in Table 6-1, as follows:

RAWF $\leftarrow$ 0
TRRQ$_W$ $\leftarrow$ 0
RERQ$_W$ $\leftarrow$ 0
SIZE$_W$ $\leftarrow$ 0
J $\leftarrow$ 1
PW $\leftarrow$ 0
PR $\leftarrow$ 0
MCRQ $\leftarrow$ 0
SDRQ $\leftarrow$ 0
CORQ $\leftarrow$ 0
MTRQF $\leftarrow$ 0
MRRQF $\leftarrow$ 0
STRQF $\leftarrow$ 0
SLREF $\leftarrow$ 0

6.4.3 Command Processing Routine

This routine is executed when CORQ has been set by the application processing routine.

The command processing routine sets a command code, in the CMR register, to set the lock state, control transmission/reception buffers, control communication, and set optional functions.

The commands for master communication and slave data transmission request are described in **Sections 6.4.4** and **6.4.5**.

Fig. 6-5 shows the flow of the command processing routine.

Fig. 6-5   Command Processing Routine
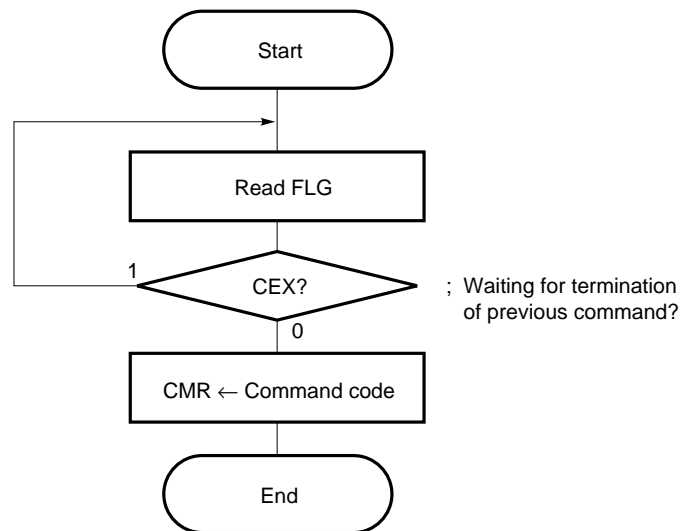
6.4.4 Master Communication Processing Routine

This routine is executed when MCRQ has been set by the application processing routine.

The master communication processing routine consists of the following three processing routines:

• **Master transmission processing routine 1**

This routine is used to transmit data, as the master unit, starting from the first data in TBF.

• **Master transmission processing routine 2**

This routine is used to start master transmission from the point at which the previous master transmission was suspended.

• **Master reception processing routine**

This routine is used to receive data, as the master unit, from a slave unit.

NEC

(1) Master transmission processing routine 1

Fig. 6-6 shows the flow of master transmission processing routine 1.

Fig. 6-6   Flow of Master Transmission Processing Routine 1
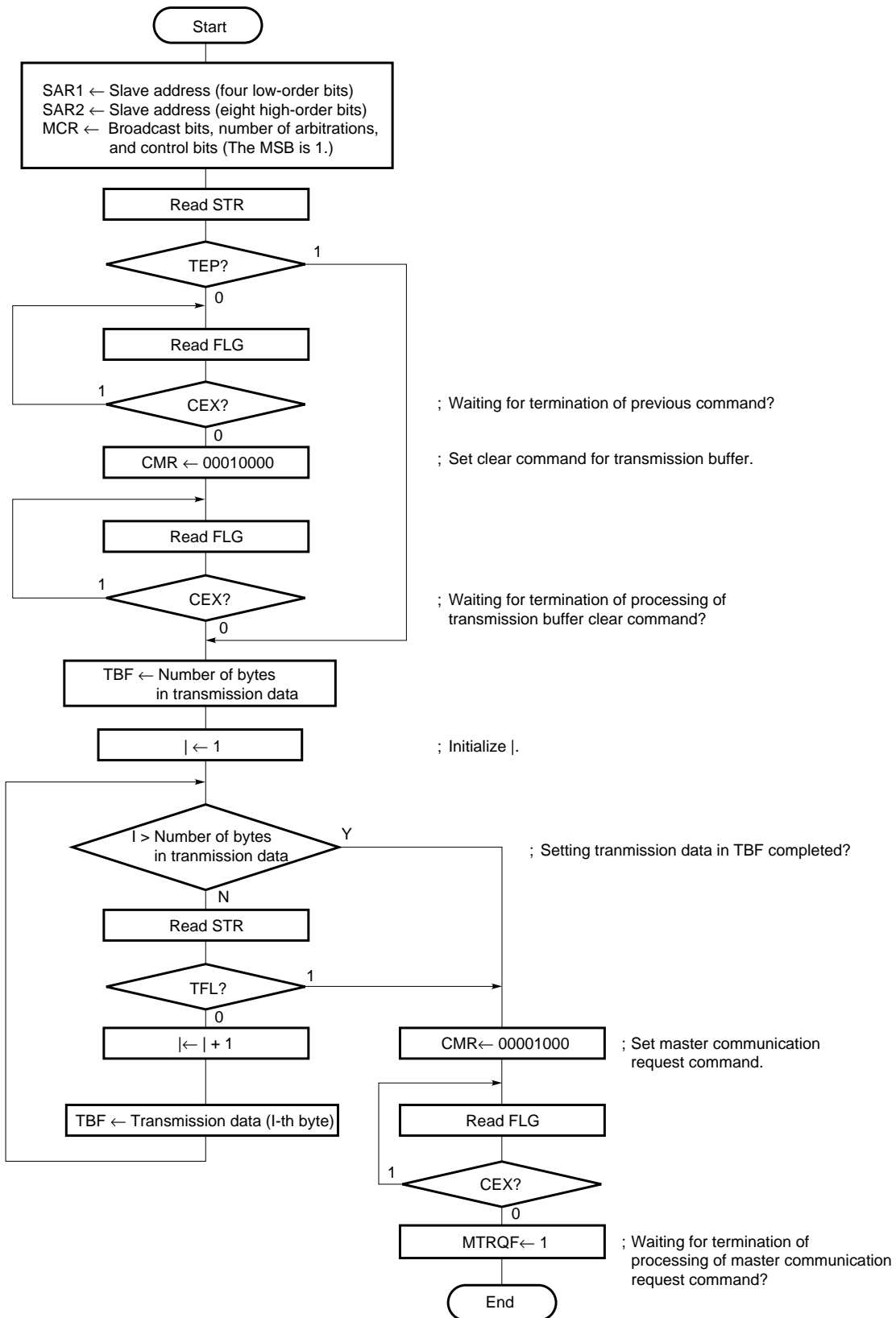
(2) Master transmission processing routine 2

Fig. 6-7 shows the flow of master transmission processing routine 2.

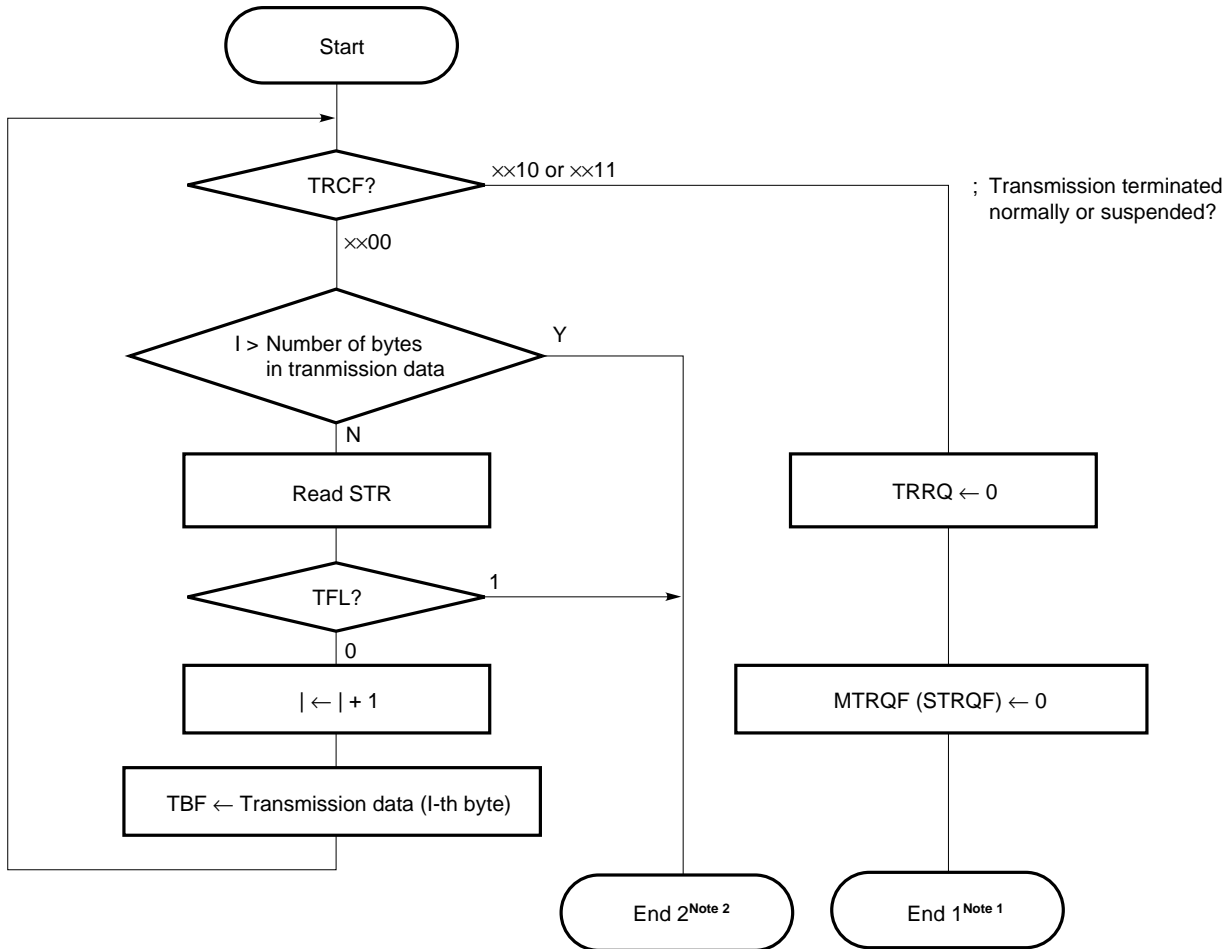**Fig. 6-7   Flow of Master Transmission Processing Routine 2**
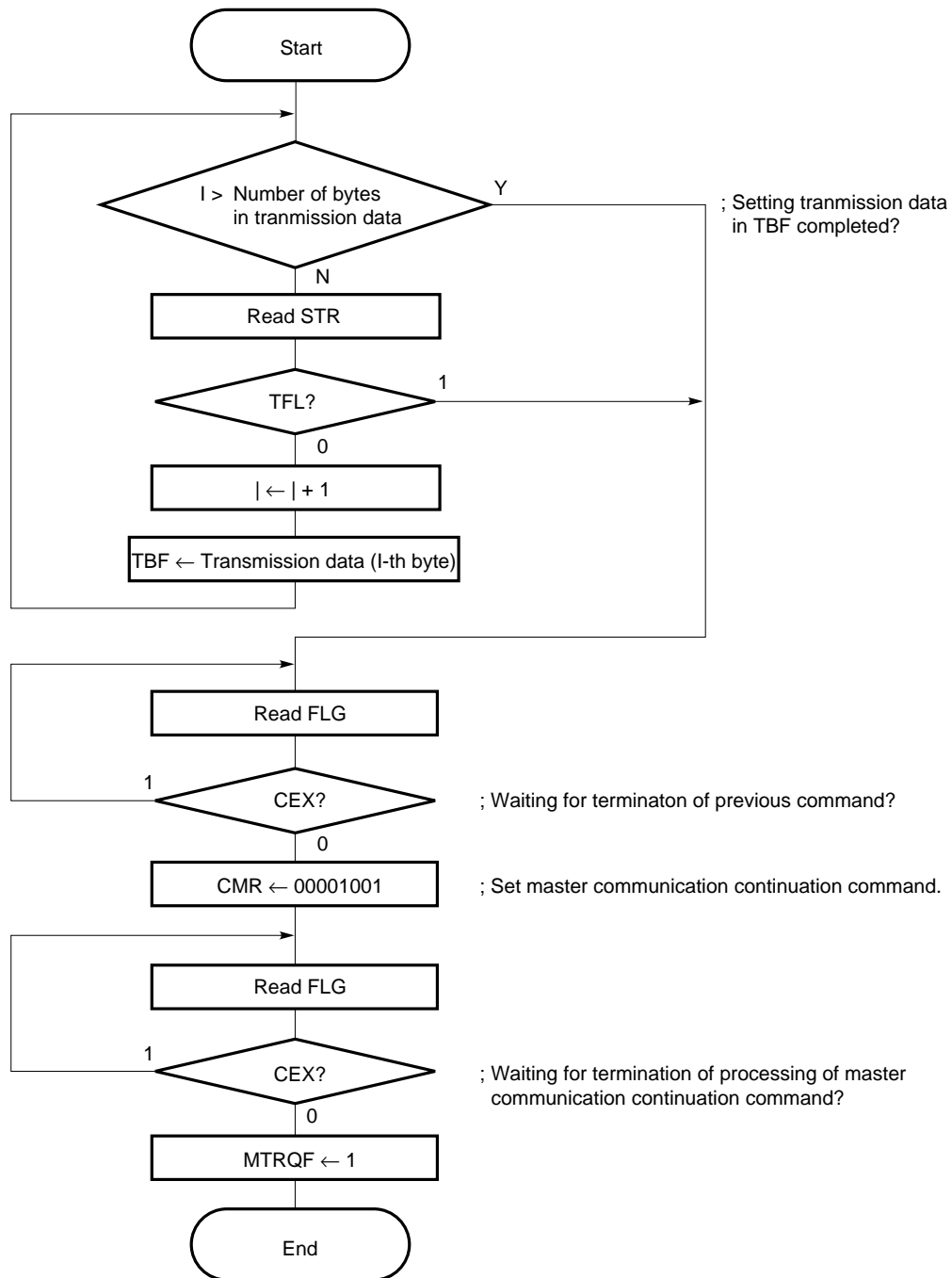
(3) Master reception processing routine

Fig. 6-8 shows the flow of the master reception processing routine.

Fig. 6-8   Flow of Master Reception Processing Routine

```
                        ┌──────────────┐
                        │    Start     │
                        └──────────────┘
                               │
        ┌────────────────────────────────────────────┐
        │ SAR1 ← Slave address (four low-order bits)   │   ; Set data only when changing
        │ SAR2 ← Slave address (eight high-order bits) │     SAR1, SAR2, or MCR.
        │ MCR  ← Broadcast bits, number of arbitrations,│
        │        and control bits (The MSB is 0.)      │
        └────────────────────────────────────────────┘
                               │
        ┌──────────────────────────────┐
   ┌───▶│          Read FLG             │
   │    └──────────────────────────────┘
   │                   │
   │  1         ◇ CEX? ◇                   ; Waiting for termination of previous command?
   └───────────       │
                     0 │
        ┌──────────────────────────────┐
        │   CMR ← 00001000              │   ; Set master communication request command.
        └──────────────────────────────┘
                               │
        ┌──────────────────────────────┐
   ┌───▶│          Read FLG             │
   │    └──────────────────────────────┘
   │                   │
   │  1         ◇ CEX? ◇                   ; Waiting for termination of processing of
   └───────────       │                      master communication request command?
                     0 │
        ┌──────────────────────────────┐
        │   MRRQF ← 1                   │
        └──────────────────────────────┘
                               │
                        ┌──────────────┐
                        │     End      │
                        └──────────────┘
```

6.4.5 Slave Data Transmission Processing Routine
This routine is executed when SDRQ has been set by the application processing routine.
The slave data transmission processing routine consists of the following two processing routines:

- **Slave data transmission processing routine 1**
  This routine is used to transmit data, starting from the first data in TBF, when requested from the master unit.

- **Slave data transmission processing routine 2**
  This routine is used to start slave data transmission from the point at which the previous slave data transmission was suspended.

(1) Slave data transmission processing routine 1
Fig. 6-9 shows the flow of slave data transmission processing routine 1.

Fig. 6-9 Flow of Slave Data Transmission Processing Routine 1
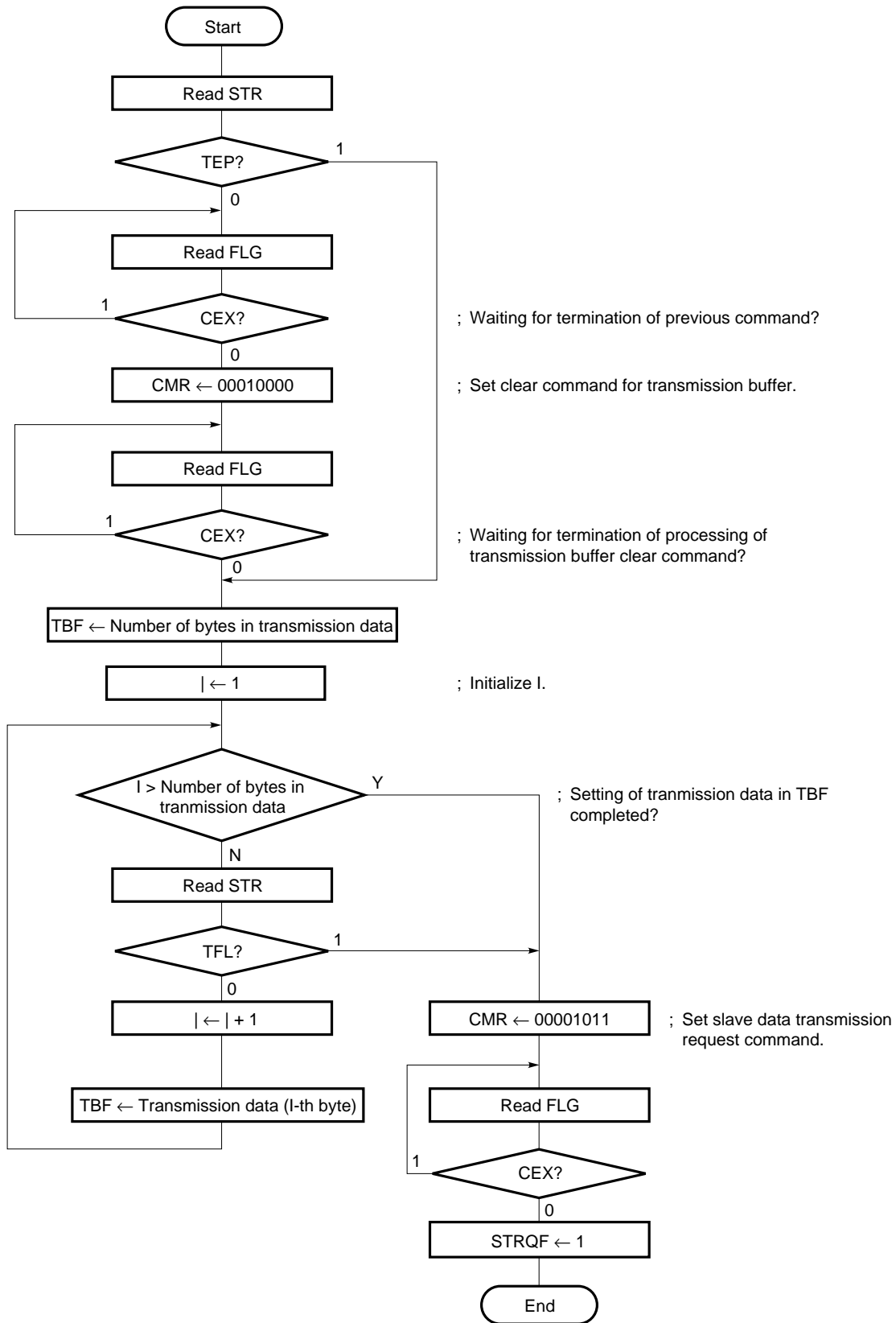
(2) Slave data transmission processing routine 2

Fig. 6-10 shows the flow of slave data transmission processing routine 2.

Fig. 6-10   Flow of Slave Data Transmission Processing Routine 2
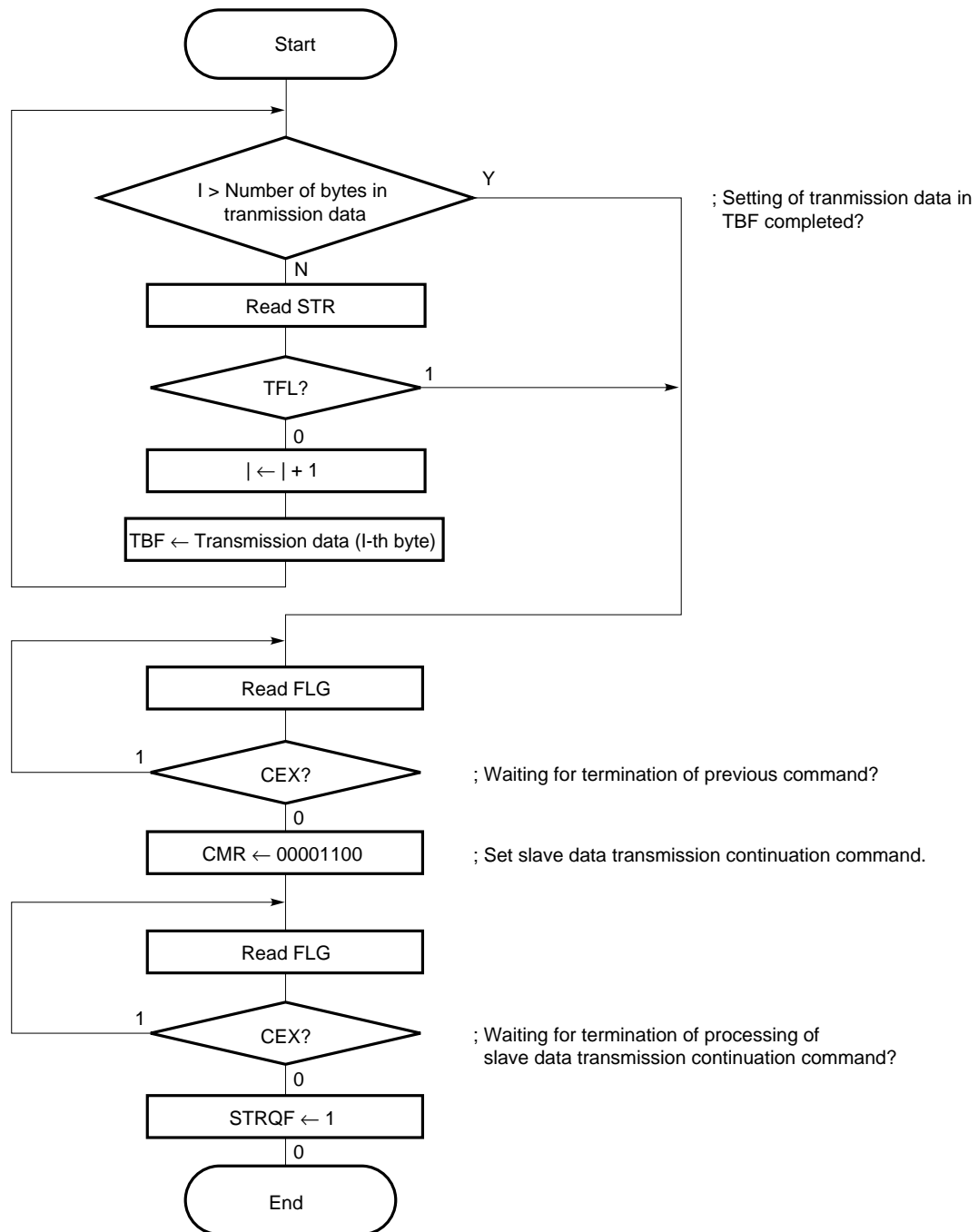
6.4.6 Transmission Processing Routine

This routine is executed when TRRQ has been set by the interrupt routine during the execution of master transmission processing routine 1 (see **6.4.4 (1)**), master transmission processing routine 2 (see **6.4.4 (2)**), or the slave data transmission processing routine (see **6.4.5**).

Fig. 6-11 shows the flow of the transmission processing routine.

Fig. 6-11   Flow of Transmission Processing Routine

Notes 1. Indicates that transmission of the communication frame has ended (terminated normally or suspended).

2. Indicates that setting of the transmission data has been completed with the current TBF.

6.4.7 Reception Processing Routine

This routine is executed when RERQ has been set by the interrupt routine.

Fig. 6-12 shows the flow of the reception processing routine.

Fig. 6-12   Flow of Reception Processing Routine
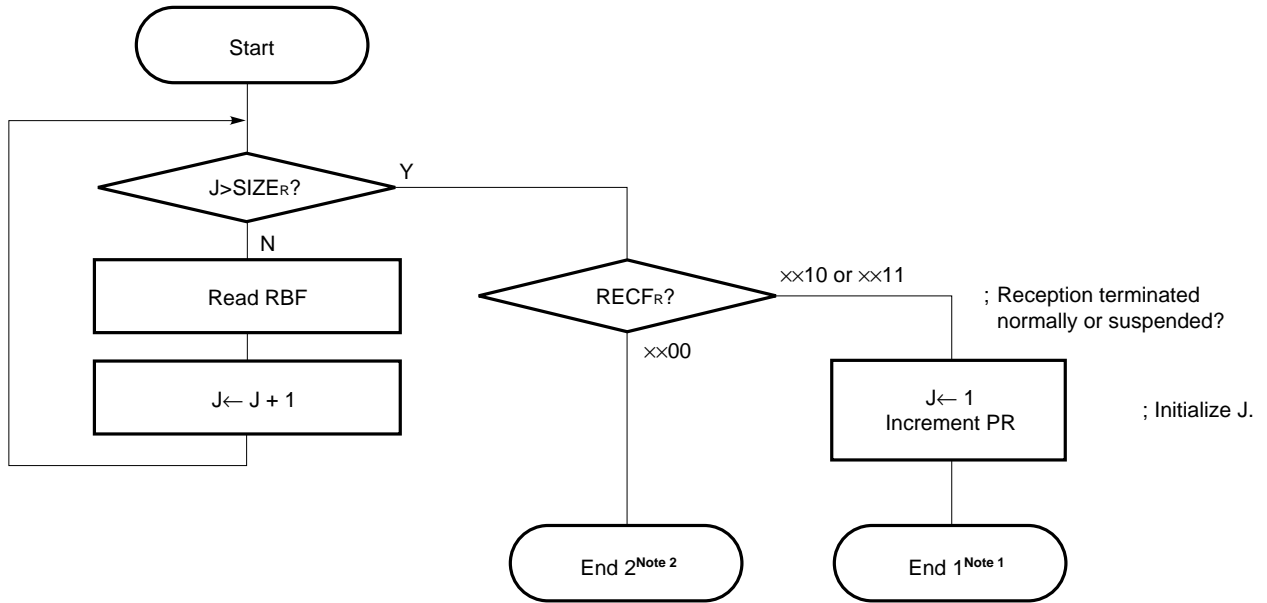
Notes 1. Indicates that reception of the communication frame has ended (terminated normally or suspended).
    2. Indicates that reading of the reception data has been completed with the current RBF.

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Rated value	Unit
Supply voltage	V_{DD}, AV_{DD}	$\mid V_{DD} - AV_{DD} \mid$ < 0.5 V	−0.5 to +7.0	V
Input voltage for logic section	V_I		−0.5 to V_{DD} + 0.3	V
Output voltage for logic section	V_O		−0.5 to V_{DD} + 0.3	V
Bus input voltage	V_{BI}		−0.5 to +6.0	V
Bus output voltage	V_{BO}		−0.5 to +6.0	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{STG}		−65 to +150	°C

Caution **Absolute maximum ratings are rated values beyond which physical damage may be caused to the unit; if any of the parameters in the table above exceeds its rated value, even momentarily, the performance and/or reliability of the product may deteriorate. Therefore, never exceed the product's rated values.**

DC CHARACTERISTICS (T_A = −40 to +85°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}		$0.8V_{DD}$		V_{DD}	V
Input low voltage	V_{IL}		0		$0.2V_{DD}$	V
Output high voltage	V_{OH}	I_{OH} = −400 μA	$0.7V_{DD}$			V
Output low voltage	V_{OL}	I_{OL} = 2.5 mA			0.4	V
Input leakage current, high	I_{LIH}	V_I = V_{DD}			10	μA
Input leakage current, low	I_{LIL}	V_I = 0 V			−10	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}			10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V			−10	μA
Supply current (normal operation mode)	I_{DD1}			3.5	10	mA
Supply current (standby mode)	I_{DD2}				50	μA

CAPACITANCE CHARACTERISTICS (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_I	f_C = 1 MHz Excluding the BUS+ and BUS- pins. 0 V for pins others than the measured pins.			15	pF
I/O capacitance	C_{IO}				15	pF

AC CHARACTERISTICS (T_A = −40 to +85°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
System clock			5.91	6.00	6.09	MHz
$\overline{SCK}$ cycle time	t_{KCY}		0.8			µs
$\overline{SCK}$ high-level width	t_{KH}		0.4			µs
$\overline{SCK}$ low-level width	t_{KL}		0.4			µs
SI (SIO)[Note 1] setup time	t_{SIK}	Referred to $\overline{SCK}\uparrow$	100			ns
SI (SIO)[Note 1] hold time	t_{KSI}	Referred to $\overline{SCK}\uparrow$	400			ns
SO (SIO)[Note 2] output delay	t_{KSO}	Referred to $\overline{SCK}\downarrow$			300	ns
$\overline{CS}$, C/$\overline{D}$ setup time	t_{SA}	Referred to $\overline{SCK}\downarrow$	50			ns
$\overline{CS}$, C/$\overline{D}$ hold time	t_{HA}	Referred to $\overline{SCK}\uparrow$	400			ns
IRQ output high-level width			8		11	µs
$\overline{RESET}$ low-level width			6			µs

SERIAL TRANSFER TIMING
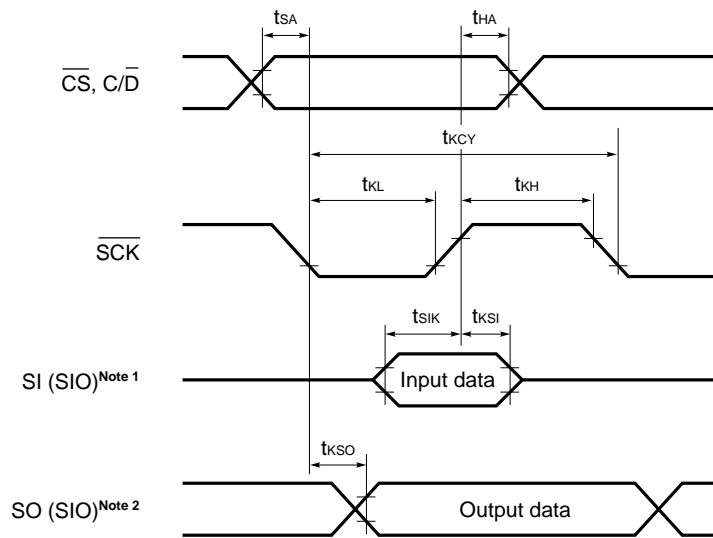
Notes 1. For 3-wire serial I/O: SI
       For 2-wire serial I/O: SIO
     2. For 3-wire serial I/O: SO
       For 2-wire serial I/O: SIO

Oscillator circuit (External system clock)
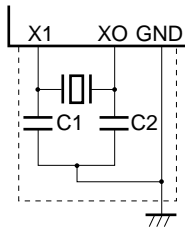
Caution When using system clock oscillator, wire the portion enclosed in broken lines in the figure as follows to avoid adverse influences on the wiring capacitance:
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over the other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as GND.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillator.**

IEBus DRIVER/RECEIVER CHARACTERISTICS (T_A = −40 to +85°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output high voltage	I_{ON}	R_L = 60 Ω ±5%	2.73		6.22	mA
Output low voltage	I_{OL}				1.0	μA
Common mode output voltage	V_{OCOM}	For high and low levels X = 1/2V_{DD}	X−0.25	1/2V_{DD}	X+0.25	V
Input high voltage	V_{IH}		120			mV
Input low voltage	V_{IL}				20.0	mV
Input hysteresis voltage	V_{IHYS}			25		mV
Common mode input voltage, high	V_{IHCOM}		1.00		V_{DD}−1.0	V
Common mode input voltage, low	V_{ILCOM}		0		V_{DD}	V
Driver output resistance	R_O	Between BUS+ and BUS−	100			kΩ
Driver output capacitance	C_O	Between BUS+ and BUS−, between BUS+ and GND, and between BUS− and GND			25	pF
Receiver input capacitance	C_I				25	pF

Circuit connected to IEBus
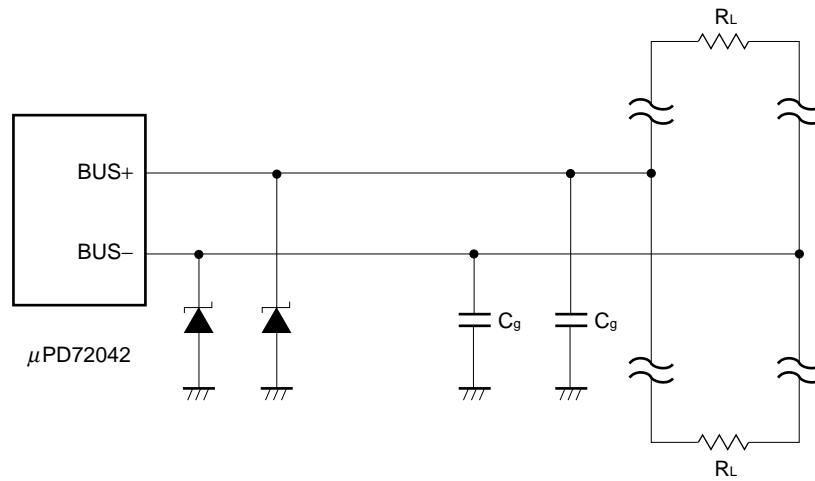
Remark Terminating resistor $R_L = 120\ \Omega \pm 5\%$
Load capacitor C_g

Please use the capacitor on the bus line under 7000 pF (between the BUS+ pin and BUS– pin)
Therefore, the total load capacitance C_T between the BUS+ pin and BUS– pin is as follows.

$$C_T = \sum^{N} \frac{1}{2}\ C_g + C_W \qquad\qquad C_W:\ \text{Wiring capacitance}$$

Cautions 1. The circuit constants in the above figure are applied when each unit connected to the IEBus line uses the μPD72042.
2. Do not insert inductive parts into the bus line.

8. PACKAGE DRAWING

16-PIN PLASTIC SOP (9.53 mm (375))

detail of lead end
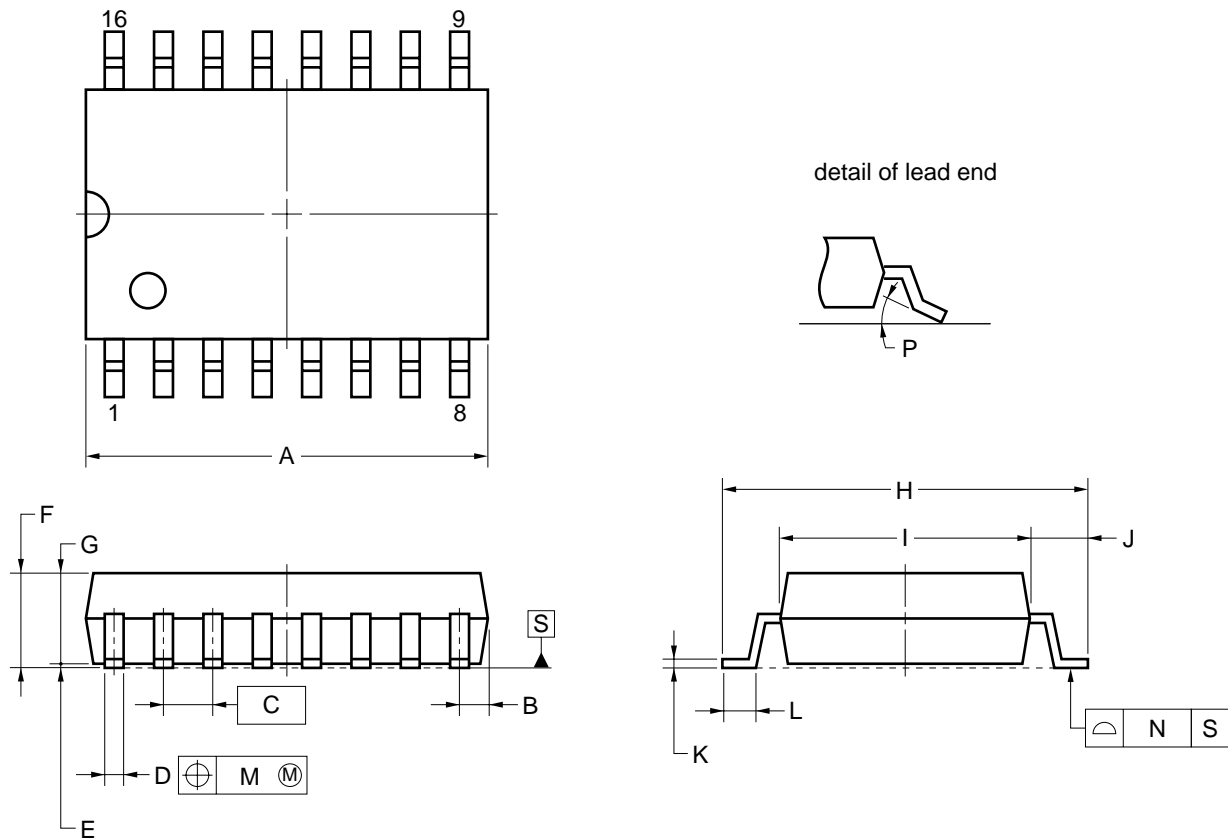
NOTE

Each lead centerline is located within 0.12 mm of
its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	10.2±0.26
B	0.805 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.125±0.075
F	2.9 MAX.
G	2.50±0.2
H	10.3±0.3
I	7.2±0.2
J	1.6±0.2
K	$0.17^{+0.08}_{-0.07}$
L	0.8±0.2
M	0.12
N	0.10
P	$3°^{+7°}_{-3°}$

P16GT-50-375B-2

9. RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Surface mount devices

μ**PD72042GT: 16-pin plastic SOP (9.53 mm (375))**

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 235 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 2 times.	IR35-00-2
VPS	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 2 times.	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature).	WS60-00-1
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

Caution   Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

APPENDIX A MAIN DIFFERENCES BETWEEN *µ*PD72042, *µ*PD72042B, AND *µ*PD6708

Item Product	*µ*PD72042A	*µ*PD72042B	*µ*PD6708
Oscillation frequency (f$_X$)	6 MHz		12 MHz
Operating voltage (V$_{DD}$)	5 V ±10%		
Operating ambient temperature (T$_A$)	−40 to +85°C		
IEBus Communication mode	Mode 0, 1		Mode 0, 1, 2
Driver/receiver	Built-in		
Protective register	Not reguired	180 Ω ±5%	Not reguired
Transmission buffer	33 bytes		4 bytes
Reception buffer	40 bytes		20 bytes
Interface with microcomputer**Note**	Serial interface (3-wire/2-wire)		Serial interface (3-wire)
	MSB first	LSB first	MSB first
Package	16-pin plastic SOP (9.53 mm (375))		16-pin plastic SOP (7.62 mm (300)) 16-pin plastic DIP (7.62 mm (300))

Note   The setting method for the commands, data, and related pins for the *µ*PD72042 and *µ*PD72042B differs from that for the *µ*PD6708.

APPENDIX B IEBus PROTOCOL ANALYZER

Naito Densei Co., Ltd. offers an IEBus protocol analyzer for monitoring communication on IEBus and evaluating application systems. For details of its functions and to place an order, contact:

Naito Densei Machida Mfg. Co., Ltd.
3-9-25, Hisamoto, Takatsu-ku
Kawasaki, Kanagawa 213-0011, JAPAN
TEL   044 (822) 3813
FAX 044 (822) 3681

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─── **NOTES FOR CMOS DEVICES** ───

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

IEBus and Inter Equipment are trademarks of NEC Corporation.