Product Brief
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microelectronics group

Lucent Technologies
Bell Labs Innovations

CelXpres™ T8206
Asynchronous Transfer Mode (ATM) Interconnect

Features

- UTOPIA cell-level handshake interface (ATM or PHY layers)
- Multi-PHY (MPHY) operation
- Programmable ATM layer supports up to 16 PHY ports
- Egress SDRAM buffer support to extend UTOPIA output priority queues for 32K to 512K cells:
  — 32 queues configurable up to four queues per PHY with programmable sizes
  — Programmable number of UTOPIA output queues with four levels of priority
- Support of ATM traffic management via partial packet discard (PPD), forward explicit congestion notification (FECN), and the cell loss priority (CLP) bit
- Controlled slew rate GTL+ I/O:
  — Programmable as bus arbiter
  — >1.5 Gbit/s cell bus operation
- Flexible per virtual channel (VC) cell counters
- Cell header insertion with virtual path identifier (VPI) and virtual channel identifier (VCI) translation via external SRAM (up to 64K entries)
- Support of network node interface (NNI) and user network interface (UNI) header types with optional generic flow control (GFC) insertion
- Programmable operations and maintenance and resource management (OAM/RM) cell routing
- Support of multicast and broadcast addresses per PHY
- Optional monitoring of misrouted cells
- Microprocessor interface, supporting both *Motorola** and *Intel*† modes (multiplexed and nonmultiplexed)
- Control cell transmission and reception through microprocessor port
- Eight GPIO pins
- JTAG support
- Compatible with *Transwitch CellBus*‡
- Seamlessly extends *WildWire*™ central-site family to the backplane
- Single 3.3 V power supply
- 3.3 V TTL I/O (5 V tolerant)
- 272-pin plastic ball grid array (PBGA) package
- Industrial temperature range (–40 °C to +85 °C)

Applications

- Asymmetric digital subscriber line (ADSL) digital subscriber line access multiplexers (DSLAMs)
- Access gateways
- Access multiplexers/concentrators
- Multiservice platforms

Description

The *CelXpres* T8206 device meets the ATM Forum's universal test and operations PHY interface for ATM (UTOPIA) Level 1, version 2.01 and Level 2, version 1.0 specifications for cell-level handshake and MPHY data path operation. The T8206 supports MPHY operation with one transmit cell available (TxCLAV) signal and one receive cell available (RxCLAV) signal for up to 16 PHY ports. In addition to the required UTOPIA signals, the optional transmit parity (TxPRTY) and receive parity (RxPRTY) signals are provided.

* *Motorola* is a registered trademark of Motorola, Inc.
† *Intel* is a registered trademark of Intel Corporation.
‡ *Transwitch* and *CellBus* are registered trademark of Transwitch Corp.

Description (continued)

The *CelXpres* T8206 device integrates all of the required functionality to transport ATM cells across a backplane architecture with high-speed cell traffic exceeding 1.5 Gbits/s to a maximum of 32 destinations. The management of multiple service classes and monitoring of performance on ATM and PHY interfaces is incorporated in the device's functionality. Traffic delivery to multi-PHYs (MPHYs) is managed through the UTOPIA interface.

The T8206 may be configured as an ATM or PHY level device providing cell routing between UTOPIA and a 32-bit wide cell bus. In addition to the 32 data signals, the bus has the following signals:

- Read clock
- Write clock
- Frame sync
- Acknowledge

ATM cells arriving at the UTOPIA receive interface may get VPI and VCI translation and routing information from a look-up table in external SRAM. An external synchronous dynamic random access memory (SDRAM) is used to extend the buffering for ATM cells destined for the UTOPIA transmit interface. This external SDRAM may be partitioned into four or less independently sized queues per PHY. The four queues may be used to implement quality of service (QoS) using different priorities for each queue.

The *CelXpres* T8206 provides a shared UTOPIA mode, which allows two devices on different cell buses to share the same UTOPIA bus in ATM mode. Using a glueless interface, the two T8206 devices resolve queue priorities and arbitrate the use of the UTOPIA bus. This shared mode can be used to provide redundancy or increase the system capacity.

In addition, an external microprocessor may send or receive control or loopback cells through the microprocessor interface. The 8-bit microprocessor interface may be configured to be *Motorola* or *Intel* compatible and is used to configure and monitor the device.

Description (continued)

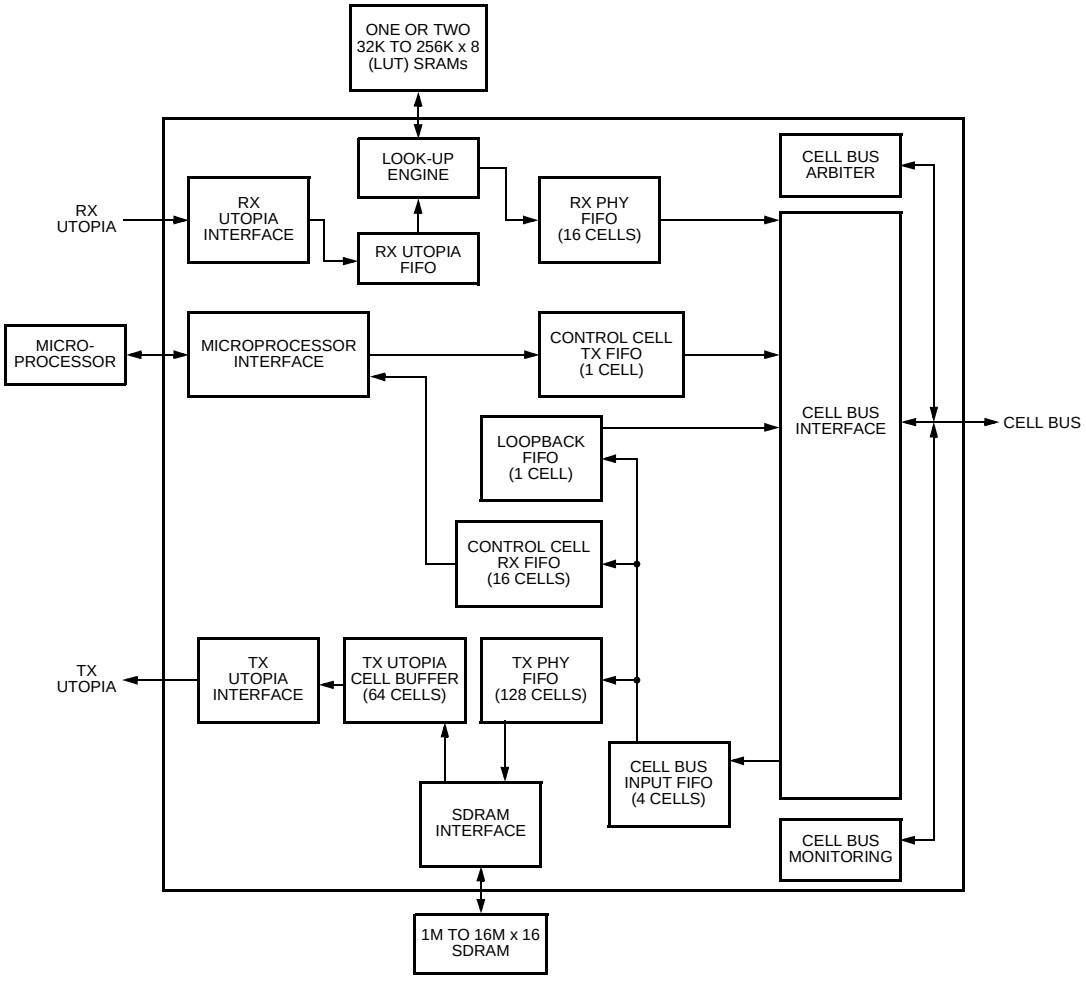

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Figure 1. Functional Block Diagram

Description (continued)

Figure 2 illustrates the use of the *CelXpres* T8206 in a system with dual backplane cell buses using shared UTOPIA mode. In this configuration, both T8206 devices on each card receive cells from the UTOPIA bus, and each device uses its translation table to determine if the cell should be transmitted on its backplane cell bus. In the egress direction, each T8206 device receives cells from its cell bus to transmit on the UTOPIA bus. Queue priorities are resolved using a two-wire interface between the two devices. Although a single ATM virtual connection cannot use both backplane cell buses simultaneously, no restrictions exist for a single PHY utilizing both backplane cell buses for different virtual connections. In the event of a bus failure, the T8206 devices may be configured for one device to assume bus responsibility from the other.

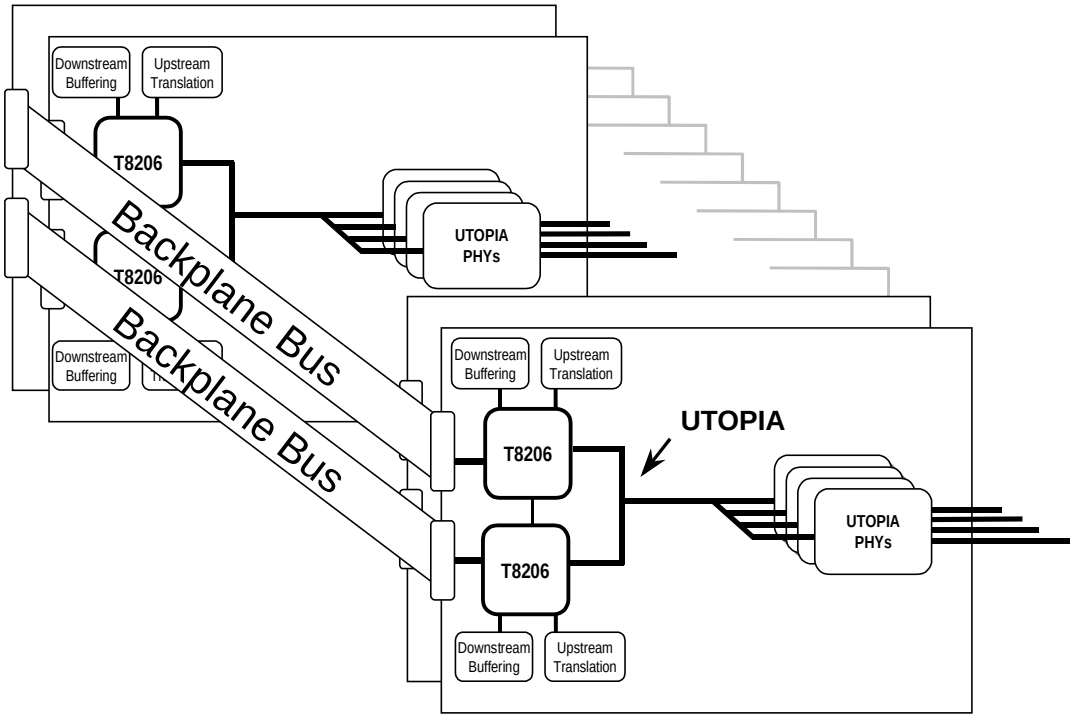

Figure 2. Dual Bus Implementation

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