PS2Adapt™ UR6HCPS2-SP40
Converts PS/2 Data to Serial or SPI

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HID & SYSTEM MANAGEMENT PRODUCTS, PROTOCOL INTERPRETER FAMILY

DESCRIPTION

The PS2Adapt™ UR6HCPS2-SP40 is an extremely low-power protocol interpreter that can link an AT / PS/2-compatible Human Input Device (HID), such as a keyboard, mouse, bar-code reader, etc. to any host system equipped with either an asynchronous serial interface or the Serial Peripheral Interface (SPI).

The IC was designed specifically for RISC-based portable devices that are limited to asynchronous and SPI interfaces. The PS2Adapt™ allows designers to easily connect PS/2 devices to their system.

The PS2Adapt™ emulates all the functions of the 8042 keyboard controller which typically resides on the AT / PS/2 motherboard. The extremely low-power PS2Adapt™ will power down even between key presses and bewteen mouse reports. Typical power consumption is only 1 µA operating between 3-5 Volts.

The extremely low-power boasts 4 external PS/2 ports that support the hot-plug connection of an external PS/2 keyboard or mouse, including MouseWheel, 5-button mice and touch screens in absolute mode.

Each of four external PS/2 ports also support more than 140 key scan codes including international language keys, internet keys, and power keys. The PS2Adapt™ also offers 4 reserved pins for LED functions.

FEATURES

- Typically consumes less than 1 µA
- Interfaces the host system via either an asynchronous serial interface or the Serial Peripheral Interface (SPI)
- Jumper selectable interface and Baud rate
- Offers four PS/2 ports for the hot-plug connection of external keyboards or mice including MouseWheel, 5-button mice and absolute mode touch screens
- Easy to use, one way communication protocol
- Operating voltage between 3 and 5 Volts
- Custom versions available in small or large quantities
- Tiny 7x7 mm package to accommodate slim designs

APPLICATIONS

- H/PCs
- Web phones
- PDAs
- System legacy support

PIN ASSIGNMENTS
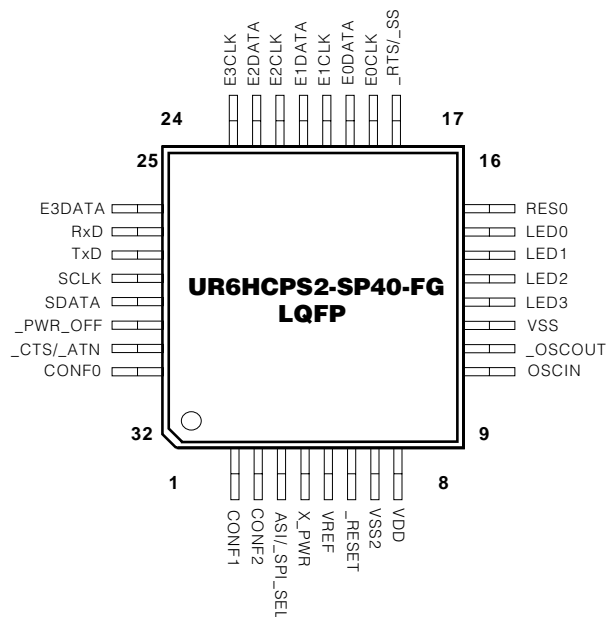
FUNCTIONAL DIAGRAM

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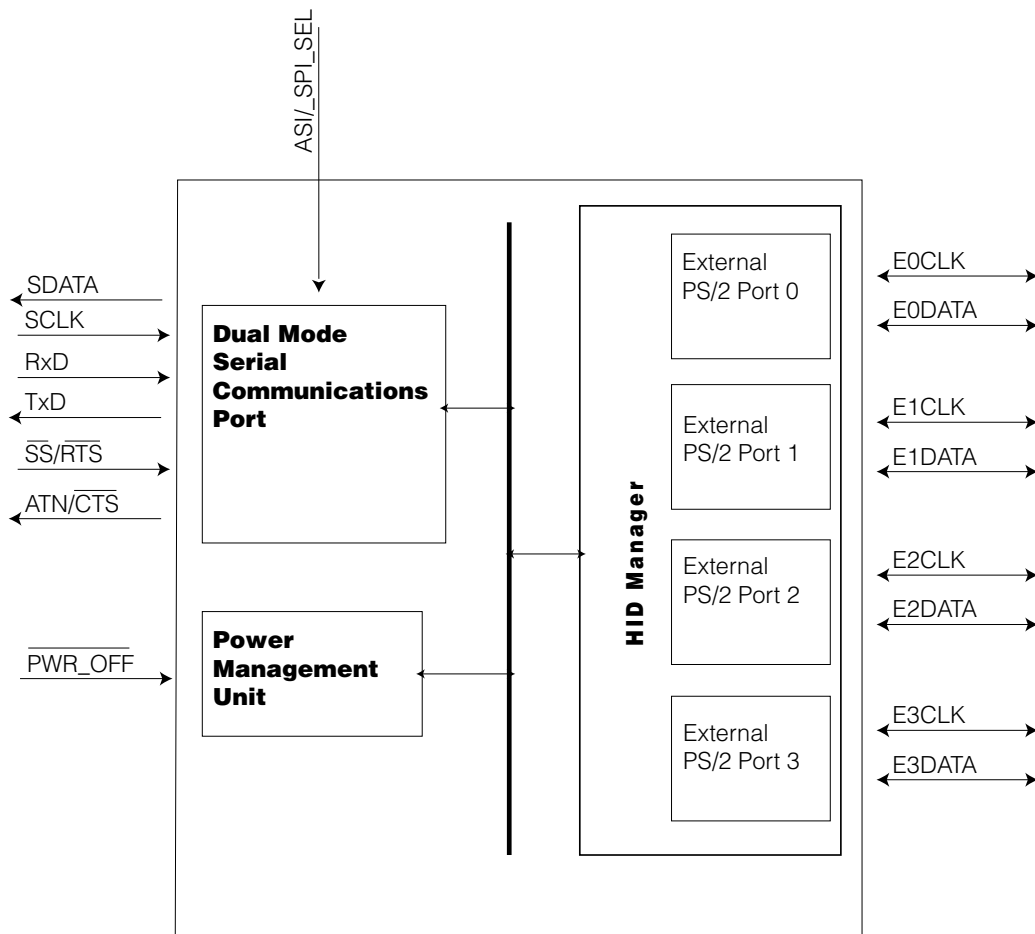
FUNCTIONAL DESCRIPTION

The PS2Adapt™ consists functionally of three major sections. These are the Dual Mode Serial Communications Interface, the Power Management Unit, and the HID Manager. All sections communicate with each other and operate concurrently.

HID MANAGER

The PS2Adapt™ Human Input Device (HID) Manager is responsible for the configuration and handling of HID devices that are attached to the controller through the four external PS/2 ports. The HID Manager has the following responsibilities:

1. Initialize PS/2 keyboards and mice

2. Mix the information from external PS/2 devices

3. Formatting and relaying reports of the HID devices to the Host.

OPERATIONS BELOW 5 V

The standard PS/2 devices are specified for supply voltage of 5V. Operations of the PS2Adapt™ at a lower voltage (3V) are only possible if the HID devices connected to ALL external PS/2 ports are capable of 3V operations.

PIN DEFINITIONS

Pin Numbers

Mnemonic	LQFP	Type	Name and Function
Power Supply			
VDD	8	PWR	**Positive supply voltage:** +3V-+5V
VREF	5	AI	**Positive analog ref voltage**
VSS	11	PWR	**Ground:** analog signal
VSS2	7	PWR	**Ground:** negative supply voltage
_RESET	6	I	**Hardware reset pin:** at lo level, this pin holds the F 2Adapt™ in a reset state.
Oscillator Pins			
OSCIN	9	I	**Oscillator input:** connect ceramic resonator with built-in load capacitors or CMOS clock from external oscillator 4 MHz operating frequency
_OSCOUT	10	O	**Oscillator output:** connect ceramic resonator with built-in load capacitors or keep open if external oscillator is used
PS/2 Ports			
E0CLK	18	I/nD	**PS/2 clock:** for external device 0
E0DATA	19	I/nD	**PS/2 data:** for external device 0
E1CLK	20	I/nD	**PS/2 clock:** for external device 1
E1DATA	21	I/nD	**PS/2 data:** for external device 1
E2CLK	22	I/nD	**PS/2 clock:** for external device 2
E2DATA	23	I/nD	**PS/2 data:** for external device 2
E3CLK	24	I/nD	**PS/2 clock:** for external device 3
E3DATA	25	I/nD	**PS/2 data:** for external device 3
System Status Monitoring			
_PWR_OFF	30	I±Int	**Power off signal:** capable of Interrupt on both positive and negative e ges
X_PWR	4	AI	**External PS/2 device power detector**
Communication Interface			
_SS/_RTS	17	I_Int	**Ready_To_Send:** Active low signal. Input low level indicates that the host system is ready to send data from PS2Adapt™.
_ATN/_CTS	31	O	**Attention (SPI mode) or Clear_To_Send (asynchronous serial mode):** Active low signal output. Low level indicates that the PS2Adapt™ has data to send to the host system.
TXD	27	O	**Transmit data (asynchronous serial mode):** Idle = "high" = 1
RXD	26	I	**Receive data (asynchronous serial mode):** Reserved for future use
SDATA	29	I	**Master-In-Slave-Out (SPI mode):** keep open for asynchronous mode or tie to ground
SCLK	28	I	**Serial Clock (SPI mode)**: in SPI mode, use the following Clock sequence:Idle-high/ negative-edge (shift data) \ positive-edge (latch data), idle-high. Keep open or tie to ground for asynchronous mode.

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PIN DEFINITIONS, (CON'T)

Pin Numbers

Mnemonic	LQFP	Type	Name and Function
Configuration Pins			
CONF0	32	I	Configuration pin 0; see Note 2
CONF1	1	I	Configuration pin 1; see Note 2
CONF2	2	I	Configuration pin 2; see Note 2
ASI/_SPI_SEL	3	I	SPI/Serial Selector pin. High:Serial;
Reserved for			
LED0	12	I/O	Reserved LED Driver / GPIO
LED1	13	I/O	Reserved LED Driver / GPIO
LED2	14	I/O	Reserved LED Driver / GPIO
LED3	15	I/O	Reserved LED Driver / GPIO
RES0	16	I/O	Reserved GPIO

Note 1: An underscore in front of the pin mnemonic denotes an active low signal.

Note 2: When asynchronous serial mode is selected, ASI/_SPI_SEL pin is high and pins CONF2:CONF1:CONF0 select the following Baud Rates:

> 111: 19200 bps; 110: 9600 bps; 101: 1200 bps; 100: 600 bps; 011: 300 bps
> 010: 31250 bps; 001: 62500 bps.

When SPI mode is selected, ASI/_SPI_SEL pin is low. If CONF0 is high, the transfer sequence is MSB to LSB, otherwise, LSB to MSB.

Note 3: For ASI/_SPI_SEL pin use the following setting:

1: Asynchronous Serial Mode; 0: Serial Peripheral Interface (SPI) mode

Note 4: In asynchronous mode, SDATA and SCLK are driven to low after reset. In SPI mode, TXD, RXD, CONF1 and CONF2 are driven to low after reset. In both asynchronous and SPI mode, LED0, LED1, LED2, LED3 and RES0 are configured as inputs with pull-up resistors.

Pin Types Legend: AI=Analog Input; I=Input; O=Output; I/O=Input or Output; I/nD=Input or Output with N-channel open drain driver;

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The PS2Adapt™ offers two modes of serial communications: Synchronous Peripheral Interface (SPI) mode and asynchronous serial mode.

The PS2Adapt™ determines the mode of communication with the host during power-up by reading the value of the ASI/_SPI_SEL pin. If the pin is tied high, asynchronous mode is enabled. If it is low, the SPI interface is enabled.

The PS2Adapt™ implements the SPI mode by single direction communication that supports bit rates up to 250 Kb/s. Several hosts and companion chips implement the SPI protocol in order to communicate with a wide range of peripherals such as EEPROMs, A/D converters, MCUs and other system components.

The PS2Adapt™ deploys the _ATN as an additional hand-shake signal in order to support low power operation of the bus.

The PS2Adapt™ implements asynchronous mode at fixed preselected baud rates: 300bps, 600bps, 1200bps, 9600bps, 19200bps, 31250bps and 62500bps, depending on the configuration pins' state on power up.
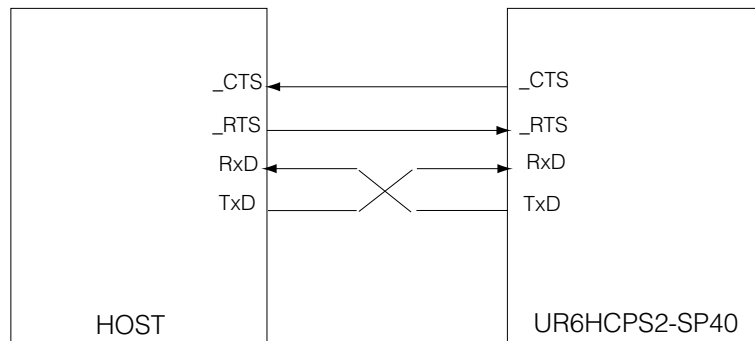
In asynchronous mode, the PS2Adapt™ deploys the _RTS & _CTS as additional hand-shake signals in order to support low power operation of the bus.

The diagrams below illustrate the SPI and asynchronous communications interfaces, respectively.

SPI Communications Interface

Asynchronous Communications Interface

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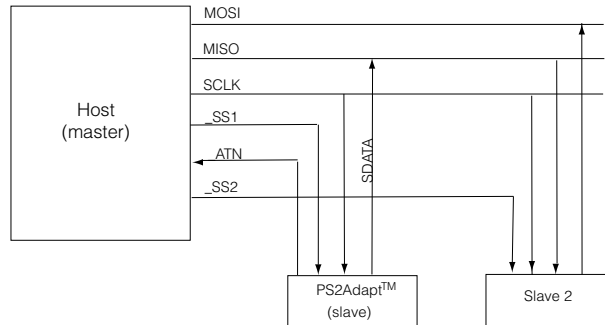
Overview

The PS2Adapt™ reports three types of packet formats for relative mouse, absolute mouse and keyboard report respectively.

Each mouse packet contains 4 bytes; each keyboard packet contains 2 bytes. The 7th bit of each byte is used for synchronization. The 7th bit for the first byte is 1 and for the other bytes is 0.

Keyboard Data Report

Each 8-bit key number (K0-K7) is an identification of a keyboard key, which is defined in the Semtech key table (see Page 7).

PS/2 Mouse Data Report

There are two different kinds of mouse data packages for the external PS/2 devices. One is absolute mode that is for touchscreens and the other is relative mode for standard PS/2 devices, including MouseWheel.

The resolution for the absolute mouse is 10 bits (1000 points) in each direction (X and Y).

The relative mouse data format accommodates data from 5-button and MouseWheel devices.

Keyboard Packet Format

					Bit Number			
Byte #	7	6	5	4	3	2	1	0
1	1	1 KBD	Not Assigned	Caps Lock 1:On /0:Off	Num Lock 1:On /0:Off	Scroll Lock 1:On /0:Off	1:Make /0:Break	K7
2	0	K6	K5	K4	K3	K2	K1	K0

Absolute Mode PS/2 Mouse Package Format

					Bit Number			
Byte #	7	6	5	4	3	2	1	0
1	1	0 Mouse	0 Absolute	0 1 penup	0 1 penup	0 1 penup	0 1 penup	0 1 penup
2	0	Y9	Y8	Y7	X*	X9	X8	X7
3	0	X6	X5	X4	X3	X2	X1	X0
4	0	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Note 4: The bits that are marked with X* are reserved for future use. Now the value given is zero.

Relative Mode PS/2 Mouse Package Format

					Bit Number			
Byte #	7	6	5	4	3	2	1	0
1	1	0 Mouse	1 Relative	Ysign	Xsign	M	R	L
2	0	X6	X5	X4	X3	X2	X1	X0
3	0	Y6	Y5	Y4	Y3	Y2	Y1	Y0
4	0	X*	B5	B4	Z3	Z2	Z1	Z0

Note 5: The bits that are marked with X* are reserved for future use. Now the value given is zero.

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Key Name	Key Number	PS/2 Set 1 Make	PS/2 Set 1 Break	PS/2 Set 2 Make	PS/2 Set 2 Break
No Event	0	None	None	None	None
Overrun Error	1	FF	None	0	None
POST Fail	2	FC	None	FC	None
ErrorUndefined	3	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
a A	4	1E	9E	1C	F0 1C
b B	5	30	B0	32	F0 32
c C	6	2E	AE	21	F0 21
d D	7	20	A0	23	F0 23
e E	8	12	92	24	F0 24
f F	9	21	A1	2B	F0 2B
g G	10	22	A2	34	F0 34
h H	11	23	A3	33	F0 33
i I	12	17	97	43	F0 43
j J	13	24	A4	3B	F0 3B
k K	14	25	A5	42	F0 42
l L	15	26	A6	4B	F0 4B
m M	16	32	B2	3A	F0 3A
n N	17	31	B1	31	F0 31
o O	18	18	98	44	F0 44
p P	19	19	99	4D	F0 4D
q Q	20	10	90	15	F0 15
r R	21	13	93	2D	F0 2D
s S	22	1F	9F	1B	F0 1B
t T	23	14	94	2C	F0 2C
u U	24	16	96	3C	F0 3C
v V	25	2F	AF	2A	F0 2A
w W	26	11	91	1D	F0 1D
x X	27	2D	AD	22	F0 22
y Y	28	15	95	35	F0 35
z Z	29	2C	AC	1A	F0 1A
1 !	30	2	82	16	F0 16
2 @	31	3	83	1E	F0 1E
3 #	32	4	84	26	F0 26
4 $	33	5	85	25	F0 25
5%	34	6	86	2E	F0 2E
6 ^	35	7	87	36	F0 36
7 &	36	8	88	3D	F0 3D
8 *	37	9	89	3E	F0 3E
9 (	38	0A	8A	46	F0 46
0)	39	0B	8B	45	F0 45
Return	40	1C	9C	5A	F0 5A
Escape	41	1	81	76	F0 76
Backspace	42	0E	8E	66	F0 66
Tab	43	0F	8F	0D	F0 0D
Space	44	39	B9	29	F0 29
-_	45	0C	8C	4E	F0 4E
= +	46	0D	8D	55	F0 55
[{	47	1A	9A	54	F0 54
] }	48	1B	9B	5B	F0 5B
\		49	2B	AB	5D	F0 5D
Europe 1 (Note 2)	50	2B	AB	5D	F0 5D
; :	51	27	A7	4C	F0 4C
' "	52	28	A8	52	F0 52
` ~	53	29	A9	0E	F0 0E

PS/2 SCAN CODE SETS ACCORDING TO THE KEY NUMBER

Key Name	USAR Key Number	PS/2 Set 1 Make	PS/2 Set 1 Break	PS/2 Set 2 Make	PS/2 Set 2 Break
, <	54	33	B3	41	F0 41
. >	55	34	B4	49	F0 49
/ ?	56	35	B5	4A	F0 4A
Caps Lock	57	3A	BA	58	F0 58
F1	58	3B	BB	5	F0 05
F2	59	3C	BC	6	F0 06
F3	60	3D	BD	4	F0 04
F4	61	3E	BE	0C	F0 0C
F5	62	3F	BF	3	F0 03
F6	63	40	C0	0B	F0 0B
F7	64	41	C1	83	F0 83
F8	65	42	C2	0A	F0 0A
F9	66	43	C3	1	F0 01
F10	67	44	C4	9	F0 09
F11	68	57	D7	78	F0 78
F12	69	58	D8	7	F0 07
Print Screen(Note 1)	70	E0 37	E0 B7	E0 7C	E0 F0 7C
Scroll Lock	71	46	C6	7E	F0 7E
Pause	72	E1 1D 45 E1 9D C5	None	E1 14 77 E1 F0 14 F0 77	None
Insert (Note 1)	73	E0 52	E0 D2	E0 70	E0 F0 70
Home (Note 1)	74	E0 47	E0 C7	E0 6C	E0 F0 6C
Page Up (Note 1)	75	E0 49	E0 C9	E0 7D	E0 F0 7D
Delete (Note 1)	76	E0 53	E0 D3	E0 71	E0 F0 71
End (Note 1)	77	E0 4F	E0 CF	E0 69	E0 F0 69
Page Down(Note 1)	78	E0 51	E0 D1	E0 7A	E0 F0 7A
Right Arrow (Note 1)	79	E0 4D	E0 CD	E0 74	E0 F0 74
Left Arrow (Note 1)	80	E0 4B	E0 CB	E0 6B	E0 F0 6B
Down Arrow(1)	81	E0 50	E0 D0	E0 72	E0 F0 72
Up Arrow (Note 1)	82	E0 48	E0 C8	E0 75	E0 F0 75
Num Lock	83	45	C5	77	F0 77
Keypad /(Note 1)	84	E0 35	E0 B5	E0 4A	E0 F0 4A
Keypad *	85	37	B7	7C	F0 7C
Keypad -	86	4A	CA	7B	F0 7B
Keypad +	87	4E	CE	79	F0 79
Keypad Enter	88	E0 1C	E0 9C	E0 5A	E0 F0 5A
Keypad 1 End	89	4F	CF	69	F0 69
Keypad 2 Down	90	50	D0	72	F0 72
Keypad 3 PageDn	91	51	D1	7A	F0 7A
Keypad 4 Left	92	4B	CB	6B	F0 6B
Keypad 5	93	4C	CC	73	F0 73
Keypad 6 Right	94	4D	CD	74	F0 74
Keypad 7 Home	95	47	C7	6C	F0 6C
Keypad 8 Up	96	48	C8	75	F0 75
Keypad 9 PageUp	97	49	C9	7D	F0 7D
Keypad 0 Insert	98	52	D2	70	F0 70
Keypad . Delete	99	53	D3	71	F0 71
Europe 2 (Note 2)	100	56	D6	61	F0 61
App	101	E0 5D	E0 DD	E0 2F	E0 F0 2F
Keyboard Power	102	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keypad =	103	59	D9	0F	F0 0F
F13	104	5D	DD	2F	F0 2F
F14	105	5E	DE	37	F0 37
F15	106	5F	DF	3F	F0 3F

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Key Name	USAR Key Number	PS/2 Set 1 Make	PS/2 Set 1 Break	PS/2 Set 2 Make	PS/2 Set 2 Break
F16	107	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
F17	108	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
F18	109	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
F19	110	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
F20	111	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
F21	112	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
F22	113	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
F23	114	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
F24	115	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Execute	116	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Help	117	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Menu	118	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Select	119	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Stop	120	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Again	121	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Undo	122	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Cut	123	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Copy	124	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Paste	125	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Find	126	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Mute	127	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Vol up	128	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Vol Dn	129	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Locking/ Caps Lock	130	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Locking Num Lock	131	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Locking Scroll Lock	132	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard , (Brazilian Keypad .)	133	7E	FE	6D	F0 6D
Keyboard Equal sign	134	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Int'l 1 (Ro)	135	73	F3	51	F0 51
Keyboard Int'l 2 (Katakana/Hiragana)	136	70	F0	13	F0 13
Keyboard Int'l 3 ¥ (Yen)	137	7D	FD	6A	F0 6A
Keyboard Int'l 4 (Henkan)	138	79	F9	64	F0 64
Keyboard Int'l 5 (Muhenkan)	139	7B	FB	67	F0 67
Keyboard Int'l 6 (PC9800 Keypad ,)	140	5C	DC	27	F0 27
Keyboard Int'l 7	141	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Int'l 8	142	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Int'l 9	143	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Lang 1 (Hanguel/English)	144	F2	None	F2	None
Keyboard Lang 2 (Hanja)	145	F1	None	F1	None
Keyboard Lang 3 (Katakana)	146	78	F8	63	F0 63

Key Name	USAR Key Number	PS/2 Set 1 Make	PS/2 Set 1 Break	PS/2 Set 2 Make	PS/2 Set 2 Break
Keyboard Lang 4 (Hiragana)	147	77	F7	62	F0 62
Keyboard Lang 5 (Zenkaku/Hankaku)	148	76	F6	5F	F0 5F
Keyboard Lang 6	149	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Lang 7	150	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Lang 8	151	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Lang 9	152	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Alternate Erase	153	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard SysReq/ Attention	154	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Cancel	155	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Clear	156	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Prior	157	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Return	158	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Separator	159	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Out	160	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Oper	161	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard Clear /Again	162	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard CrSel/Props	163	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Keyboard ExSel	164	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Left Control	165	1D	9D	14	F0 14
Left Shift	166	2A	AA	12	F0 12
Left Alt	167	38	B8	11	F0 11
Left GUI	168	E0 5B	E0 DB	E0 1F	E0 F0 1F
Right Control	169	E0 1D	E0 9D	E0 14	E0 F0 14
Right Shift	170	36	B6	59	F0 59
Right Alt	171	E0 38	E0 B8	E0 11	E0 F0 11
Right GUI	172	E0 5C	E0 DC	E0 27	E0 F0 27
System Power	173	E0 5E	E0 DE	E0 37	E0 F0 37
System Sleep	174	E0 5F	E0 DF	E0 3F	E0 F0 3F
System Wake	175	E0 63	E0 E3	E0 5E	E0 F0 5E
Scan Next Track	176	E0 19	E0 99	E0 4D	E0 F0 4D
Scan Previous Track	177	E0 10	E0 90	E0 15	E0 F0 15
Stop	178	E0 24	E0 A4	E0 3B	E0 F0 3B
Play/ Pause	179	E0 22	E0 A2	E0 34	E0 F0 34
Mute	180	E0 20	E0 A0	E0 23	E0 F0 23
Bass Boost	181	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Loudness	182	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Volume Up	183	E0 30	E0 B0	E0 32	E0 F0 32
Volume Down	184	E0 2E	E0 AE	E0 21	E0 F0 21
Bass Up	185	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Bass Down	186	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Treble Up	187	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Treble Down	188	UNASSIGNED	UNASSIGNED	UNASSIGNED	UNASSIGNED
Media Select	189	6D	E0 ED	E0 50	E0 F0 50
Mail	190	E0 6C	E0 EC	E0 48	E0 F0 48
Calculator	191	E0 21	E0 A1	E0 2B	E0 F0 2B

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Key Name	Key Number	PS/2 Set 1 Make	PS/2 Set 1 Break	PS/2 Set 2 Make	PS/2 Set 2 Break
My Computer	192	E0 6B	E0 EB	E0 40	E0 F0 40
WWW Search	193	E0 65	E0 E5	E0 10	E0 F0 10
WWW Home	194	E0 32	E0 B2	E0 3A	E0 F0 3A
WWW Back	195	E0 6A	E0 EA	E0 38	E0 F0 38
WWW Forward	196	E0 69	E0 E9	E0 30	E0 F0 30
WWW Stop	197	E0 68	E0 E8	E0 28	E0 F0 28
WWW Refresh	198	E0 67	E0 E7	E0 20	E0 F0 20
WWW Favorites	199	E0 66	E0 E6	E0 18	E0 F0 18

Note 1: In PS/2 mode, Scan Set 1 & 2, each keycode is preceded or followed by additional bytes of data. These codes are documented in WHQLKEYS.DOC, available from Microsoft.

Note 2: These keys have various legends depending upon the locale for which the keyboard is manufactured. Europe 1 is typically in AT-101 Key Position 42 next to the Enter key. Europe 2 is typically in AT-101 Key Position 45, between the Left Shift and Z keys.

Baud rate:

The PS2Adapt™ implements asynchronous mode at fixed preselected Baud rates: 300bps, 600bps, 1200bps, 9600bps, 19200bps, 31250bps and 62500bps, depending on the configuration pins' state on power up. The IC can achieve these standard Baud rates by using a 4MHz oscillator.

Protocol:

In asynchronous mode, the PS2Adapt™ supports transmission in one direction only (PS2Adapt™ to host). The PS2Adapt™ starts the transmission to the system when it has mouse/keyboard package pending. The data format is one start bit, 8 data bits, no parity and one stop bit.

1. The PS2Adapt™ asserts _CTS low to indicate that a packet transfer will start.
2. The host asserts _RTS low to indicate that it is ready to receive data.
     _RTS low means that system can receive data (e.g. UART is operational).
3. The PS2Adapt™ places data on TXD line when it detects the _RTS low.
4. When one package is successfully transmitted, the IC raises _CTS.

Notes on the Protocol:

To assure fast transmission, the system must assert _RTS low as soon as possible. If the system is ready to receive the data, it doesn't have to raise _RTS between packages.

The PS2Adapt™ checks _RTS after every byte transmission. If _RTS returns to high, it means that the transmission was unsuccessful. The PS2Adapt™ then raises _CTS to abort the transmission and the entire package will be re-transmitted.

The maximum time of T1 is 10ms. If the system cannot assert _RTS low after 10ms of _CTS low, the PS2Adapt™ then raises _CTS to abort the transmission request. After that, the PS2Adapt™ tries to start the transmission again.
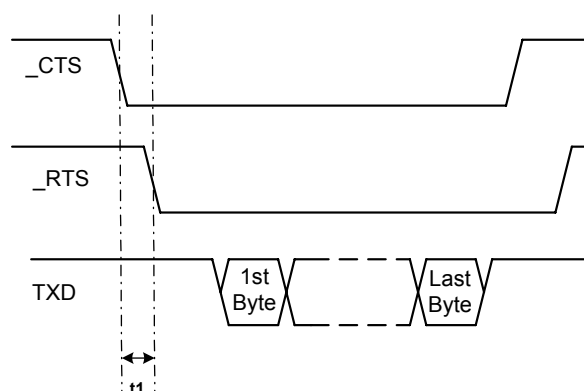
Figure 1: Serial Transmission Timing

SERIAL PERIPHERAL INTERFACE (SPI) MODE

The Serial Peripheral Interface (SPI) is a synchronous bi-directional multi-slave protocol. In SPI mode, the PS2Adapt™ acts as a slave device. The PS2Adapt™ supports only transmission and doesn't support receiving. SPI data transfer can be performed at a maximum clock rate of 500 KHz. If the CONF0 pin is high, the data transfer sequence is MSB to LSB; if CONF0 pin is low the sequence is LSB to MSB. The SDATA pin outputs data every time the transfer clock changes from high to low level.

Protocol:

1. The PS2Adapt™ asserts _ATN low to indicate that a mouse packet is waiting for transfer.
2. The host asserts _SS low to indicate that it is ready to receive data. _SS low means the system selected SPI PS2Adapt™ as its communication device.
3. On detecting _SS low, the IC enables the SPI interface and places data in the SPI data TX buffer. After a short delay, the system supplies eight clocks to get the data from the IC. The minimum time t2 from _SS low to first SPI clock is 50µs.
4. When a byte is transferred successfully, the system has to wait a minimum of 50µs to begin the clocks for next byte transmission.
5. When the four-byte mouse package / 2-byte keyboard package is transmitted, the system stops the SPI clock. If it needs to communicate with other SPI devices, it has to wait for _ATN return to high. _ATN high means the SPI port of PS2Adapt™ is now in high Impedance State.
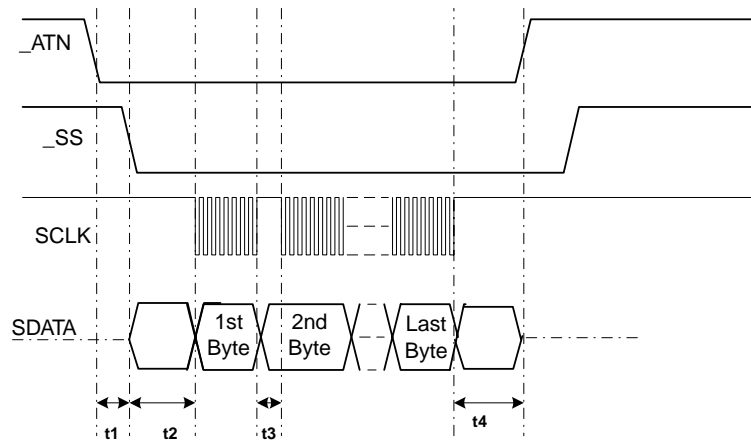
Figure 2: SPI Transmission Timing: (_SS toggles for every package).

Notes on the Protocol:

To assure fast transmission, system must assert _SS low as soon as possible, see Figure 2. If the system is ready to get data, it doesn't have to raise _SS between packages, see Figure 3.

SPI Communication Timing Parameters

Symbol	Description	Min	Max	Units
t1	_ATN low to _SS low		10	ms
t2	_SS low to first clock (_SS toggles for every package)	50	5000	µs
t2'	_ATN low to first clock (_SS low)	50	5000	µs
t3	Last clock of transmitted byte to next byte's first clock	50	5000	µs
t4	Last byte TX finish to _ATN to high		30	µs
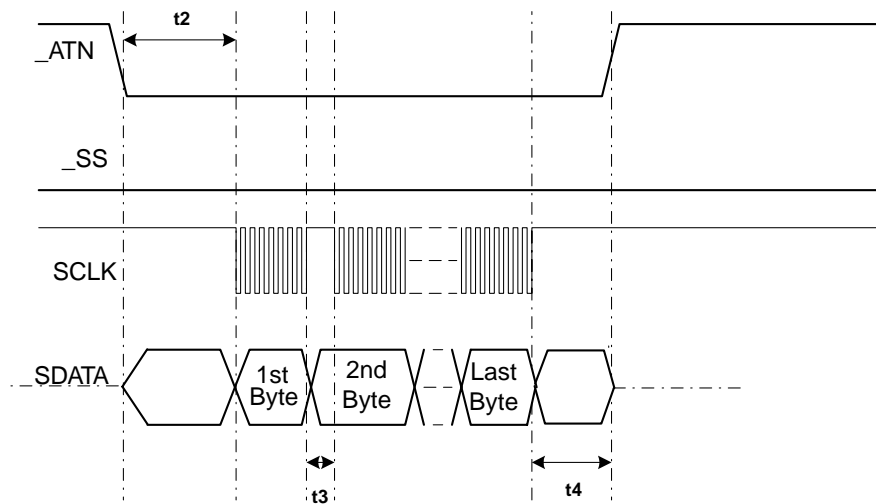
Figure 3: SPI Packet Transmission Timing: (_SS always low).

POWER MANAGEMENT

Modes of Operation

The PS2Adapt™ has two modes of operation relating to its power consumption.

The "Stop" mode is the lowest power consumption mode. In this mode, the oscillator is stopped and the IC consumes only 1 μA of leakage current. This is the default mode. The The PS2Adapt™ reverts to this mode when it is idle.

The "Run" mode is entered briefly, only to process an event or while an interrupt-generating signal condition persists. The PS2Adapt™ will remain in this mode until there are no tasks to handle, such as PS/2 reports or inititalization of PS/2 devices.

The PS/2 devices connected to the four external PS/2 ports are initialized at different sampling rates, depending on the port: PS/2 port 0 and PS/2 port 1 to 100 packages per second and 40 packages per second for PS/2 port 3 and PS/2 port 4. When mice plugged into PS/2 port 0 and 1 are moved, the PS2Adapt™ will typically stay in stop mode for 25% of the working time. When mice plugged into PS/2 port 3 and 4 are moved with a slower sampling rate, the PS2Adapt™ will typically stay in stop mode for 72% of working time. Therefore, we recommend that PS/2 port 3 and 4 are used for mice, if there is no specific requirement of mice sampling rate.

Note 1: When there is no mouse motion, all ports have same power consumption, less than 1 μA.
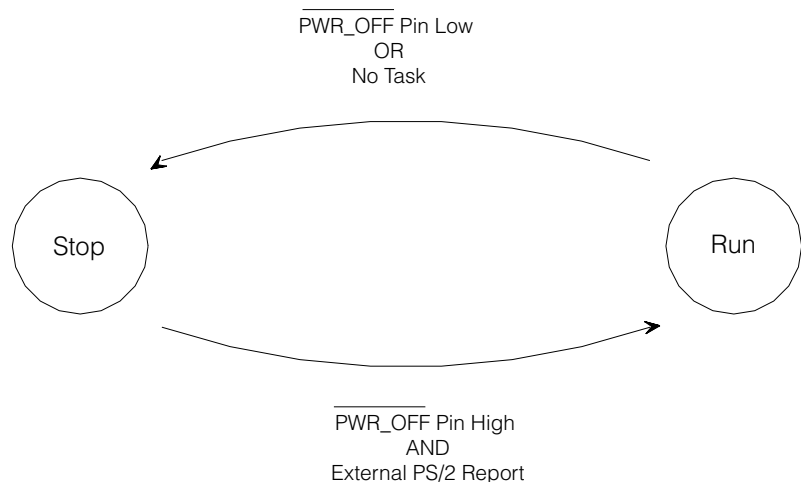
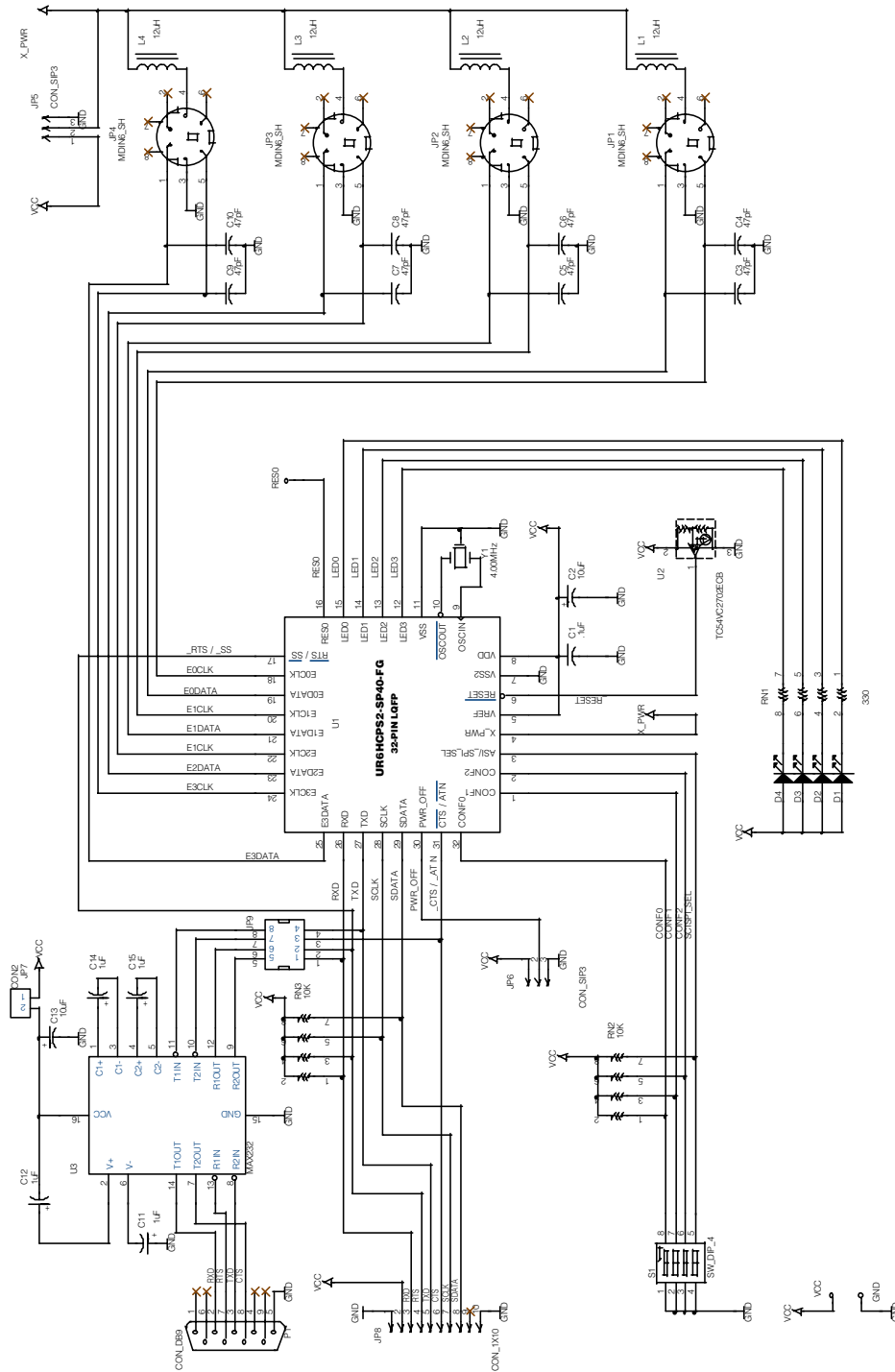**Note 2:** When a keyboard is plugged into these ports, the power consumption is the same, less than 1 μA.

The PS2Adapt™ implements two power management methods: system-coordinated power management and Self Power Management™ (SPM).

System-coordinated power management is implemented by the _PWR_OFF pin (Power Off). If the _PWR_OFF pin is low, the PS2Adapt™ disables all external PS/2 device reports to save power and to turn off keyboard LEDs.

Self-Power Management™ is a method implemented by the PS2Adapt™ that, independently of any system intervention, results in the lowest power consumption possible within the given parameters of its operation. Through Self Power Management™, the PS2Adapt™ is capable of typically operating at only 1 μA, independent of the state of the system. Self Power Management™ primarily determines the actual power consumption of the PS2Adapt™.

Even when the host is in the active state, the IC can still operate most of the time at only 1 μA, even with active external PS/2 devices attached to it.
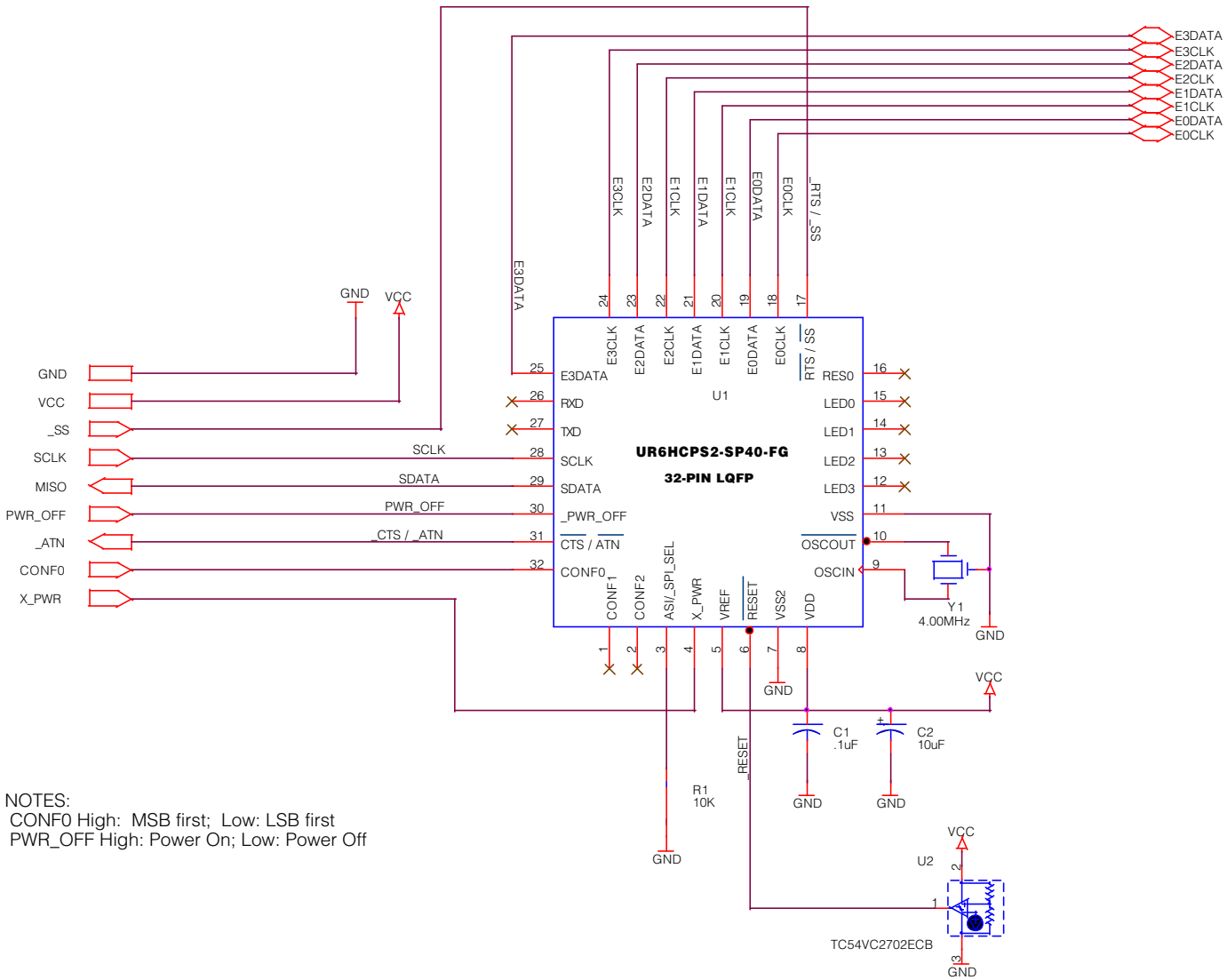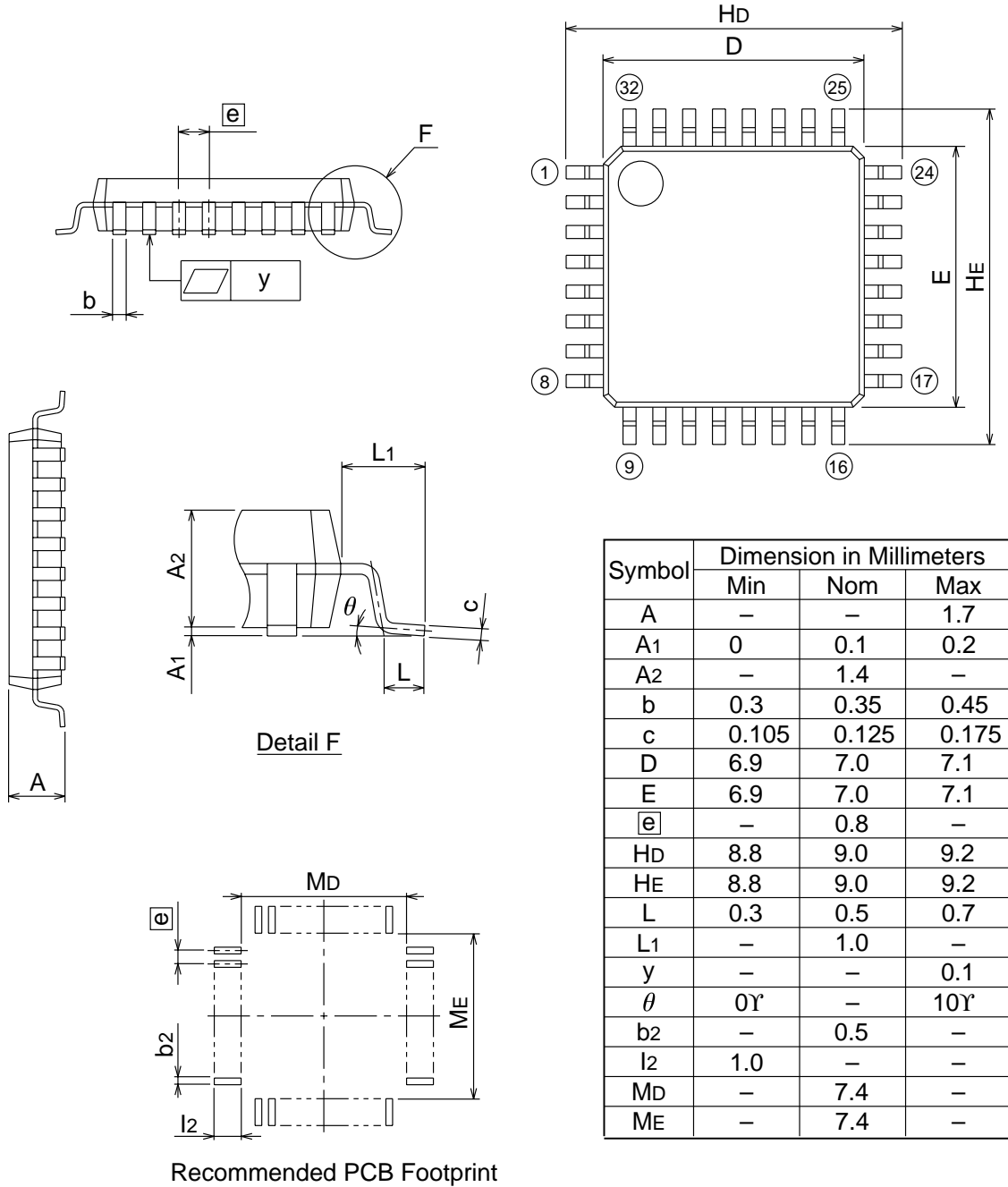
$\overline{PWR\_OFF}$ Pin Low
OR
No Task

Stop   Run

$\overline{PWR\_OFF}$ Pin High
AND
External PS/2 Report

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SUGGESTED SCHEMATIC FOR THE PS2ADAPT™ IN SPI MODE

NOTES:
 CONF0 High: MSB first; Low: LSB first
 PWR_OFF High: Power On; Low: Power Off

U1
UR6HCPS2-SP40-FG
32-PIN LQFP

U2
TC54VC2702ECB

Y1
4.00MHz

R1
10K

C1
.1uF

C2
10uF

SUGGESTED SCHEMATIC FOR THE PS2ADAPT™ IN ASYNCHRONOUS SERIAL MODE

NOTES:
PWR_OFF High: Power On;Low: Power Off

CONF2 CONF1 CONF0
111: 19200 bps
110: 9600   bps
101: 1200   bps
100: 600   bps
011: 300   bps
010: 31250 bps
001: 62500 bps

E3DATA
E3CLK
E2DATA
E2CLK
E1DATA
E1CLK
E0DATA
E0CLK

GND VCC

GND
VCC
_RTS
RXD
TXD
PWR_OFF
_CTS
CONF0
CONF1
CONF2

X_PWR

U1
UR6HCPS2-SP40-FG
32-PIN LQFP

E3DATA 25
RXD 26
TXD 27
SCLK 28
SDATA 29
_PWR_OFF 30
CTS / ATN 31
CONF0 32

E3CLK 24
E2DATA 23
E2CLK 22
E1DATA 21
E1CLK 20
E0DATA 19
E0CLK 18
RTS / SS 17

RES0 16
LED0 15
LED1 14
LED2 13
LED3 12
VSS 11
OSCOUT 10
OSCIN 9

CONF1 1
CONF2 2
ASI/_SPI_SEL 3
X_PWR 4
VREF 5
RESET 6
VSS2 7
VDD 8

Y1
4.00MHz
GND

GND
VCC

C1
.1uF
C2
10uF
GND GND

VCC
U2
TC54VC2702ECB
GND

Detail F

Recommended PCB Footprint

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A$_1$	0	0.1	0.2
A$_2$	–	1.4	–
b	0.3	0.35	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.8	–
H$_D$	8.8	9.0	9.2
H$_E$	8.8	9.0	9.2
L	0.3	0.5	0.7
L$_1$	–	1.0	–
y	–	–	0.1
θ	0Υ	–	10Υ
b$_2$	–	0.5	–
l$_2$	1.0	–	–
M$_D$	–	7.4	–
M$_E$	–	7.4	–

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Ratings	Symbol	Value	Unit
Supply voltage	Vdd	-0.3 to 7.0	V
Input voltage	Vin	Vss -0.3 to Vdd +0.3	V
Current drain per pin (not including Vss or Vdd)	I	20	mA
Operating temperature UR6HCSP2-SP40	Ta	T low to T high -20 to +85	°C
Storage temperature range	Tstg	-40 to +125	°C

DC Electrical Characteristics, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage		3.0	5.0	5.5	V
Output voltage (10 μA load)	Voh	Vdd–0.1			V
	Vol			0.1	
Input high voltage	Vih	0.8 x Vdd		Vdd	V
Input low voltage	Vil	Vss		0.2xVdd	V
Input current	Iin			+/- 1	μA
Supply current (Vdd=5.0 Vdc+/-10%, Vss=0)	Idd		3.0	TBD	mA

Control Timing (Vdd=5.0 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	fosc				MHz
■ Resonator option			4.0		
■ External clock option			4.0		

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