

DESCRIPTION

The PT9250 is an advanced single chip GPS receiver to integrate baseband, RF and flash memory into the 7mm x 10mm package making for an extremely compact design. This advanced solution offers best-in-class acquisition & tracking sensitivity, TTFF and accuracy. The PT9250 architecture uses an FFT and Matched Filter that delivers performance equivalent to more than 75,000 correlators. This represents a quantum leap forward in GPS performance. The PT9250's architecture enables unmatched TTFF at low signal levels. The PT9250 includes a powerful GPS DSP integrated with a 32-bit RISC microprocessor, 1Mb of SRAM and 4 Mb flash memories. The PT9250 also integrates a built-in low power RTC circuit for low power operation and battery backup RAM for satellite information. PTC supports full reference design, demonstration system, software evaluation tools and other supporting documentation.

APPLICATIONS

- GPS receivers
- Vehicle navigator
- Cellular phone
- PDA
- PMP

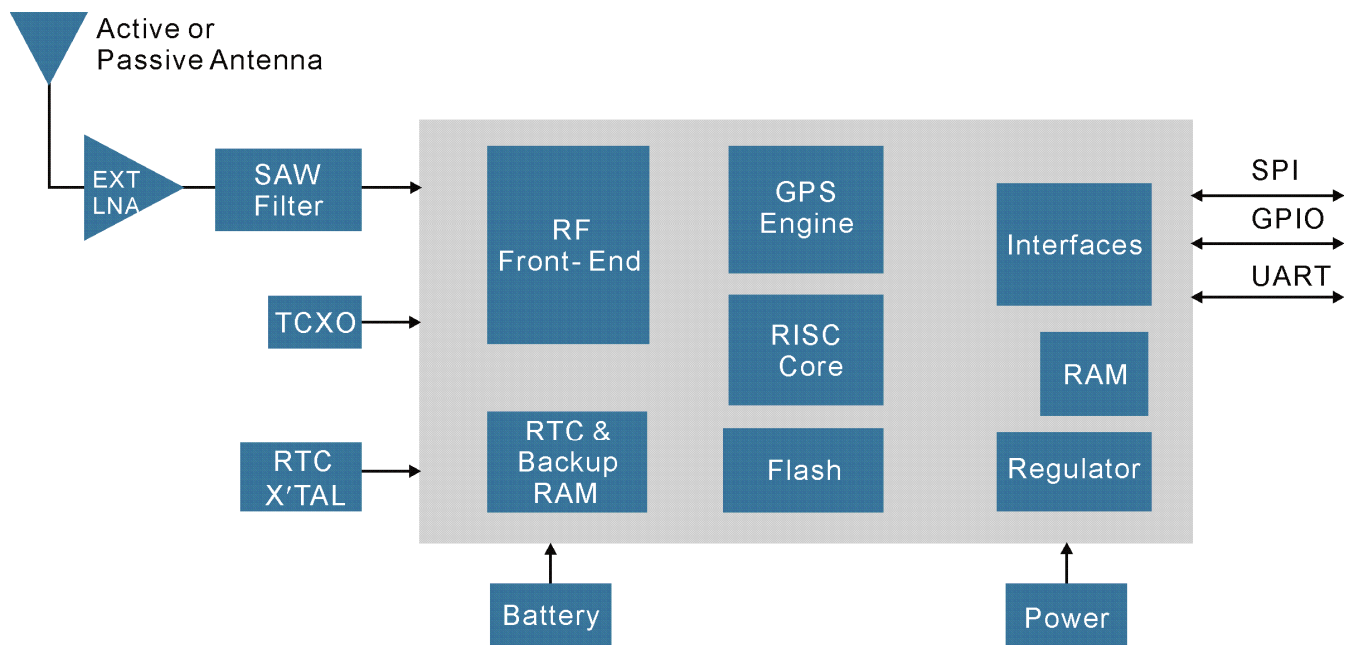
FEATURES

- Reception frequency : 1575.42 MHz (L1 band, CA code)
- Reference clock (TCXO) frequency : 16.368 MHz or 16.369 MHz
- Best-in-class acquisition and tracking sensitivity, TTFF and accuracy ¹.
 - Tracking sensitivity -159 dBm
 - Acquisition sensitivity -142 dBm
 - Cold start 33 sec, warm start 32 sec and hot start 1 sec
 - 5m position accuracy for autonomous²
- SoC to integrate major RF receiver, digital baseband and flash memory
- 48 channel acquisition and tracking engine
- 32 bits RISC CPU (MIPS)
- Internal Low power Real Time Clock
- Battery back-up SRAM
- 2-channel UART communication port
- SPI host interface
- 2 External interrupts
- Watch dog timer support
- 16 GPIOs
- 1 PPS output
- Support NMEA-0183(V3.01)
- 140 balls LFBGA
- Temperature range -40°C/+85°C

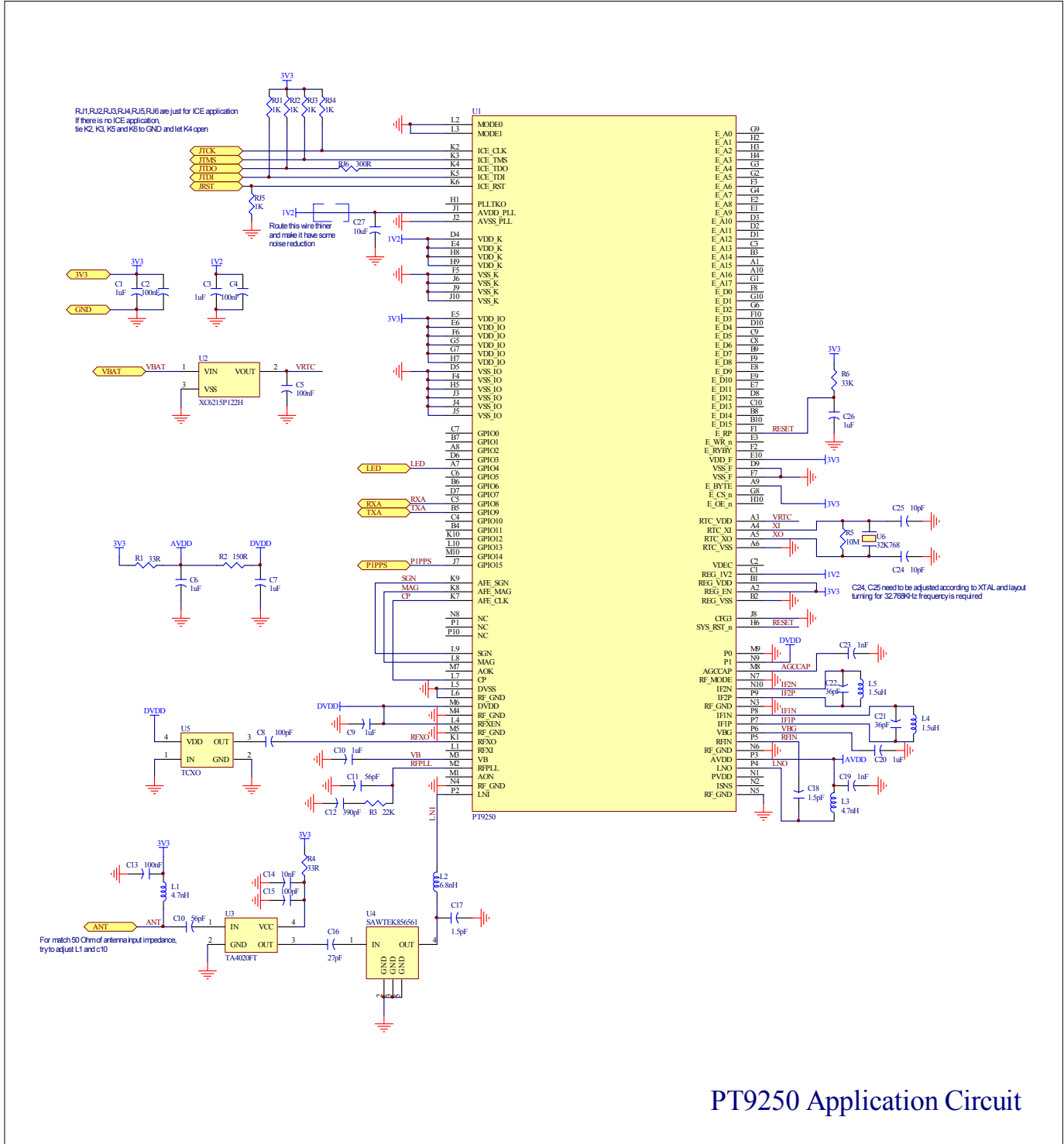
Notes :

1. Under open sky environment, -130 dBm signal level on PTC evaluation platform.
2. Under 24hr, 50% possibility and -130 dBm signal level.

BLOCK DIAGRAM



APPLICATION CIRCUITS



PT9250 Application Circuit

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT9250	10mmx7mm LFBGA	PT9250

BALL CONFIGURATION

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
E_A15	REG_EN	RTC_VDD	RTC_XI	RTC_XO	RTC_VSS	GPIO4	GPIO2	E_BYTE	E_A16
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
REG_VDD	REG_VSS	E_A14	GPIO11	GPIO9	GPIO6	GPIO1	E_D14	E_D7	E_D15
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
REG_1V2	VDEC	E_A13	GPIO10	GPIO8	GPIO5	GPIO0	E_D6	E_D5	E_D13
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
E_A12	E_A11	E_A10	VDD_K	VSS_IO	GPIO3	GPIO7	E_D12	VSS_F	E_D4
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
E_A9	E_A8	E_WR_n	VDD_K	VDD_IO	VDD_IO	E_D11	E_D9	E_D10	VDD_F
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
E_RP	E_RYBY	E_A6	VSS_IO	VSS_K	VDD_IO	VSS_F	E_D0	E_D8	E_D3
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
E_A17	E_A5	E_A4	E_A7	VDD_IO	E_D2	VDD_IO	E_CS_n	E_A0	E_D1
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
PLLTKO	E_A1	E_A2	E_A3	GND_IO	SYS_RST_n	VDD_IO	VDD_K	VDD_K	E_OE_n
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
AVDD_PLIA	VSS_PLL	VSS_IO	VSS_IO	VSS_IO	VSS_K	GPIO15	CFG3	VSS_K	VSS_K
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
RFXO	ICE_CLK	ICE_TMS	ICE_TDO	ICE_TDI	ICE_RST_n	AFE_CLK	AFE_MAG	AFE_SGN	GPIO12
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10
RFXI	MODE0	MODE1	RFXEN	DVSS	RF_GND	CP	MAG	SGN	GPIO13
M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
AON	RFPLL	VB	RF_GND	RF_GND	DVDD	AOK	AGCCAP	P0	GPIO14
N1	N2	N3	N4	N5	N6	N7	N8	N9	N10
PVDD	ISNS	RFGND	RF_GND	RF_GND	RF_GND	RF_MODE	NC	P1	IF2N
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10
NC	LNI	AVDD	LNO	RFIN	VBG	IF1P	IF1N	IF2P	NC

IMPORTANT NOTICE

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