®
AMCC

DUAL SERIAL BACKPLANE DEVICE

S2062

FEATURES

- Broad operating rate range (0.77 - 1.3 GHz)
  - 1062 MHz (Fibre Channel)
  - 1250 MHz (Gigabit Ethernet) line rates
  - 1/2 Rate Operation
- Dual Transmitter with phase-locked loop (PLL) clock synthesis from low speed reference
- Dual Receiver PLL provides clock and data recovery
- Internally series terminated TTL outputs
- On-chip 8B/10B line encoding and decoding for two separate parallel 8-bit channels
- 2x8 Bit parallel TTL interface
- Low-jitter serial PECL interface
- Local Loopback
- Interfaces with coax, twinax, or fiber optics
- Single +3.3V supply, 1.37 W power dissipation
- Compact 21mm x 21mm 156 TBGA package

APPLICATIONS

- Ethernet Backbones
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

GENERAL DESCRIPTION

The S2062 facilitates high-speed serial transmission of data in a variety of applications including Gigabit Ethernet, Fibre Channel, serial backplanes, and proprietary point to point links. The chip provides two separate transceivers which can be operated individually for a data capacity of >2 Gbps.

Each bi-directional channel provides 8B/10B coding/decoding, parallel to serial and serial to parallel conversion, clock generation/recovery, and framing. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip dual receive PLL is used for clock recovery and data retiming on the two independent data inputs. The transmitter and receiver each support differential PECL-compatible I/O for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a 3.3V power supply and dissipates 1.37 watts.

Figure 1 shows the S2062 and S2068 in a Gigabit Ethernet application. Figure 2 combines the S2062 with a crosspoint switch to demonstrate a serial backplane application. Figure 3 is the input/output diagram. Figures 4 and 5 show the transmit and receive block diagrams, respectively.

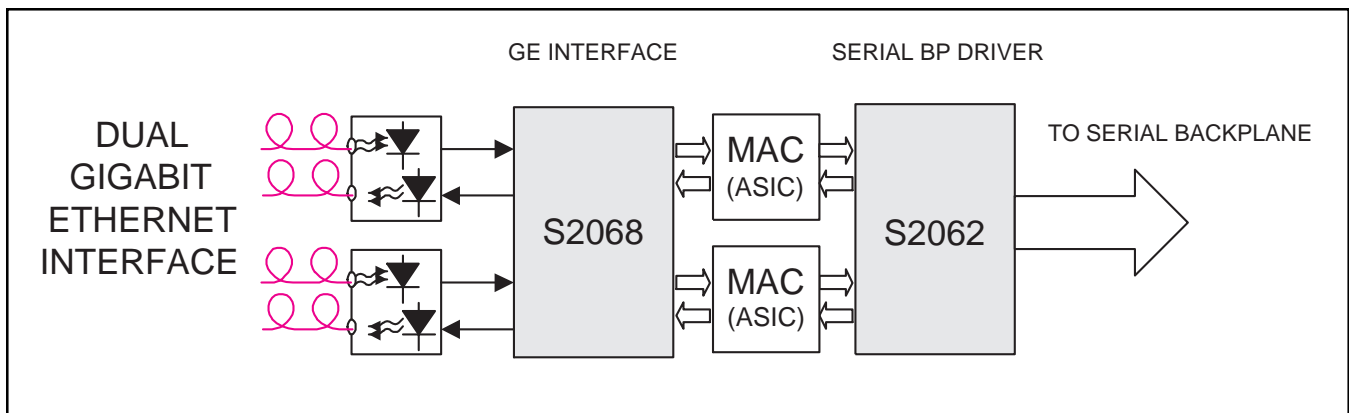*Figure 1. Typical Dual Gigabit Ethernet Application*
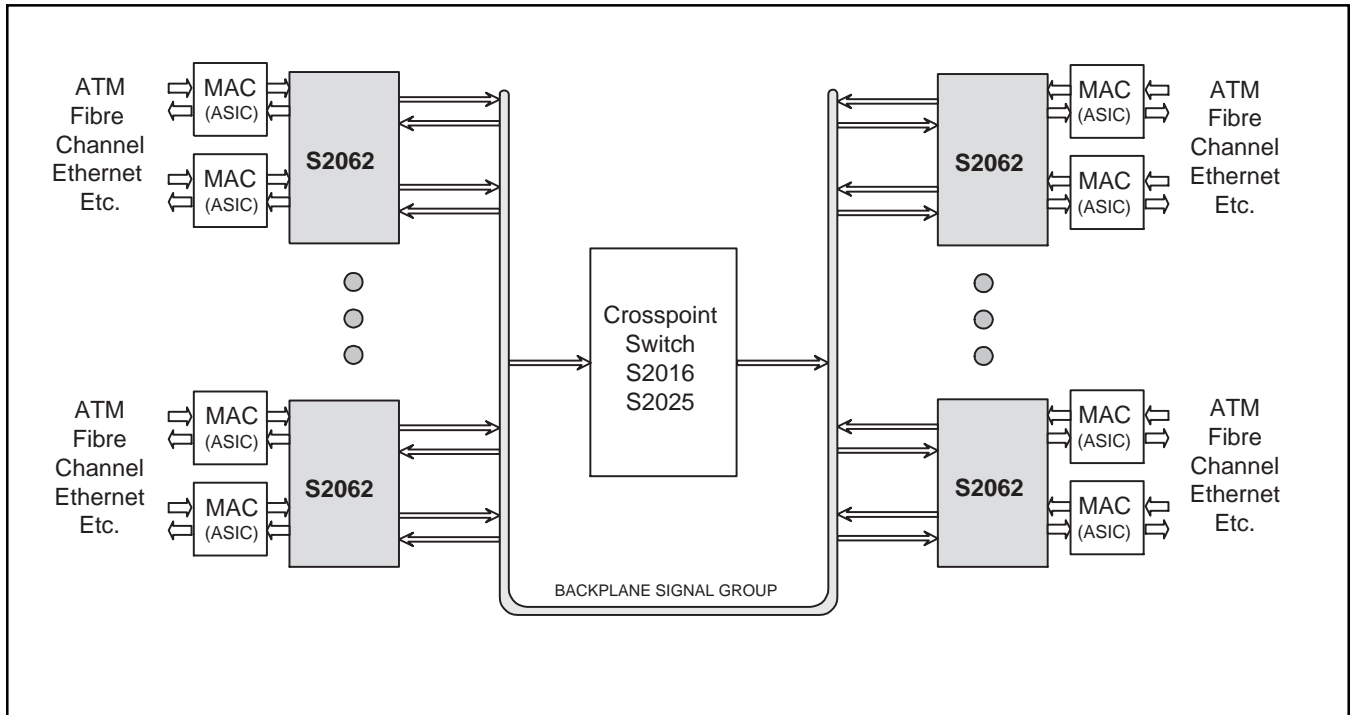
Figure 2. Typical Backplane Application
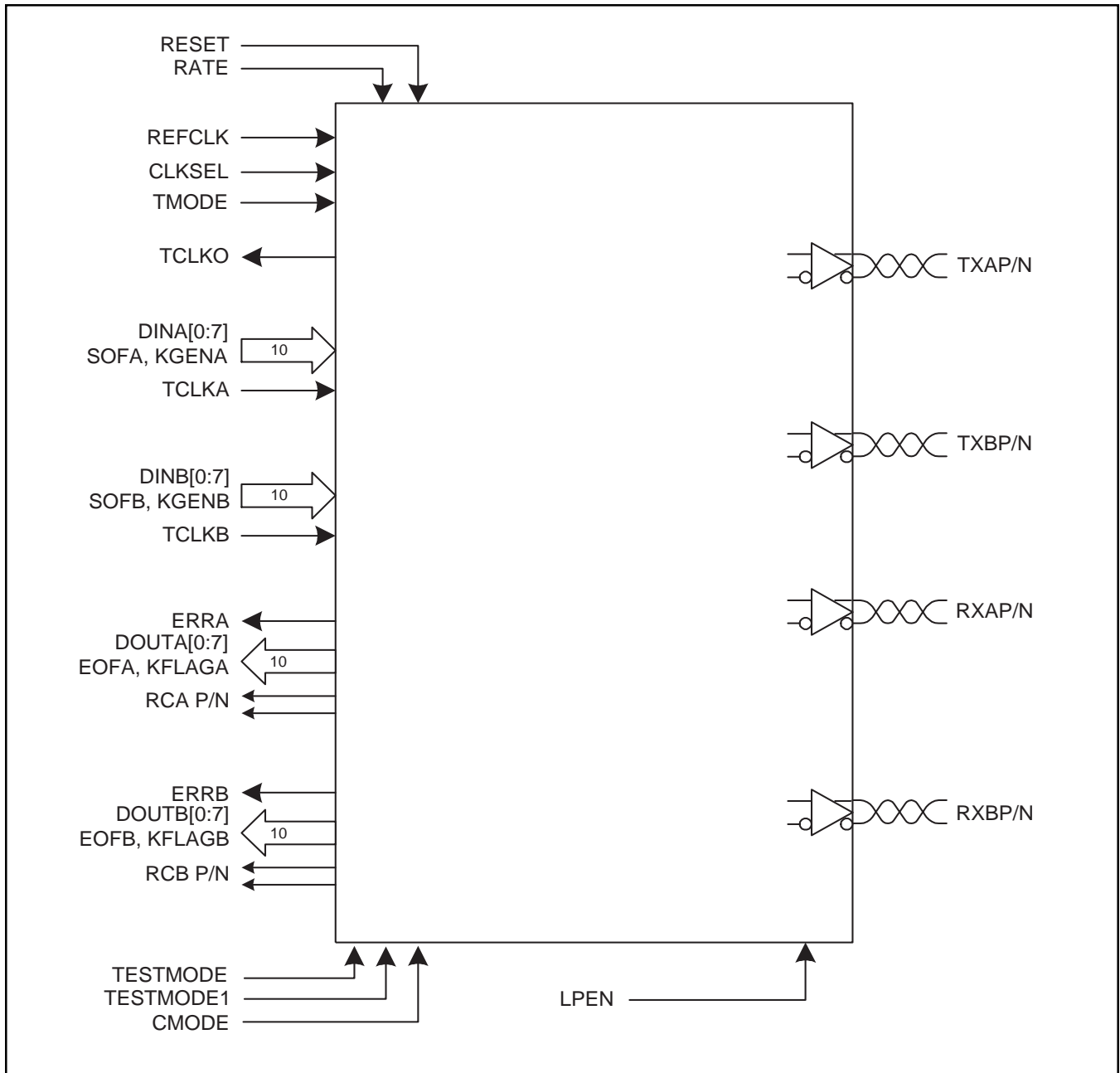
Figure 3. S2062 Input/Output Diagram

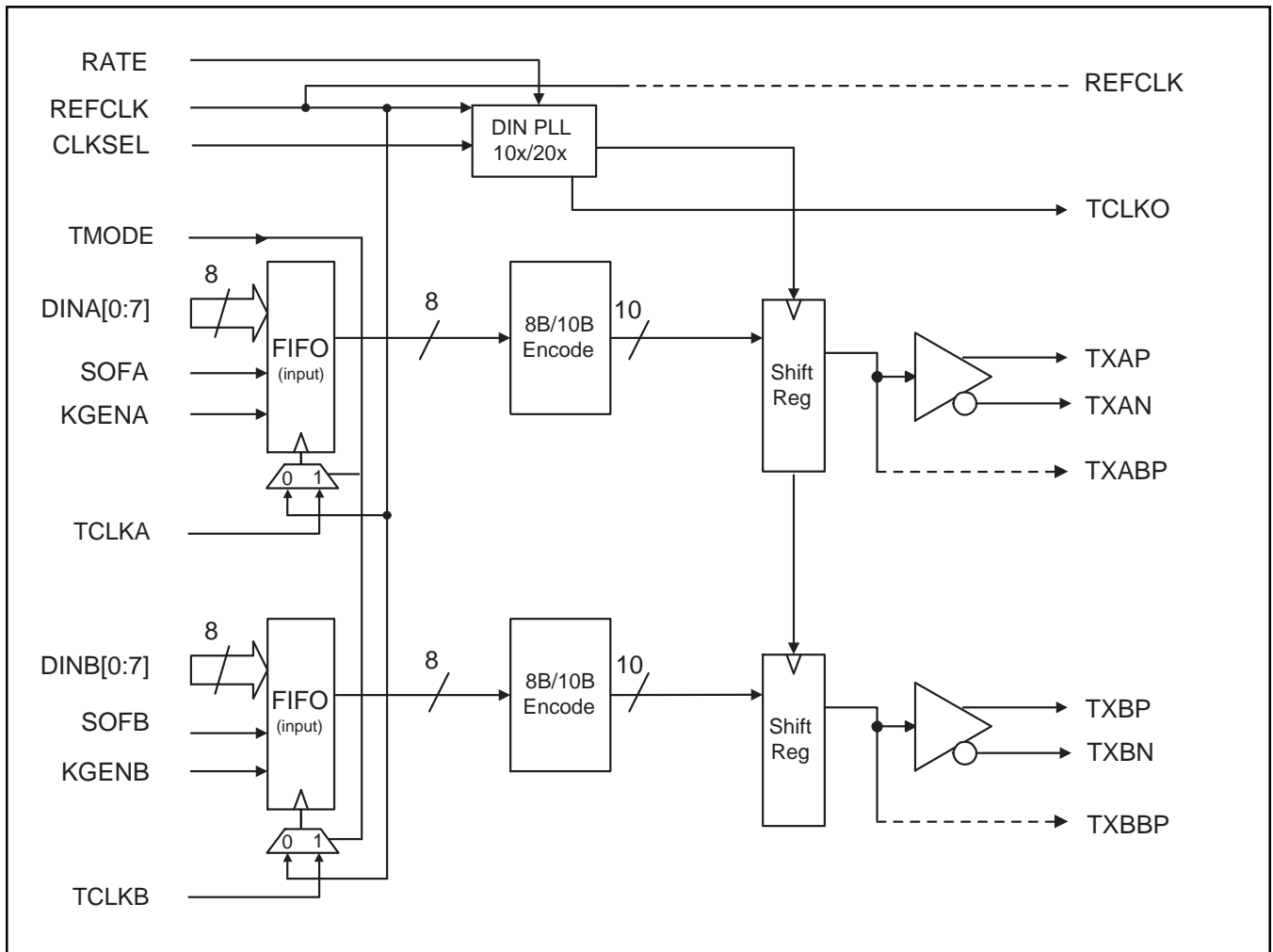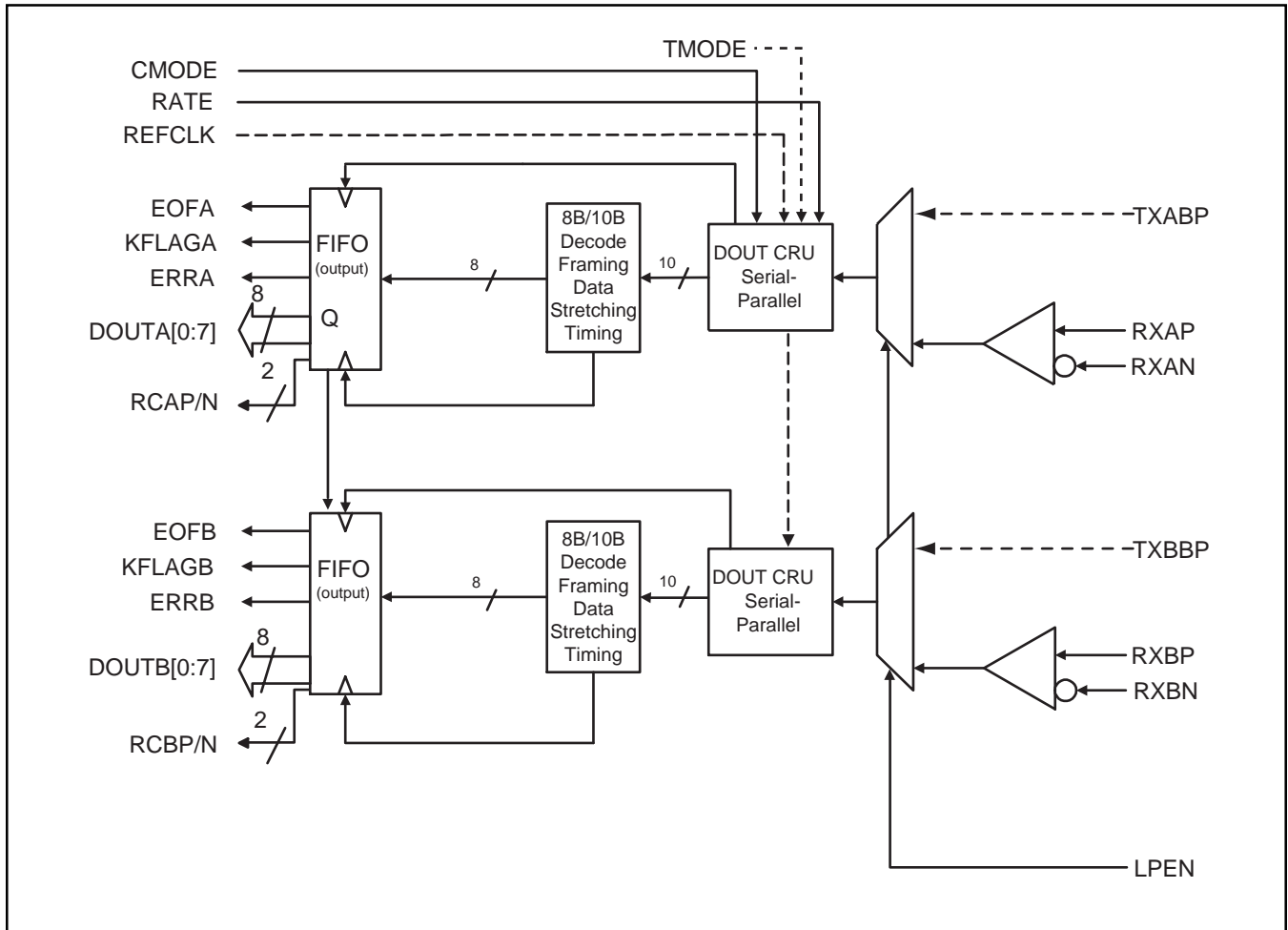*Figure 4. Transmitter Block Diagram*

Figure 5. Receiver Block Diagram

TRANSMITTER DESCRIPTION

The transmitter section of the S2062 contains a single PLL which is used to generate the serial rate transmit clock for all transmitters. Two channels are provided with a variety of options regarding input clocking and loopback. The transmitters can operate in the range of 0.77 GHz to 1.3 GHz, 10 or 20 times the reference clock frequency.

Data Input

The S2062 has been designed to simplify the parallel interface data transfer and provides the utmost in flexibility regarding clocking of parallel data. Prior, or less sophisticated, implementations of this function have either forced the user to synchronize transmit data to the reference clock or to provide the output clock as a reference to the PLL, resulting in increased jitter at the serial interface. The S2062 incorporates a unique FIFO structure on both the parallel inputs and the parallel outputs which enables the user to provide a "clean" reference source for the PLL and to accept a separate external clock which is used exclusively to reliably clock data into the device.

Data is input to each channel of the S2062 nominally as a 10 bit wide word. This consists of eight data bits of user data, KGEN, and SOF. An input FIFO and a clock input, TCLKx, are provided for each channel of the S2062. The S2062 can be configured to use either the TCLKx (TCLK MODE) input or the REFCLK input (REFCLK MODE). In TCLK or REFCLK mode, each byte of data is clocked into its FIFO with the TCLKx provided with each byte. Table 1 provides a summary of the input modes for the S2062.

Operation in the TCLK MODE makes it easier for users to meet the relatively narrow setup and hold time window required by the parallel 10-bit interface. The TCLK signal is used to clock the data into an internal holding register and the S2062 synchronizes its internal data flow to insure stable operation. However, regardless of the clock mode, REFCLK is always the VCO reference clock. This facilitates the provision of a clean reference clock resulting in minimum jitter on the serial output. The TCLK must be frequency locked to REFCLK, but may have an arbitrary but fixed phase relationship. Adjustment of internal timing of the S2062 is performed during reset. Once synchronized, the S2062 can tolerate up to ±3ns of phase drift between TCLK and REFCLK.

Figure 6 demonstrates the flexibility afforded by the S2062. A low jitter reference is provided directly to the S2062 at either 1/10 or 1/20 the serial data rate.

This insures minimum jitter in the synthesized clock used for serial data transmission. A system clock output at the parallel word rate, TCLKO, is derived from the PLL and provided to the upstream circuit as a system clock. The frequency of this output is constant at the parallel word rate, 1/10 the serial data rate, regardless of whether the reference is provided at 1/10 or 1/20 the serial data rate. This clock can be buffered as required without concern about added delay. There is no phase requirement between TCLKO and TCLKx, which is provided back to the S2062, other than that they remain within ± 3ns of the phase relationship established at reset.

The S2062 also supports the traditional REFCLK (TBC) clocking found in Fibre Channel and Gigabit Ethernet applications and is illustrated in Figure 7.

Half Rate Operation

The S2062 supports full and 1/2 rate operation for all modes of operation. When RATE is LOW, the S2062 serial data rate equals the VCO frequency. When RATE is HIGH, the VCO is divided by 2 before being provided to the chip. Thus the S2062 can support Fibre Channel and serial backplane functions at both full and 1/2 the VCO rate.

8B/10B Coding

The S2062 provides 8B/10B line coding for each channel. The 8B/10B transmission code includes serial encoding and decoding rules, special characters, and error control. Information is encoded, 8 bits at a time, into a 10 bit transmission character. The characters defined by this code ensure that enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple errors that might occur during the transmission and reception of data[1].

The 8B/10B transmission code includes D-characters, used for data transmission, and K-characters, used for control or protocol functions. Each D-character and K-character has a positive and a negative parity version. The parity of each codeword is selected by the encoder to control the running disparity of the data stream. K-character generation is controlled individually for each channel using the KGENx input. When KGEN is asserted, the data on the parallel input is mapped into the corresponding control character. The parity of the K-character is selected to minimize running disparity in the serial data stream. Table 3 lists the K characters supported by the S2062 and identifies the mapping of the DIN[7:0] bits to each character.

A special input, SOF, is provided for each channel to simplify the generation of the K28.5 character. When SOF is asserted, the K28.5 character is generated regardless of the data on the parallel input. The K28.5 character can be of either positive or negative parity, depending on the current running disparity. Table 4 shows the mapping of the 8B/10B characters representation. Data is transmitted bit "a" or DIN[0] first.

In addition to data and K characters, the S2062 can also generate a unique sync sequence consisting of 16 consecutive K28.5 characters. This event is initiated by the simultaneous assertion of KGENx and SOFx for one clock period. The SOFx and KGENx inputs should be held low until the sync sequence has completed. The sync sequence may start with either a positive or negative parity K28.5. (Depending on the current running disparity.) The parity of the second and third K28.5 are inverse with respect to a valid 8B/

10B sequence. Parity of the remaining K28.5 alternate in accordance with the 8B/10B coding standard. Thus, the parity of the K28.5 pattern consists of + + - - + - + - + - + - + - + - or - - + - + - + - + - + - + - +. Table 2 shows the transmitter control signals.

Frequency Synthesizer (PLL)

The S2062 synthesizes a serial transmit clock from the reference signal. Upon startup, the S2062 will obtain phase and frequency lock within 2500 bit times after the start of receiving reference clock inputs. Reliable locking of the transmit PLL is assured, but a lock-detect output is NOT provided.

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[1] 1. A.X. Widner and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC9391, May 1982.

Table 1. Input Modes

TMODE	Operation
0	REFCLK Mode. REFCLK used to clock data into FIFOs for all channels.
1	TBC Mode. TBCx used to clock data into FIFOs for all channels.

Note that internal synchronization of FIFOs is performed upon de-assertion of RESET.

Table 2. Transmitter Control Signals

SOFx	KGENx	S2062 DIN Output
0	0	Encoded Parallel Data
0	1	K Character as defined by Table 3 and DIN[7:0]
1	0	K28.5 Character
1	1	Special 16 word character, + + - - + - + - + - + - + - or - - + - + - + - + - + - + - +

Figure 6. DIN Data Clocking with TCLK
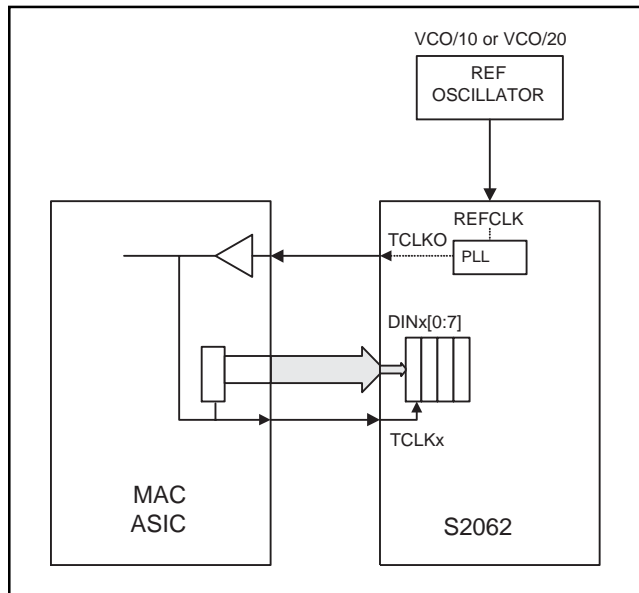
Figure 7. DIN Clocking with REFCLK
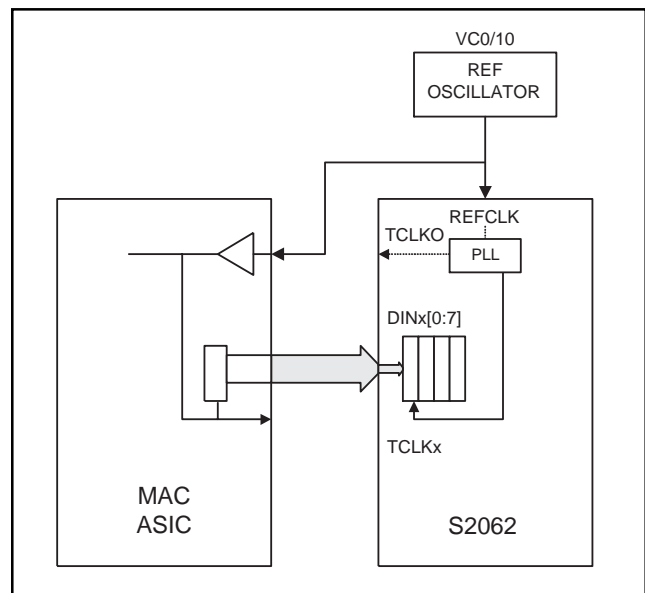
Table 3. K Character Generation (SOFx = 0)

K Character	DIN[7:0]	KGEN	Current RD+ abcdei fghj	Current RD- abcdei fghj	Comments
K28.0	000 11100	1	110000 1011	001111 0100	
K28.1	001 11100	1	110000 0110	001111 1001	
K28.2	010 11100	1	110000 1010	001111 0101	
K28.3	011 11100	1	110000 1100	001111 0011	
K28.4	100 11100	1	110000 1101	001111 0010	
K28.5	101 11100	1	110000 0101	001111 1010	Sync Character
K28.6	110 11100	1	110000 1001	001111 0110	
K28.7	111 11100	1	110000 0111	001111 1000	
K23.7	111 10111	1	000101 0111	111010 1000	
K27.7	111 11011	1	001001 0111	110110 1000	
K29.7	111 11101	1	010001 0111	101110 1000	
K30.7	111 11110	1	100001 0111	011110 1000	

Table 4. Data to 8B/10B Alphabetic Representation

	Data Byte									
DIN[0:9] or DOUT[0:9]	0	1	2	3	4	5	6	7	8	9
8B/10B Alphanumeric Representation	a	b	c	d	e	i	f	g	h	j

Reference Clock Input

The reference clock input must be supplied with a low-jitter clock source. All reference clocks in a system must be within 200 ppm of each other to insure that the clock recovery units can lock to the serial data.

The frequency of the reference clock must be either 1/10 the serial data rate, CLKSEL = 0, or 1/20 the serial data rate, CLKSEL=1. In both cases the frequency of the parallel word rate output, TCLKO, is constant at 1/10 the serial data rate. See Table 5.

Serial Data Outputs

The S2062 provides LVPECL level serial outputs. Each high speed output should be provided with a resistor to VSS (Gnd) near the device. A value of 4.5 KΩ provides optimal performance with minimum impact on power dissipation. The resistance may be as low as 450 Ω, but this will dissipate additional power with no substantive performance improvement. Outputs are designed to perform optimally when AC-coupled.

Transmit FIFO Initialization

The transmit FIFO must be initialized after stable delivery of data and TCLK to the parallel interface, and before entering the normal operational state of the circuit. FIFO initialization is performed upon the de-assertion of the RESET signal. TCLKO will operate normally regardless of the state of RESET.

Table 5. Operating Rates

RATE	CLKSEL	REFCLK Frequency	Serial Output Rate	TCLKO Frequency
0	0	SDR/10	0.77–1.3 GHz	SDR/10
0	1	SDR/20	0.77–1.3 GHz	SDR/10
1	0	SDR/10	0.39-0.65 GHz	SDR/10
1	1	SDR/20	0.39-0.65 GHz	SDR/10

Note: SDR = Serial Data Rate.

RECEIVER DESCRIPTION

Each receiver channel is designed to implement a Serial Backplane receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 5.

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. After acquiring bit synchronization, the S2062 searches the serial bit stream for the occurrence of a K28.5 character on which to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the decoded data on its parallel outputs.

Data Input

A differential input receiver is provided for each channel of the S2062. Each channel has a loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function for both channels is controlled by the loopback enable signal, LPEN.

The high speed serial inputs to the S2062 are internally biased to VDD-1.3V. All that is required externally are AC-coupling and line-to-line differential termination.

Clock Recovery Function

Clock recovery is performed on the input data stream for each channel of the S2062. The receiver PLL has been optimized for the anticipated needs of Serial Backplane systems. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the serial data inputs. If at any time the frequency or run length checks are violated, the state machine forces the VCO to lock to the reference clock. This allows the VCO to maintain the correct frequency in the absence of data.

Table 6. Lock to Reference Frequency Criteria

Current Lock State	PLL Frequency (vs. REFCLK)	New Lock State
Locked	< 488 ppm	Locked
	488 to 732 ppm	Undetermined
	> 732 ppm	Unlocked
Unlocked	< 244 ppm	Locked
	244 to 366 ppm	Undetermined
	> 366 ppm	Unlocked

The 'lock to reference' frequency criteria insure that the S2062 will respond to variations in the serial data input frequency (compared to the reference frequency). The new Lock State is dependent upon the current lock state, as shown in Table 6.

The run-length criteria insure that the S2062 will respond appropriately and quickly to a loss of signal. The run-length checker flags a condition of consecutive ones or zeros across 12 parallel words. Thus 119 or less consecutive ones or zeros does not cause signal loss, 129 or more causes signal loss, and 120 - 128 may or may not, depending on how the data aligns across byte boundaries.

If both the off-frequency detect circuitry test and the run-length test are satisfied, the CRU will attempt to lock to the incoming data. When lock is achieved, LOCK-DET is asserted on the ERR, EOF, and KFLAG status lines. It is possible for the run length test to be satisfied due to noise on the inputs, even if no signal is present. In this case the lock detect status may periodically assert as the VCO frequency approaches that of the REFCLK.

In any transfer of PLL control from the serial data to the reference clock, the RCxP/N outputs remain phase continuous and glitch free, assuring the integrity of downstream clocking.

When operating in TCLK mode, both PLL lock status are indicated by a 1-0-1 on the ERR, EOF, and KFLAG outputs, respectively.

Reference Clock Input

A single reference clock, which serves both transmitter and receiver, must be provided from a low jitter clock source. The frequency of the received data stream (divided-by-10 or -20) must be within 200 ppm of the reference clock to insure reliable locking of the receiver PLL.

Serial-to-Parallel Conversion

Once bit synchronization has been attained by the S2062 CRU, the S2062 must synchronize to the 10 bit word boundary. Word synchronization in the S2062 is accomplished by detecting and aligning to the 8B/10B K28.5 codeword. The S2062 will detect and byte-align to either polarity of the K28.5. Each channel of the S2062 will detect and align to a K28.5 anywhere in the data stream. For TCLK or REFCLK mode operation, the presence of a K28.5 is indicated for each channel by the assertion of the EOFx signal. Table 7 details the function of the EOF, KFLAG, and ERR pins in status reporting. As indicated in Table 7, a 1-0-1 on the ERR, EOF, and KFLAG signals on any channel is indicative of CRU lock failure.

Table 7. Error and Status Reporting

ERR	EOF	KFLAG	Description	Rank
0	0	0	Normal Character. Indicates that a valid data character has been detected.	5
0	0	1	K Character (not K28.5). Indicates that a K Character other than K28.5 has been detected.	5
0	1	0	Not used.	
0	1	1	K28.5+ or K28.5-. Indicates that a K28.5 character of arbitrary parity has been detected.	3
1	0	0	Codeword Violation. Indicates that a word not corresponding to any valid Dx.x or Kx.x mapping has been received.	2
1	0	1	Operation in the TCLK mode, indicates loss of CRU bit lock.	1
1	1	0	Parity Error. Indicates that a running disparity error has been observed.	4
1	1	1	Not used.	

8B/10B Decoding

After serial to parallel conversion, the S2062 provides 8B/10B decoding of the data. The received 10-bit codeword is decoded to recover the original 8-bit data. The decoder also checks for errors and flags, either invalid codeword errors or running disparity errors by assertion of the ERRx signal. Error type is determined by examining the EOF output in accordance with Table 7. When more than one reportable condition occurs simultaneously, reporting is in accordance with the rank assigned by Table 7.

Data Output

Data is output on the DOUT[0:7] outputs. K-characters are flagged using the KFLAG signal. The EOF (with KFLAG) is used to indicate the reception of a valid K28.5 character. Invalid codewords and decoding errors are indicated on the ERR output. KFLAG, EOF, and ERR are buffered with the data in the FIFO to insure that all outputs are synchronized at the S2062 outputs. Errors are reported independently for each channel in TCLK or REFCLK mode operation.

The S2062 TTL outputs are optimized to drive 65Ω line impedances. Internal source matching provides good performance on unterminated lines of reasonable length.

Parallel Output Clock Rate

Two output clock modes are supported, as shown in Table 8. When CMODE is HIGH, a complementary TTL clock at the data rate is provided on the RCxP/N outputs. Data should be clocked on the rising edge of RCxP. When CMODE is LOW, a complementary TTL clock at 1/2 the data rate is provided. Data should be latched on the rising edge of RCxP and the rising edge of RCxN.

In Fibre Channel and Gigabit Ethernet applications, multiple consecutive K28.5 characters cannot be generated. However, for serial backplane applications this can occur. The S2062 must be able to operate properly when multiple K28.5 characters are received. After the first K28.5 is detected and aligned, the RCxP/N clock will operate without glitches or loss of cycles.

Table 8. Output Clock Mode

Mode	CMODE	RCx P/N Freq
Half Clock Mode	0	VCO/20
Full Clock Mode	1	VCO/10

OTHER OPERATING MODES

Operating Frequency Range

The S2062 is designed to operate at serial baud rates of 0.77 GHz to 1.3 GHz (616 Mbps to 1040 Mbps user data rate). The part is specified at Fibre Channel (1062 MHz) and Gigabit Ethernet (1.25 GHz) serial baud rates, but will operate satisfactorily at any rate in this range.

Loopback Mode

When loopback mode is enabled, the serial data from the transmitter is provided to the serial input of the receiver, as shown in Figure 8. This provides the ability to perform system diagnostics and off-line testing of the interface to verify the integrity of the serial channel before enabling the transmission medium. Loopback mode can be simultaneously enabled for both channels using the loopback-enable input, LPEN. Note that the high speed outputs are disabled during loopback operation.

TEST MODES

The RESET pin is used to initialize the Transmit FIFOs and must be asserted (LOW) prior to entering the normal operational state (see section Transmit FIFO Initialization).

Figure 8. S2062 Diagnostic Loopback Operation
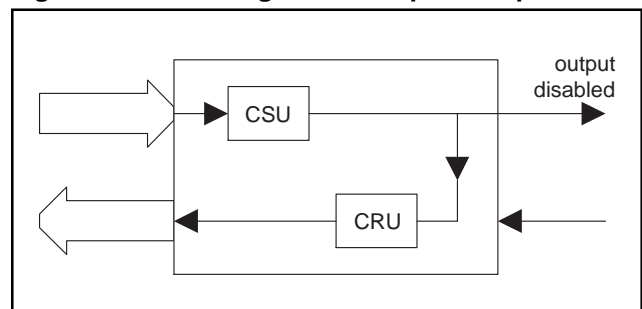
Table 9. Transmitter Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DINA7 DINA6 DINA5 DINA4 DINA3 DINA2 DINA1 DINA0	TTL	I	P12 T14 R12 P11 T13 R11 T12 P10	Transmit Data for Channel A. Parallel data on this bus is clocked in on the rising edge of TCLKA or REFCLK.
SOFA	TTL	I	T15	Start of Frame A. SOFA High causes the K28.5 character of appropriate parity to be transmitted on channel A outputs.
KGENA	TTL	I	R13	K-Character Generation. KGENA High causes the data on DINA[0:7] to be encoded into a K-Character.
TCLKA	TTL	I	R10	Transmit Data Clock A. When TMODE is High, this signal is used to clock Data on DINA[0:7], KGENA, and SOFA into the S2062. When TMODE is Low, TCLKA is ignored.
DINB7 DINB6 DINB5 DINB4 DINB3 DINB2 DINB1 DINB0	TTL	I	M16 M15 M14 N16 N15 N14 P16 P15	Transmit Data for Channel B. Parallel data on this bus is clocked in on the rising edge of TCLKB or REFCLK.
SOFB	TTL	I	L15	Start of Frame B. SOFB High causes the K28.5 character of appropriate parity to be transmitted on channel B outputs.
KGENB	TTL	I	L14	K-Character Generation. KGENB High causes the data on DINB[0:7] to be encoded into a K-Character.
TCLKB	TTL	I	R16	Transmit Data Clock B. When TMODE is High, this signal is used to clock Data on DINB[0:7], KGENB, and SOFB into the S2062. When TMODE is Low, TCLKB is ignored.

Table 10. Transmitter Output Signals

Pin Name	Level	I/O	Pin #	Description
TXAP TXAN	Diff. LVPECL	O	D16 E15	High speed serial outputs for Channel A.
TXBP TXBN	Diff. LVPECL	O	G15 G16	High speed serial outputs for Channel B.
TCLKO	TTL	O	K14	TTL Output Clock at the Parallel data rate. This clock is provided for use by up-stream circuitry.

Table 11. Mode Control Signals

Pin Name	Level	I/O	Pin #	Description
TESTMODE	TTL	I	D3	Test Mode Control. Keep Low for normal operation.
TESTMODE1	TTL	I	L16	Test Mode Control. Keep Low for normal operation.
TMODE	TTL	I	A13	Transmit Mode Control. When TMODE is Low, REFCLK is used to clock data on DINx[0:7], SOFx, and KGENx into the S2062. When TMODE is High, TCLKx is used to clock data into the S2062.
CLKSEL	TTL	I	B11	REFCLK Select Input. This signal configures the PLL for the appropriate REFCLK frequency. When CLKSEL = 0, the REFCLK frequency should equal the parallel word rate. When CLKSEL = 1, the REFCLK frequency should be 1/2 the parallel data rate.
REFCLK	TTL	I	J15	Reference Clock is used for the transmit VCO and frequency check for the clock recovered from the receiver serial data.
RESET	TTL	I	B15	When Low, the S2062 is held in reset. The receiver PLL is forced to lock to the REFCLK. The FIFOs are initialized on the rising edge of RESET. When High, the S2062 operates normally.
RATE	TTL	I	C11	When Low, the S2062 operates with the serial output rate equal to the VCO frequency. When High, the S2062 operates with the VCO internally divided by 2 for all functions.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 12. Receiver Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DOUTA7 DOUTA6 DOUTA5 DOUTA4 DOUTA3 DOUTA2 DOUTA1 DOUTA0	TTL	O	L2 L1 K2 K1 J3 J1 H3 H2	Channel A Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCAP in full clock mode and valid on the rising edge of both RCAP and RCAN in half clock mode.
EOFA	TTL	O	G1	Channel A End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTA[0:7].
KFLAGA	TTL	O	G2	Channel A K-Character Flag. A High in KFLAGA indicates that a valid control character has been detected. Data present on the parallel interface DOUTA[0:7] should be used to indicate which character was received.
ERRA	TTL	O	J2	Channel A Receive Error. A High on ERRA signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data.
RCAP RCAN	TTL	O	M1 L3	Receive Data Clock. Parallel receive data, DOUTA[0:7], EOFA, KFLAGA, and ERRA are valid on the rising edge of RCAP when in full clock mode and valid on the rising edge of both RCAP and RCAN in half clock mode.
DOUTB7 DOUTB6 DOUTB5 DOUTB4 DOUTB3 DOUTB2 DOUTB1 DOUTB0	TTL	O	P8 T5 R6 P6 R5 T3 P5 R3	Channel B Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCBP in full clock mode and valid on the rising edge of both RCBP and RCBN in half clock mode.
EOFB	TTL	O	P2	Channel B End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTB[0:7].
KFLAGB	TTL	O	R1	Channel B K-Character Flag. A High in KFLAGB indicates that a valid control character has been detected. Data present on the parallel interface DOUTB[0:7] should be used to indicate which character was received.
ERRB	TTL	O	P4	Channel B Receive Error. A High on ERRB signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data.
RCBP RCBN	TTL	O	R7 P7	Receive Data Clock. Parallel receive data, DOUTB[0:7], EOFB, KFLAGB, and ERRB are valid on the rising edge of RCBP when in full clock mode and valid on the rising edge of both RCBP and RCBN in half clock mode.

Table 13. Receiver Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RXAP RXAN	Diff. LVPECL	I	B5 A4	Differential LVPECL compatible inputs for channel A. RXAP is the positive input, RXAN is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RXBP RXBN	Diff. LVPECL	I	B10 A11	Differential LVPECL compatible inputs for channel B. RXBP is the positive input, RXBN is the negative. Internally biased to VDD-1.3V for AC coupled applications.

Table 14. Receiver Control Signals

Pin Name	Level	I/O	Pin #	Description
LPEN	TTL	I	C14	Loopback Enable. When Low, input source is the high speed serial input for each channel. When High, the serial output for each channel is looped back to its input.
CMODE	TTL	I	C2	Clock Mode Control. When Low, the parallel output clocks (RCxP/N) rate is equal to 1/2 the data rate. When High, the parallel output clocks (RCxP/N) rate is equal to the data rate.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 15. Power and Ground Signals

Pin Name	Qty.	Pin #	Description
VDDA	3	B8, B13, C5	Analog Power (VDD) low noise.
VSSA	3	A8, B4, C13	Analog Ground (VSS).
VDD	3	A10, B12, C6	Power for High Speed Circuitry (VDD).
VSS VSSSUB	8	A3, A5, A7, A12, A14, C8, C10, C12	Ground for High Speed Circuitry (VSS).

Table 15. Power and Ground Signals (Continued)

Pin Name	Qty.	Pin #	Description
PECLPWR	2	G14, J16	PECL Power (VDD).
PECLGND	3	C16, D15, F16	PECL Ground (VSS).
DIGPWR	5	B2, C1, D2, K16, N1	Core Circuitry Power (VDD).
DIGGND	8	C3, D1, E2, E3, J14, K15, P1, T1	Core Circuitry Ground (VSS).
TTLPWR	9	F1, G3, H1, M2, N3, P9, R4, R8, T7	Power for TTL I/O (VDD).
TTLGND	11	E1, F2, F3, K3, M3, N2, P3, T2, T4, T8, T11	Ground for TTL I/O (VSS).
PWR	3	A2, A16, B9	Power.
GND	10	A6, A9, B1, B3, B6, C9, E16, F15, H15, H16	Ground.
CAP1 CAP2	2	A15 B14	Pins for external loop filter capacitor.
NC	20	A1, B7, B16, C4, C7, C15, D14, E14, F14, H14, P13, P14, R2, R9, R14, R15 T6, T9, T10, T16	Not Connected. Used as Test Pins. Do Not Connect.

Figure 9. S2062 Pinout (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
1	NC	GND	DIGPWR	DIGGND	TTLGND	TTLPWR	EOFA	TTLPWR	DOUTA2	DOUTA4	DOUTA6	RCAP	DIGPWR	DIGGND	KFLAGB	DIGGND
2	PWR	DIGPWR	CMODE	DIGPWR	DIGGND	TTLGND	KFLAGA	DOUTA0	ERRA	DOUTA5	DOUTA7	TTLPWR	TTLGND	EOFB	NC	TTLGND
3	VSSSUB	GND	DIGGND	TEST MODE	DIGGND	TTLGND	TTLPWR	DOUTA1	DOUTA3	TTLGND	RCAN	TTLGND	TTLPWR	TTLGND	DOUTB0	DOUTB2
4	RXAN	VSSA	NC											ERRB	TTLPWR	TTLGND
5	VSS	RXAP	VDDA											DOUTB1	DOUTB3	DOUTB6
6	GND	GND	VDD											DOUTB4	DOUTB5	NC
7	VSSSUB	NC	NC											RCBN	RCBP	TTLPWR
8	VSSA	VDDA	VSSSUB											DOUTB7	TTLPWR	TTLGND
9	GND	PWR	GND											TTLPWR	NC	NC
10	VDD	RXBP	VSS											DINA0	TCLKA	NC
11	RXBN	CLKSEL	RATE											DINA4	DINA2	TTLGND
12	VSSSUB	VDD	VSSSUB											DINA7	DINA5	DINA1
13	TMODE	VDDA	VSSA											NC	KGENA	DINA3
14	VSS	CAP2	LPEN	NC	NC	NC	PECL PWR	NC	DIGGND	TCLKO	KGENB	DINB5	DINB2	NC	NC	DINA6
15	CAP1	RESET	NC	PECL GND	TXAN	GND	TXBP	GND	REFCLK	DIGGND	SOFB	DINB6	DINB3	DINB0	NC	SOFA
16	PWR	NC	PECLGND	TXAP	GND	PECL GND	TXBN	GND	PECL PWR	DIGPWR	TEST MODE1	DINB7	DINB4	DINB1	TCLKB	NC

Note: NC used as Test Pins. Do Not Connect.

Figure 10. S2062 Pinout (Top View)

	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
	DIGGND	KFLAGB	DIGGND	DIGPWR	RCAP	DOUTA6	DOUTA4	DOUTA2	TTLPWR	EOFA	TTLPWR	TTLGND	DIGGND	DIGPWR	GND	NC	**1**
	TTLGND	NC	EOFB	TTLGND	TTLPWR	DOUTA7	DOUTA5	ERRA	DOUTA0	KFLAGA	TTLGND	DIGGND	DIGPWR	CMODE	DIGPWR	PWR	**2**
	DOUTB2	DOUTB0	TTLGND	TTLPWR	TTLGND	RCAN	TTLGND	DOUTA3	DOUTA1	TTLPWR	TTLGND	DIGGND	TEST MODE	DIGGND	GND	VSSSUB	**3**
	TTLGND	TTLPWR	ERRB											NC	VSSA	RXAN	**4**
	DOUTB6	DOUTB3	DOUTB1											VDDA	RXAP	VSS	**5**
	NC	DOUTB5	DOUTB4											VDD	GND	GND	**6**
	TTLPWR	RCBP	RCBN											NC	NC	VSSSUB	**7**
	TTLGND	TTLPWR	DOUTB7											VSSSUB	VDDA	VSSA	**8**
	NC	NC	TTLPWR											GND	PWR	GND	**9**
	NC	TCLKA	DINA0											VSS	RXBP	VDD	**10**
	TTLGND	DINA2	DINA4											RATE	CLKSEL	RXBN	**11**
	DINA1	DINA5	DINA7											VSSSUB	VDD	VSSSUB	**12**
	DINA3	KGENA	NC											VSSA	VDDA	TMODE	**13**
	DINA6	NC	NC	DINB2	DINB5	KGENB	TCLKO	DIGGND	NC	PECL PWR	NC	NC	NC	LPEN	CAP2	VSS	**14**
	SOFA	NC	DINB0	DINB3	DINB6	SOFB	DIGGND	REFCLK	GND	TXBP	GND	TXAN	PECL GND	NC	RESET	CAP1	**15**
	NC	TCLKB	DINB1	DINB4	DINB7	TEST MODE1	DIGPWR	PECL PWR	GND	TXBN	PECL GND	GND	TXAP	PECLGND	NC	PWR	**16**

Note: NC used as Test Pins. Do Not Connect.

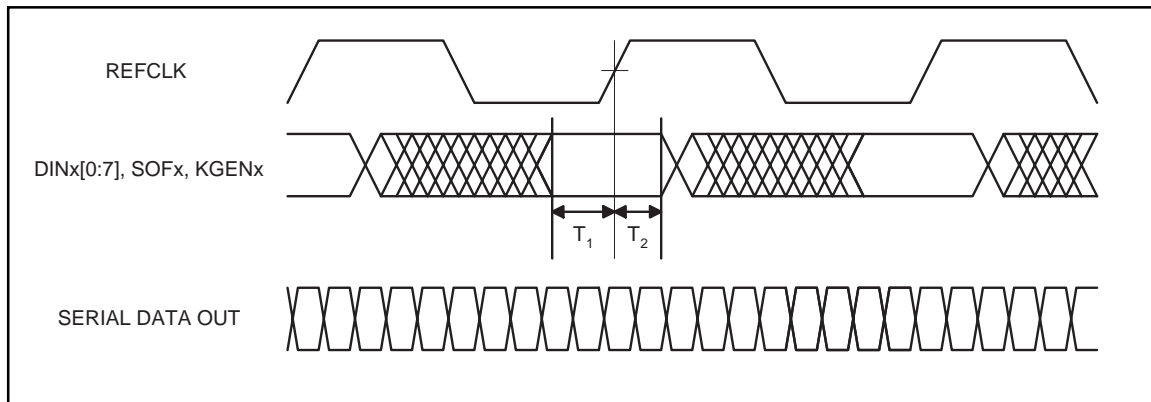**Figure 11. Compact 21mm x 21mm 156 TBGA Package**
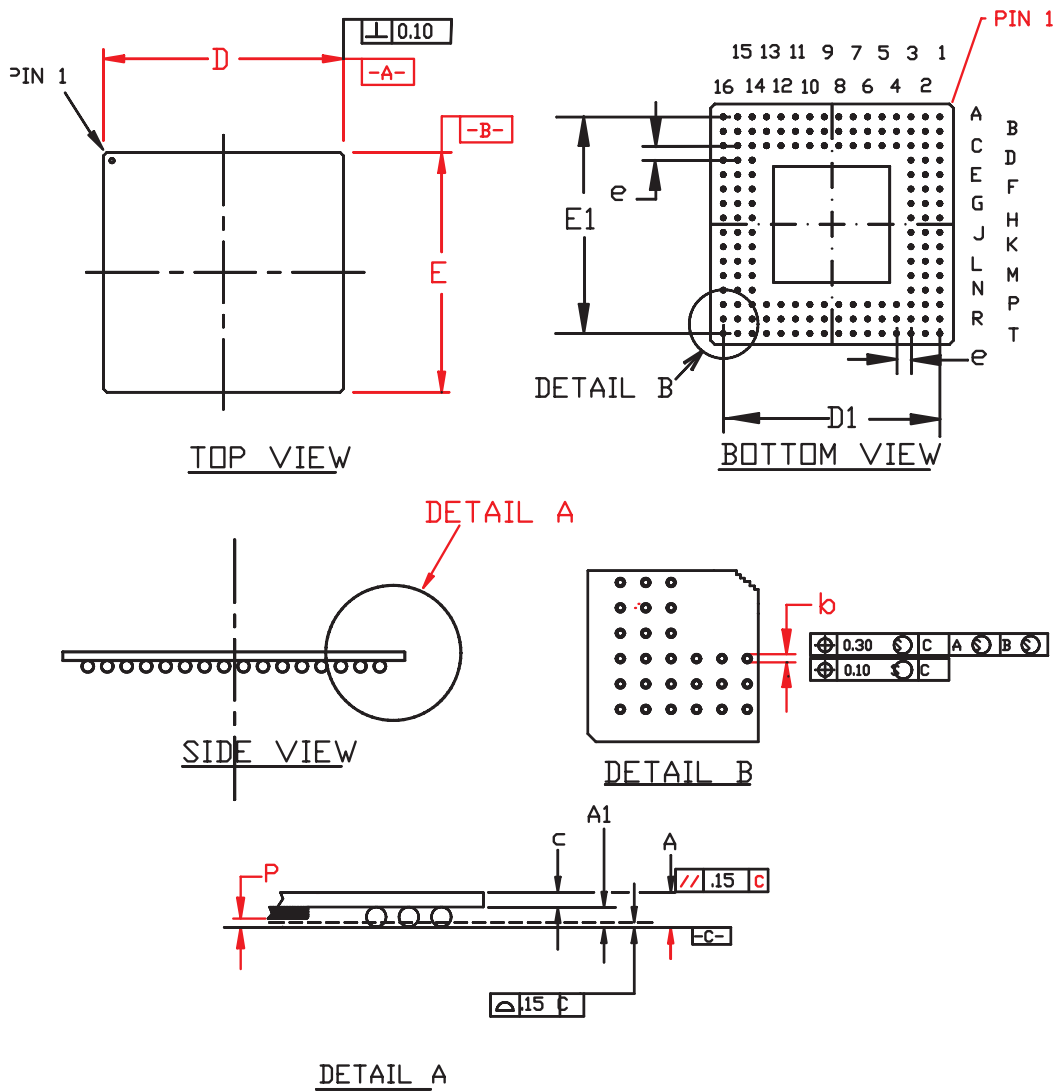
DIMENSIONS (are in millimeters)										
UNIT	A	A₁	D	D₁	E	E₁	P	b	c	e
MIN	1.45	0.60	20.80	19.05 BSC.	20.80	19.05 BSC.		0.65	0.85	1.27 BSC.
NOM	1.55	0.65	21.00		21.00			0.75	0.90	
MAX	1.65	0.70	21.20		21.20		0.25	0.85	0.95	

Thermal Management

Device	Θja	Θjc
S2062	19.8°C/W	3.5°C/W

Figure 12. Transmitter Timing (REFCLK Mode, TMODE = 0)

Table 16. S2062 Transmitter Timing (REFCLK Mode, TMODE = 0)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ REFCLK	0.5	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ REFCLK	1.3	-	ns	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 13. Transmitter Timing (TCLK Mode, TMODE = 1)
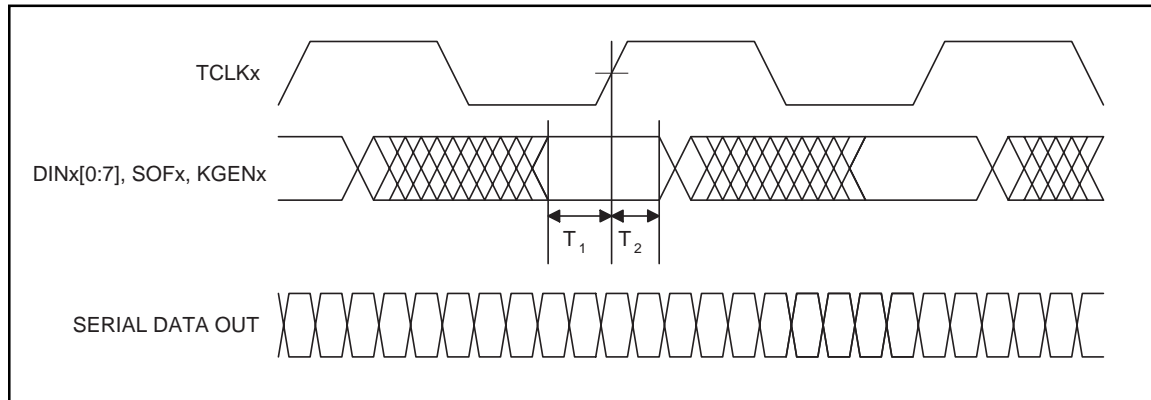
Table 17. S2062 Transmitter Timing (TCLK Mode, TMODE = 1)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ TCLK	1.0	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ TCLK	0.5	-	ns	
	Phase drift between TCLKx and REFCLK	-3	+3	ns	

1. All AC measurements are made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 14. Receiver Timing (Full Clock Mode, CMODE = 1)
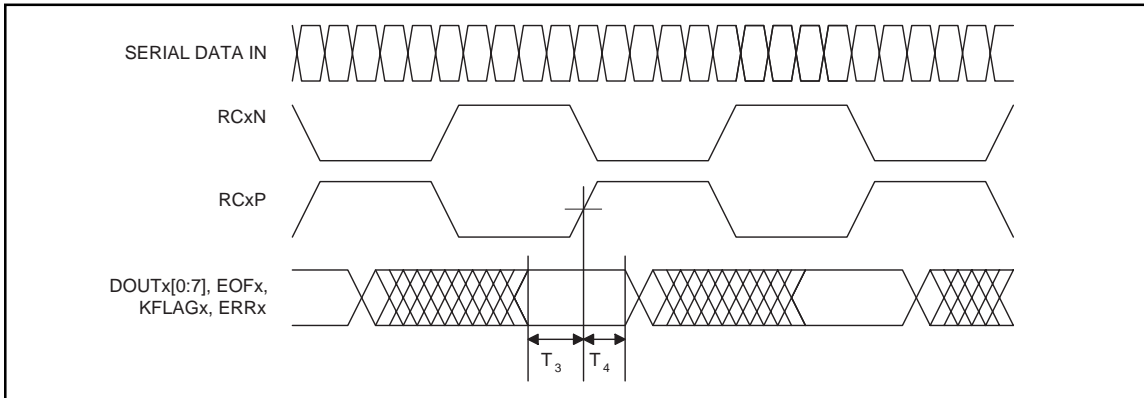
Figure 15. Receiver Timing (Half Clock Mode, CMODE = 0)
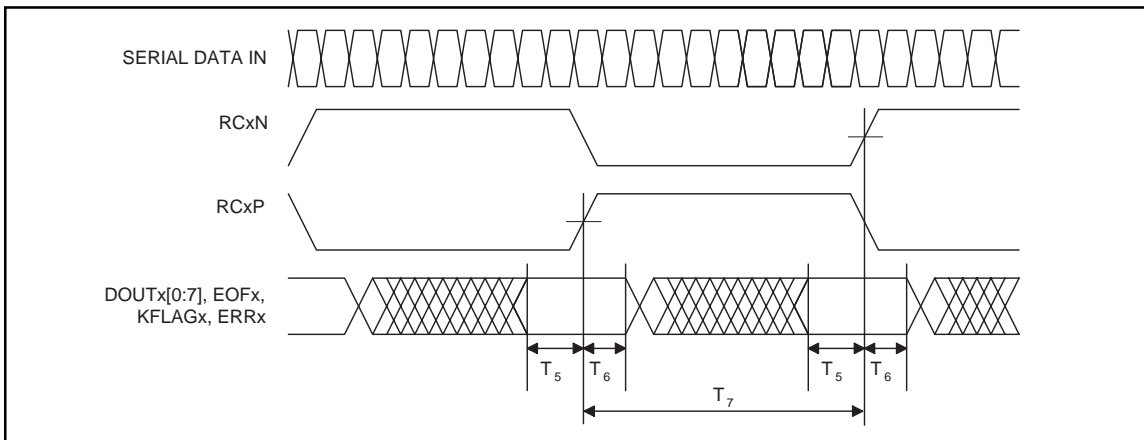
Table 18. S2062 Receiver Timing (Full and Half Clock Mode)

Parameters	Description	Min	Max	Units	Conditions
T_3	Data Setup w.r.t. ↑RCxP/N	2.75 3.5		ns	at 1.25 Gbps at 1.062 Gbps[1]
T_4	Data Hold w.r.t. ↑RCxP/N	2.0		ns	
T_5	Data Setup w.r.t. ↑RCxP/N	2.5 3.5		ns	at 1.25 Gbps at 1.062 Gbps[1]
T_6	Data Hold w.r.t. ↑RCxP/N	2.0		ns	
T_7	Time from RCxP rise to RCxN rise	7.8 9.3	8.82 10.4	ns ns	at 1.25 Gbps at 1.062 Gbps[1]
T_{RP}, T_{FP}	RCxP Rise and Fall Times		3.0	ns	See Figure 18.
T_{RN}, T_{FN}	RCxN Rise and Fall Times		3.0	ns	See Figure 18.
T_{DR}, T_{DF}	DOUTx Rise and Fall Times		3.0	ns	See Figure 17.
Duty Cycle	RCxP/N Duty Cycle	40	60	%	

1. Measurements made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 16. TCLKO Timing
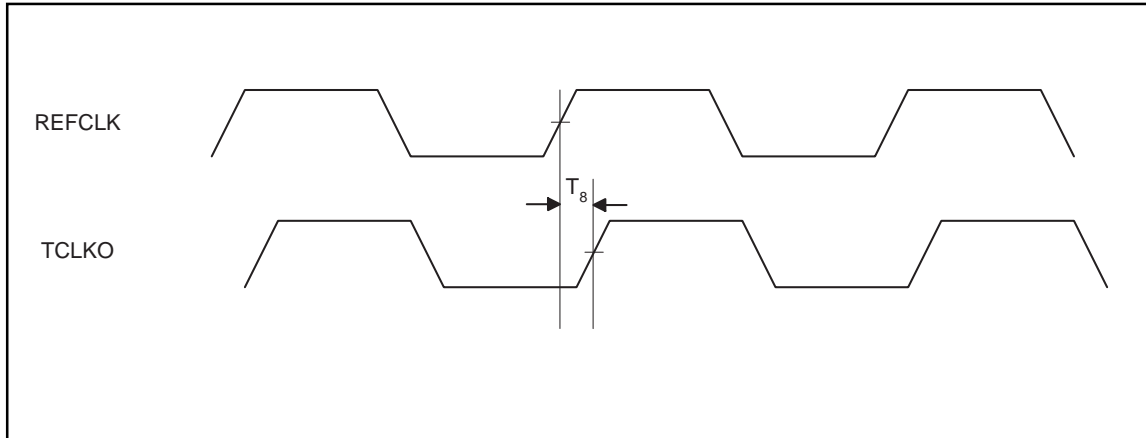
Table 19. S2062 Transmitter (TCLKO Timing)

Parameters	Description	Min	Max	Units	Conditions
T_8	↑ TCLKO w.r.t. ↑ REFCLK	2	7.5	ns	
	TCLKO Duty Cycle	40%	60%	%	

Note: Measurements are made at 1.4V level of clocks.

Table 20. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	-55		125	˚C
Junction Temperature Under Bias	-55		150	˚C
Storage Temperature	-65		150	˚C
Voltage on VDD with Respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.5		3.47	V
Voltage on any PECL Input Pin	0		VDD	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			30	mA
Static Discharge Voltage, TTL I/O		2000		V
Static Discharge Voltage, PECL I/O		1500		V

Table 21. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on any Power Pin with respect to GND/VSS	3.13	3.3	3.47	V
Voltage on TTL Input Pin	0		3.47	V
Voltage on any PECL Input Pin	VDD -2V		VDD	V

Table 22. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% - 80%.
—	Jitter		80	ps	Peak-to-Peak, to maintain ≥ 77% eye opening.

Table 23. Serial Data Timing, Transmit Outputs

Parameters	Description	Min	Typ	Max	Units	Comments
Total Jitter	Serial Data Output total jitter			192	ps	Peak-to-Peak.
T_{DJ}	Serial Data Output deterministic jitter			80	ps	Peak-to-Peak.
T_{SR}, T_{SF}	Serial Data Output rise and fall time			300	ps	20% - 80%. 4.5 kΩ to ground.

Table 24. Serial Data Timing, Receive Inputs

Parameters	Description	Min	Typ	Max	Units	Comments
T_{LOCK} (Frequency)	Frequency Acquisition Lock Time (Loss of Lock) (1.25 Gbps)			175	µs	8B/10B idle pattern sample basis, from device start up.
T_{LOCK} (Phase)	Phase Acquisition Lock Time (Phase Discontinuity) (1.25 Gbps)			150	ns	90% Input data eye (see Figure 22).
				180	ns	70% Input data eye.
T_{DJ}	Deterministic Input Jitter Tolerance	370			ps	
Input Jitter Tolerance	Serial Data Input total jitter tolerance	599			ps	Peak-to-Peak, as specified by IEEE 802.3z.
R_{SR}, R_{SF}	Serial Data Input rise and fall time			350	ps	20% - 80%.

Table 25. DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL)	2.4	2.8	VDD	V	VDD = min I_{OH} = -4mA
V_{OL}	Output Low Voltage (TTL)	GND	.025	0.5	V	VDD = min I_{OL} = 4mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4V, VDD = Max
I_{IL}	Input Low Current (TTL)			600	µA	V_{IN} = 0.8V, VDD = Max
IDD	Supply Current		415	533	mA	1010 Pattern.
P_D	Power Dissipation		1.37	1.84	W	1010 Pattern.
V_{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		2200	mV	See Figure 20.
ΔV_{OUT}	Differential Serial Output Voltage Swing	1500	1900	2200	mV	AC coupled with 4.5 kΩ pulldown and 100 Ω differential termination. See Figure 19.
C_{IN}	Input Capacitance			3	pf	

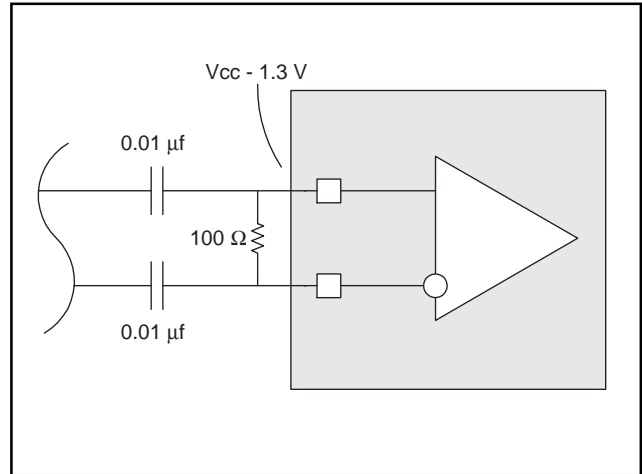## OUTPUT LOAD

The S2062 serial outputs require a resistive load to set the output current. The recommended resistor value is 4.5 kΩ to ground. This value can be varied to adjust drive current, signal voltage swing, and power usage on the board.
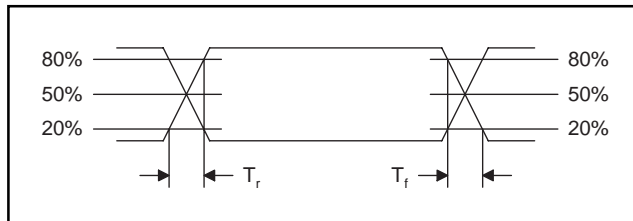
ACQUISITION TIME

With the input eye diagram shown in Figure 22, the S2062 will recover data with a ≤1E-9 BER within the time specified by T_{LOCK} in Table 24 after an instantaneous phase shift of the incoming data.
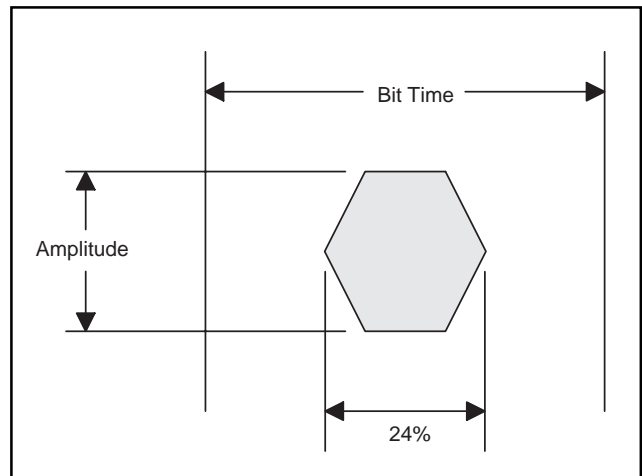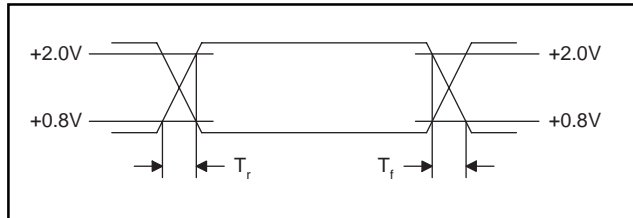
Figure 20. High Speed Differential Inputs

Figure 17. Serial Input/Output Rise and Fall Time

Figure 18. TTL Input/Output Rise and Fall Time

Figure 19. Serial Output Load

Figure 21. Receiver Input Eye Diagram Jitter Mask
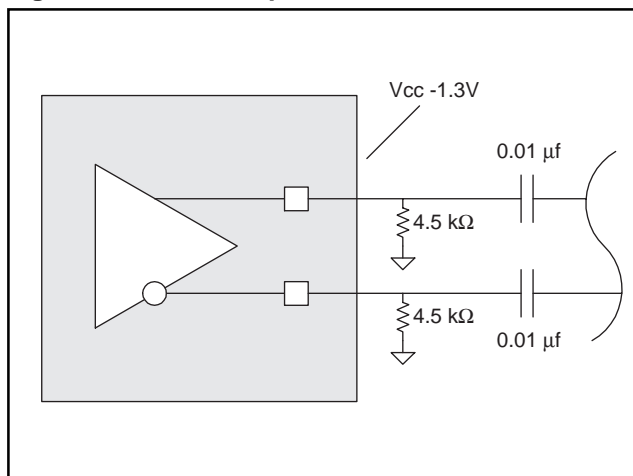
Figure 22. Acquisition Time Eye Diagram
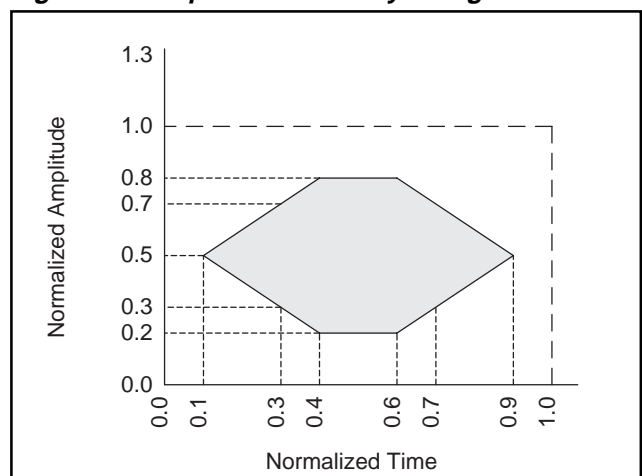
Figure 23. Loop Filter Capacitor Connections
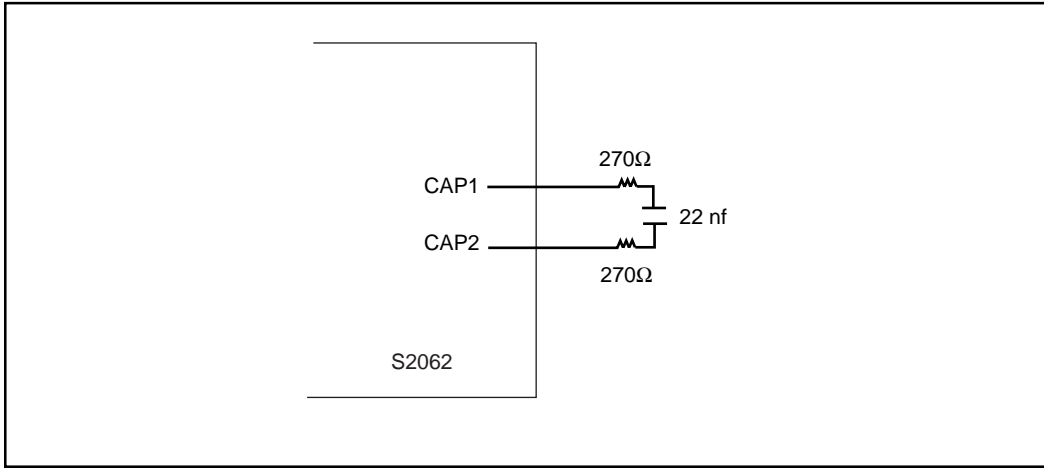
Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	2062	TB – 156 TBGA

<u>X</u> <u>XXXX</u> <u>X</u>
Prefix   Device   Package

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