REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device types 03 and 04; added vendor CAGE code 65896 as vendor for device type 01. Modified figure 3 waveforms. Editorial changes throughout.	92-08-04	M. L. Poelking

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

SC N/A

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DRAWING APPROVAL DATE
7 November 1989

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS 64-BIT OUTPUT CORRELATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89711

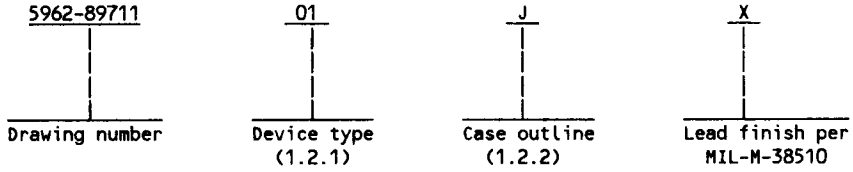
SHEET 1

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Correlation Rate
01	TMC2023V, L10C23	CMOS digital output correlator, 64-bit	25 MHz
02	TMC2023V1	CMOS digital output correlator, 64-bit	30 MHz
03	TMC2023V2	CMOS digital output correlator, 64-bit	35 MHz
04	TMC2023V3	CMOS digital output correlator, 64-bit	50 MHz

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line package
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
3	CQCC1-N28	28	Square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to V_{DD} + 0.5 V dc
Applied output voltage range 1/	-0.5 V dc to V_{DD} + 0.5 V dc
Forced output current range 2/	-3.0 mA to +6.0 mA
Output short circuit duration 3/	1.0 second
Power dissipation, unloaded (P_D): 4/	
Device type 01	305 mW
Device type 02	415 mW
Device type 03	415 mW
Device type 04	550 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case outlines J, L, and 3	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1/ Applied voltage must be current-limited to specified range and measured with respect to ground.

2/ Forcing voltage must be limited to specified range.

3/ Applies to single output in high state to ground.

4/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	4.5 V dc to 5.5 V dc
Clock pulse width, low, clocks, LDR (t_{PWL}):	
Device type 01	15 ns minimum
Device type 02	14 ns minimum
Device type 03	14 ns minimum
Device type 04	10 ns minimum
Clock pulse width, high, clocks, LDR (t_{PWH}):	
Device type 01	15 ns minimum
Device type 02	14 ns minimum
Device type 03	14 ns minimum
Device type 04	8 ns minimum
Data input setup time, correlator, IO_{0-6} (t_{SCOR}):	
Device type 01	14 ns minimum
Device type 02	10 ns minimum
Device type 03	10 ns minimum
Device type 04	10 ns minimum
Data input setup time, shift register, A_{IN}, B_{IN}, M_{IN} (t_{SSR}):	
Device type 01	13 ns minimum
Device type 02	10 ns minimum
Device type 03	10 ns minimum
Device type 04	9 ns minimum
Data input hold time, A_{IN}, B_{IN}, M_{IN}, IO_{0-6} (t_H)	0 ns minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Input high voltage (V_{IH})	2.0 V dc minimum
Input high voltage, A, B, M, S Clks (V_{IHC})	2.4 V dc minimum
Output low current (I_{OL})	4.0 mA maximum
Output high current (I_{OH})	-2.0 mA minimum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Quiescent supply current	I_{DDQ}	V_{DD} = 5.5 V, V_{IN} = 0 V, T_S = 5.0 V		1,2,3	All		10	mA
Dynamic supply current	I_{DD}	V_{DD} = 5.5 V, T_S = 5.0 V	f = 25 MHz	1,2,3	01		55	mA
			f = 30 MHz 2/		02		75	mA
			f = 35 MHz 2/		03		75	mA
			f = 50 MHz 2/		04		100	mA
Input low current	I_{IL}	V_{DD} = 5.5 V, V_{IN} = 0 V		1,2,3	All		-20	µA
Input high current	I_{IH}	V_{DD} = 5.5 V, V_{IN} = V_{DD}		1,2,3	All		+20	µA
Output low voltage	V_{OL}	V_{DD} = 4.5 V, V_{IN} = 0.8 V, 2.0 V	I_{OL} = 4.0 mA	1,2,3	All		0.4	V
Output high voltage	V_{OH}		I_{OH} = -2.0 mA	1,2,3	All	2.4		V
Three-state output leakage current, output low 3/	I_{OZL}	V_{DD} = 5.5 V, V_{IN} = 0 V		1,2,3	All		-40	µA
Three-state output leakage current, output high 3/	I_{OZH}	V_{DD} = 5.5 V, V_{IN} = 5.5 V		1,2,3	All		+40	µA
Output short-circuit current 2/ 4/	I_{OS}	V_{DD} = 5.5 V, output high, one pin to ground, t = 1.0 sec maximum		1,2,3	All		-125	mA
Input capacitance	C_{IN}	T_A = 25°C, f = 1.0 MHz, see 4.3.1c		4	All		10	pF
Output capacitance	C_{OUT}	T_A = 25°C, f = 1.0 MHz, see 4.3.1c		4	All		10	pF
Functional tests		V_{DD} = 5.0 V, see 4.3.1d		7,8	All			
Clk frequency, correlator, shift register and flag 5/ 6/	F_{CLK}	V_{DD} = 4.5 V, see figure 3		7,8	01	25		MHz
					02	30		MHz
					03	35		MHz
					04	50		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital output delay, correlator 5/	t_{DCOR}	V_{DD} = 4.5 V, see figure 3	9,10,11	01	4 2/	25	ns
				02	4 2/	20	ns
				03	4 2/	20	ns
				04	4 2/	18	ns
Digital output delay, shift register 5/	t_{DSR}		9,10,11	01	4 2/	25	ns
				02	4 2/	22	ns
				03	4 2/	22	ns
				04	4 2/	20	ns
Digital output delay, flag 5/	t_{DF}		9,10,11	01	4 2/	22	ns
				02	4 2/	19	ns
				03	4 2/	19	ns
				04	4 2/	17	ns
Three-state output enable delay	t_{ENA}		9,10,11	01		25	ns
				02		20	ns
				03		20	ns
				04		18	ns
Three-state output disable delay	t_{DIS}		9,10,11	01		24	ns
				02		18	ns
				03		18	ns
				04		16	ns

1/ All testing will be performed under worst-case conditions unless otherwise specified.

2/ If not tested, shall be guaranteed to the limits specified in table I.

3/ Due to the IO_{0-6} and T register interconnections, these values are the I_{IH} and I_{IL} of the T register outputs.

4/ Not more than one output should be shorted at a time. Maximum duration of one second.

5/ All transitions are measured at a 1.5 V level. Inputs are driven at V_{IL} = 0 V and V_{IH} = 3.0 V during dynamic testing.

6/ Not directly tested, but verified during functional tests by operating the device at the specified frequency.

Device types	All	
Case Outlines	J and L	3
Terminal number	Terminal symbol	
1	V_{DD}	V_{DD}
2	M_{IN}	V_{DD}
3	A_{IN}	M_{IN}
4	B_{IN}	A_{IN}
5	CLK T	NC
6	CLK S	B_{IN}
7	INV	CLK T
8	TS	CLK S
9	IO_6	INV
10	IO_5	TS
11	IO_4	IO_6
12	IO_3	IO_5
13	IO_2	IO_4

FIGURE 1. Terminal Connections

Device types	All	
Case Outlines	J and L	3
Terminal number	Terminal symbol	
14	IO_1	IO_3
15	IO_0	IO_2
16	GND	IO_1
17	TFLG	IO_0
18	B_{OUT}	NC
19	A_{OUT}	GND
20	M_{OUT}	GND
21	LDR	TFLG
22	CLK A	B_{OUT}
23	CLK M	A_{OUT}
24	CLK B	M_{OUT}
25	---	LDR
26	---	CLK A
27	---	CLK M
28	---	CLK B

FIGURE 1. Terminal Connections - Continued.

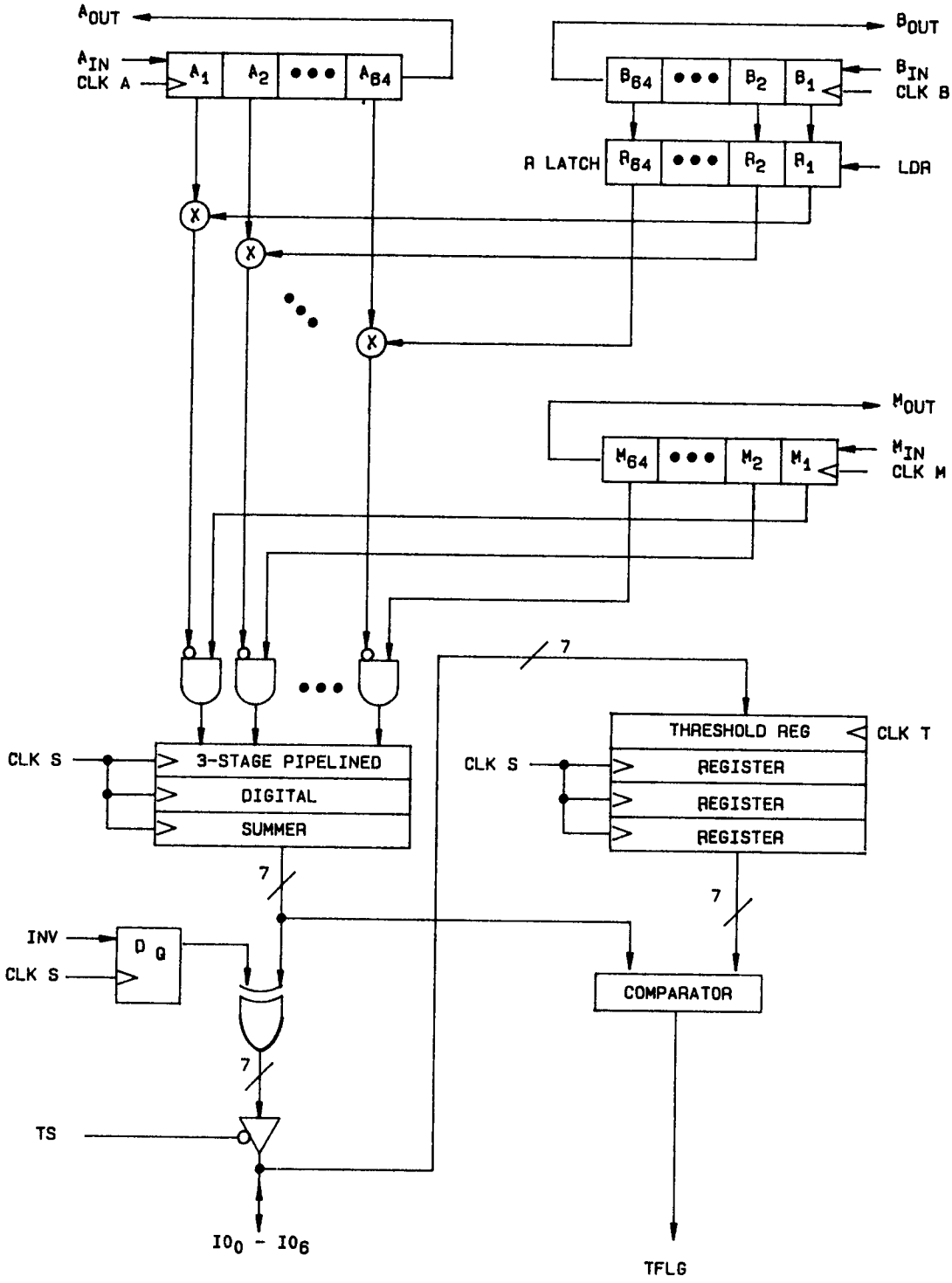


FIGURE 2. Block Diagram.

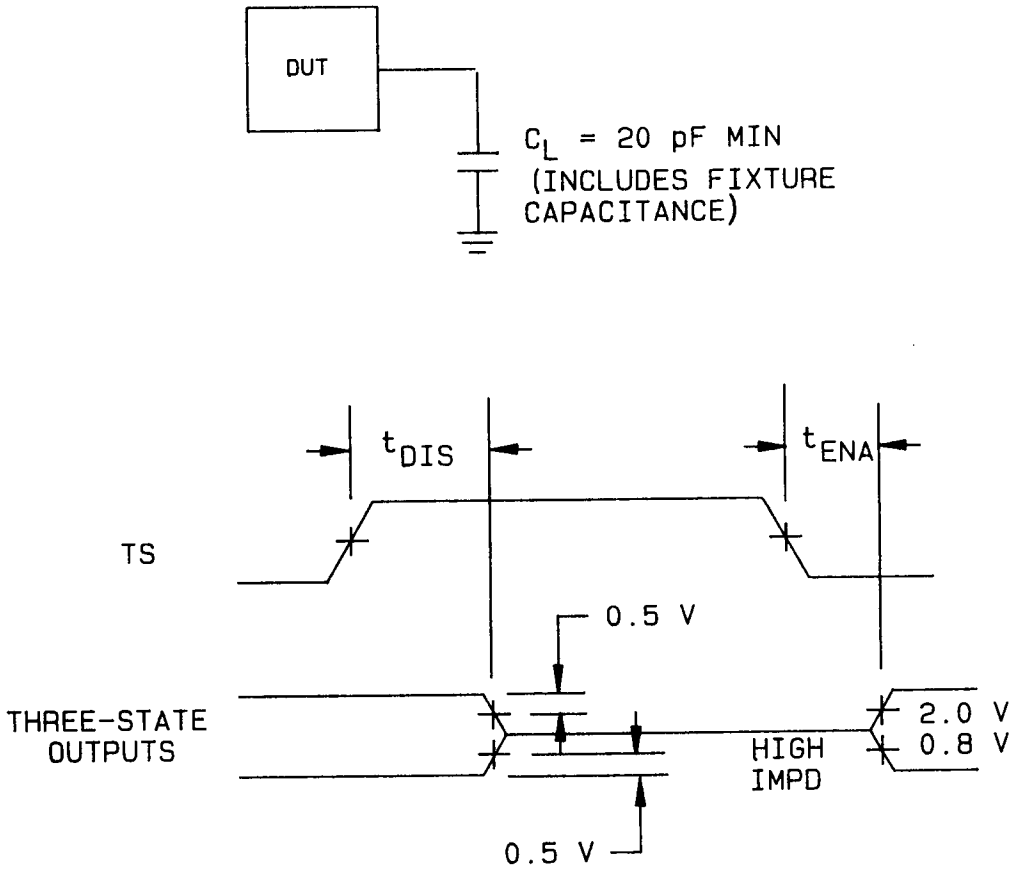
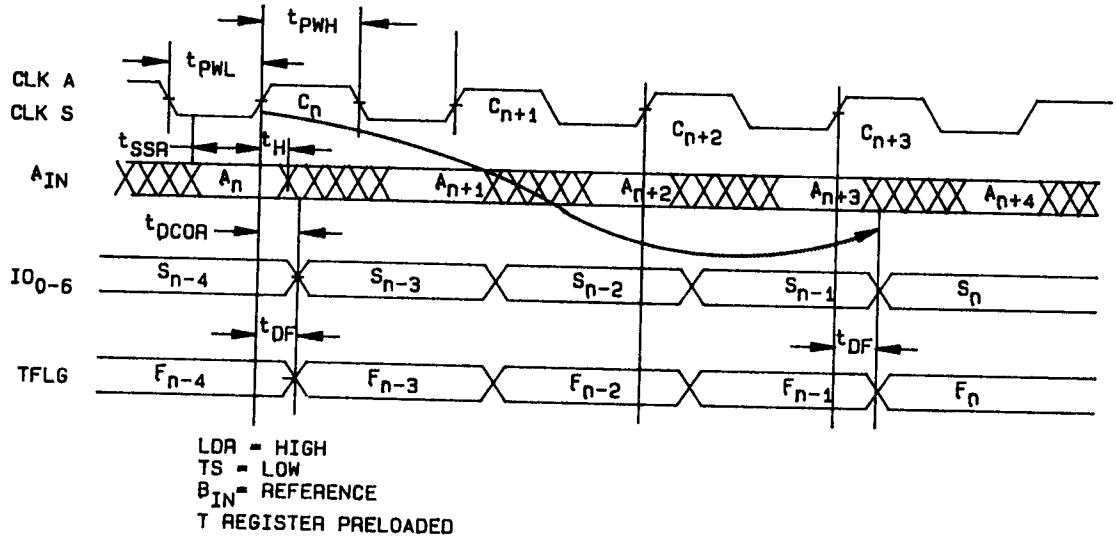


FIGURE 3. Switching times test circuit and waveforms.

Continuous correlation



Cross-correlation

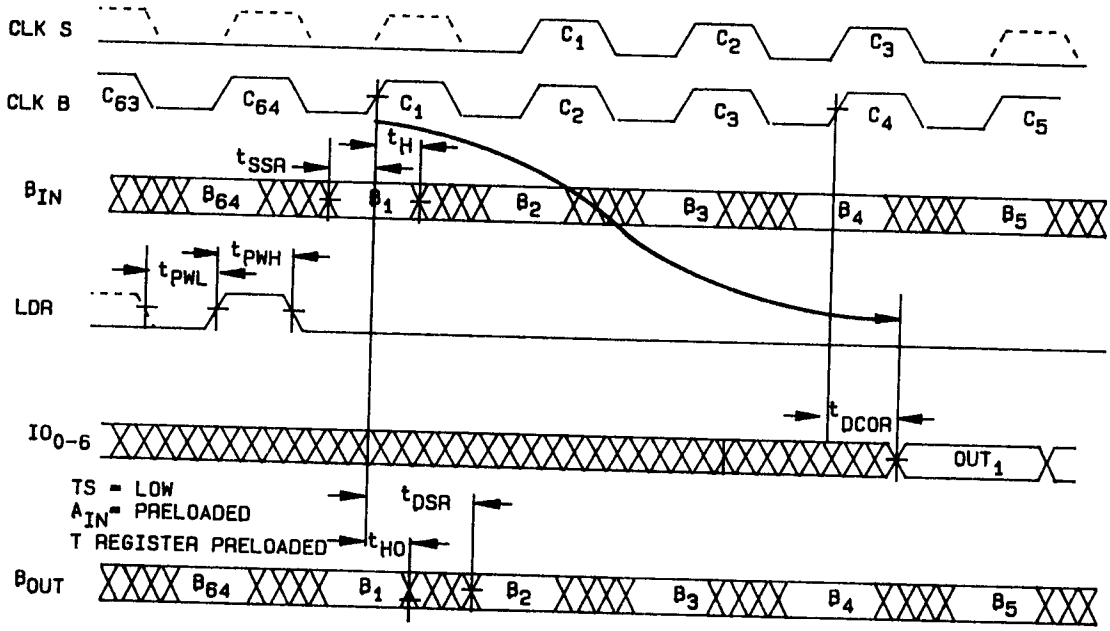
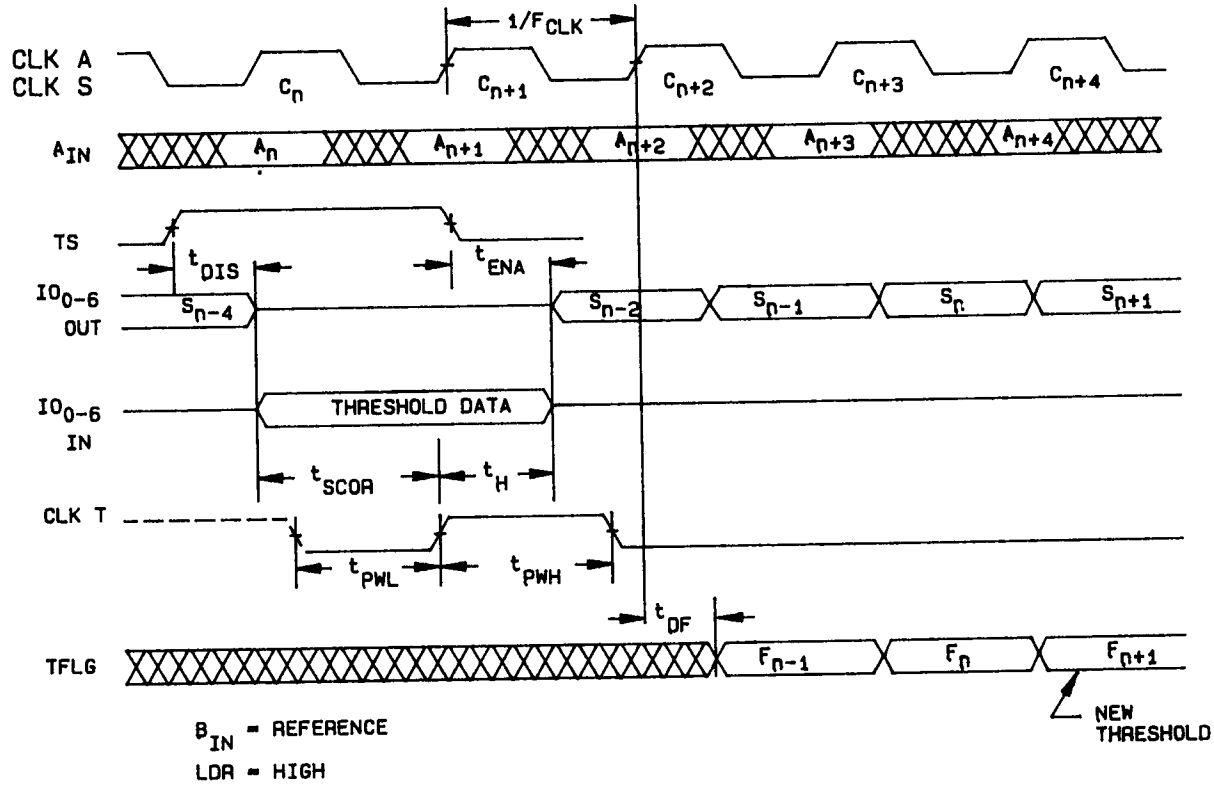
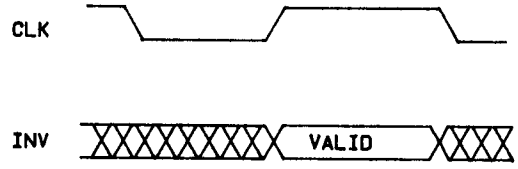


FIGURE 3. Switching times test circuit and waveforms - Continued.

Threshold register load



Invert control timing (see note)



NOTE: The INV control must be asserted on or before the rising edge of CLK, and held in the desired state until after the falling edge of CLK.

FIGURE 3. Switching times test circuit and waveforms - Continued.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN/OUT}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available from the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 7, 9

*PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECT, telephone (513) 296-6022.

6.5 Symbols, definitions, and functional descriptions. See table III.

6.6 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

TABLE III. Pin functions.

Pin Number	Pin functions
V_{DD}, GND	The device operates from a single +5.0 V supply. All V_{DD} and GND pins must be connected.
INV	Control that inverts the 7-bit digital output. When a high level is applied to this pin, the outputs IO_{0-6} are logically inverted. See figure 3 for constraints if this is to be clocked.
TS	Control that enables the three-state output. When a high level is applied to this pin, it forces outputs into the high-impedance state.
LDR	Control that allows parallel data to be loaded from the B register into the reference latch for correlations. If LDR is held high, the R latch is transparent.
CLK A, CLK B, CLK M	Input clocks. Clock input pins for the A, B, and M registers respectively. Each register may be independently clocked.
CLK T	Threshold register clock. Clock input for T register.
CLK S	Digital summer clock. Clock input that allows independent clocking of pipelined summer network.
M_{IN}	Mask register input allows the user to choose "no-compare" bit positions. A "0" in any bit location will result in a no-compare state for that location.
A_{IN}, B_{IN}	Shift register inputs to the A and B 64-bit serial registers.
IO_{0-6}	Bi-directional data pins. When outputs are enabled, (TS low), data is a 7-bit binary representation of the correlation between the unmasked portions of the R latch and the A register. IO_6 is the MSB. These pins also serve as parallel inputs to load the threshold register. Data present one setup time before CLK T goes high will be latched into the threshold register.
TFLG	The TFLG output goes high whenever the correlation score is equal to or greater than the number loaded into the T register (0 to 64).
A_{OUT}, B_{OUT}, M_{OUT}	Shift register outputs of the three 64-bit shift registers: A, B, and M respectively. These outputs may be used to cascade the device.