ANALOG DEVICES

Fast, 16-Bit, 100 kSPS A/D Converter with Serial Interface

SMD/883B AD677

Scope

This specification covers the detail requirements for a 16-bit resolution, sampling A/D converter with a serial output interface. The electrical specifications match the Standard Microcircuit Drawing (SMD) 5962-95592 in effect at the release of this data sheet. For a copy of the latest official SMD, contact DESC-ELDS.

Part Number/Case Outline

For case outline dimensions, see Package Information Appendix of General Specification ADI-M-1000. The complete part numbers of these SMD and 883 devices are as follows:

Device Type	SMD Part Number	ADI 883B Part Number	Package Description	Package Designation ADI	Package Designation MIL-STD-1835
01	5962-9559201MEA	AD677TD/883B	16-Pin Side Braze Ceramic DIP	D-16	CDIP2-T16

Absolute Maximum Ratings (T_A = +25°C unless otherwise noted)[1]

V_{CC} to V_{EE} ..... −0.3 V to +26.4 V
V_{DD} to DGND ..... −0.3 V to +7 V
V_{CC} to AGND ..... −0.3 V to +18 V
V_{EE} to AGND ..... −18 V to +0.3 V
AGND to DGND ..... ±0.3 V
Digital Inputs (CAL, SAMPLE, CLK) to DGND ..... 0 V to +5.5 V
Analog Inputs (V_{IN}, V_{REF}, AGND SENSE) to AGND ..... (V_{CC} + 0.3 V) to (V_{EE} − 0.3 V)
Power Dissipation (P_D) 10 V ..... 630 mW
Power Dissipation (P_D) 5 V ..... 530 mW
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Recommended Operating Conditions[2]

Ambient Operating Temperature Range (T_A) ..... −55°C to +125°C
Positive Analog Supply Voltage (V_{CC}) ..... 11.4 V to 12.6 V
Negative Analog Supply Voltage (V_{EE}) ..... −11.4 V to −12.6 V
Digital Supply Voltage (V_{DD}) ..... 4.5 V to 5.5 V
Analog Reference Voltage (V_{REF}) ..... 5 V to 10 V
Analog Input Voltage Range (V_{IN}) ..... $-V_{REF}$ to V_{REF}
Analog Ground Sense Voltage ..... −0.1 V to 0.1 V

Thermal Characteristics

Thermal Resistance, Junction-to-Case (θ_{JC}) ..... 15°C/W
Thermal Resistance, Junction-to-Ambient (θ_{JA}) ..... 80°C/W

NOTES
[1]Permanent damage may occur if any absolute maximum rating is exceeded. Functional operation is not implied and device reliability may be impaired by exposure to higher-than-recommended voltages for extended periods of time.
[2]AGND and DGND tied at ADC.

REV. A

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AD677—SPECIFICATIONS

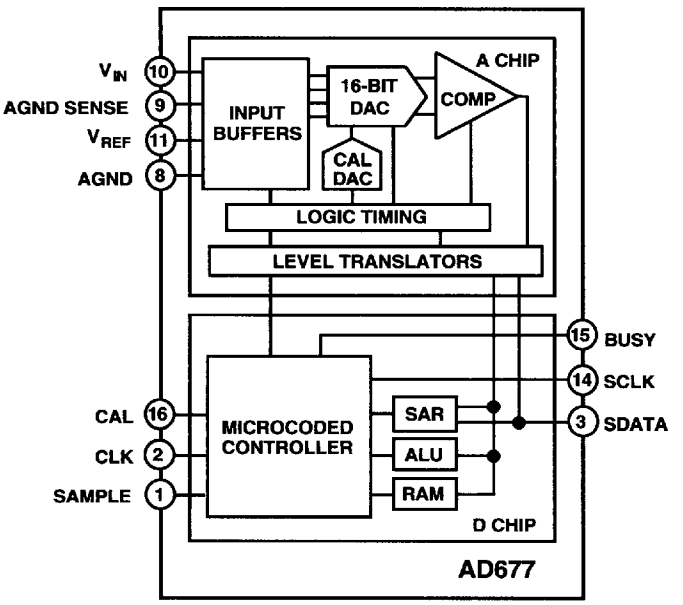
Table 1. Electrical Performance Characteristics

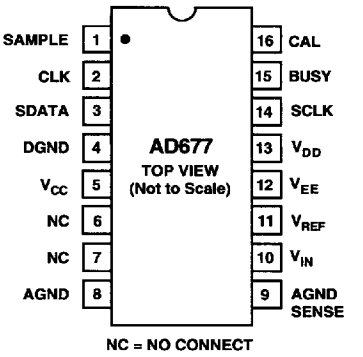
Test	Symbol	Conditions V_{CC} = +12 V, V_{EE} = –12 V, V_{DD} = +5 V, V_{REF} = 10 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V unless otherwise specified	Group A Subgroups	Device Type	Limits Min	Limits Max	Units
Logic Input High Voltage	V_{IH}		1, 2, 3	01	2.0		V
Logic Input Low Voltage	V_{IL}		1, 2, 3	01		0.8	V
Logic Input Current	I_{LIN}	V_{IH} = 5 V; V_{IL} = 0 V	1, 2, 3	01	–10	+10	µA
Logic Output High Voltage	V_{OH}	I_{OH} = 0.5 mA	1, 2, 3	01	2.4		V
Logic Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA	1, 2, 3	01		0.4	V
Power Supply Current	I_{CC}	V_{REF} = 10 V, Device Converting	1, 2, 3	01		24	mA
	I_{EE}					–24	mA
	I_{DD}					5	mA
	I_{CC}	V_{REF} = 5 V, Device Converting	1, 2, 3	01		20	mA
	I_{EE}					–20	mA
	I_{DD}					5	mA
Power Dissipation	P_D	10 V	1, 2, 3	01		630	mW
		5 V				530	
Integral Nonlinearity	INL	All Codes	1	01		±1.5	LSB
			2, 3			±2	
Differential Nonlinearity[1]	DNL	All Codes	1, 2, 3	01	16		Bits
Bipolar Zero Error	B_{PZE}	Code = 32767.5	1	01		±3	LSB
			2, 3			±4	
Negative Full-Scale Error	A_N	Code = 0.5	1	01		±3	LSB
			2, 3			±4	
Positive Full-Scale Error	A_P	Code = 65535.5	1	01		±3	LSB
			2, 3			±4	
Voltage Reference Input	V_{REF}		1, 2, 3	01	5	10	V
Signal-to-Noise + Distortion[2]	S/(N + D)	f_{IN} = 1 kHz	4, 5, 6	01	89		dB
Total Harmonic Distortion[2]	THD	f_{IN} = 1 kHz	4, 5, 6	01		–95	dB
Conversion Time	t_C	See Figures 1, 2	9, 11	01	10		µs
			10		13.3		
CLK Period	t_{CLK}	See Figures 1, 2	9, 11	01	480		ns
			10		670		
Calibration Time	t_{CT}	See Figures 1, 2	9, 10, 11	01		85532	t_{CLK}
Sampling Time (Included in t_C)	t_S	See Figures 1, 2	9, 10, 11	01	2		µs
CAL to BUSY Delay	t_{CALB}	See Figures 1, 2	9, 10, 11	01		50	ns
Last CLK to SAMPLE Delay	t_{LCS}	See Figures 1, 2	9, 10, 11	01	2.1		µs
SAMPLE to BUSY Delay	t_{SB}	See Figures 1, 2	9, 10, 11	01		75	ns
CLK High	t_{CH}	See Figures 1, 2	9, 10, 11	01	50		ns
CLK Low	t_{CL}	See Figures 1, 2	9, 10, 11	01	50		ns
1st CLK Delay	t_{FCD}	See Figures 1, 2	9, 10, 11	01	50		ns
SCLK Low	t_{SCL}	See Figures 1, 2	9, 10, 11	01	35		ns

Test	Symbol	Conditions V_{CC} = +12 V, V_{EE} = –12 V, V_{DD} = +5 V, V_{REF} = 10 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V unless otherwise specified	Group A Subgroups	Device Type	Limits Min	Limits Max	Units
CLK to Busy Delay	t_{CB}	See Figures 1, 2	9, 10, 11	01		350	ns
CLK to SDATA Valid	t_{CD}	See Figures 1, 2	9, 10, 11	01	50	200	ns
CLK to SCLK High	t_{CSH}	See Figures 1, 2	9, 10, 11	01	75	350	ns
SDATA to SCLK High	t_{DSH}	See Figures 1, 2	9, 10, 11	01	35		ns
Sample Low	t_{SL}	See Figures 1, 2	9, 10, 11	01	100		ns
CAL HIGH	t_{CALH}	See Figures 1, 2	9, 10, 11	01	50		ns

NOTES
[1]Minimum resolution for which "No Missing Codes" is guaranteed.
[2]V_{IN} = 0.05 dB, f_{IN} = 1 kHz, all measurements referred to a 0 dB (20 V p-p) input signal. The full Nyquist bandwidth is used for all values.

Functional Block Diagram and Terminal Assignment



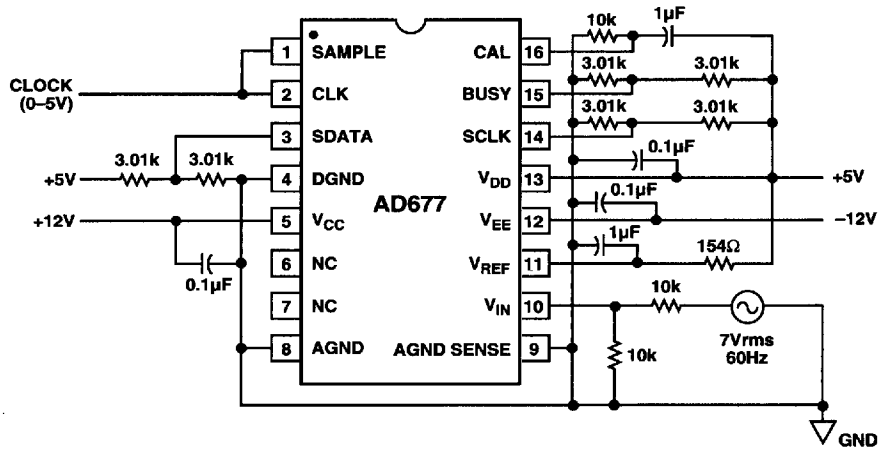


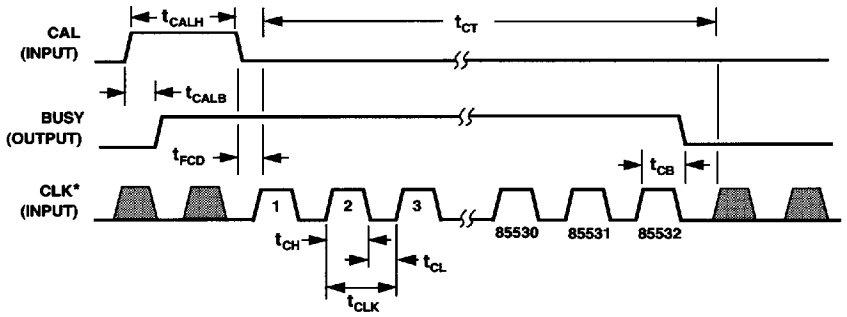
Microcircuit Technology Group

This microcircuit is covered by technology group (H).

Life Test /Burn-In Circuit

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015.





*SHADED PORTIONS OF INPUT SIGNALS ARE OPTIONAL. FOR BEST PERFORMANCE, WE RECOMMEND THAT THESE SIGNALS BE HELD LOW EXCEPT WHEN EXPLICITLY SHOWN HIGH.

Figure 1. Calibration Timing

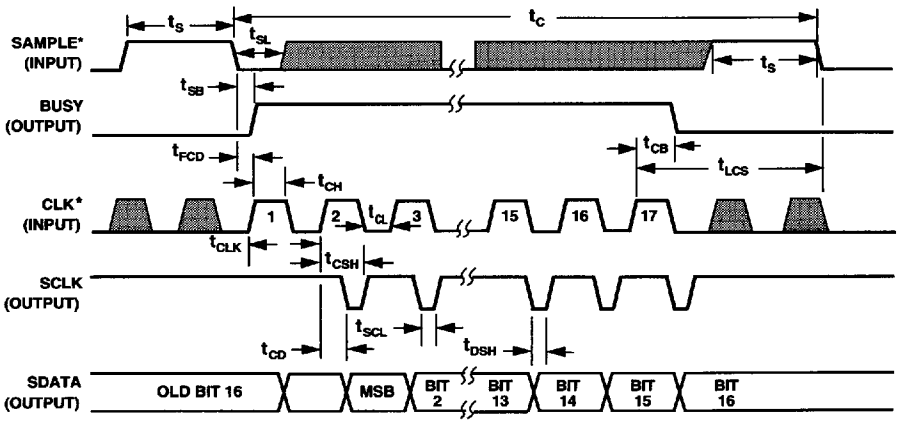


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Figure 2. General Conversion Timing