ROHM

BR28C16A

PRELIMINARY

2K X 8 CMOS Electrically Erasable PROM

FEATURES

- Fast Read Access Time
  - 120 ns
- 5 Volt-only Operation
  - Including Write
- Fast Nonvolatile Write Cycle
  - Internally Latched Data and Address
  - 150 ns Byte-load Cycle
  - 5 ms Byte-Write Cycle
- Automatic Page Write
  - 1 to 16 Bytes in a Single High Voltage Cycle
  - Full-chip Rewrite in .08 Second
- On-chip False Write Protection
- 10,000 Rewrites per Byte
  - High Voltage Applied Only to Updated Bytes

OVERVIEW

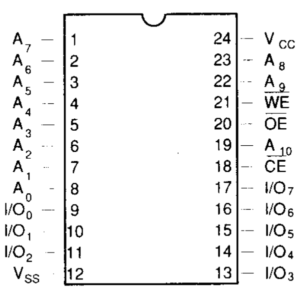
The BR28C16A is a full-featured, 2K x 8 bit CMOS E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 16K devices, but it offers improved speed and power efficiency. (Read access times can be as low as 120 ns; standby current, less than 100 μA). It features a page-wide input buffer and improved protection against inadvertent writes. Most operating modes function from a single 5 V power supply, and the BR28C16A is manufactured with ROHM's 1.5μ CMOS process.

PIN NAMES

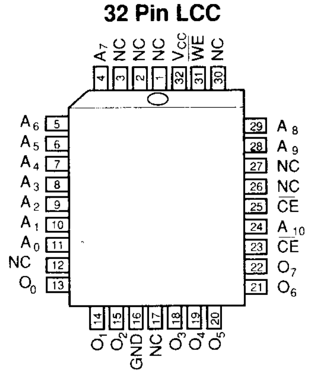
A_0-A_{10}	Address Inputs
I/O_0-I/O_9	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

PIN CONFIGURATIONS

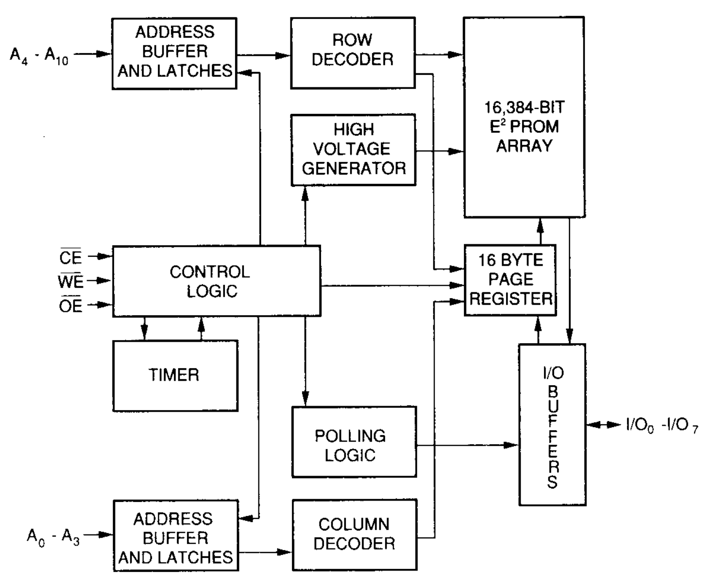
24 Pin DIP



32 Pin LCC



BLOCK DIAGRAM



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The fully-automatic, 16-byte page-write allows the entire memory to be programmed in less than .1 seconds. Internal latches, for address and data, free the system bus during the 5 ms self-timed, nonvolatile write period. Moreover, the byte-load cycle time matches the read access time, adding to system performance.

The BR28C16A features power-on reset and noise protected $\overline{WE}$, to inhibit inadvertent writes.

The BR28C16A is compatible with existing 16K E^2PROMS — both pinout and operating modes conform to industry standards. This compatibility extends to higher and lower density E^2PROMS as well.

APPLICATIONS

The nonvolatile storage in the BR28C16A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The BR28C16A is ideal in applications that are self-adapting (such as video games and systems that require automatic re-calibration), as well as those that must tolerate power failures.

ENDURANCE and DATA RETENTION

The BR28C16A is designed for applications requiring up to 10,000 rewrites per E^2PROM byte. It provides 10 years of secure data retention, with or without power applied.

DEVICE OPERATION-STANDARD MODES

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard, user operating modes for the BR28C16A. Chip erase requires a higher supply voltage on one input pin. (This conforms with existing E^2PROM technology.)

Read Mode

Data is read from the BR28C16A by bringing both $\overline{CE}$ and $\overline{OE}$ low while keeping $\overline{WE}$ high. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the controlling line goes low ($\overline{CE}$ or $\overline{OE}$), or the time when the address is established.The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle

Write Mode

The BR28C16A uses a two-step process to store new data. Byte-load cycles fill latches in a page buffer. A subsequent high voltage cycle transfers new entries in the page-buffer to the E^2PROM array.

The BR28C16A contains 16, 16-byte pages. Address line A_4-A_{10} identify the page; lines A_0-A_3 identify the byte within the page. All bytes written within one write cycle must be on the same page (A_4-A_{10} must remain unchanged). Any number of the 16 bytes in the page can be written or re-written, in any order; the last data written is retained.

Either $\overline{WE}$ or $\overline{CE}$ can be used to trigger the byte-load cycle. The address is latched into internal address latches upon the falling edge of $\overline{WE}$ or $\overline{CE}$ (the other line already being low). A byte-load timer is started on the subsequent rising edge of the controlling line. The timer provides a 100 μS window for initiating the next byte-load cycle. Byte-loading can continue indefinitely if each new load cycle is started within the timeout period. Please note that all write cycles require that $\overline{OE}$ be held high.

When the timer times out, additional byte-loads are inhibited and data is automatically transferred from the page buffer to the E^2PROM array by a high voltage cycle. Byte flags, set during the byte-load cycles, ensure that high voltage is applied only to newly written bytes. By avoiding the unnecessary cycling of bytes, the endurance of the array is extended. The high voltage cycle is immune to any overlapping control pin activity.

A write-latch is set on the first byte-load of each write cycle. Output pins remain in a high impedance state except during a byte-load (when they contain new input data) or during a status register read (see below). When the high voltage cycle is completed, the write-latch is reset and the operating mode is again determined by the control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$).

Output Disable Mode

If, while in the read mode, $\overline{OE}$ is brought high, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a high impedance state).

Standby Mode

Whenever $\overline{CE}$ is brought high, the device operates in standby mode, with the I/O pins in a high impedance state. Standby power dissipation is less than 100 μA with CMOS level inputs. While $\overline{CE}$ remains high, all input pins in standby, insulating the device from activity on the system busses.

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DEVICE OPERATION — HIGH VOLTAGE MODES

Chip Erase Mode

The chip erase mode allows the user to erase the entire E²PROM array with a single command. There are two methods of performing chip erase. The first method requires the application of high voltage (12 V) on $\overline{OE}$ pin, with $\overline{CE}$ and $\overline{WE}$ at V_{IL}. The other method requires the application of high voltage on $\overline{OE}$ and $\overline{WE}$ with $\overline{CE}$ at V_{IL}. Chip erase occurs after the first byte-load cycle, but in this case, the data on the I/O pins is ignored. A byte containing all "1's" is automatically written to all locations in the E²PROM array. (Refer to Mode Selection chart).

MONITORING DEVICE STATUS

Because the byte-load timer and its high voltage cycle are completely under the control of the BR28C16A, a status register allows the host system to monitor device status.

Status Register

Since the byte-load time-out and entire high voltage cycle are controlled by the BR28C16A, a status register is provided for the host system to determine the status of these operations using the system busses. No additional external hardware is required. Any attempt to read the part while the write mode latch is set will be interpreted as a status register read. Status register read is performed by exercising the control pins in the same fashion as for a normal read. Also like normal reads, the addresses are not latched. Reading the status register has no effect on the byte-load timer, contents of the page buffer and byte-load flags, or the high voltage cycle timing.

$\overline{\text{Data}}$ Polling requires a single read with the same address as the last byte loaded into the page buffer. Whenever the write latch is set, data on I/O_7 will be the comlement of bit 7 in the last byte loaded; whenever the write latch is reset, data on I/O_7 will be the same as bit 7 in the last byte loaded. In the latter case, the write operation is complete and the read is a normal read cycle that accesses the E²PROM array location corresponding to the last byte loaded. The system determines device status by comparing bit 7 of the last byte loaded with bit 7 read from the device.

Definition of all status register bits and their interpretation is as follows:

I/O_7	I/O_6 ,	I/O_5,	I/O_4 ,	I/O_3,	I/O_2 ,	I/O_1,	I/O_0
$\overline{\text{Data}}$ Polling	0	0	0	0	0	0	0

I/O_0 : I/O_3, I/O_5: I/O_4: Not used. Always set to "0"

I/O_7: $\overline{\text{Data}}$ Polling. Complement = write mode,
Same = read mode

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
V_{IH}	X	X	Standby	High Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}		5 V Byte Write	D_{IN}	Active
V_{IL}	V_{IH}	V_{IH}	Read and Write Inhibit	High Z	Active
V_{IL}	V_H*	V_{IL}	Chip Erase	Data In =X	Active
V_{IL}	V_H*	V_{IH}	Chip Erase	Data In =X	Active

*V_H = 12 V

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WRITE PROTECT MECHANISMS

The BR28C16A features several mechanisms to protect it from inadvertent writes that might occur during power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following are built in.

Power on Reset

At power on, operation is inhibited until V_{CC} is stable and sufficiently high. All modes are disabled until V_{CC} reaches 3.0 V. Read operations are enabled as soon as V_{CC} is adequate; write operations are enabled 1 ms later.

Noise Protection

Write pulses of less than 10 ns duration on the $\overline{WE}$ pin will not set the write-latch.

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ....-65 to +135°C
Storage temperature...............................-65 to +150°C
Voltage on any pin*.................................-0.6 to +7.0 V
Voltage on OE pin*..................................-0.6 to +15 V
DC output current...5 mA

*With respect to ground

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to avoid any voltages higher than the rated maxima.

D.C. CHARACTERISTICS

TA = 0^{o}C to 70^{o}C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Max	Units	Test Conditions
I_{CC}	V_{CC} Current-Active		30	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} WE = V_{IH} I/O's = open AO-A12 = toggling f = 5 MHz
I_{SB}	V_{CC} Current-Standby		1	mA	$\overline{CE}$ = $\overline{WE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open A_0 -A_{12} = V_{CC}
I_{SBC}	V_{CC} Current-CMOS Standby		100	uA	$\overline{CE}$ = $\overline{WE}$ >= V_{CC}-.2 $\overline{OE}$ = V_{IL} I/O's = open A_0-A_{12} = V_{CC}
I_{LI}	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	-10	10	uA	V_{OUT} = GND to V_{CC} $\overline{CE}$ = V_{IH}
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL}= 2.1 mA
V_{OH}	Output High Voltage	2.4 V_{CC}-0.1		V V	I_{OH} = -400 uA I_{OH} = -10 uA

CAPACITANCE

TA = +25^{o}C, f = 1.0 MHz

Symbol	Test	Max.	Units	Test Conditions
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	6	pF	V_{IN} = 0V

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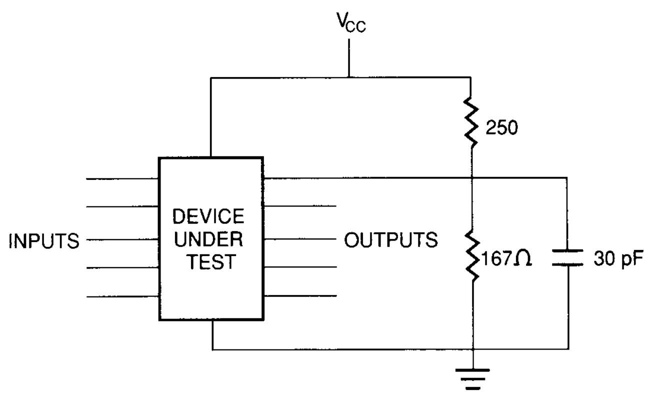
AC OPERATING CHARACTERISTICS

READ CYCLE (See Figures 1&2)

Symbol	Parameter	Min	Max	Units
t_{RC}	Read Cycle Time	150		nS
t_{AA}	Address Access Time		150	nS
t_{CE}	Chip Enable Access Time		150	nS
t_{OE}	Output Enable Access Time		70	nS
t_{LZ}	Chip Enable to Output in Low Z	5		nS
t_{HZ}	Chip Disable to Output in High Z	5	50	nS
t_{OLZ}	Output Enable to Output in Low Z	5		nS
t_{OHZ}	Output Disable to Output in High Z	5	35	nS
t_{OH}	Output Hold from Address Change	30		nS

WRITE CYCLE (See Figure 3, 4, 5)

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		5	mS
t_{BLC}	Byte Load Cycle	150		nS
t_{BLT}	Byte Load Time		100	µS
t_{AS}	Address Setup Time	0		nS
t_{AH}	Address Hold Time	40		nS
t_{CS}	Write Setup Time	0		nS
t_{CH}	Write Hold Time	0		nS
t_{CP}	Chip Enable Pulse Width	90		nS
t_{OES}	Output Enable Setup Time	5		nS
t_{OEH}	Output Enable Hold Time	5		nS
t_{WP}	Write Enable Pulse Width	90		nS
t_{WPH}	Write Pulse Width High	60		nS
t_{DS}	Data Setup Time	30		nS
t_{DH}	Data Hold Time	0		nS



Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns from 1V to 2V
Frequency	10 MHz
Timing Reference Value	1.5V

Figure 1. AC Test Conditions

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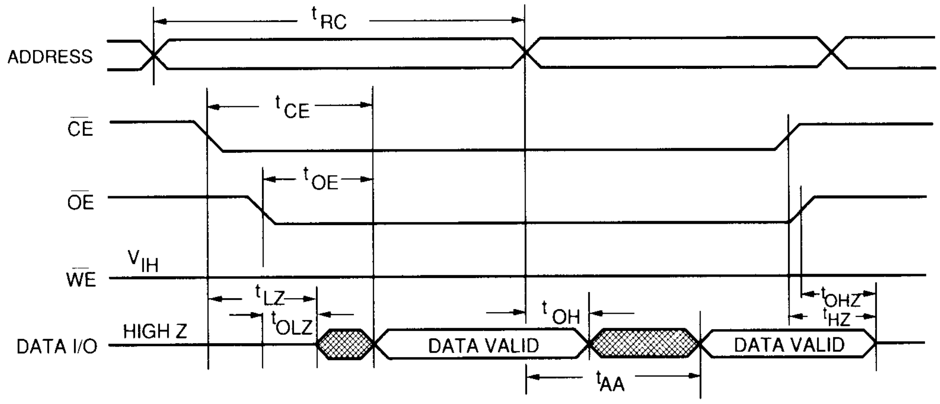

Figure 2. Read Cycle Timing

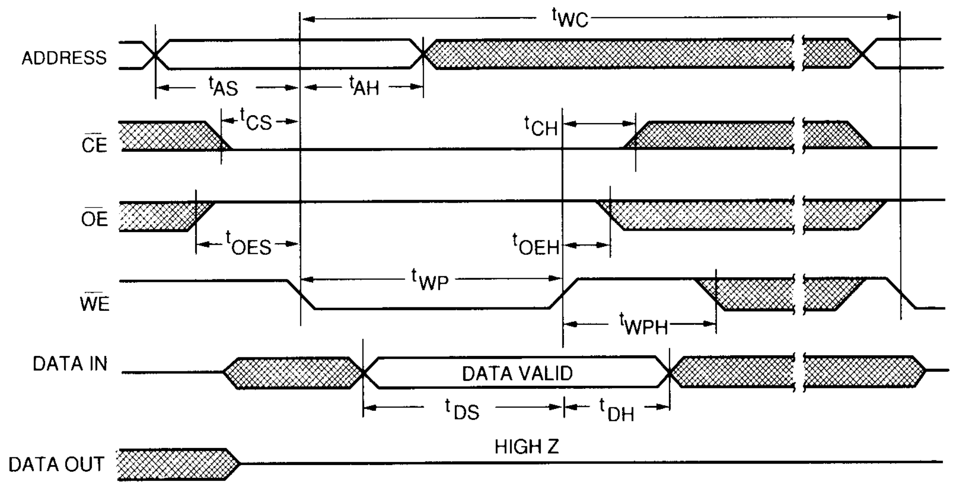

Figure 3. $\overline{WE}$ Controlled Write Cycle Timing

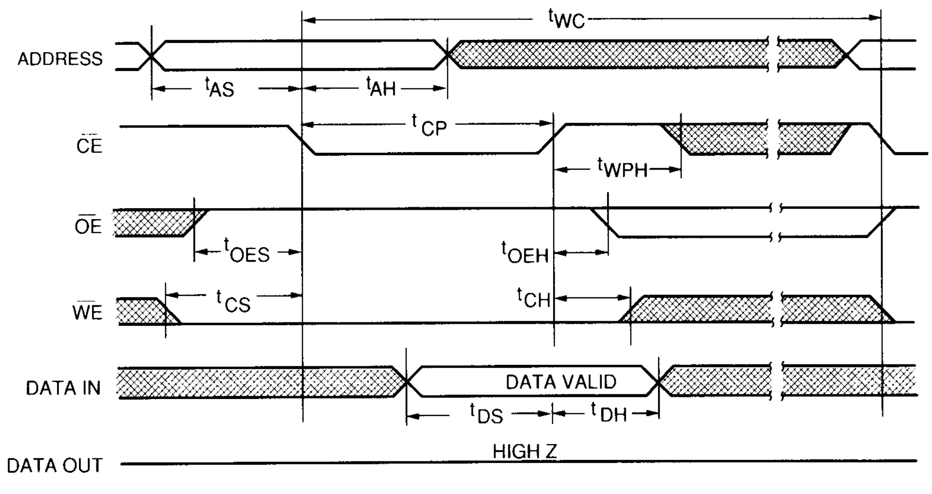

Figure 4. $\overline{CE}$ Controlled Write Cycle Timing

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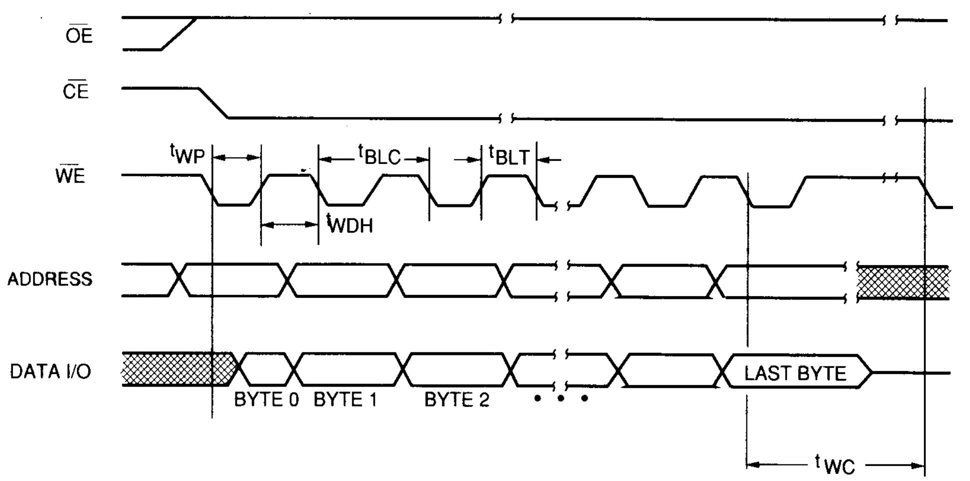

Figure 5. Page Mode Write Cycle Timing

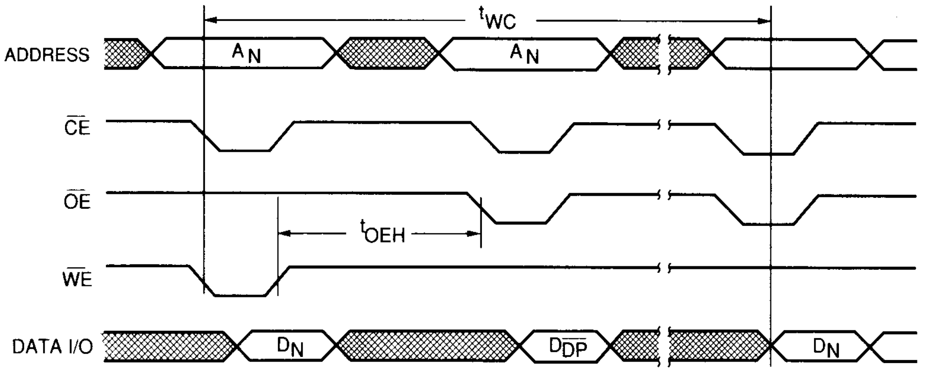

Figure 6. $\overline{\text{DATA}}$ Polling Timing

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ORDERING INFORMATION

Standard Configurations:

Prefix	Temperature Range	Part Type	Package* Type	Access Time ns
BR	S	28C16A	C, D, P, J	100, 120, 150
BR	E	28C16A	C, D, P, J	100, 120, 150
BR	M	28C16A	C	100, 120, 150

*Contact ROHM for your special packaging requirements

Part Numbers:

BR S 28C16A D — 150

Prefix — BR

Temperature Range — S
S — 0°C to +70°C
E — -40°C to +85°C
M — -55°C to +125°C

Part Type — 28C16A

Package Type* — D
C-CERDIP
D-Plastic Leaded Chip Carrier
P-Plastic DIP (0.600 inch)
J-Small Outline Package

Access Time — 150
100 —100 ns
120 —120 ns
150 —150 ns

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