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National Semiconductor

DM54ALS/DM74ALS160B, 161B, 162B, 163B Synchronous Four-Bit Counter

General Description

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The ALS160B and ALS162B are four-bit decade counters, while the ALS161B and ALS163B are four-bit binary counters. The ALS160B and ALS161B clear asynchronously, while the ALS162B and ALS163B clear synchronously. The carry output is decoded to prevent spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable, that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with set up data after the next clock pulse regardless of the levels of enable input. Low to high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs.

The ALS160B and ALS161B clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. These two counters are provided with a clear on power-up feature. The ALS162B and ALS163B clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low to high transitions at the clear input of the ALS162B and ALS163B are also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count enable inputs (P and T) and a ripple carry output. Both count enable inputs must be high to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. High to low level transitions at the enable P or T inputs of the ALS160B through ALS163B may occur regardless of the logic level on the clock.

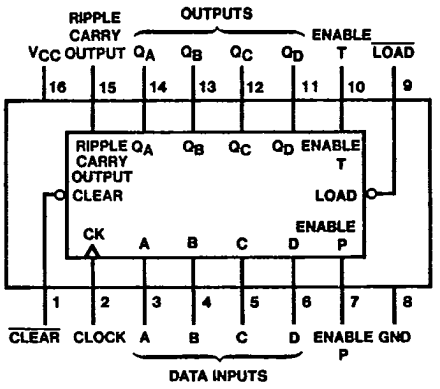
The ALS160B through ALS163B feature a fully independent clock circuit. changes made to control inputs (enable P or T, or load) that will modify the operating mode will have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- ESD inputs

Connection Diagram

Dual-In-Line Package



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Order Number DM54ALS161BJ, 163BJ, DM74ALS160BM, 161BM, 162BM, 163BM or DM74ALS160BN, 161BN, 162BN, 163BN
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θJA	
N Package	78.1°C/W
M Package	106.8°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter			DM54ALS 161B, 163B			DM74ALS 160B, 161B, 162B, 163B			Units
				Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
I_{OH}	High Level Output Current					−0.4			−0.4	mA
I_{OL}	Low Level Output Current					4			8	mA
f_{CLK}	Clock Frequency			0		22	0		40	MHz
t_{SETUP}	Setup Time	Data; A, B, C, D		20↑			15↑			ns
		En P, En T	ALS160B/161B	25↑			15↑			ns
			ALS162B/163B	20↑			15↑			ns
		$\overline{\text{Load}}$		20↑			15↑			ns
		$\overline{\text{Clear}}$ (Only for 162B and 163B)	Low	20↑			15↑			ns
			High	10↑			10↑			ns
	Setup 1 (Only for 160B and 161B)	$\overline{\text{Clear}}$ Inactive		10	4		10	4		ns
t_{HOLD}	Hold Time	Data; A, B, C, D		0↑	−3		0↑	−3		ns
		En P, En T		0↑	−3		0↑	−3		ns
		$\overline{\text{Load}}$		0↑	−4		0↑	−4		ns
		$\overline{\text{Clear}}$ (Only for 162B and 163B		0↑	−7		0↑	−7		ns
	Hold 0 (Only for 160B and 161B)	$\overline{\text{Clear}}$		0	−4		0	−4		ns
t_W	Width of Clock or $\overline{\text{Clear}}$ Pulse	CLK High or Low		20			12.5			ns
		ALS160B/161B $\overline{\text{CLR}}$ Low		20			15			ns
	Width of Load Pulse			20			15			ns
T_A	Operating Free Air Temperature			−55		125	0		70	°C

Note 1: The symbol (↑) indicates that the rising edge of the clock is used as a reference.

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Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			12	21	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS 161B		DM74ALS 160B, 161B		Units
					Min	Max	Min	Max	
f_{MAX}	Max. Clock Freq.	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			25		40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Ripple Carry	5	24	5	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Ripple Carry	5	20	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	4	15	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	6	20	6	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		En T	Ripple Carry	3	13	3	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		En T	Ripple Carry	3	13	3	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear	Any Q	8	24	8	24	ns
			Clear	Ripple Carry	11	24.5	11	23	ns

Note 1: See Section 1 for test waveforms and output load.

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'ALS162B, 'ALS163B Switching Characteristics

over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS 163B		DM74ALS 162B, 163B		Units
					Min	Max	Min	Max	
f_{MAX}	Max. Clock Freq.	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF, T_A = Min to Max			35		40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Ripple Carry	5	35	5	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Ripple Carry	5	26	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	4	21	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	6	25	6	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		En T	Ripple Carry	3	20	3	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		En T	Ripple Carry	3	16	3	13	ns

Note 1: See Section 1 for test waveforms and output load.

Timing Diagrams

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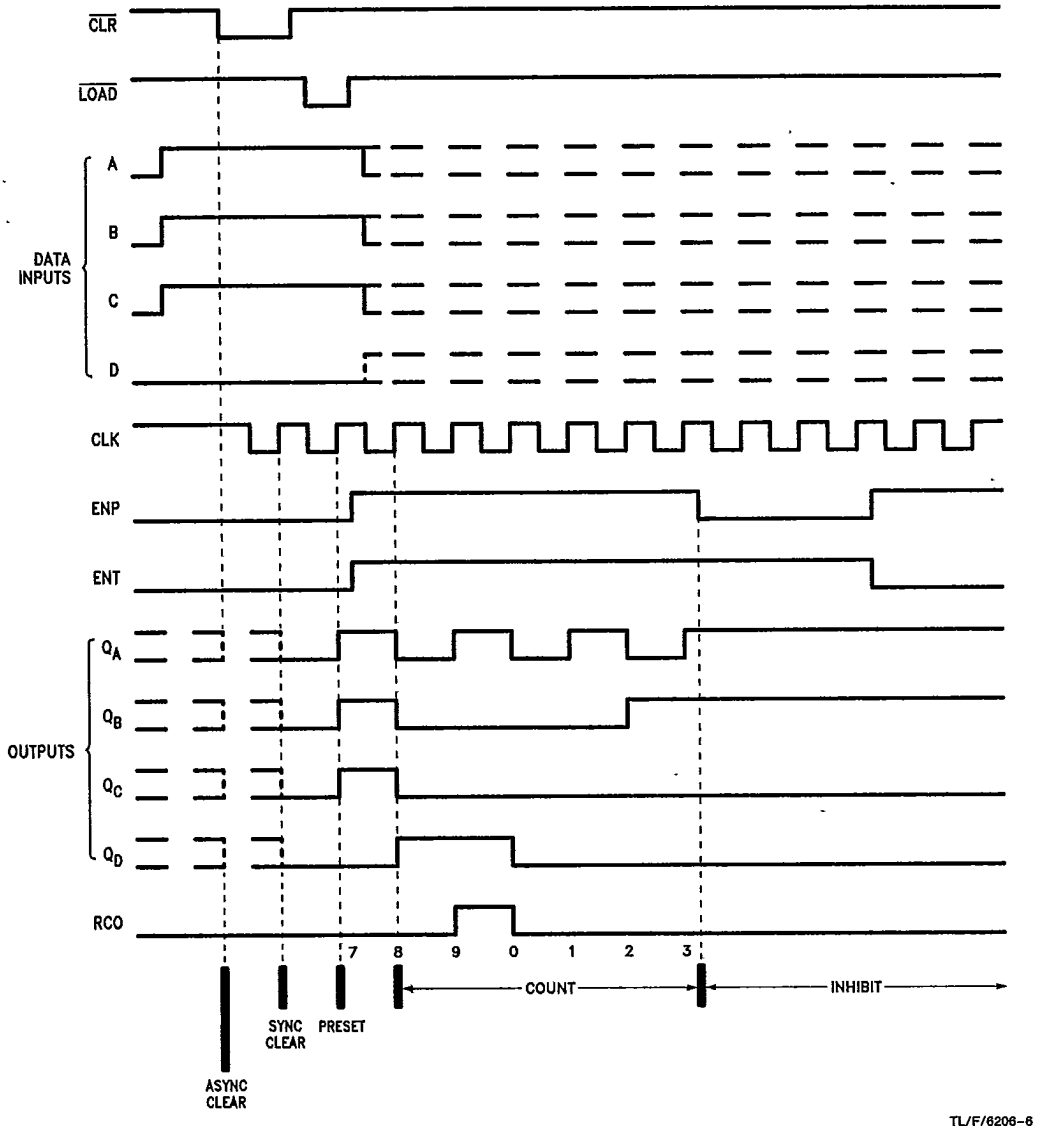
ALS160B, ALS162B



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Timing Diagrams (Continued)

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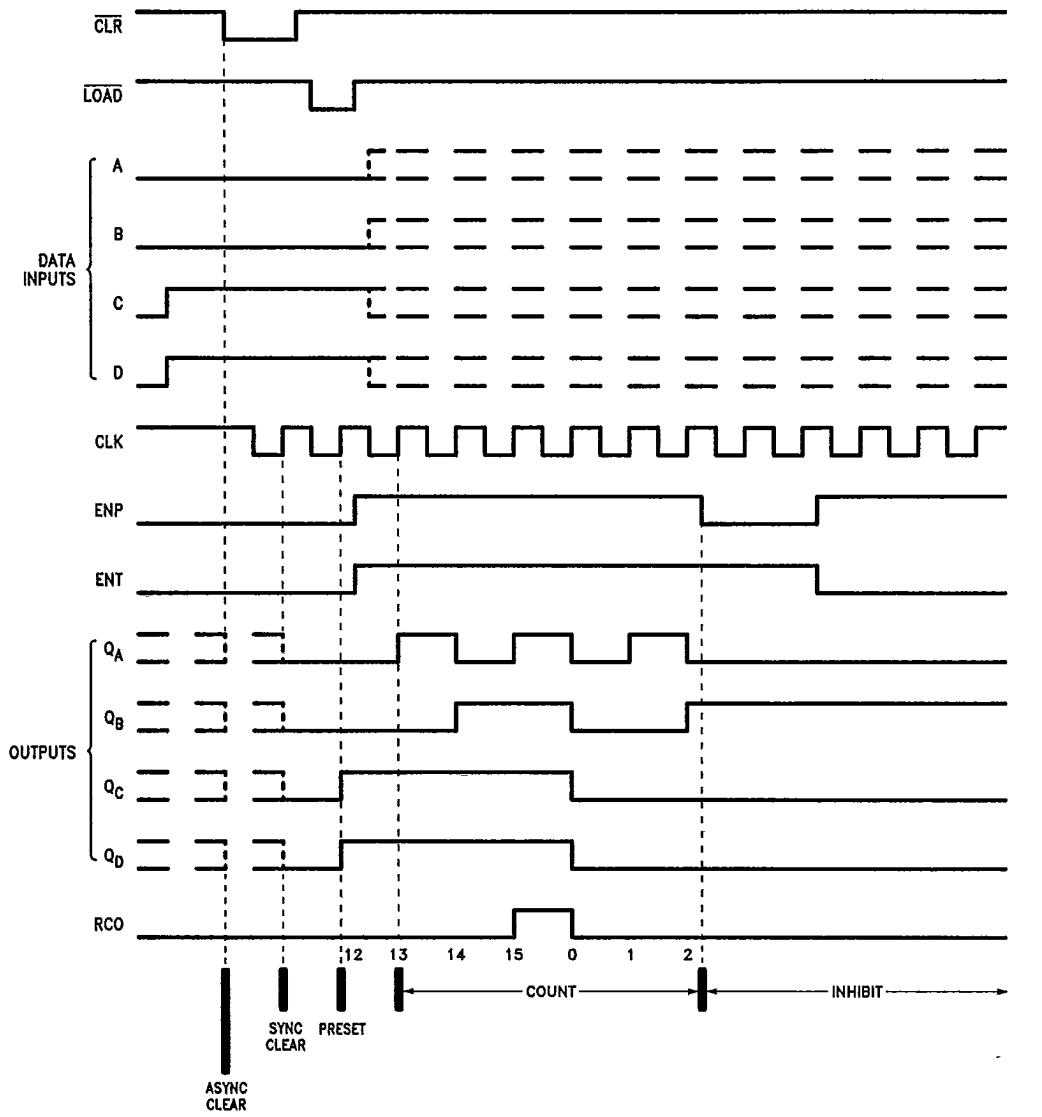
ALS161B, ALS163B



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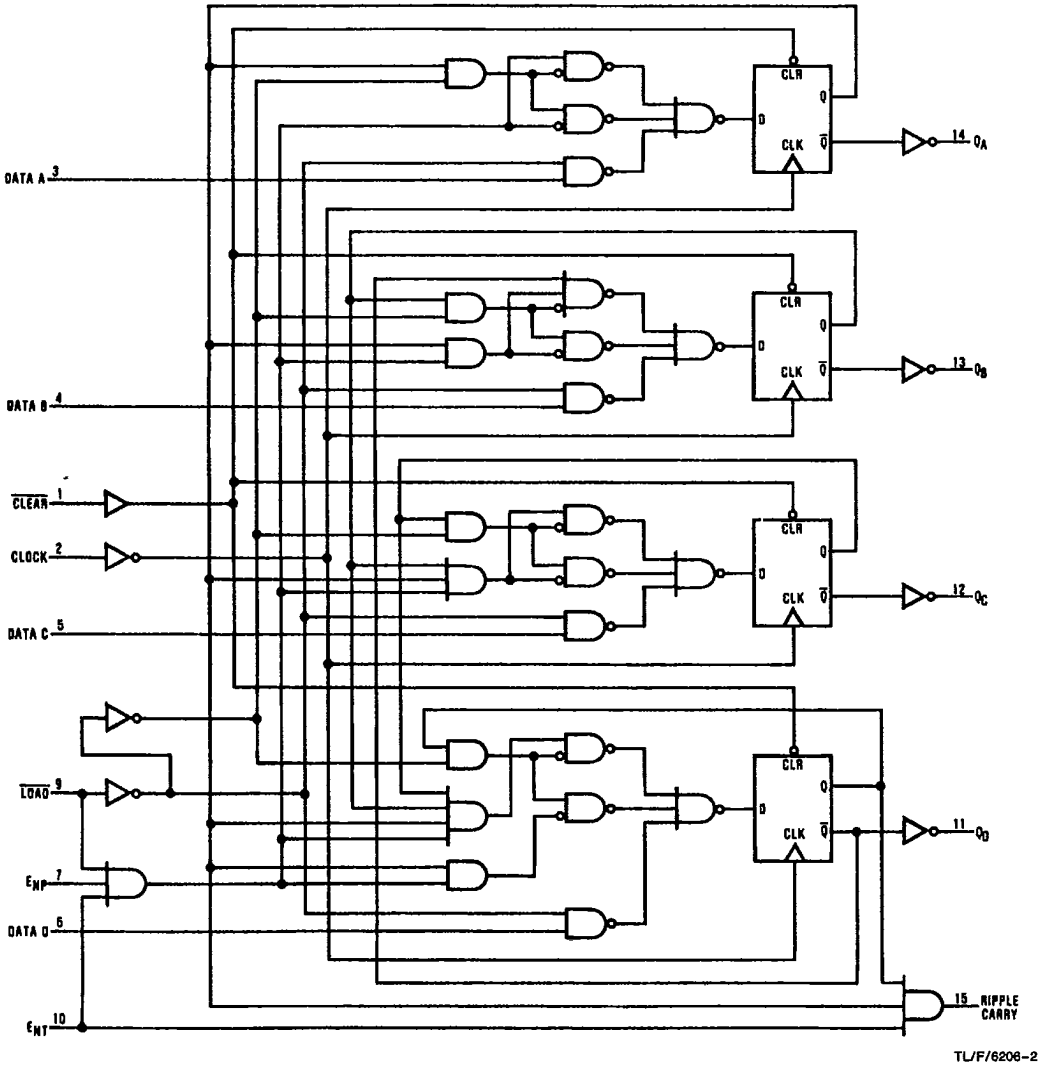
Logic Diagrams

ALS160B



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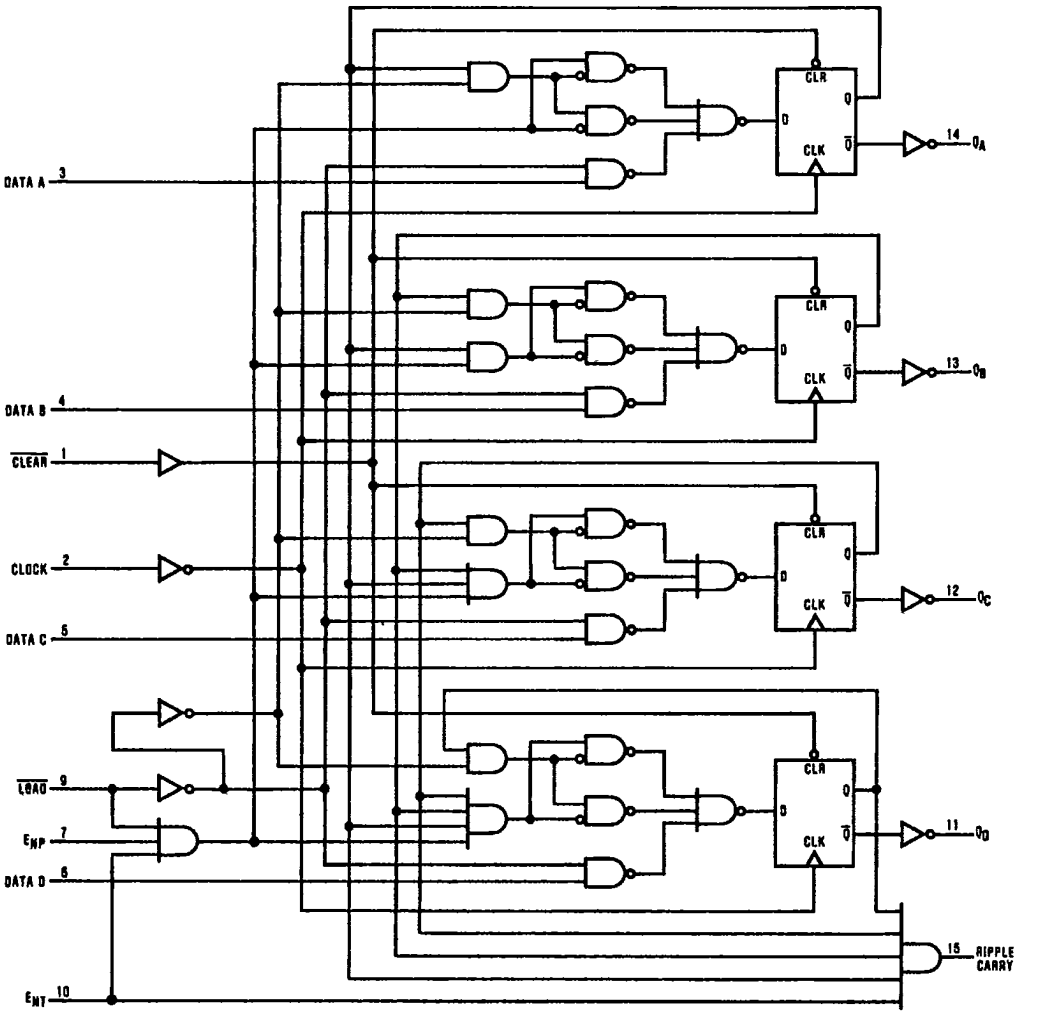
Logic Diagrams (Continued)

ALS161B



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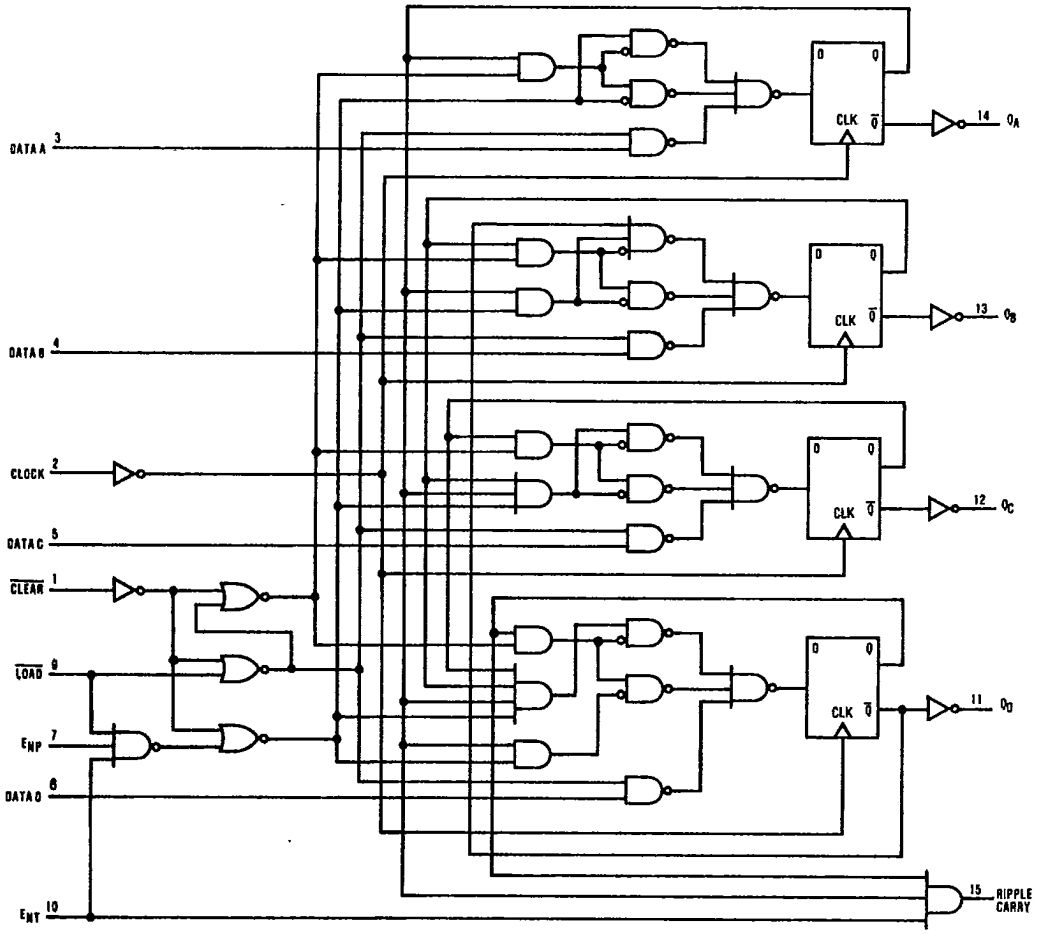
Logic Diagrams (Continued)

ALS162B



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Logic Diagrams (Continued)

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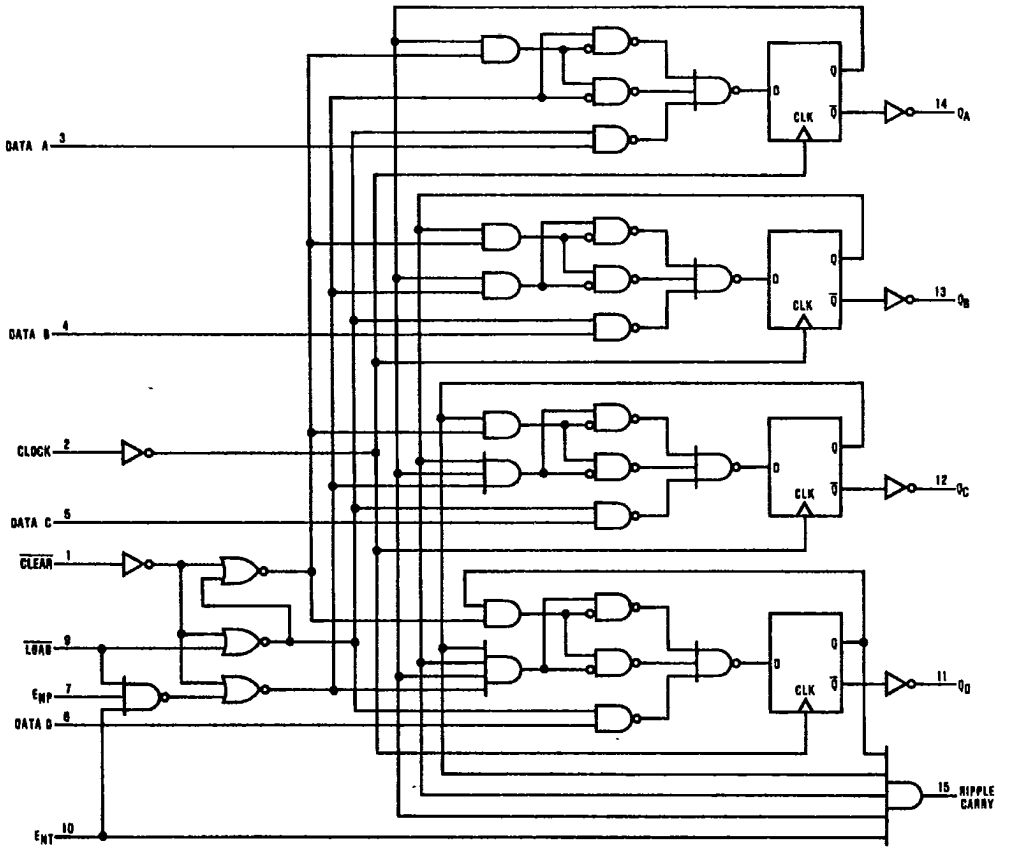
ALS163B



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