2.5V 512/256K X 18 Synchronous Dual-port SRAM with 3.3V or 2.5V interface

Features

- True Dual-Port memory cells that allow simultaneous access of the same memory location
- Organisation: 524,288/262,144 × 18[1]
- Fully Synchronous, independent operation on both ports
- Selectable Pipeline or Flow-Through output mode
- Fast clock speeds in Pipeline output mode: 250 MHz operation (9Gbps bandwidth)
- Fast clock to data access: 2.8ns for Pipeline output mode
- Asynchronous output enable control
- Fast $\overline{OE}$ access times: 2.8ns
- Double Cycle Deselect (DCD) for Pipeline Output Mode
- 19/18[1]-bit counter with Increment, Hold and Repeat features on each port
- Dual Chip enables on both ports for easy depth expansion
- Interrupt and Collision Detection Features
- 2.5 V power supply for the core
- LVTTL compatible, selectable 3.3V or 2.5V power supply for I/Os, addresses, clock and control signals on each port
- Snooze modes for each port for standby operation
- 15mA typical standby current in power down mode
- Available in 256-pin Ball Grid Array (BGA), 144-pin Thin Quad Flatpack (TQFP) and 208-pin fine pitch Ball Grid Array (fpBGA)
- Supports JTAG features compliant with IEEE 1149.1

Note:
1. AS9C25512M2018L/AS9C25256M2018L

Selection guide

Feature	-250	-200	-166	-133	Units
Minimum cycle time	4	5	6	7.5	ns
Maximum Pipeline clock frequency	250	200	166	133	MHz
Maximum Pipeline clock access time	2.8	3.4	3.6	4.2	ns
Maximum flow-through clock frequency	150	133	100	83	MHz
Maximum flow-through clock access time	6.5	7.5	10	12	ns
Maximum operating current	TBD	350	300	260	mA
Maximum snooze mode current	18	18	18	18	mA

PRELIMINARY

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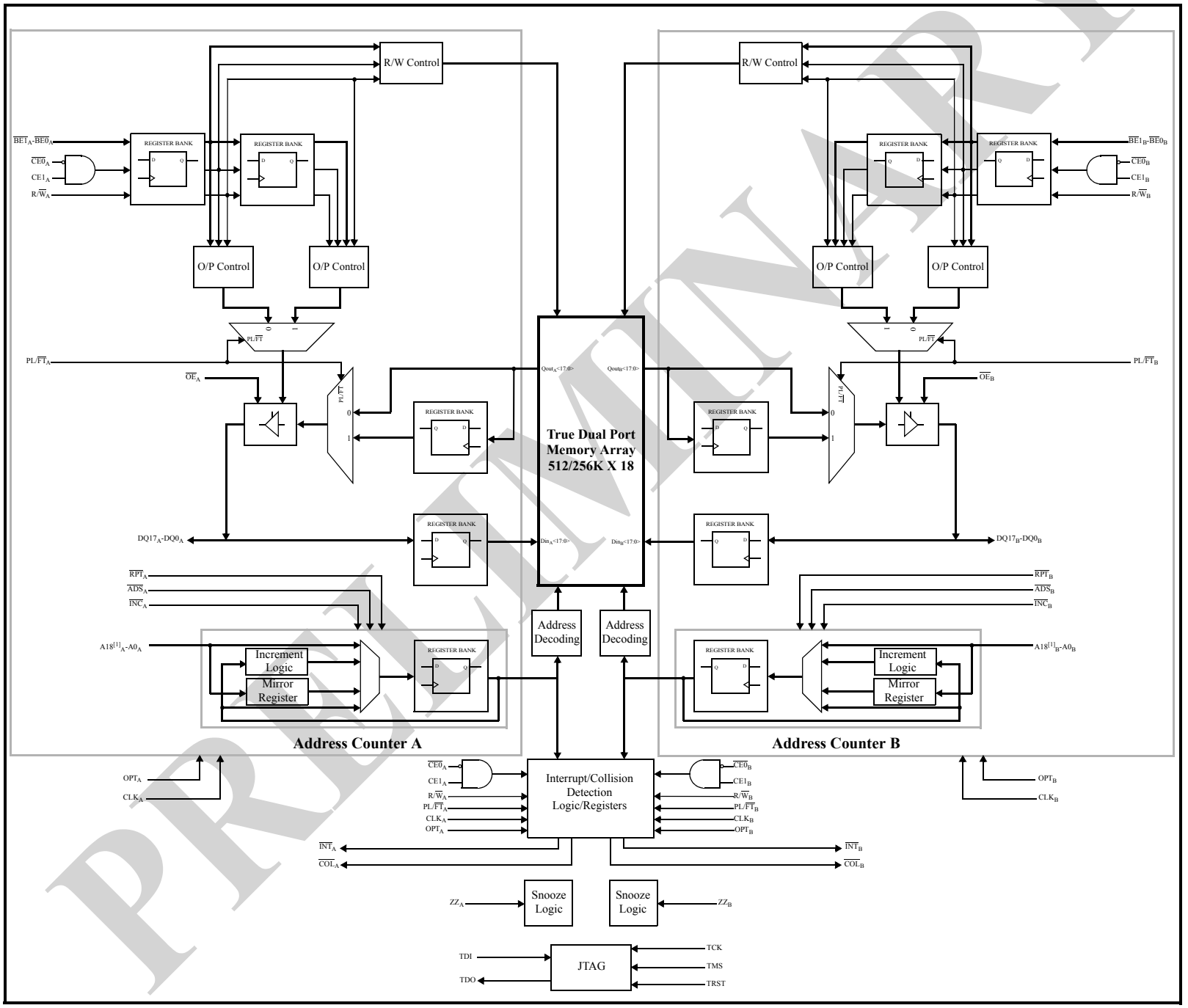
Dual port logic block diagram



Note:

1. Address A18 is a NC for AS9C25256M2018L

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General Description

The AS9C25512M2018L/AS9C25256M2018L is a high-speed CMOS 9/4.5-Mbit synchronous Dual-Port Static Random Access Memory device, organized as 524,288/262,144 × 18 bits. It incorporates a selectable Flow-Through/Pipeline output feature for user flexibility. Clock-to-data valid time is 2.8ns at 250 MHz for "Pipeline output" mode of operation.

Each port contains a 19/18 bit linear burst counter on the input address register that can loop through the whole address sequence. After externally loading the counter with the initial address, it can be Incremented or Held for the next cycle. A new address can also be Loaded or the "Previous Loaded" address can be re-accessed (Repeated) using counter controls (More description to follow). The Registers on control, data, and address inputs provide minimal setup and hold times.

The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. A particular port can write to a certain location while another port is reading from the same location, but the validity of read data is not guaranteed. However, the reading port is informed about the possible collision through its collision alert signal. The result of writing to the same location by more than one port at the same time is undefined.

The Asynchronous Output Enable input pin allows asynchronous disabling of output buffers at any given time. The Byte Enable inputs allow individual byte read/write operations (refer Byte Control Truth Table). An automatic power down feature, controlled by $\overline{CE0}$ and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode.

AS9C25512M2018L/AS9C25256M2018L can support an operating voltage of either 3.3V or 2.5V on either or both ports, which is controlled by the OPT pins. The power supply for the core of the device (VDD) is at 2.5V. This device is available in 256-pin Ball Grid Array (BGA), 208-pin fine pitch Ball Grid Array (fpBGA) and 144-pin Thin Quad Flatpack (TQFP)

Address Counter

The AS9C25512M2018L/AS9C25256M2018L carries an internal 19/18 bit address counter for each port which can loop through the entire memory array. The Address counter features are discussed below:

Load: Any required external address can be loaded on to the counter. This feature is similar to normal address load in conventional memories.

Increment: The address counter has the capability to internally increment the address value, potentially covering the entire memory array. Once the whole address space is completed, the counter will wrap around. The address counter is not initailized on Power-up, hence a known location has to be loaded before Increment operation.

Hold: The value of the counter register can be held for an unlimited number of clock cycles by de-asserting $\overline{ADS}$, $\overline{INC}$, and $\overline{RPT}$ inputs.

Repeat: The previously loaded address (loaded using a valid Load operation) can be re-accessed by asserting $\overline{RPT}$ input. A separate 19/18 bit register called "Mirror register" is used to hold the last loaded address.This register is not initialized on Power-up, hence a known location has to be loaded before Repeat operation (Refer Counter control truth table for details).

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Ball Assignment - 256-ball BGA

AS9C25512M2018L/AS9C25256M2018L
B - 256
Top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	TDI	NC	$A17_A$	$A14_A$	$A11_A$	$A8_A$	NC	$CE1_A$	$\overline{OE}_A$	$\overline{INC}_A$	$A5_A$	$A2_A$	$A0_A$	NC	NC	A
B	$\overline{INT}_A$	NC	TDO	$A18^{[1]}_A$	$A15_A$	$A12_A$	$A9_A$	$\overline{BE1}_A$	$\overline{CE0}_A$	$R/\overline{W}_A$	$\overline{RPT}_A$	$A4_A$	$A1_A$	VDD	NC	NC	B
C	$\overline{COL}_A$	$DQ9_A$	VSS	$A16_A$	$A13_A$	$A10_A$	$A7_A$	NC	$\overline{BE0}_A$	CLK_A	$\overline{ADS}_A$	$A6_A$	$A3_A$	OPT_A	NC	$DQ8_A$	C
D	NC	$DQ9_B$	NC	$PL/\overline{FT}_A$	$VDDQ_A$	$VDDQ_A$	$VDDQ_B$	$VDDQ_B$	$VDDQ_A$	$VDDQ_A$	$VDDQ_B$	$VDDQ_B$	VDD	NC	NC	$DQ8_B$	D
E	$DQ10_B$	$DQ10_A$	NC	$VDDQ_A$	VDD	VDD	NC	VSS	VSS	VSS	VDD	VDD	$VDDQ_B$	NC	$DQ7_A$	$DQ7_B$	E
F	$DQ11_A$	NC	$DQ11_B$	$VDDQ_A$	VDD	NC	NC	VSS	VSS	VSS	VSS	VDD	$VDDQ_B$	$DQ6_B$	NC	$DQ6_A$	F
G	NC	NC	$DQ12_A$	$VDDQ_B$	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	$VDDQ_A$	$DQ5_A$	NC	NC	G
H	NC	$DQ12_B$	NC	$VDDQ_B$	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	$VDDQ_A$	NC	NC	$DQ5_B$	H
J	$DQ13_A$	$DQ14_B$	$DQ13_B$	$VDDQ_A$	ZZ_B	VSS	VSS	VSS	VSS	VSS	VSS	ZZ_A	$VDDQ_B$	$DQ4_B$	$DQ3_B$	$DQ4_A$	J
K	NC	NC	$DQ14_A$	$VDDQ_A$	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	$VDDQ_B$	NC	NC	$DQ3_A$	K
L	$DQ15_A$	NC	$DQ15_B$	$VDDQ_B$	VDD	NC	NC	VSS	VSS	VSS	VSS	VDD	$VDDQ_A$	$DQ2_A$	NC	$DQ2_B$	L
M	$DQ16_B$	$DQ16_A$	NC	$VDDQ_B$	VDD	VDD	NC	VSS	VSS	VSS	VDD	VDD	$VDDQ_A$	$DQ1_B$	$DQ1_A$	NC	M
N	NC	$DQ17_B$	NC	$PL/\overline{FT}_B$	$VDDQ_B$	$VDDQ_B$	$VDDQ_A$	$VDDQ_A$	$VDDQ_B$	$VDDQ_B$	$VDDQ_A$	$VDDQ_A$	VDD	NC	$DQ0_B$	NC	N
P	$\overline{COL}_B$	$DQ17_A$	TMS	$A16_B$	$A13_B$	$A10_B$	$A7_B$	NC	$\overline{BE0}_B$	CLK_B	$\overline{ADS}_B$	$A6_B$	$A3_B$	NC	NC	$DQ0_A$	P
R	$\overline{INT}_B$	NC	$\overline{TRST}$	$A18^{[1]}_B$	$A15_B$	$A12_B$	$A9_B$	$\overline{BE1}_B$	$\overline{CE0}_B$	$R/\overline{W}_B$	$\overline{RPT}_B$	$A4_B$	$A1_B$	OPT_B	NC	NC	R
T	NC	TCK	NC	$A17_B$	$A14_B$	$A11_B$	$A8_B$	NC	$CE1_B$	$\overline{OE}_B$	$\overline{INC}_B$	$A5_B$	$A2_B$	$A0_B$	NC	NC	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Note:

1. Address A18 is a NC for AS9C25256M2018L

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Ball Assignment - 208-ball fpBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	$DQ9_A$	$\overline{INT}_A$	VSS	TDO	NC	$A16_A$	$A12_A$	$A8_A$	NC	VDD	CLK_A	$\overline{INC}_A$	$A4_A$	$A0_A$	OPT_A	NC	VSS	A
B	NC	VSS	$\overline{COL}_A$	TDI	$A17_A$	$A13_A$	$A9_A$	NC	$\overline{CE0}_A$	VSS	$\overline{ADS}_A$	$A5_A$	$A1_A$	NC	$VDDQ_B$	$DQ8_A$	NC	B
C	$VDDQ_A$	$DQ9_B$	$VDDQ_B$	$PL/\overline{FT}_A$	$A18^{[1]}{}_A$	$A14_A$	$A10_A$	$\overline{BE1}_A$	$CE1_A$	VSS	$R/\overline{W}_A$	$A6_A$	$A2_A$	VDD	$DQ8_B$	NC	VSS	C
D	NC	VSS	$DQ10_A$	NC	$A15_A$	$A11_A$	$A7_A$	$\overline{BE0}_A$	VDD	$\overline{OE}_A$	$\overline{RPT}_A$	$A3_A$	VDD	NC	$VDDQ_A$	$DQ7_A$	$DQ7_B$	D
E	$DQ11_A$	NC	$VDDQ_B$	$DQ10_B$										$DQ6_A$	NC	VSS	NC	E
F	$VDDQ_A$	$DQ11_B$	NC	VSS										VSS	$DQ6_B$	NC	$VDDQ_B$	F
G	NC	VSS	$DQ12_A$	NC										NC	$VDDQ_A$	$DQ5_A$	NC	G
H	VDD	NC	$VDDQ_B$	$DQ12_B$										VDD	NC	VSS	$DQ5_B$	H
J	$VDDQ_A$	VDD	VSS	ZZ_B										ZZ_A	VDD	VSS	$VDDQ_B$	J
K	$DQ14_B$	VSS	$DQ13_B$	VSS										$DQ3_B$	$VDDQ_A$	$DQ4_B$	VSS	K
L	NC	$DQ14_A$	$VDDQ_B$	$DQ13_A$										NC	$DQ3_A$	VSS	$DQ4_A$	L
M	$VDDQ_A$	NC	$DQ15_B$	VSS										VSS	NC	$DQ2_B$	$VDDQ_B$	M
N	NC	VSS	NC	$DQ15_A$										$DQ1_B$	$VDDQ_A$	NC	$DQ2_A$	N
P	$DQ16_B$	$DQ16_A$	$VDDQ_B$	$\overline{COL}_B$	$\overline{TRST}$	$A16_B$	$A12_B$	$A8_B$	NC	VDD	CLK_B	$\overline{INC}_B$	$A4_B$	NC	$DQ1_A$	VSS	NC	P
R	VSS	NC	$DQ17_B$	TCK	$A17_B$	$A13_B$	$A9_B$	NC	$\overline{CE0}_B$	VSS	$\overline{ADS}_B$	$A5_B$	$A1_B$	NC	$VDDQ_A$	$DQ0_B$	$VDDQ_B$	R
T	NC	$DQ17_A$	$VDDQ_A$	TMS	$A18^{[1]}{}_B$	$A14_B$	$A10_B$	$\overline{BE1}_B$	$CE1_B$	VSS	$R/\overline{W}_B$	$A6_B$	$A2_B$	VSS	NC	VSS	NC	T
U	VSS	$\overline{INT}_B$	$PL/\overline{FT}_B$	NC	$A15_B$	$A11_B$	$A7_B$	$\overline{BE0}_B$	VDD	$\overline{OE}_B$	$\overline{RPT}_B$	A3B	$A0_B$	VDD	OPT_B	NC	$DQ0_A$	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

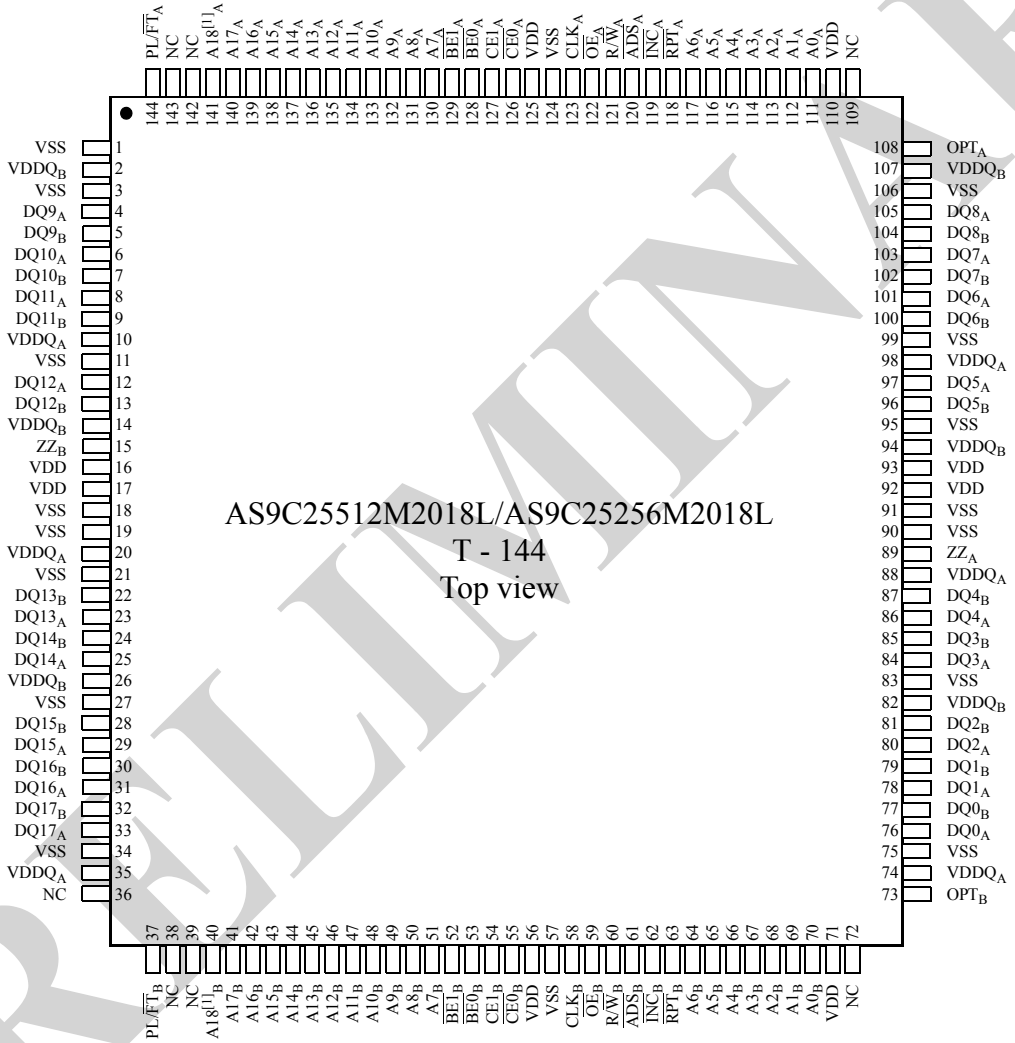
AS9C25512M2018L/AS9C25256M2018L
F - 208
Top view

PRELIMINARY

Note:

1. Address A18 is a NC for AS9C25256M2018L

Pin Assignment - 144-pin TQFP



Note:

1. Address A18 is a NC for AS9C25256M2018L

PRELIMINARY

Signal description

Signal		I/O	Properties	Description	Notes
Port A	Port B				
CLK_A	CLK_B	I	CLOCK	Clock. Each port has an independent Clock input that can be of different frequencies. All inputs except $\overline{OE}_x$ and ZZ_x are synchronous to the corresponding port's clock and must meet setup and hold time about the rising edge of the clock.	1
$A0_A$ - $A18_A$	$A0_B$ - $A18_B$	I	SYNC	External Address. Sampled on the rising edge of corresponding port clock	6
$DQ0_A$ - $DQ17_A$	$DQ0_B$ - $DQ17_B$	I/O	SYNC	Bidirectional data pins	
$\overline{CE0}_A$, $CE1_A$	$\overline{CE0}_B$, $CE1_B$	I	SYNC	Chip enable inputs. Active low and high, respectively. Sampled on the rising edge of corresponding port clock.	
R/W_A	R/W_B	I	SYNC	Read/Write enable. Drive this pin LOW to write to, or HIGH to Read from the memory array.	
$\overline{BE0}_A$ - $\overline{BE1}_A$	$\overline{BE0}_B$ - $\overline{BE1}_B$	I	SYNC	Byte Enable Inputs. Active low. Asserting these signals enables Read and Write operations to the corresponding bytes of the memory array. (Refer Byte Control Truth Table)	
$\overline{ADS}_A$	$\overline{ADS}_B$	I	SYNC	Address Strobe Enable.Active low. Loads external address onto the counter. (Refer Counter Control Truth Table)	
$\overline{INC}_A$	$\overline{INC}_B$	I	SYNC	Address Counter Increment. Active low. Increments the counter value. (Refer Counter Control Truth Table)	
$\overline{RPT}_A$	$\overline{RPT}_B$	I	SYNC	Address Counter Repeat. Active low. Reloads the counter with the previously loaded external address.(Refer Counter Control Truth Table)	
$\overline{OE}_A$	$\overline{OE}_B$	I	ASYNC	Asynchronous output enable. I/O pins are driven when the $\overline{OE}$ is low and the chip is in Read mode. A high on $\overline{OE}$ tristates the I/O pins.	
ZZ_A	ZZ_B	I	ASYNC	Snooze Mode Input. Places the device in low power mode. Data is retained. This pin has an internal pull-down and can be floating.	
$PL/\overline{FT}_A$	$PL/\overline{FT}_B$	I	STATIC	Pipeline/Flow-Through Select. When low, enables single register flow-through mode. When high, enables double register Pipeline mode. This pin has an internal pull-up and can be left floating to operate in pipeline mode.	
OPT_A	OPT_B	I	STATIC	$VDDQ_x$ Option. OPT_x selects the operating voltage levels for the I/Os, addresses, clock, and controls on that port. This pin has an internal pull-up and can be left floating to operate in 3.3V mode.	1,2,3
$\overline{INT}_A$	$\overline{INT}_B$	O	SYNC	Interrupt Flag. Used for message passing between two ports. (Refer Interrupt Logic Truth Table)	5
$\overline{COL}_A$	$\overline{COL}_B$	O	SYNC	Collision Alert Flag. Used to indicate collision during simultaneous memory access to the same location by both the ports (Refer Collision Detection Truth Table)	5
$VDDQ_A$	$VDDQ_B$	I	POWER	Power to I/O bus. Can be 3.3V or 2.5V depending on OPT_x input.	1,2,3
VDD		I	POWER	Power Inputs (To be connected to 2.5V Power supply)	2
VSS		I	GROUND	Ground Inputs (To be connected to Ground supply)	
TCK		I	CLOCK (JTAG)	JTAG Test Clock Input. All JTAG signals except $\overline{TRST}$ are synchronous to this clock.	4,5
TDI		I	SYNC (JTAG)	JTAG Test Data Input. Data on the TDI input will be shifted serially into selected registers.	4,5
TDO		O	SYNC (JTAG)	JTAG Test Data Output. TDO transitions occur on the falling edge of TCK. TDO is normally tristated except when the captured data is shifted out of the JTAG TAP.	5
TMS		I	SYNC (JTAG)	JTAG Test Mode Select Input. It controls the JTAG TAP state machine. State machine transitions occur on the rising edge of TCK.	4,5
$\overline{TRST}$		I	ASYNC (JTAG)	JTAG Test Reset Input. Asynchronous input used to initialize TAP controller.	4,5

Notes:
1. Subscript 'x' represents 'A' for Port A and 'B' for Port B.
2. OPT_x,$VDDQ_x$ and VDD must be set to appropriate operating levels before applying inputs on the I/Os and controls for that port.
3. OPT_x = VDD (2.5V) implies that corresponding port's I/Os, addresses, clock, and controls will operate at 3.3V level and $VDDQ_x$ must be supplied at 3.3V.
   OPT_x = VSS (0V) implies that corresponding port's I/Os, addresses, clock, and controls will operate at 2.5V level and $VDDQ_x$ must be supplied at 2.5V.
   Each port can independently operate on either of the VDDQ levels.
4. If unused JTAG inputs may be left unconnected.
5. JTAG, Collision Detection & Interrupt features are not supported in TQFP package.
6. Address A18 is a NC for AS9C25256M2018L.

PRELIMINARY

Byte control truth table[1,2,3,4,5]

$\overline{BE1}$	$\overline{BE0}$	CLK	Mode
H	H	L to H	All Bytes Deselected - NOP
H	L	L to H	Read or Write Byte 0
L	H	L to H	Read or Write Byte 1

Notes:
1. L = low, H = high
2. $\overline{CE0}$ = L, CE1 = H (Chip in Select mode)
3. R/$\overline{W}$ = H for a Read operation, R/$\overline{W}$ = L for a Write operation
4. Byte 1 - DQ[17:9], Byte 0 - DQ[8:0]
5. More than one byte enable may be simultaneously asserted

Read/write control truth table[1,4]

$\overline{CE}$[2]	R/$\overline{W}$	$\overline{BE_n}$[3]	CLK	Operation	DQ_n[0:8][3,7]
H	X	X	L to H	Chip Deselect	Hi-Z[5,9]
L	X	H	L to H	Byte Deselect	Hi-Z[5,9]
L	L	L	L to H	Byte Write	Din[6]
L	H	L	L to H	Byte Read	Qout[5,8]

Notes:
1. L = low, H = high, X = don't care
2. $\overline{CE}$ is an internal signal. $\overline{CE}$ = H implies 'Chip is Deselected' ($\overline{CE0}$ = H or CE1 =L), $\overline{CE}$ = L implies 'Chip is Selected' ($\overline{CE0}$ = L and CE1 =H)
3. $\overline{BE_n}$ refers to any one of the 2 byte controls [n = 1 or 0] and DQ_n refers to the corresponding Byte
4. Snooze de-asserted (ZZ=L)
5. True in flow-through mode. For Pipeline mode there will be a 1 cycle latency [refer timing diagrams]
6. For a write command issued before the completion of a read command, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. All DQs are tristated on power-up
8. $\overline{OE}$ should be asserted ($\overline{OE}$ = L) (Refer Read timing waveform)
9. In pipeline mode the DQs are HighZ-ed in the same cycle if R/$\overline{W}$=L

Counter control truth table[1,2,5,6]

CLK	$\overline{ADS}$[3]	$\overline{INC}$[3]	$\overline{RPT}$[3]	External Address	Previous Address Accessed	Mirror Register Content[4]	Address Accessed	Operation
L to H	L	X	H	An	X	An	An	Load[4]
L to H	H	L	H	X	An	Am	An + 1	Increment
L to H	H	H	H	X	An	Am	An	Hold
L to H	X	X	L	X	X	Am	Am	Repeat

Notes:
1. L = low, H = high, X = don't care
2. Cycle can be Read, Write or Deselect (Controlled by appropriate setting of R/$\overline{W}$, $\overline{CE0}$, CE1 and $\overline{BE_n}$)
3. $\overline{ADS}$, $\overline{INC}$, $\overline{RPT}$ are independent of all other memory controls including R/$\overline{W}$, $\overline{CE0}$,CE1 and $\overline{BE_n}$ (i.e Counter works independent of R/$\overline{W}$, $\overline{CE0}$,CE1 and $\overline{BE_n}$)
4. The 'Mirror register' used for the Repeat operation is loaded with External address during every valid $\overline{ADS}$ access. “Am” refers to the mirror register content.
5. Clock to the counter is disabled during Snooze mode (True for both ports).
6. The counter and the mirror registers are not initialized on Power-up (refer Counter description).

PRELIMINARY

Package Thermal Resistance

Description	Conditions		Symbol	Typical	Units
Thermal Resistance (junction to ambient)[1]	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	BGA	θ_{JA}	TBD	°C/W
		fpBGA	θ_{JA}	TBD	°C/W
		TQFP	θ_{JA}	TBD	°C/W
Thermal Resistance (junction to top of case)[1]			θ_{JC}	TBD	°C/W

Notes:
1. This parameter is sampled.

Capacitance[1] (T_A = +25 °C, F = 1.0 Mhz)[2]

Parameter	Symbol	Signals	Test Condition[3]	BGA (Max)	fpBGA (Max)	TQFP (Max)	Unit
Input Capacitance	C_{IN}	Address and Control pins	V_{IN} = L to H or H to L	TBD	TBD	TBD	pF
Output Capacitance	C_{OUT}	Flag Output pins	V_{OUT} = L to H or H to L	TBD	TBD	TBD	pF
I/O Capacitance	$C_{I/O}$	I/O pins	$V_{I/O}$ = L to H or H to L	TBD	TBD	TBD	pF

Notes:
1. Sampled, not 100% tested
2. T_A stands for 'Ambient temperature'.
3. L = 0V; H = 3V

Absolute maximum ratings[1]

Parameter	Symbol	Rating		Unit
		Min	Max	
Core supply voltage relative to VSS	VDD	-0.5	3.6	V
I/O supply voltage relative to VSS	VDDQ	-0.3	3.9	V
Input and I/O voltage relative to VSS	V_{IN}	-0.3	VDDQ + 0.3	V
Power Dissipation	P_D	-	TBD	W
Short circuit output current	I_{OUT}	-	TBD	mA
Storage Temperature	T_{STG}	-65	150	°C
Storage Temperature under Bias	T_{BIAS}	-55	125	°C
Junction Temperature	T_{JN}	-	TBD	°C

Notes:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating for extended periods may affect reliability.

PRELIMINARY

Recommended operating Temperature

Grade	Ambient Temperature (T_A)
Commercial	0°C to 70°C
Industrial	-40°C to 85°C

Recommended operating conditions

Parameter	Symbol	VDDQ = 2.5V[1]			VDDQ = 3.3V[2]			Unit
		Min	Typ	Max	Min	Typ	Max	
Core Supply Voltage	VDD	2.4	2.5	2.6	2.4	2.5	2.6	V
I/O supply Voltage	VDDQ	2.4	2.5	2.6	3.15	3.3	3.45	V
Ground	VSS	0	0	0	0	0	0	V

Notes:
1. OPT pin for a given port must be set to VSS(0V) to operate at VDDQ = 2.5V levels on the I/Os, addresses, clock and controls of that port.
2. OPT pin for a given port must be set to VDD(2.5V) to operate at VDDQ = 3.3V levels on the I/Os, addresses, clock and controls of that port.

DC Electrical Characteristics (VDD = 2.5 V ± 100 mV)

Parameter	Symbol	VDDQ = 2.5V			VDDQ = 3.3V			Units
		Test Conditions	Min	Max	Test Conditions	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	VDDQ = Max; $0V \le V_{IN} \le VDDQ$	-	2	VDDQ = Max; $0V \le V_{IN} \le VDDQ$	-	2	µA
PL/$\overline{FT}$ and ZZ Input Leakage Current	$\|I_{LI}\|$	VDD = Max; $0V \le V_{IN} \le VDD$	-	2	VDD = Max; $0V \le V_{IN} \le VDD$	-	2	µA
Output Leakage Current[1]	$\|I_{LO}\|$	$\overline{OE}$>=VIH; $0V \le V_{OUT} \le VDDQ$	-	2	$\overline{OE}$>=VIH; $0V \le V_{OUT} \le VDDQ$	-	2	µA
Input high (logic 1) voltage (Address, Control, Clock & Data Inputs)	V_{IH}	-	1.7	VDDQ + 0.1V	-	2	VDDQ + 0.15V	V
Input high voltage (ZZ,OPT,PL/$\overline{FT}$)	V_{IH}	-	VDD - 0.2V	VDD + 0.1V	-	VDD - 0.2V	VDD + 0.1V	V
Input low (logic 0) voltage (Address, Control, Clock & Data Inputs)	V_{IL}	-	-0.3	0.7	-	-0.3	0.8	V
Input low voltage (ZZ,OPT,PL/$\overline{FT}$)	V_{IL}	-	-0.3	0.2	-	-0.3	0.2	V
Output low voltage	V_{OL}	I_{OL} = +2mA; VDDQ = Min	-	0.4	I_{OL} = +4mA; VDDQ = Min	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -2mA; VDDQ = Min	2.0	-	I_{OH} = -4mA; VDDQ = Min	2.4	-	V

Notes:
1. Outputs disabled (High-Z condition).

PRELIMINARY

I_{DD} operating conditions and maximum limits[4] (VDD = 2.5 V ± 100 mV)

Parameter	Symbol	Test Conditions	-250		-200		-166		-133		Units
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Operating current (Both ports active) Pipeline mode ($PL/\overline{FT} \geq V_{IH}$)	I_{CC}	Both ports enabled ($\overline{CE}_A = \overline{CE}_B = L$[3]), Outputs disabled ($I_{OUT}$ = 0mA), $ZZ_A = ZZ_B \leq V_{IL}$, f=f_{Max}[1]	TBD	TBD	TBD	350	TBD	300	TBD	260	mA
Operating current (Both ports active) Flow-through mode ($PL/\overline{FT} \leq V_{IL}$)			TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
Standby current (Both ports)	I_{SB1}	Both ports disabled ($\overline{CE}_A = \overline{CE}_B$ = H), $ZZ_A = ZZ_B \leq V_{IL}$, f=f_{Max}[1]	TBD	TBD	TBD	105	TBD	90	TBD	80	mA
Standby current (One port)	I_{SB2}	One port enabled ($\overline{CE}_A$ = L and $\overline{CE}_B$ = H)[5], Active port's outputs disabled, $ZZ_A = ZZ_B \leq V_{IL}$, f=f_{Max}[1]	TBD	TBD	TBD	265	TBD	225	TBD	190	mA
Full standby current (Both ports)	I_{SB3}	Both ports disabled ($\overline{CE}_A = \overline{CE}_B$ = H), $ZZ_A = ZZ_B \leq V_{IL}$, f=0[2]	20	25	20	25	20	25	20	25	mA
Full standby current (One port)	I_{SB4}	One port in Snooze ($ZZ_A \geq V_{IH}$, $ZZ_B \leq V_{IL}$, and $\overline{CE}_B$ = L)[5], Active port's outputs disabled, f=f_{Max}[1]	TBD	TBD	TBD	265	TBD	225	TBD	190	mA
Snooze mode current	I_{ZZ}	Both ports in Snooze ($ZZ_A = ZZ_B \geq V_{IH}$), f=f_{Max}[1]	15	18	15	18	15	18	15	18	mA

Notes:

1. f=f_{Max} implies address and controls (except $\overline{OE}$) are cycling at maximum clock frequency using AC test conditions (Refer AC test conditions).
2. f = 0 implies address and controls are static. Corresponding current numbers indicated are true for both CMOS ($V_{IN} \geq$ VDDQ - 0.2V or $V_{IN} \leq$ 0.2V) and TTL ($V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$) level inputs.
3. $\overline{CE}_A$ and $\overline{CE}_B$ are internal signals ($\overline{CE}_x$ = L implies $\overline{CE0}_x \leq V_{IL}$ and $CE1_x \geq V_{IH}$, $\overline{CE}_x$ = H implies $\overline{CE0}_x \geq V_{IH}$ or $CE1_x \leq V_{IL}$).
4. Subscript 'x' represents 'A' for Port A and 'B' for Port B.
5. "A" and "B" are interchangeable.

PRELIMINARY

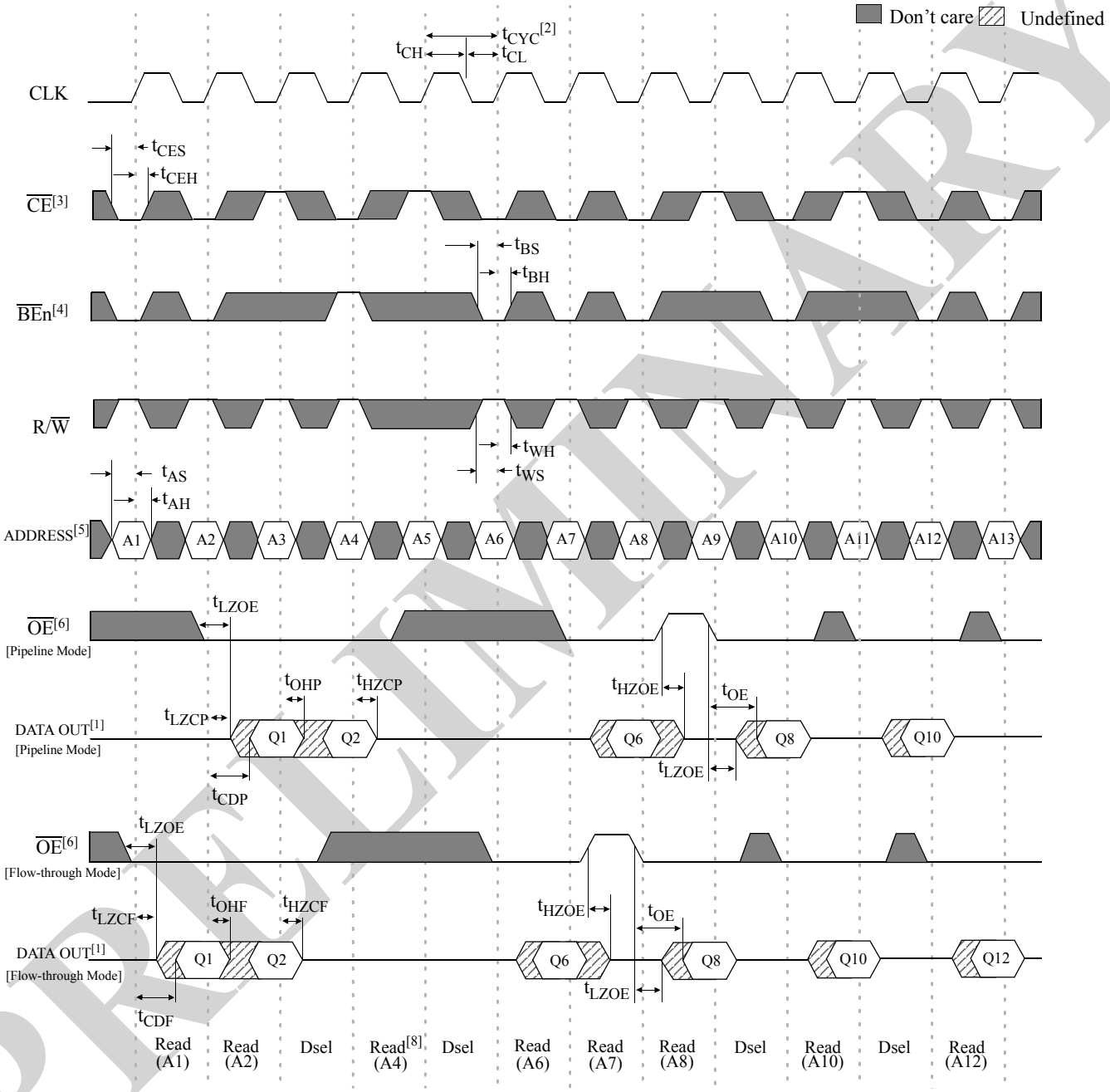
AC timing characteristics[1,2,5,6] (VDD = 2.5 ± 100mV)

Parameter	Symbol	-250		-200		-166		-133		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Clock											
Cycle Time (Pipeline)	t_{CYCP}	4	-	5	-	6	-	7.5	-	ns	3
Clock High Pulse Width (Pipeline)	t_{CHP}	1.7	-	2	-	2.4	-	3	-	ns	3
Clock Low Pulse Width (Pipeline)	t_{CLP}	1.7	-	2	-	2.4	-	3	-	ns	3
Cycle Time (Flow-Through)	t_{CYCF}	6.5	-	7.5	-	10	-	12	-	ns	3
Clock High Pulse Width (Flow-Through)	t_{CHF}	1.7	-	2	-	2.4	-	3	-	ns	3
Clock Low Pulse Width (Flow-Through)	t_{CLF}	1.7	-	2	-	2.4	-	3	-	ns	3
Output											
Clock access time (Pipeline)	t_{CDP}	-	2.8	-	3.4	-	3.6	-	4.2	ns	3
Output Data Hold from Clock High (Pipeline)	t_{OHP}	1	-	1	-	1	-	1	-	ns	
Clock High to Output Low-Z (Pipeline)	t_{LZCP}	1	-	1	-	1	-	1	-	ns	3,8
Clock High to Output High-Z (Pipeline)	t_{HZCP}	1	2.8	1	3.4	1	3.6	1	4.2	ns	3,8
Clock access time (Flow-Through)	t_{CDF}	-	6.5	-	7.5	-	10	-	12	ns	3
Output Data Hold from Clock High (Flow-Through)	t_{OHF}	1	-	1	-	1	-	1	-	ns	
Clock High to Output Low-Z (Flow-Through)	t_{LZCF}	1	-	1	-	1	-	1	-	ns	3,8
Clock High to Output High-Z (Flow-Through)	t_{HZCF}	1	2.8	1	3.4	1	3.6	1	4.2	ns	3,8
Output Enable to Data Valid	t_{OE}	-	2.8	-	3.4	-	3.6	-	4.2	ns	4
Output Enable Low to Output Low-Z	t_{LZOE}	1	-	1	-	1	-	1	-	ns	4
Output Enable High to Output High-Z	t_{HZOE}	1	2.8	1	3.4	1	3.6	1	4.2	ns	4
Setup											
Address Setup to Clock High	t_{AS}	1.2	-	1.5	-	1.7	-	1.8	-	ns	
Chip Enable Setup to Clock High	t_{CES}	1.2	-	1.5	-	1.7	-	1.8	-	ns	
Byte Enable Setup to Clock High	t_{BS}	1.2	-	1.5	-	1.7	-	1.8	-	ns	
R/$\overline{W}$ Setup to Clock High	t_{WS}	1.2	-	1.5	-	1.7	-	1.8	-	ns	
Input Data Setup to Clock High	t_{DS}	1.2	-	1.5	-	1.7		1.8	-	ns	
$\overline{ADS}$ Setup to Clock High	t_{ADSS}	1.2	-	1.5	-	1.7	-	1.8	-	ns	
$\overline{INC}$ Setup to Clock High	t_{INCS}	1.2	-	1.5	-	1.7	-	1.8	-	ns	
$\overline{RPT}$ Setup to Clock High	t_{RPTS}	1.2	-	1.5	-	1.7	-	1.8	-	ns	
Hold											
Address Hold from Clock High	t_{AH}	0.3	-	0.5	-	0.5	-	0.5	-	ns	
Chip Enable Hold from Clock High	t_{CEH}	0.3	-	0.5	-	0.5	-	0.5	-	ns	
Byte Enable Hold from Clock High	t_{BH}	0.3	-	0.5	-	0.5	-	0.5	-	ns	
R/$\overline{W}$ Hold from Clock High	t_{WH}	0.3	-	0.5	-	0.5	-	0.5	-	ns	
Input Data Hold from Clock High	t_{DH}	0.3	-	0.5	-	0.5	-	0.5	-	ns	
$\overline{ADS}$ Hold from Clock High	t_{ADSH}	0.3	-	0.5	-	0.5	-	0.5	-	ns	
$\overline{INC}$ Hold from Clock High	t_{INCH}	0.3	-	0.5	-	0.5	-	0.5	-	ns	
$\overline{RPT}$ Hold from Clock High	t_{RPTH}	0.3	-	0.5	-	0.5	-	0.5	-	ns	
Flag											
Interrupt Flag Set Time	t_{SINT}	-	6	-	6	-	6	-	7	ns	
Interrupt Flag Reset Time	t_{RINT}	-	6	-	6	-	6	-	7	ns	
Collision Flag Set Time	t_{SCOL}	-	2.8	-	3.4	-	3.6	-	4.2	ns	
Collision Flag Reset Time	t_{RCOL}	-	2.8	-	3.4	-	3.6	-	4.2	ns	
Port-to-Port Delay											
Clock-to-Clock Delay	t_{CCO}	3.0	-	3.5	-	4	-	5	-	ns	7

Notes:
1. All timings are same for both ports.
2. These values are valid for either level of VDDQ (2.5V/3.3V)
3. A particular port will operate in Pipeline output mode if PL/$\overline{FT}$ = VDD and in flow-through output mode if PL/$\overline{FT}$ = 0V. Each port can independently operate in any of these modes.
4. Output Enable ($\overline{OE}$) is an asynchronous input.
5. PL/$\overline{FT}$ and OPT should be treated as DC signals and should reach steady state before normal operation.
6. Refer AC Test Conditions to view the test conditions used for these measurements.
7. This parameter has to be taken care to avoid collision during simultaneous memory access of the same location.
8. To avoid bus contention, at a given voltage and temperature t_{LZC} is more than t_{HZC} (True in both Pipeline and flow-through output mode).

PRELIMINARY

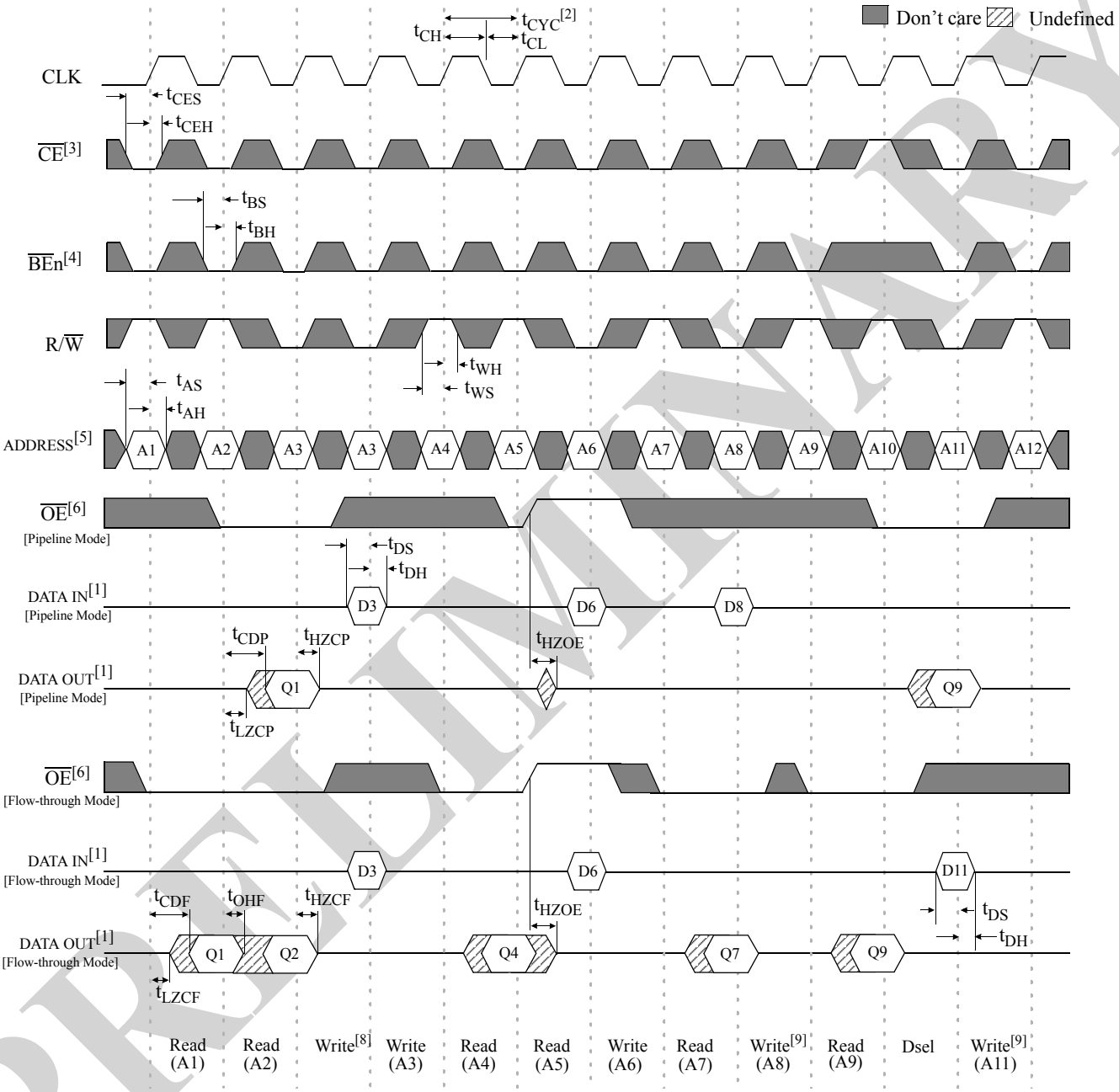
Timing waveform of read cycle[7]



Notes:
1. Both Flow-through and Pipeline Outputs indicated. A particular port is configured in Flow-through mode if PL/$\overline{FT}$ for that port is driven low, and in Pipeline mode if PL/$\overline{FT}$ is driven high or left unconnected.
2. Parameters t_{CYC}, t_{CH} and t_{CL} are different in Flow-through and Pipeline modes of operation (Refer AC Timing characteristics).
3. $\overline{CE}$ is an internal signal.$\overline{CE}$ = H implies 'Chip is Deselected' ($\overline{CE0}$ = H or CE1 =L), $\overline{CE}$ = L implies 'Chip is Selected' ($\overline{CE0}$ = L and CE1 =H). Timings indicated for $\overline{CE}$ hold good for $\overline{CE0}$ and CE1
4. $\overline{BE}$n refers to any one of the 2 byte controls [n = 1 or 0] and DATA OUT refers to the corresponding Byte.
5. Counter set in "Load" mode ($\overline{ADS}$ = L,$\overline{INC}$ = X,$\overline{RPT}$ = H).
6. $\overline{OE}$ is an asynchronous input.
7. All timings are similar for both ports.
8. Read with Byte disabled. Data is not read out.Bus in High-Z condition.

PRELIMINARY

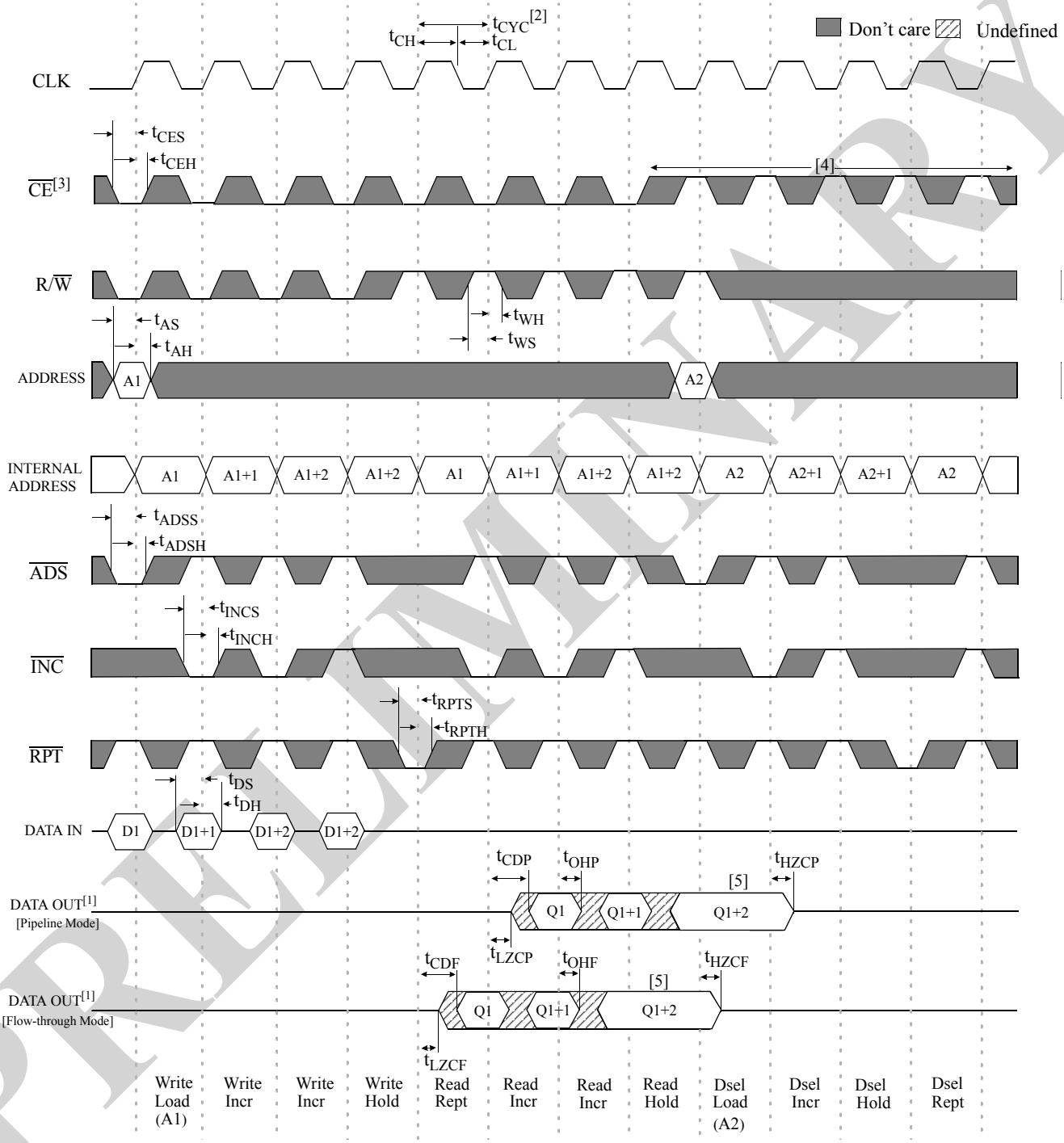
Timing wave form read/write cycle[7]



Notes:
1. Both Flow-through and Pipeline Inputs/Outputs indicated.A particular port is configured in Flow-through mode if PL/$\overline{FT}$ for that port is driven low, and in Pipeline mode if PL/$\overline{FT}$ is driven high or left unconnected.
2. Parameters t_{CYC},t_{CH} and t_{CL} are different in Flow-through and Pipeline modes of operation.(Refer AC Timing characteristics)
3. $\overline{CE}$ is an internal signal.$\overline{CE}$ = H implies 'Chip is Deselected' ($\overline{CE0}$ = H or CE1 =L), $\overline{CE}$ = L implies 'Chip is Selected' ($\overline{CE0}$ = L and CE1 =H). Timings indicated for $\overline{CE}$ hold good for $\overline{CE0}$ and CE1
4. $\overline{BE}$n refers to any one of the 2 byte controls [n = 1 or 0] and DATA OUT refers to the corresponding Byte.
5. Counter set in "Load" mode ($\overline{ADS}$ = L,$\overline{INC}$ = X,$\overline{RPT}$ = H).
6. $\overline{OE}$ is an asynchronous input.
7. All timings are similar for both ports.
8. Invalid write. Memory Content of the selected location may get corrupted and should be re-written before future readback.
9. Write (A11) is invalid in Pipeline mode and Write (A8) is invalid in Flow-through mode. Memory Content of the selected location may get corrupted and should be re-written before future readback.

PRELIMINARY

Timing waveform of address counter[6]



Notes:
1. Both Flow-through and Pipeline Outputs indicated. A particular port is configured in Flow-through mode if PL/$\overline{FT}$ for that port is driven low, and in Pipeline mode if PL/$\overline{FT}$ is driven high or left unconnected.
2. Parameters t_{CYC},t_{CH} and t_{CL} are different in Flow-through and Pipeline modes of operation (Refer AC Timing characteristics).
3. $\overline{CE}$ is an internal signal. $\overline{CE}$ = H implies 'Chip is Deselected' ($\overline{CE0}$ = H or CE1 =L), $\overline{CE}$ = L implies 'Chip is Selected' ($\overline{CE0}$ = L and CE1 =H). Timings indicated for $\overline{CE}$ hold good for $\overline{CE0}$ and CE1.
4. These cycles indicate that Counter works independent of all memory controls including R/$\overline{W}$,$\overline{CE}$ and $\overline{BE}$n.
5. If a Hold operation is performed for a Read access, the Data-out is held valid for the subsequent clock cycle also.
6. All timings are similar for both ports.

PRELIMINARY

Mailbox Interrupts

The AS9C25512M2018L/AS9C25256M2018L has an Inbuilt Mailbox Logic that can be used for communication between the two ports. One memory location is assigned as mail box (message center) for each port. The location 7FFFE (HEX) is assigned as the message center for Port A and 7FFFF (HEX) for Port B (3FFFE and 3FFFF for AS9C25256M2018L). The port A interrupt flag ($\overline{INT}_A$) is asserted when the port B writes to memory location 7FFFE (HEX) (3FFFE for AS9C25256M2018L). The port A clears the interrupt flag by reading the address location 7FFFE (HEX) (3FFFE for AS9C25256M2018L). Likewise, the port B interrupt flag ($\overline{INT}_B$) is asserted when the port A writes to memory location 7FFFF (HEX) (3FFFF for AS9C25256M2018L) and to clear the interrupt flag ($\overline{INT}_B$), the port B must read the memory location 7FFFF (3FFFF for AS9C25256M2018L).(Refer Interrupt Logic Truth Table).

The interrupt flag is asserted in a flow-through mode (i.e., it follows the clock edge of the writing port). Also, the flag is reset in a flow-through mode (i.e., it follows the clock edge of the reading port). Each port can read the other port's mailbox without de-asserting the interrupt and each port can write to its own mailbox without asserting the interrupt. If an application does not require message passing, $\overline{INT}$ pins can be ignored.

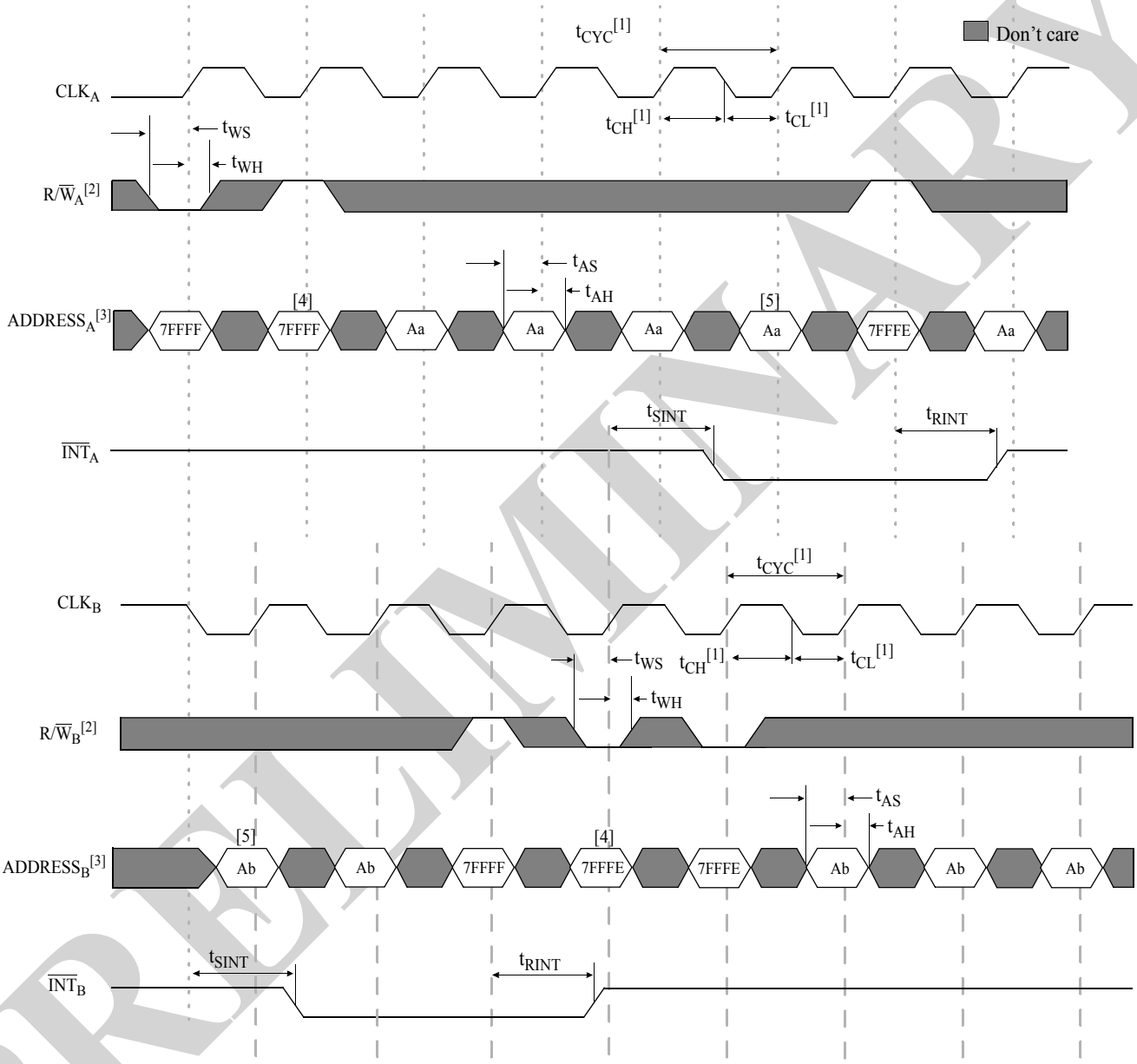
Interrupt logic truth table[1,4,5]

CLK_A	$R/\overline{W}_A$	$\overline{CE}_A$[2]	$A18_A$-$A0_A$[3,6]	CLK_B	$R/\overline{W}_B$	$\overline{CE}_B$[2]	$A18_B$-$A0_B$[3,6]	$\overline{INT}_A$	$\overline{INT}_B$	Function
L to H	L	L	7FFFF	L to H	X	X	X	X	L	Assert Port B Interrupt Flag
L to H	X	X	X	L to H	H	L	7FFFF	X	H	De-assert Port B Interrupt Flag
L to H	X	X	X	L to H	L	L	7FFFE	L	X	Assert Port A Interrupt Flag
L to H	H	L	7FFFE	L to H	X	X	X	H	X	De-assert Port A Interrupt Flag

Notes:
1. L = low, H = high, X = don't care
2. $\overline{CE}_x$ is an internal signal ('x' = 'A' or 'B'). $\overline{CE}_x$ = H implies 'Chip is Deselected' ($\overline{CE0}_x$ = H or $CE1_x$ =L), $\overline{CE}_x$ = L implies 'Chip is Selected' ($\overline{CE0}_x$ = L and $CE1_x$ =H)
3. Address specified here is the internal address (refer Counter control truth table).
4. Both Interrupt Flags are De-asserted on power-up.
5. Interrupt feature is not supported in TQFP package.
6. Address A18 is a NC for AS9C25256M2018L, hence Interrupt addresses are 3FFFF and 3FFFE

PRELIMINARY

Interrupt timing wave form[2]



Notes:
1. Parameters t_{CYC},t_{CH} and t_{CL} are different in Flow-through and Pipeline mode of operation and can be different for different ports (Refer AC Timing characteristics).
2. Chip Selected ($\overline{CE0}$ = L and CE1 =H). True for both ports.
3. Address indicated is the Internal Address used and is dependent on the Address counter control inputs for that cycle.
4. 7FFFF (3FFFF for AS9C25256M2018L) is the Mailbox for port B and 7FFFE (3FFFE for AS9C25256M2018L) is the Mailbox for port A.
5. "Aa" and "Ab" refer to any other valid address other than 7FFFF or 7FFFE (3FFFF or 3FFFE for AS9C25256M2018L).

PRELIMINARY

Collision detection

Three different cases of collisions can be listed depending on the type of access from two ports:

Simultaneous Read: A true dual-ported memory cell allows data to be read simultaneously from both ports of the device. Hence no data is corrupted, lost, or incorrectly output, and none of the collision alert flags is asserted.

Simultaneous Write: When both ports are writing simultaneously to the same location, both write operations would fail. Therefore, the collision flag is asserted on both ports.

Simultaneous Read and Write: When one port is writing and the other port is reading from the same location in the memory, the data written will be valid. However, the read operation would fail and hence the reading port's collision flag is asserted.

The alert flag ($\overline{COL}_X$) is asserted on the 3rd (for both pipe-lined and flow-through output mode) rising clock edge of the affected port following the collision, and remains low for one cycle. On continuous collisions (one or both ports writing during each access), the collision alert flag will be asserted and de-asserted every alternate cycle.

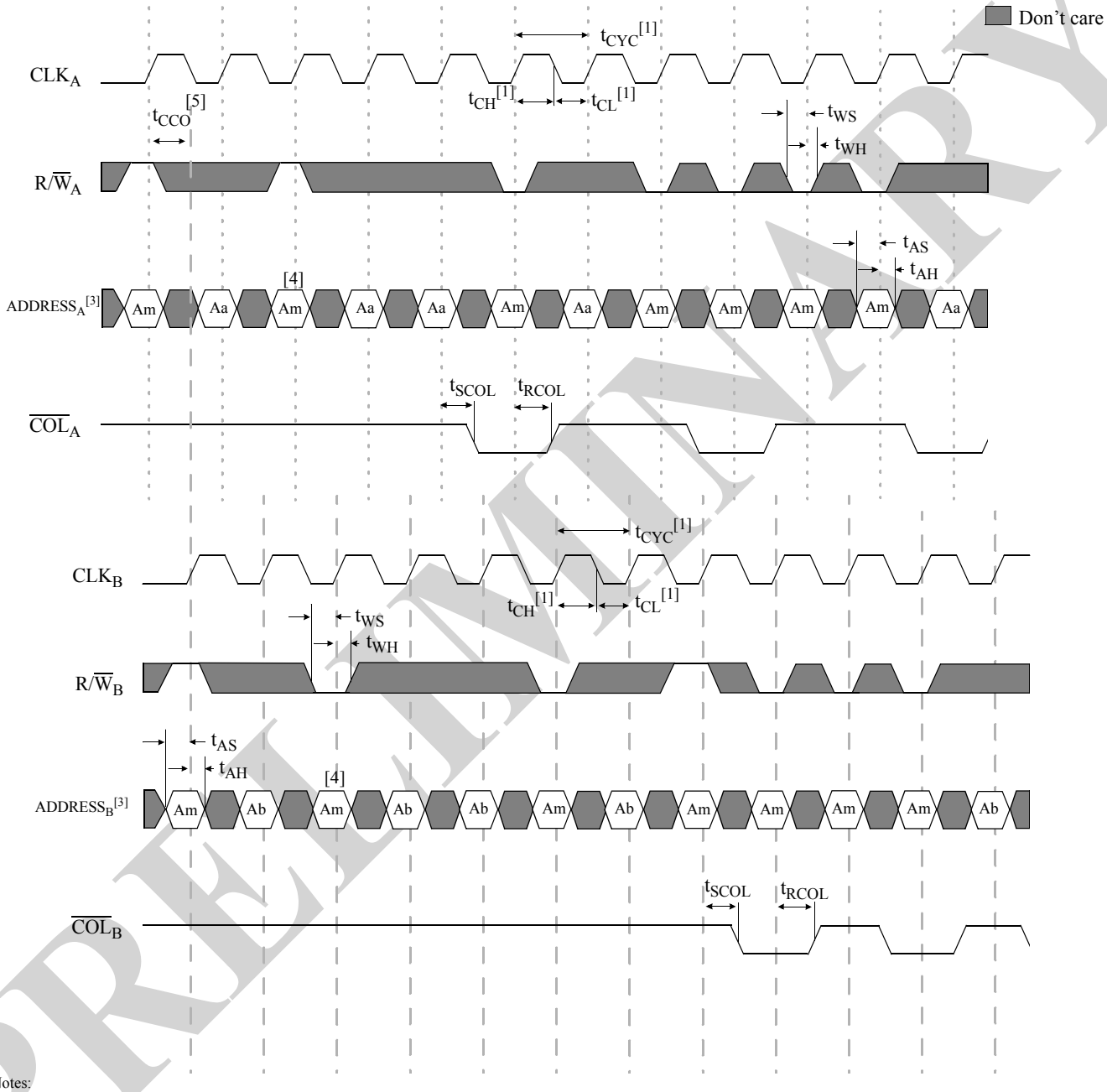
Collision detection truth table[1,2,4,5]

CLK_A	$R/\overline{W}_A$	CLK_B	$R/\overline{W}_B$	Port address[3]	$\overline{COL}_A$	$\overline{COL}_B$	Function
L to H	H	L to H	H	MATCH	H	H	Both ports reading. Not a valid collision. No collision flag asserted on either port.
L to H	H	L to H	L	MATCH	L	H	Port A reading, Port B writing. Valid collision. Collision flag asserted on port A.
L to H	L	L to H	H	MATCH	H	L	Port B reading, Port A writing. Valid collision. Collision flag asserted on port B.
L to H	L	L to H	L	MATCH	L	L	Both ports writing. Valid collision. Collision flag asserted on both ports.
L to H	L	L to H	H	NO MATCH	H	H	No match. No collision flag asserted on either port.

Notes:
1. L = low, H = high, X = don't care
2. Chip Selected ($\overline{CE0}$ = L and CE1 =H). True for both ports. Collision flag is not affected if any one or both ports are deselected.
3. "MATCH" indicates that internal addresses of both the ports are the same (refer Counter control truth table).
4. Both Collision Flags are De-asserted on power-up.
5. Collision detection feature is not supported in TQFP package.

PRELIMINARY

Collision timing waveform[2]

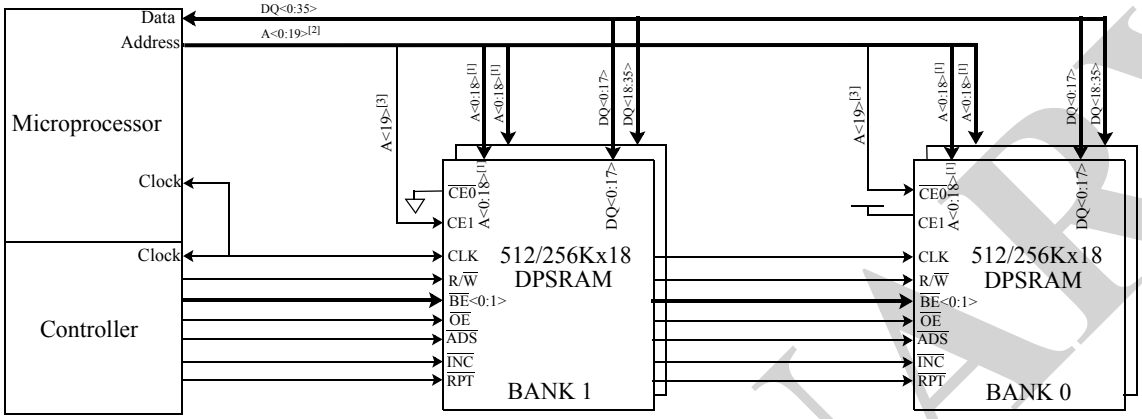


Notes:
1. Parameters t_{CYC},t_{CH} and t_{CL} are different in Flow-through and Pipeline mode of operation and can be different for different ports (Refer AC Timing characteristics).
2. Chip Selected ($\overline{CE0}$ = L and CE1 =H). True for both ports.
3. Address indicated is the Internal Address used and is dependent on the Address counter control inputs for that cycle.
4. "Am" refers to matched address. "Aa" and "Ab" refer to any other valid address.
5. During address collision the data validity is guaranteed only if t_{CCO} is greater than the minimum specified (Refer AC timing characteristics).

PRELIMINARY

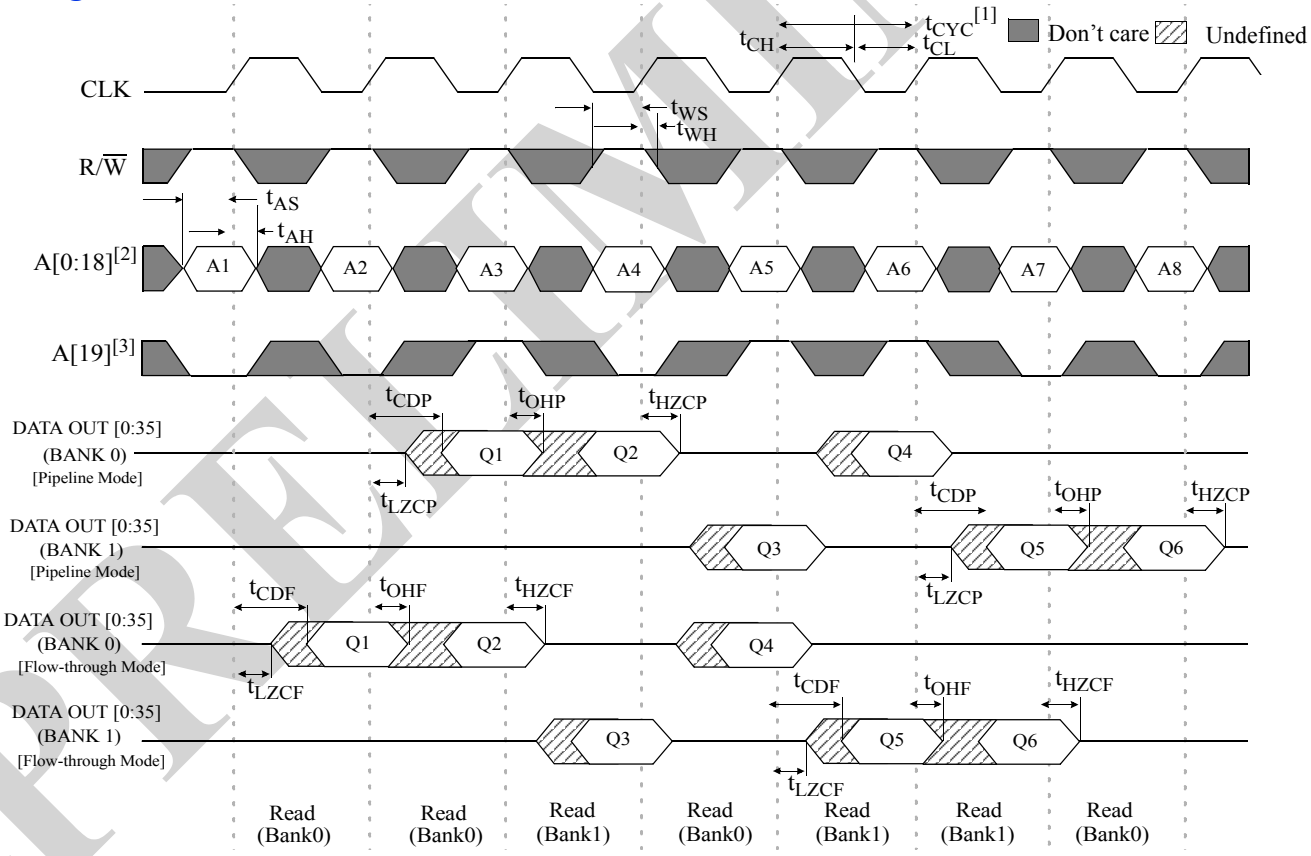
Depth and Width expansion

AS9C25512M2018L/AS9C25256M2018L has two chipselects (one active high and other active low) for simple depth expansion. This permits easy upgrade from 512/256K depth to 1M/512K depth without extra logic. Two such parts can also be combined to obtain an expanded width of 36 bits or wider.



Notes:
1. A<0:18> for AS9C25512M2018L, A<0:17> for AS9C25256M2018L
2. A<0:19> for AS9C25512M2018L, A<0:18> for AS9C25256M2018L
3. A<19> for AS9C25512M2018L, A<18> for AS9C25256M2018L

Timing waveform of multi device read[4,5,6]



Notes:
1. Parameters t_{CYC}, t_{CH} and t_{CL} are different in Flow-through and Pipeline mode of operation (Refer AC Timing characteristics).
2. A<0:18> for AS9C25512M2018L, A<0:17> for AS9C25256M2018L
3. A<19> for AS9C25512M2018L, A<18> for AS9C25256M2018L
4. Refer to the above block diagram for the assumed setup.
5. One Bank is assumed to have two AS9C25512M2018L/AS9C25256M2018Ls combined to have an expanded width of 36 bits. Two such Banks are used for depth expansion.
6. All $\overline{BE}$n's = L, Counter set in "Load" mode ($\overline{ADS}$ = L, $\overline{INC}$ = X, $\overline{RPT}$ = H), $\overline{OE}$ =L.

PRELIMINARY

Snooze mode

Snooze mode is a low-current, power-down mode in which the corresponding port is deselected and its current is reduced to a very low value. Both ports are equipped with independent SNOOZE inputs (ZZ). During Snooze mode, all inputs of the port except ZZ are internally disabled and all its Outputs go to High-Z.

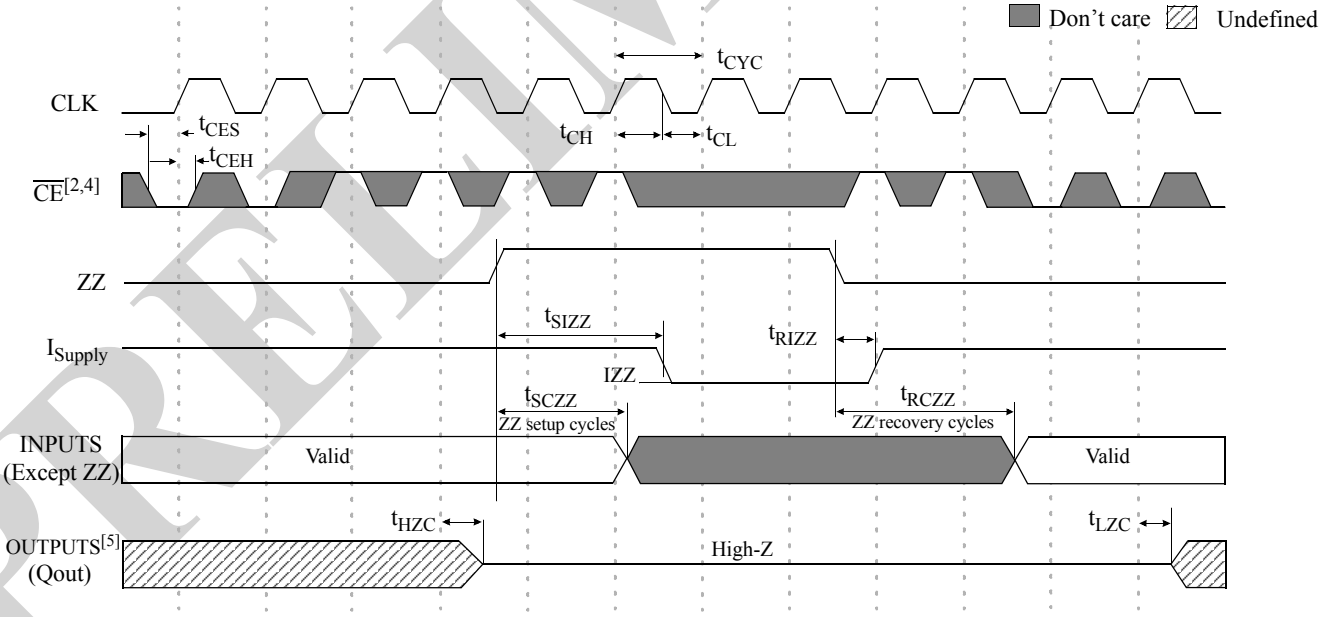
ZZ is an asynchronous, active HIGH input that causes the selected port to enter Snooze mode. If both ports go into Snooze mode, the device is deselected and current is reduced to I_{ZZ}. When ZZ_A and ZZ_B become a logic HIGH, I_{ZZ} is guaranteed after the setup time t_{SCZZ} is met.

Any READ or WRITE operation pending when the port enters Snooze mode is not guaranteed to complete. Therefore, Snooze mode must not be initiated until valid pending operations are completed. Similarly during the time t_{RCZZ}, when the port is transitioning out of snooze mode, only DESELECT cycles should be given.

Snooze mode electrical characteristics

Description	Conditions	Symbol	Min	Max	Units
SNOOZE MODE Current	$ZZ_A = ZZ_B >= V_{IH}$	I_{ZZ}	15	18	mA
ZZ active to input ignored		t_{SCZZ}	-	2	cycle
ZZ inactive to input sampled		t_{RCZZ}	2	-	cycle
ZZ active to enter Snooze Current		t_{SIZZ}	-	2	cycle
ZZ inactive to exit Snooze Current		t_{RIZZ}	0	-	cycle

Snooze mode timing waveform[1,3]



Notes:
1. During Snooze mode, all dynamic inputs are disabled (except JTAG inputs). During JTAG operations, ZZ_x must be held Low in order to capture the parallel inputs of the boundary scan register. All static inputs (i.e. PL/FT_x,OPT_x) and ZZ_x themselves are not affected during snooze mode.
2. $\overline{CE}$ is an internal signal. $\overline{CE}$ = H implies 'Chip is Deselected' ($\overline{CE0}$ = H or CE1 =L), $\overline{CE}$ = L implies 'Chip is Selected' ($\overline{CE0}$ = L and CE1 =H).
3. All timings are same for Port A and Port B.
4. Minimum of two deselect cycles should be given before asserting snooze and minimum of two deselect cycles should be given after de-asserting snooze to guarantee data integrity.
5. Select cycles indicated before and after Snooze are Read cycles. They can also be Write cycles.

PRELIMINARY

AC test conditions

Input Pulse Level (Address and Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2V/ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference levels	1.5V/1.25V
Output Load (for t_{LZC}, t_{HZC}, t_{LZOE}, t_{HZOE})	Fig. C
Output Load (for all other measurements)	Fig. B

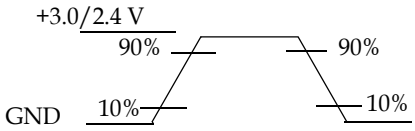


Figure A: Input Waveform

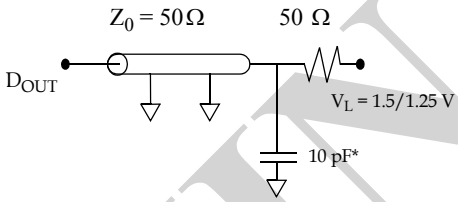


Figure B: Output Load (A)

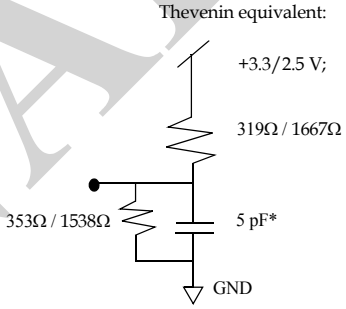


Figure C: Output Load (B)

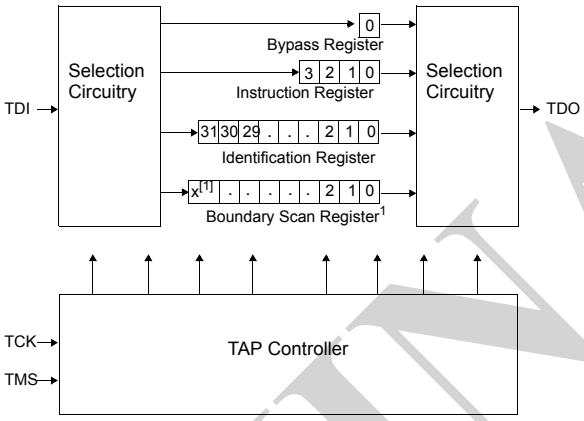
* Including scope and jig capacitance

PRELIMINARY

IEEE 1149.1 Serial boundary scan (JTAG)

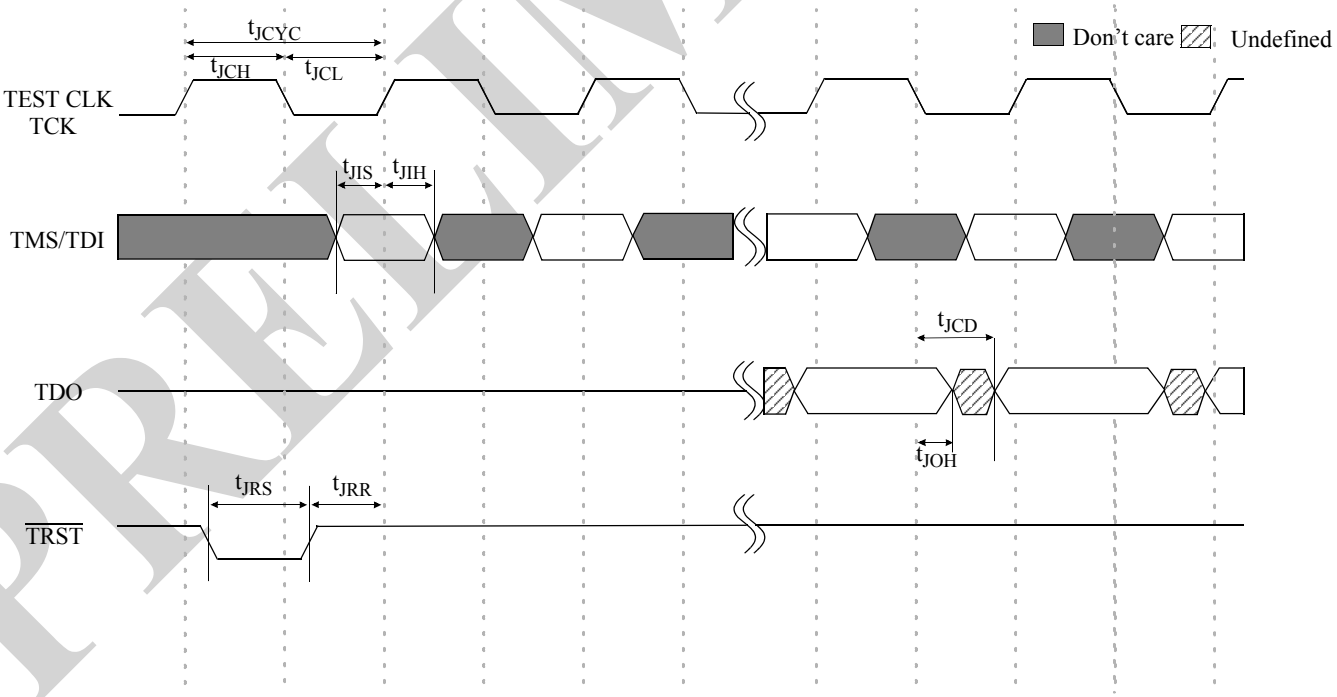
The SRAM incorporates a serial boundary scan Test Access Port (TAP). All JTAG pins operate using JEDEC standard 2.5V I/O logic levels. In order to operate the device without using the JTAG feature, all JTAG pins may be left unconnected. On power-up, the device will start in a reset state which will not interfere with normal device operation.

TAP Controller block diagram



Note:
1. x = 111

JTAG timing waveform



PRELIMINARY

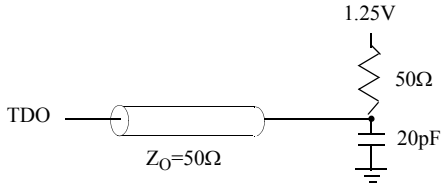
TAP AC electrical characteristics[2]

Description	Symbol	Min	Max	Units
Clock				
Clock cycle time	t_{JCYC}	100	-	ns
Clock frequency	f_{JTAG}	-	10	MHz
Clock high time	t_{JCH}	40	-	ns
Clock low time	t_{JCL}	40	-	ns
Output Times				
TCK low to TDO unknown	t_{JOH}	0	-	ns
TCK low to TDO valid	t_{JCD}	-	20	ns
Setup Times				
TMS/TDI setup	t_{JIS}	10	-	ns
Capture setup	t_{JCS}[1]	10	-	ns
Hold Times				
TMS/TDI hold	t_{JIH}	10	-	ns
Capture hold	t_{JCH}[1]	10	-	ns
Reset Times				
JTAG Reset	t_{JRS}	50	-	ns
JTAG Reset Recovery	t_{JRR}	50	-	ns

Notes:
1. t_{JCS} and t_{JCH} refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in the figure TAP AC output load equivalent.

TAP AC test conditions & output load equivalent

Input pulse levels	Vss to 2.5V
Input rise and fall times	1V/ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Test load termination supply voltage	1.25V



TAP DC electrical characteristics and operating conditions (VDD=2.5V ± 100 mV)

Description	Symbol	Conditions	Min	Max	Units
Input high (logic 1) voltage	V_{IH}		1.7	VDD + 0.3	V
Input low (logic 0) voltage	V_{IL}		-0.3	0.7	V
Input leakage current	$\|I_{LI}\|$	VDD = Max; 0V < V_{IN} < VDD	0	10	µA
Output leakage current	$\|I_{LO}\|$	Outputs disabled, 0V < V_{OUT} < VDDQ (DQ_x)	0	10	µA
Output low voltage	V_{OLC}	I_{OLC} = 100µA		0.2	V
Output low voltage	V_{OLT}	I_{OLT} = 2mA		0.7	V
Output high voltage	V_{OHC}	I_{OHC} = -100µA	2.1		V
Output high voltage	V_{OHT}	I_{OHT} = -2mA	1.7		V

PRELIMINARY

Identification register definitions

Instruction field	Value	Description
Revision number (31:28)	TBD	Version Number
Device depth (27:12)	TBD	ALSC part number
JEDEC ID code (11:1)	00001010010	Manufacturer Identity Code (ALSC)
Indicator Bit (0)	1	ID Register presence indicator

Scan register sizes

Register name	Bit size
Instruction Register (IR)	4
Bypass Register (BYR)	1
Identification Register (IDR)	32
Boundary Scan Register (BSR)	112

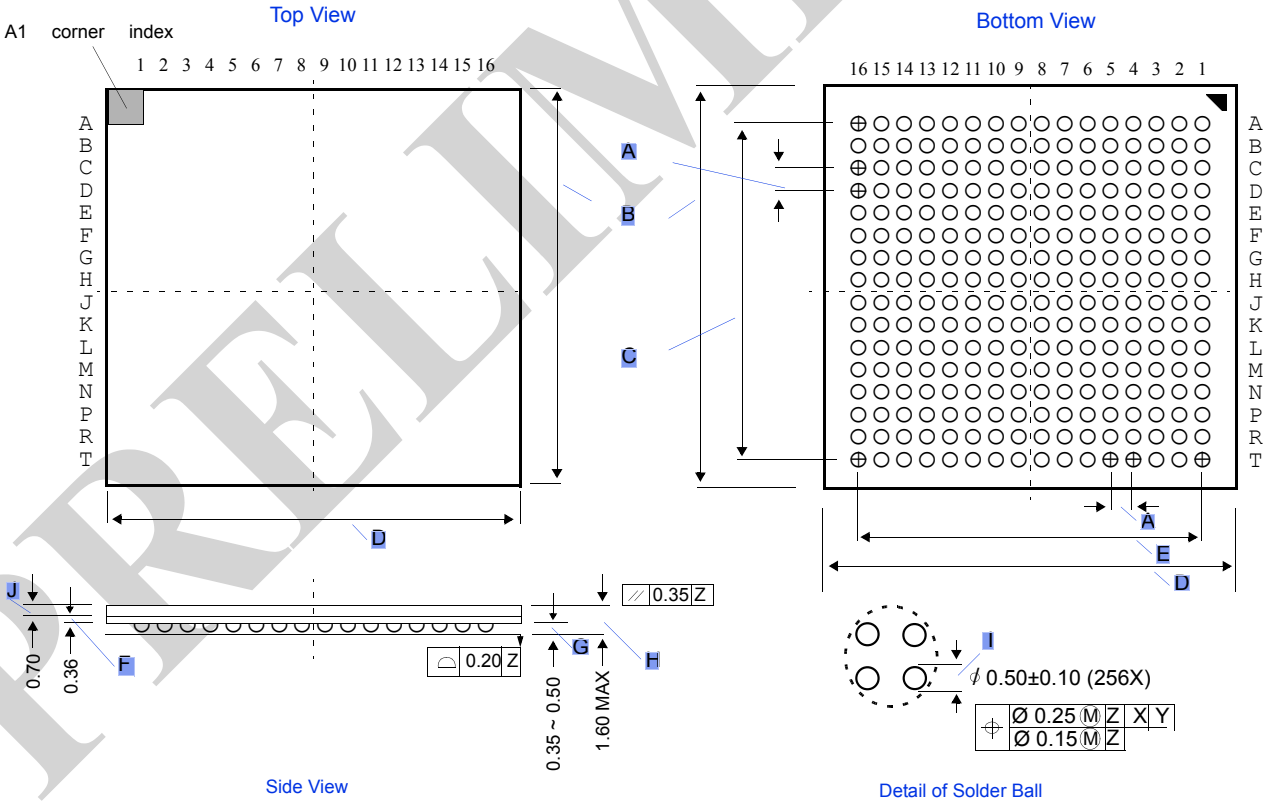
Instruction codes

Instruction	Code	Description	Selected Reg
EXTEST	0000	Forces contents of the BSR onto the device outputs.	BSR
SAMPLE/PRELOAD	0001	Samples the I/O ring contents. Preloads test data into the BSR.	BSR
IDCODE	0010	Loads the IDR with the vendor ID code and places the register between TDI and TDO.	IDR
CLAMP	0011	Forces contents of the BSR onto the device outputs.	BYR
HIGHZ	0100	Forces all device 2-state and 3-state outputs to High-Z.	BYR
RESERVED	0101 - 1110	Reserved states. Do not use.	BYR
BYPASS	1111	Places the BYR between TDI and TDO.	BYR

PRELIMINARY

Package Diagram: 256-ball Ball Grid Array (BGA)

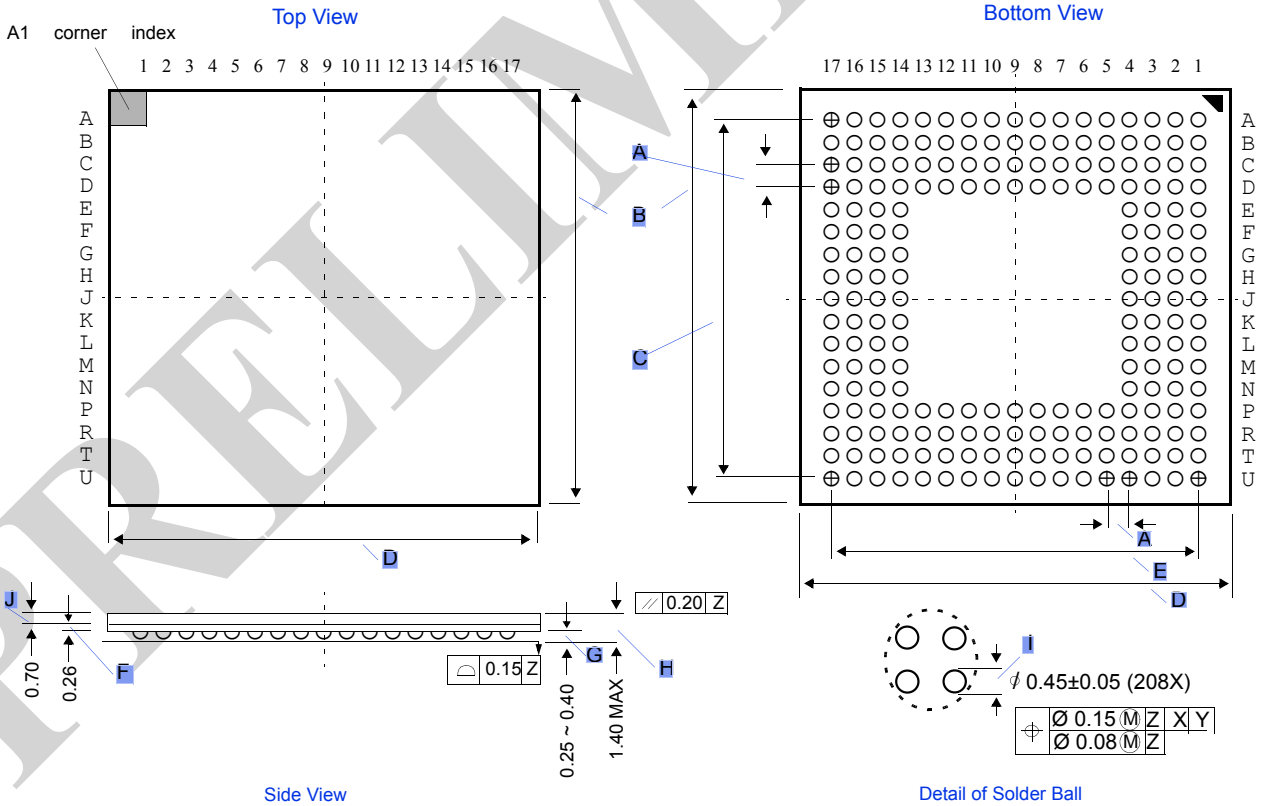
All measurements are in mm.			
	Min	Typ	Max
A		1.00	
B	16.95	17.00	17.05
C		15.00	
D	16.95	17.00	17.05
E		15.00	
F		0.36	
G	0.35		0.50
H			1.60
I	0.40	0.50	0.60
J		0.70	



PRELIMINARY

Package Diagram: 208-ball fine pitch Ball Grid Array (fpBGA)

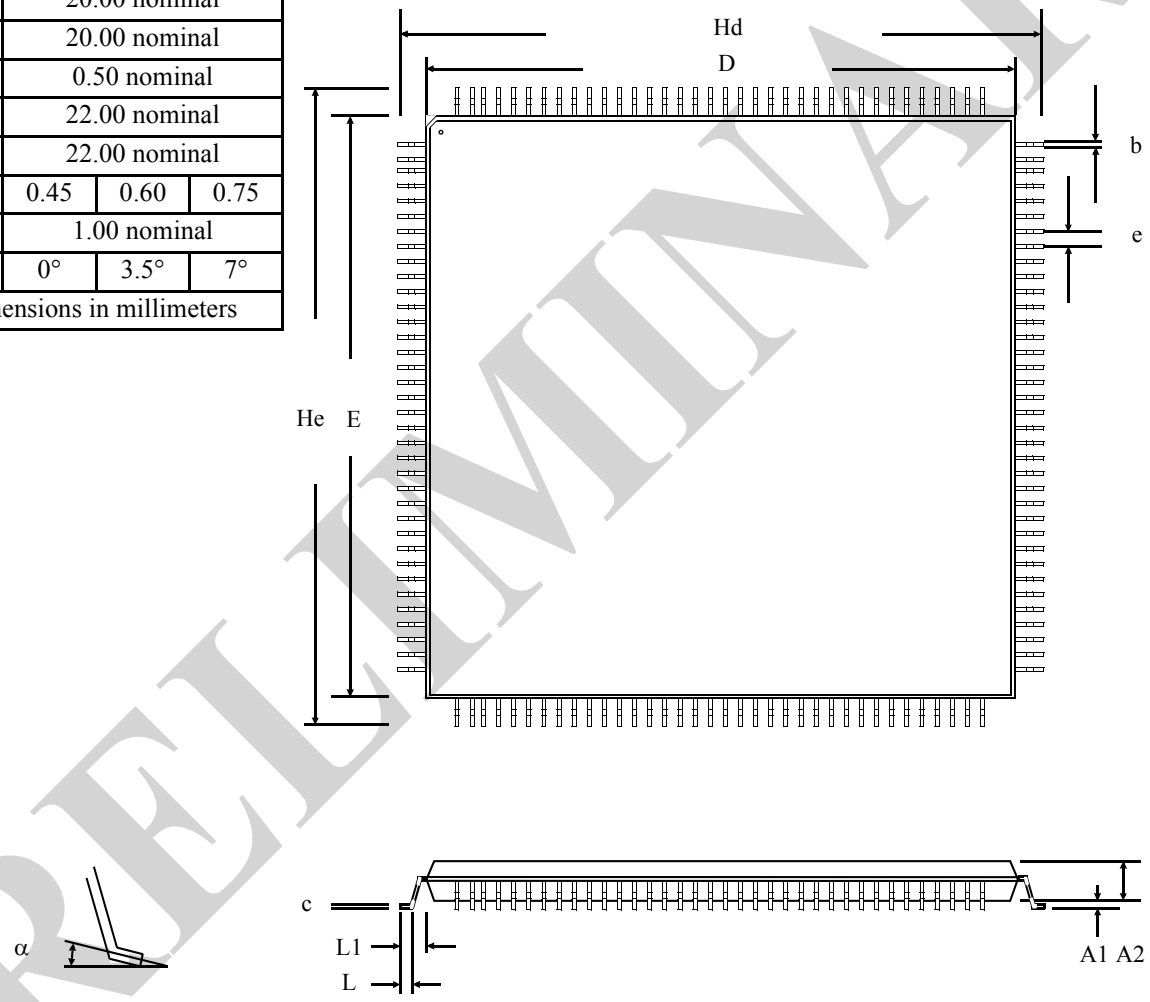
All measurements are in mm.			
	Min	Typ	Max
A		0.80	
B	14.95	15.00	15.05
C		12.80	
D	14.95	15.00	15.05
E		12.80	
F		0.26	
G	0.25		0.40
H			1.40
I	0.40	0.45	0.50
J		0.70	



PRELIMINARY

Package Diagram: 144-pin Thin Quad Flat Pack (TQFP)

	TQFP		
	Min	Typ	Max
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09		0.20
D	20.00 nominal		
E	20.00 nominal		
e	0.50 nominal		
Hd	22.00 nominal		
He	22.00 nominal		
L	0.45	0.60	0.75
L1	1.00 nominal		
α	0°	3.5°	7°
Dimensions in millimeters			



PRELIMINARY

Ordering Information

Package & Width	-250	-200	-166	-133
512K X 18				
BGA X 18	AS9C25512M2018L - 250BC	AS9C25512M2018L - 200BC	AS9C25512M2018L -166BC	AS9C25512M2018L - 133BC
	AS9C25512M2018L - 250BI	AS9C25512M2018L - 200BI	AS9C25512M2018L - 166BI	AS9C25512M2018L - 133BI
fpBGA X 18	AS9C25512M2018L - 250FC	AS9C25512M2018L - 200FC	AS9C25512M2018L - 166FC	AS9C25512M2018L - 133FC
	AS9C25512M2018L - 250FI	AS9C25512M2018L - 200FI	AS9C25512M2018L - 166FI	AS9C25512M2018L - 133FI
TQFP X 18	AS9C25512M2018L - 250TC	AS9C25512M2018L - 200TC	AS9C25512M2018L - 166TC	AS9C25512M2018L - 133TC
	AS9C25512M2018L - 250TI	AS9C25512M2018L - 200TI	AS9C25512M2018L - 166TI	AS9C25512M2018L - 133TI
256K X 18				
BGA X 18	AS9C25256M2018L - 250BC	AS9C25256M2018L - 200BC	AS9C25256M2018L -166BC	AS9C25256M2018L - 133BC
	AS9C25256M2018L - 250BI	AS9C25256M2018L - 200BI	AS9C25256M2018L - 166BI	AS9C25256M2018L - 133BI
fpBGA X 18	AS9C25256M2018L - 250FC	AS9C25256M2018L - 200FC	AS9C25256M2018L - 166FC	AS9C25256M2018L - 133FC
	AS9C25256M2018L - 250FI	AS9C25256M2018L - 200FI	AS9C25256M2018L - 166FI	AS9C25256M2018L - 133FI
TQFP X 18	AS9C25256M2018L - 250TC	AS9C25256M2018L - 200TC	AS9C25256M2018L - 166TC	AS9C25256M2018L - 133TC
	AS9C25256M2018L - 250TI	AS9C25256M2018L - 200TI	AS9C25256M2018L - 166TI	AS9C25256M2018L - 133TI

Part Numbering Guide

AS	9C	25	512/256	M20	18	L	-XXX	T or B or F	C/I
1	2	3	4	5	6	7	8	9	10

1. Alliance Semiconductor prefix
2. Speciality Memory
3. Operating Voltage: 25 - VDD = 2.5V
4. Device depth: 512 - 512K; 256 - 256K
5. M20 - Multiport - 2port, SSRAM, DCD
6. I/O width - 18
7. I/O interface: L - LVTTL
8. Clock speed (MHz)
9. Package Type: T - TQFP, B - BGA, F - fpBGA
10. Operating Temperature: C - Commercial (0^0C to 70^0C); I -Industrial (-40^0C to 85^0C)

PRELIMINARY

Alliance Semiconductor Corporation
2575, Augustine Drive,
Santa Clara, CA 95054
Tel: 408 - 855 - 4900
Fax: 408 - 855 - 4999

www.alsc.com

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