

Document Title

32M DDR SYNCHRONOUS SRAM

Revision History

<u>Rev No.</u>	<u>History</u>	<u>DraftData</u>	<u>Remark</u>
Rev. 0.0	Initial document.	Dec. 2002	Advance
Rev. 0.1	Remove /G operation thru the Spec. - Remove /G from PUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION, TRUTH TABLE and TIMING WAVEFORMs Add 300MHz Speed bin. - Add Part ID at ORDERING INFORMATION & I _{DD30} at DC CHARACTERISTICS Change I _{LI} and I _{LO} at DC CHARCATERISTICS - I _{LI} : MIN -1 -> -3, MAX 1 -> 3, I _{LO} : MIN -1 -> -5, MAX 1 -> 5 Change the comment of Programmable Impedance Output Driver.	Jan. 2003	Advance

PRE- PUBLICATION DRAFT
SUBJECT TO CHANGE WITHOUT NOTICE

	Change AC TEST CONDITIONS : TR/R _F : 0.4/0.4 -> 0.5/0.5 Change AC TIMING CHARACTERISTICS - t _{CHCL} : t _{KHKL} -0.1 -> t _{KHKL} -0.2 , t _{CLCH} : t _{KLKH} -0.1 -> t _{KLKH} -0.2 - t _{CXCV} : 2.10 -> 2.30		
Rev 0.2	Change VDDQ RANGE - In FEATURES : 1.5V VDDQ -> 1.5~1.8V VDDQ - In RECOMENDED DC OPERATING CONDITIONS : Max VDDQ : 1.6 -> 1.9 Change TRUTH TABLE : Remove Clock Stop Change DC CHARACTERISTICS - x36 IDD : I _{DD50} : 950 -> 1050, I _{DD45} : 850 -> 950, I _{DD40} : 800 -> 860, I _{DD30} : 750 -> 760 - x18 IDD: I _{DD50} : 850 -> 1000, I _{DD45} : 800 -> 900, I _{DD40} : 750 -> 810, I _{DD30} : 700 -> 710 - I _{SB1} : 150 -> 200 Change PIN CAPACITANCE : C _{IN} : 3.1 -> 3.2, C _{OUT} : 4 -> 4.2 Change AC TIMING CHARACTERISTICS - MIN t _{KHKL} , t _{KHKL} : -40 : 1.1 -> 1.2, -30 : 1.1 -> 1.4 - MIN t _{AVKH} , t _{BVKH} , t _{KHAX} , t _{KHBX} : -45 : 0.25 -> 0.27 - t _{CXCV} MIN/MAX : 0.8/2.3 -> 1.0/2.5 Change PACKAGE THERMAL CHARACTERISTICS	Feb. 2003	Advance

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

Revision History

<u>Rev No.</u>	<u>History</u>	<u>DraftData</u>	<u>Remark</u>
Rev 0.3	Change DC CHARACTERISTICS - x36 IDD : IDD50 : 1050 -> 1150 , IDD45 : 950 -> 1050, IDD40: 860 -> 960, IDD30: 760 -> 860 - x18 IDD: IDD50 : 1000 -> 1100, IDD45 : 900 -> 1000, IDD40: 810 -> 910, IDD30: 710 -> 810 - ISB1 : 200 -> 300	May. 2003	Advance
Rev 0.4	Change 300Mhz speed bin to 333Mhz	Jun. 2003	Advance

FEATURES

- 1Mx36 or 2Mx18 Organizations.
- 1.8~2.5V V_{DD}/1.5V ~1.8V_{DDQ}.
- HSTL Input and Outputs.
- Single Differential HSTL Clock.
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write.
- Free Running Active High and Active Low Echo Clock Output Pin.
- Registered Addresses, Burst Control and Data Inputs.
- Registered Outputs.
- Double and Single Data Rate Burst Read and Write.
- Burst Count Controllable With Max Burst Length of 4
- Interleaved and Linear Burst mode support
- Bypass Operation Support
- Programmable Impedance Output Drivers.
- JTAG Boundary Scan (subset of IEEE std. 1149.1)
- 153(9x17) Flip Chip Ball Grid Array Package(14mmx22mm)

GENERAL DESCRIPTION

The K7D323674A and K7D321874A are 37,748,736 bit Synchronous Pipeline Burst Mode SRAM devices. They are organized as 1,048,576 words by 36 bits for K7D323674A and 2,097,152 words by 18 bits for K7D321874A, fabricated using Samsung's advanced CMOS technology.

Single differential HSTL level clock, K and \bar{K} are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses and burst control inputs are registered internally. Data inputs are registered one cycle after write addresses are asserted(Late Write), at the rising edge of K clock for single data rate (SDR) write operations and at rising and falling edge of K clock for a double data rate (DDR) write operations.

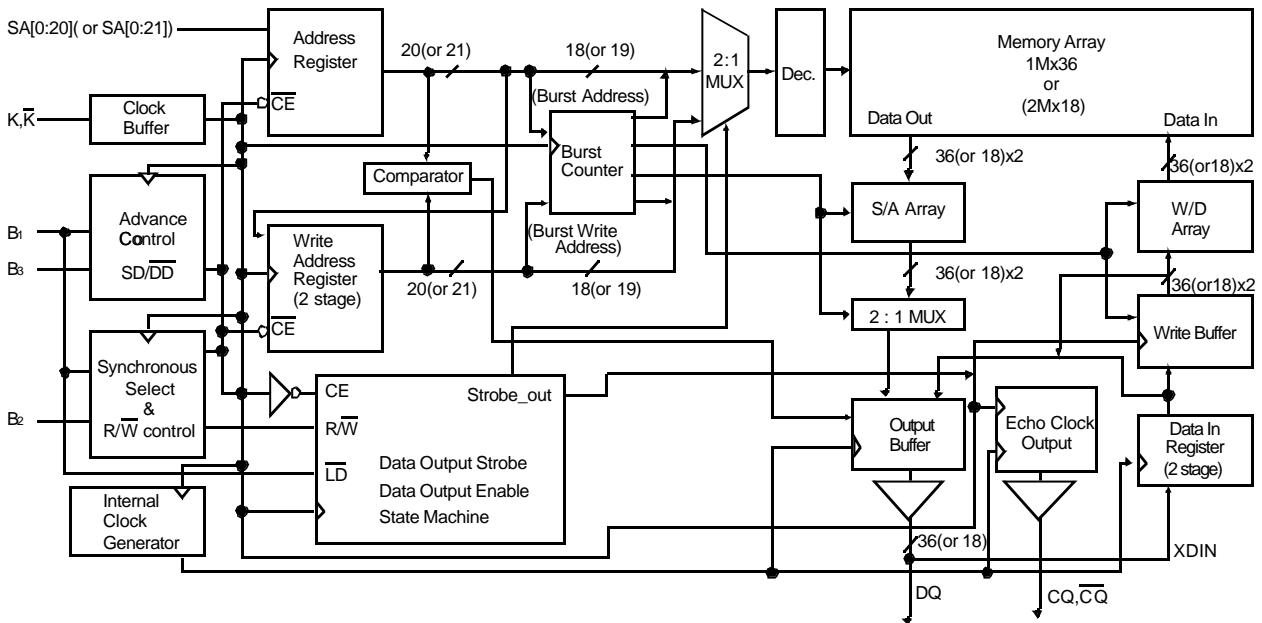
Data outputs are updated from output registers off the rising edges of K clock for SDR read operations and off the rising and falling edges of K clock for DDR read operations. Free running echo clocks are supported which are representative of data output access time for all SDR and DDR operations.

The chip is operated with 1.8~2.5V power supply and is compatible with HSTL input and output. The package is 9x17(153) Ball Grid Array balls on a 1.27mm pitch.

ORDERING INFORMATION

Part Number	Organization	Maximum Frequency
K7D323674A-HC50	1Mx36	500MHz
K7D323674A-HC45		450MHz
K7D323674A-HC40		400MHz
K7D323674A-HC33		333MHz
K7D321874A-HC50	2Mx18	500MHz
K7D321874A-HC45		450MHz
K7D321874A-HC40		400MHz
K7D321874A-HC33		333MHz

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, \bar{K}	Differential Clocks	TCK	JTAG Test Clock
SA	Synchronous Address Input	TMS	JTAG Test Mode Select
SA0, SA1	Synchronous Burst Address Input (SA0 = LSB)	TDI	JTAG Test Data Input
DQ	Synchronous Data I/O	TDO	JTAG Test Data Output
CQ, \bar{CQ}	Differential Output Echo Clocks	VREF	HSTL Input Reference Voltage
B1	Load External Address	VDD	Power Supply
B2	Burst R/W Enable	VDDQ	Output Power Supply
B3	Single/Double Data Selection	VSS	GND
\bar{LBO}	Linear Burst Order	NC	No Connection
ZQ	Output Driver Impedance Control Input		

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7D323674A(1Mx36)

	1	2	3	4	5	6	7	8	9
A	VSS	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	VSS
B	DQ20	DQ19	SA	VSS	B1	VSS	SA	DQ16	DQ15
C	VSS	VDDQ	SA	SA	SA	SA	SA	VDDQ	VSS
D	DQ30	DQ28	SA	V _{SS} (5)	VDD	V _{SS} (6)	SA	DQ7	DQ5
E	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
F	DQ21	CQ	DQ18	VDD	VDD	VDD	DQ17	CQ	DQ14
G	VSS	VDDQ	VSS	VSS	K	VSS	VSS	VDDQ	VSS
H	DQ31	DQ29	DQ27	VDD	\overline{K}	VDD	DQ8	DQ6	DQ4
J	VSS	VDDQ	VSS	VDD	VDD	VDD	VSS	VDDQ	VSS
K	DQ22	DQ24	DQ26	VSS	B2	VSS	DQ9	DQ11	DQ13
L	VSS	VDDQ	VSS	\overline{LBO} (7)	B3	MODE(9)	VSS	VDDQ	VSS
M	DQ32	\overline{CQ}	DQ35	VDD	VDD	VDD	DQ0	\overline{CQ}	DQ3
N	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
P	DQ23	DQ25	NC*	VSS	VDD(2)	VSS	SA	DQ10	DQ12
R	VSS	VDDQ	VDD(4)	SA	SA1	SA	VDD(3)	VDDQ	VSS
T	DQ33	DQ34	SA	VSS	SA0	VSS	SA	DQ1	DQ2
U	VSS	VDDQ	TMS	TDI	TCK	TDO	NC(8)	VDDQ	VSS

K7D321874A(2Mx18)

	1	2	3	4	5	6	7	8	9
A	VSS	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	VSS
B	NC	DQ10	SA	VSS	B1	VSS	SA	NC	DQ5
C	VSS	VDDQ	SA	SA	SA	SA	SA	VDDQ	VSS
D	DQ11	NC	SA	V _{SS} (5)	VDD	V _{SS} (6)	SA	DQ7	NC
E	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
F	NC	CQ	NC	VDD	VDD	VDD	DQ8	NC	DQ4
G	VSS	VDDQ	VSS	VSS	K	VSS	VSS	VDDQ	VSS
H	DQ12	NC	DQ9	VDD	\overline{K}	VDD	NC	DQ6	NC
J	VSS	VDDQ	VSS	VDD	VDD	VDD	VSS	VDDQ	VSS
K	NC	DQ15	NC	VSS	B2	VSS	DQ0	NC	DQ3
L	VSS	VDDQ	VSS	\overline{LBO} (7)	B3	MODE(9)	VSS	VDDQ	VSS
M	DQ13	NC	DQ17	VDD	VDD	VDD	NC	\overline{CQ}	NC
N	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
P	NC	DQ16	SA	VSS	VDD(2)	VSS	SA	NC	DQ2
R	VSS	VDDQ	VDD(4)	SA	SA1	SA	VDD(3)	VDDQ	VSS
T	DQ14	NC	SA	VSS	SA0	VSS	SA	DQ1	NC
U	VSS	VDDQ	TMS	TDI	TCK	TDO	NC(8)	VDDQ	VSS

(1) Variable address see "Variable address assignment table"
 (2) Variable address see "Variable address assignment table"
 (3) Variable address see "Variable address assignment table"
 (4) Variable address see "Variable address assignment table"
 (5) Variable address see "Variable address assignment table"
 (6) Variable address see "Variable address assignment table"
 (7) LBO for DDR1, M₂ for DDR3
 (8) NC for DDR1, ZT for DDR3
 (9) Internally NC since DDR2 is not supported

VARIABLE ADDRESS ASSIGNMENT TABLE

Density	Ball 5C (1)	Ball 5P (2)	Ball 7R (3)	Ball 3R (4)	Ball 4D (5)	Ball 6D (6)
32 Mb	SA	VDD	VDD	VDD	V _{ss}	V _{ss}
64 Mb	SA	SA	VDD	VDD	V _{ss}	V _{ss}
144 Mb	NC	SA	SA	SA	V _{ss}	V _{ss}
288 Mb	SA	SA	SA	SA	V _{ss}	V _{ss}
576 Mb	NC	SA	SA	SA	SA	SA
1152 Mb	SA	SA	SA	SA	SA	SA

NOTE : - SRAM density definition beyond 144Mb will include the parity bits.

Read Operation(Single and Double)

During SDR read operations, addresses and controls are registered at the first rising edge of K clock and then the internal array is read between first and second rising edges of K clock. Data outputs are updated from output registers off the second rising edge of K clock. During DDR read operations, addresses and controls are registered at the first rising edge of K clock, and then the internal array is read twice between first and second rising edges of K clock. Data outputs are updated from output registers sequentially by burst order off the second rising and falling edge of K clock.

Interleave and linear burst operation is controlled by $\overline{\text{LBO}}$ pin and the burst count is controllable with the maximum burst length of 4. To avoid data contention, at least one NOP operations are required between the last read and the first write operation.

Write Operation(Late Write)

During SDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered at the following rising edge of K clock. During DDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered twice at the following rising and falling edge of K clock. Write addresses and data inputs are stored in the data in registers until the next write operation, and only at the next write operation are data inputs fully written into SRAM array.

Echo clock operation

Free running type of Echo clocks are generated from K clock regardless of read, write and NOP operations. They will stop operation only when K clock is in the stop mode.

Echo clocks are designed to represent data output access time and this allows the echo clocks to be used as reference to capture data outputs outputs.

Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. For this case, data outputs are from the data in registers instead of SRAM array.

Programmable Impedance Output Driver

The data output and echo clock driver impedance are adjusted by an external resistor, R_Q , connected between ZQ pin and Vss, and are equal to $R_Q/5$. For example, 250 Ω resistor will give an output impedance of 50 Ω . Output driver impedance tolerance is 15% by test(10% by design) and is periodically readjusted to reflect the changes in supply voltage and temperature. Output driver impedance is updated every 64 clock cycles of Non-Read operation (Write or NOP) but since the echo clock drivers are in operation even during Non-Read operation, the impedance is update only the drivers are not in operation. Therefore impedance updates for "0s" or pull down drivers occur whenever the echo clock driver is driving "1s" or vice versa. Furthermore, to guarantee optimum output driver impedance after power up, the SRAM need 2048 deselect (or write) cycles.

TRUTH TABLE

K	B1	B2	B3	DQ	Operation
↑	H	L	X	Hi-Z	No Operation, Pipeline High-Z
↑	L	H	H	DOUT	Load Address, Single Read
↑	L	H	L	DOUT	Load Address, Double Read
↑	L	L	H	DIN	Load Address, Single Write
↑	L	L	L	DIN	Load Address, Double Write
↑	H	H	X	B	Increment Address, Continue

NOTE : - B(Both) is DIN in write cycle and DOUT in read cycle. Byte write function is not supported. X means "Don't Care".
- K & \bar{K} are complementary.

BURST SEQUENCE TABLE

4 Burst Operation for Interleaved Burst ($\overline{LBO} = V_{DDQ}$)

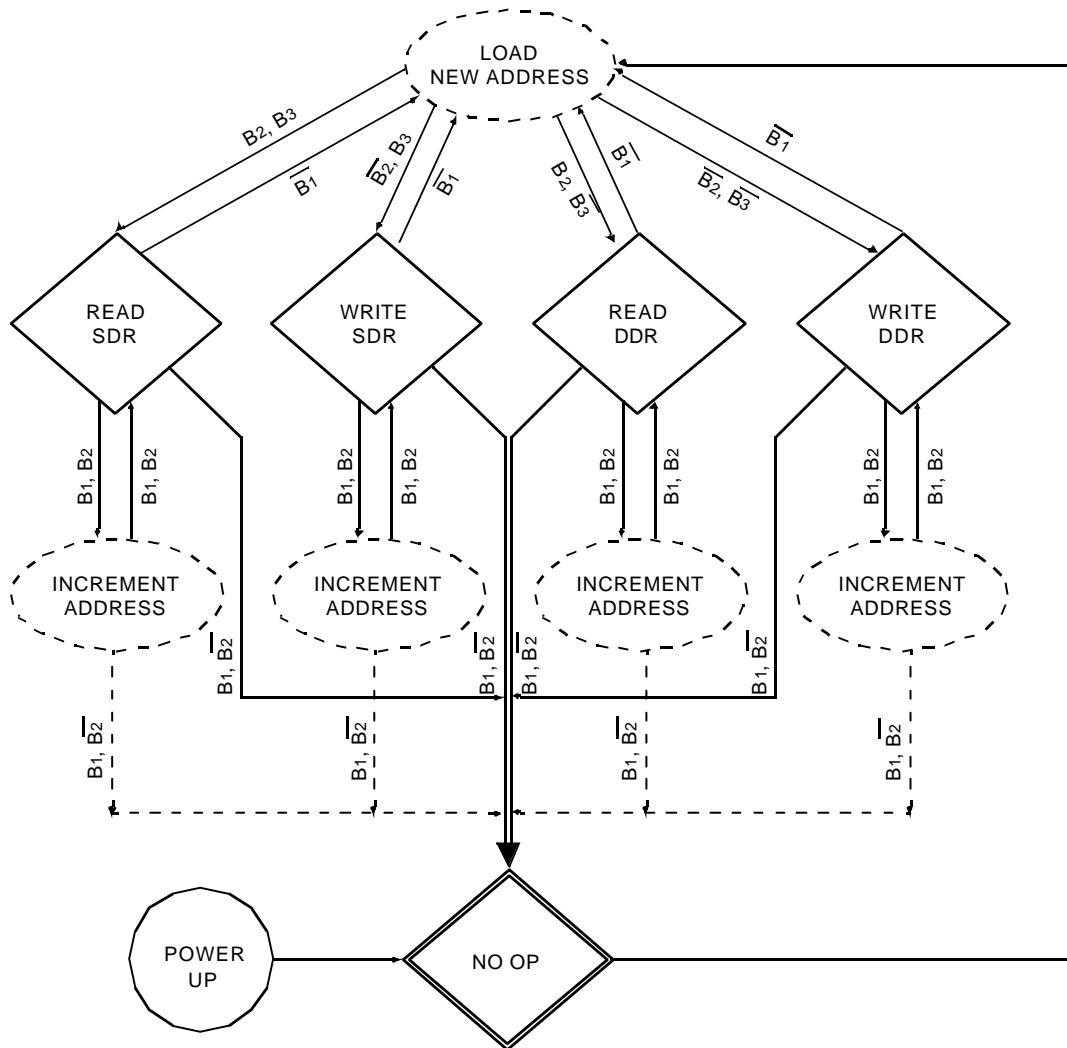
Interleaved Burst	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

NOTE : - For Interleave Burst $\overline{LBO} = V_{DDQ}$ is recommended. If $\overline{LBO} = V_{DD}$, it must not exceed 2.63V.

4 Burst Operation for Linear Burst ($\overline{LBO} = V_{SS}$)

Linear Burst Mode	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

BUS CYCLE STATE DIAGRAM



NOTE:

- State transitions ; $\overline{B_1}$ =(Load Address), B_1 =(Increment Address, Continue)
 B_2 =(Read), $\overline{B_2}$ =(Write)
 B_3 =(Single Data Rate), $\overline{B_3}$ =(Double Data Rate)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to VSS	VDD	-0.5 to 3.13	V
Output Supply Voltage Relative to VSS	VDDQ	-0.5 to 2.3	V
Voltage on any pin Relative to VSS	VIN	-0.5 to VDDQ+0.5 (2.3V MAX)	V
Output Short-Circuit Current(per I/O)	IOUT	25	mA
Storage Temperature	TSTR	-55 to 125	°C
Maximum Junction Temperature	TJ	110	°C
Maximum Power Dissipation	PD	3.0	W

NOTE : Power Dissipation Capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data. Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stressrating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	VDD	1.7	2.5	2.6	V	
Output Power Supply Voltage	VDDQ	1.4	1.5	1.9	V	
Input High Level Voltage	VIH	VREF+0.1	-	VDDQ+0.3	V	1, 2
Input Low Level Voltage	VIL	-0.3	-	VREF-0.1	V	1, 3
Input Reference Voltage	VREF	0.68	0.75	1.0	V	

NOTE :1. These are DC test criteria. DC design criteria is VREF±50mV. The AC VIH/VL levels are defined separately for measuring timing parameters.

- VH (Max)DC=VDDQ+0.3, VH (Max)AC=2.6V (2.1V for DQs) (pulse width ≤ 20% of cycle time).
- VL (Min)DC=-0.3V, VL (Min)AC=-1.0V (-0.5V for DQs) (pulse width ≤ 20% of cycle time).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current(x36) (Cycle time = tKHKH min)	IDD50		1150	mA	1,2
	IDD45	-	1050		
	IDD40		960		
	IDD33		900		
Average Power Supply Operating Current(x18) (Cycle time = tKHKH min)	IDD50		1100	mA	1,2
	IDD45	-	1000		
	IDD40		910		
	IDD33		850		
Stop Clock Standby Current (VIN=VDD-0.2V or 0.2V fixed, K=Low, \bar{K} =High)	ISB1	-	300	mA	1
Input Leakage Current (VIN=VSS or VDDQ)	ILI	-3	3	µA	
Output Leakage Current (VOUT=VSS or VDDQ)	ILO	-5	5	µA	
Output High Voltage(Programmable Impedance Mode)	VOH1	VDDQ/2	VDDQ	V	3
Output Low Voltage(Programmable Impedance Mode)	VOL1	VSS	VDDQ/2	V	4
Output High Voltage(I _{OH} =-0.1 mA)	VOH2	VDDQ-0.2	VDDQ	V	
Output Low Voltage(I _{OL} =0.1 mA)	VOL2	VSS	0.2	V	

NOTE :1. Minimum cycle. I_{OUT}=0mA.
2. 50% read cycles.
3. $|I_{OH}|=(V_{DDQ}/2)/(RQ/5) \pm 15\%$ @ $V_{OH}=V_{DDQ}/2$ for $175\Omega \leq RQ \leq 300\Omega$.
4. $|I_{OL}|=(V_{DDQ}/2)/(RQ/5) \pm 15\%$ @ $V_{OL}=V_{DDQ}/2$ for $175\Omega \leq RQ \leq 300\Omega$.

PIN CAPACITANCE

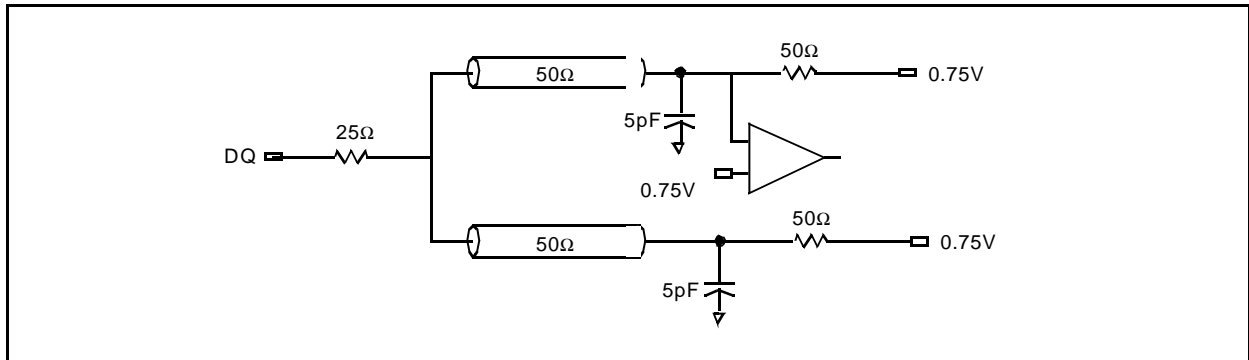
Parameter	Symbol	Test Condition	TYP	Max	Unit
Input Capacitance	C _{IN}	V _{IN} =0V	-	3.2	pF
Data Output Capacitance	C _{OUT}	V _{OUT} =0V	-	4.2	pF

NOTE : Periodically sampled and not 100% tested.(T_A=25°C, f=500MHz)

AC TEST CONDITIONS (T_A=0 to 70°C, V_{DD}=2.37 -2.63V, V_{DDQ}=1.5V)

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	1.25/0.25	V	-
Input Reference Level	V _{REF}	0.75	V	-
Input Rise/Fall Time	T _R /T _F	0.5/0.5	ns	-
Output Timing Reference Level		0.75	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load		See Below		-

AC TEST OUTPUT LOAD

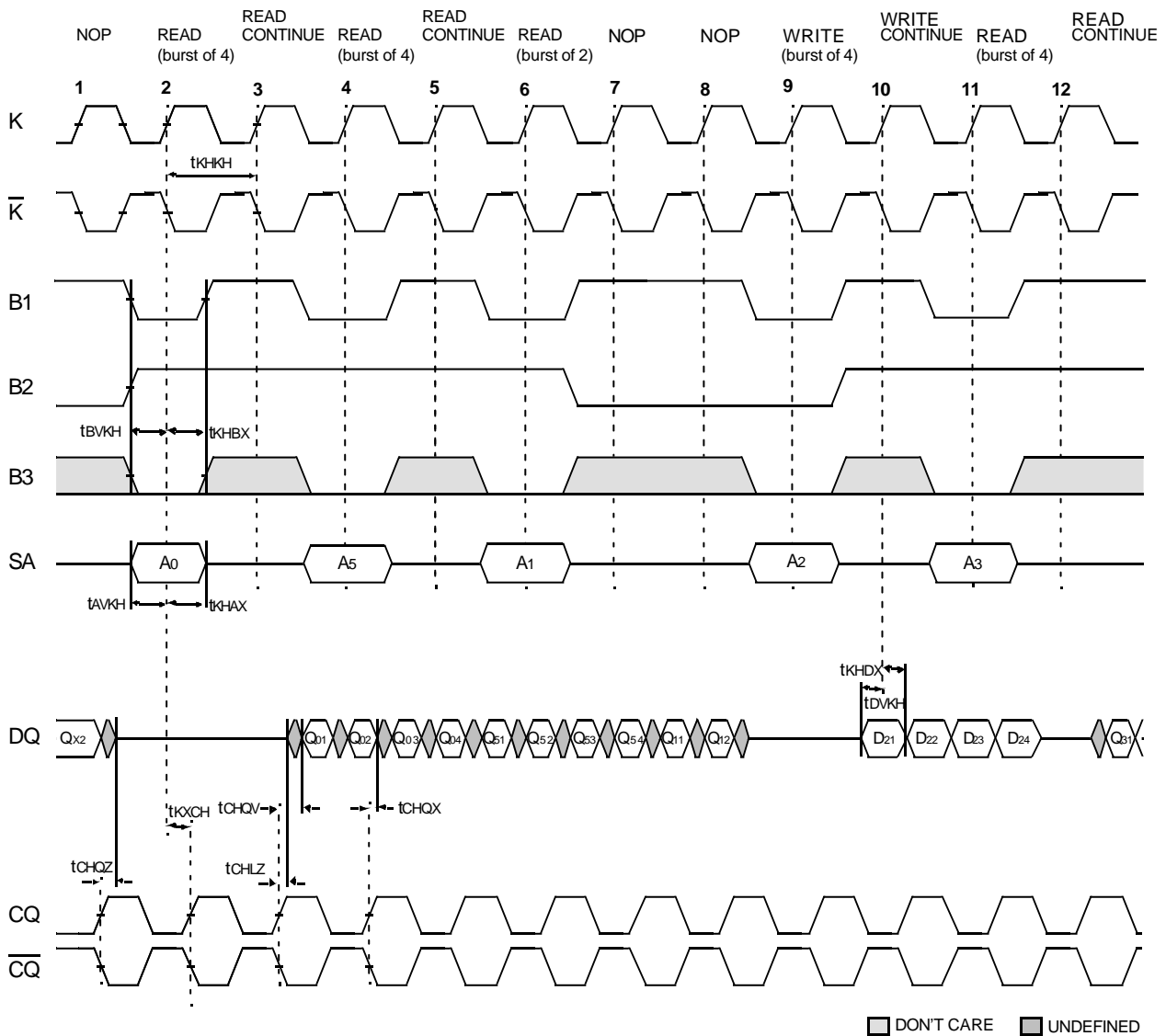


AC TIMING CHARACTERISTICS

PARAMETER	SYMBOL	-50		-45		-40		-33		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock											
Clock Cycle Time	tKHKH	2.00	4.00	2.20	4.40	2.50	5.00	3.00	6.00	ns	1
Clock High Pulse Width	tKHKL	0.90		1.00		1.20		1.40		ns	
Clock Low Pulse Width	tCLKH	0.90		1.00		1.20		1.40		ns	
Setup Times											
Address Setup Time	tAVKH	0.25		0.27		0.30		0.30		ns	
Control(B1,B2,B3) Setup Time	tBVKH	0.25		0.27		0.30		0.30		ns	
Data Setup Time	tDVXK	0.17		0.20		0.20		0.20		ns	2
Hold Times											
Address Hold Time	tKHAX	0.25		0.27		0.30		0.30		ns	
Control(B1,B2,B3) Hold Time	tKHBX	0.25		0.27		0.30		0.30		ns	
Data Hold Time	tKXDX	0.17		0.20		0.20		0.20		ns	2
Output Times											
Echo Clock High Pulse Width	tCHCL	tKHKL-0.2	tKHKL+0.2	tKHKL-0.2	tKHKL+0.2	tKHKL-0.2	tKHKL+0.2	tKHKL-0.2	tKHKL+0.2	ns	2
Echo Clock Low Pulse Width	tCLCH	tCLKH-0.2	tCLKH+0.2	tCLKH-0.2	tCLKH+0.2	tCLKH-0.2	tCLKH+0.2	tCLKH-0.2	tCLKH+0.2	ns	2
Clock to Echo Clock Valid	tKXCV	1.00	2.50	1.00	2.50	1.00	2.50	1.00	2.50	ns	
Data Output Tracking	tQTRK	-0.20	0.20	-0.20	0.20	-0.20	0.20	-0.20	0.20	ns	2,3

- Notes:**
1. The maximum cycle time must be limited to guarantee AC timing specification.
 2. This parameter is guaranteed by design, and may not be tested at values shown in the table.
 3. This parameter refers to CQ and \overline{CQ} rising and falling edges.
 4. This parameter is only for 32Mb density
 5. K and \overline{K} Clocks must be used differentially to meet AC timing specifications.

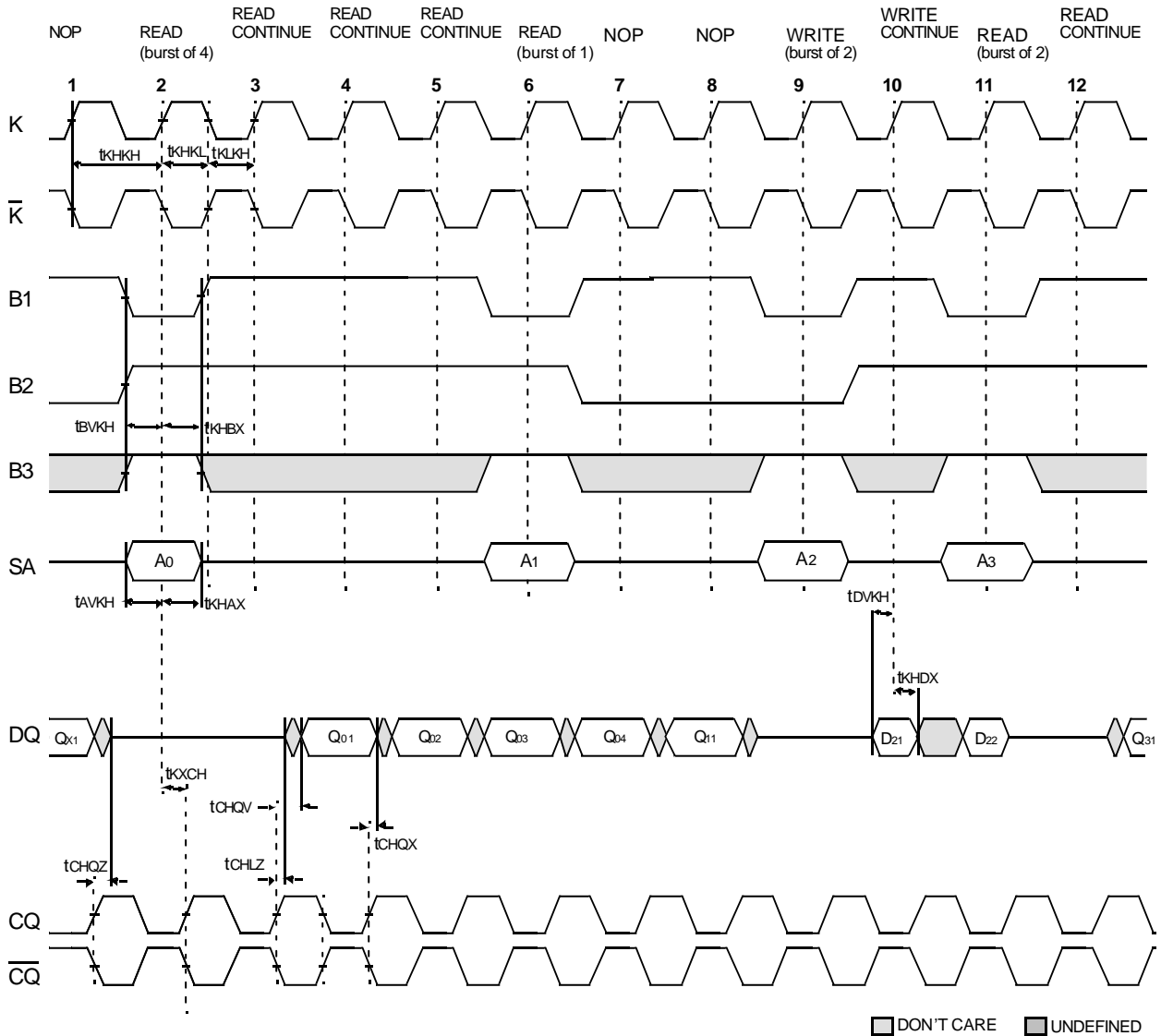
**TIMING WAVEFORMS FOR DOUBLE DATA RATE CYCLES
(Burst Length=4, 2)**



NOTE

1. Q₀₁ refers to output from address A. Q₀₂ refers to output from the next internal burst address following A, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. Doing more than one Read Continue or Write Continue will cause the address to wrap around.

**TIMING WAVEFORMS FOR SINGLE DATA RATE CYCLES
(Burst Length=4, 2, 1)**



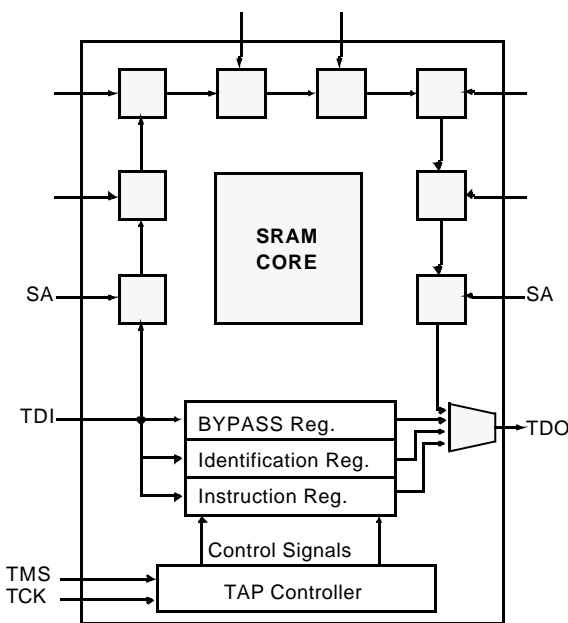
NOTE :

1. Q₀₁ refers to output from address A₀. Q₀₂ refers to output from the next internal burst address following A₀, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. This device supports cycle lengths of 1, 2, 4. Continue(B1=HIGH, B2=HIGH, B3=X) up to three times following a B1 operation. Any further Continue assertions constitute invalid operations.
4. This device will have an address wraparound if further Continues are applied.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

The SRAM provides a limited set of IEEE standard 1149.1 JTAG functions. This is to test the connectivity during manufacturing between SRAM, printed circuit board and other components. Internal data is not driven out of SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to VSS to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and therefore can be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



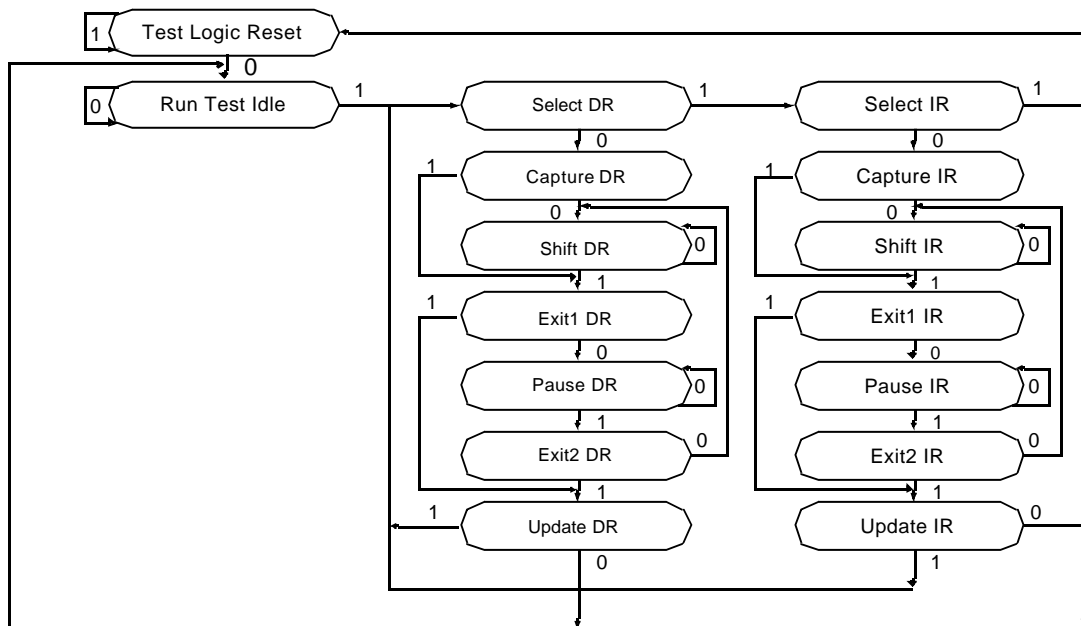
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	PRIVATE3	Bypass Register	3,5
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	PRIVATE2	Bypass Register	3,5
1	1	0	PRIVATE1	Bypass Register	3,5
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. Input terminators are switched off.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to VSS when BYPASS instruction is invoked.
The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not place DQs in Hi-Z.
5. PRIVATE1 and PRIVATE2 are reserved for the exclusive use of SAM-SUNG. This instruction should not be used.

TAP Controller State Diagram



BOUNDARY SCAN EXIT ORDER(x36)

1	5P	VDD(2)		38	5C	SA
2	5R	SA1		39	4A	SA
3	5T	SA0		40	4C	SA
4	6R	SA		41	4D	VSS(2)
5	7T	SA		42	3A	SA
6	7R	VDD(2)		43	3B	SA
7	7P	SA		44	3C	SA
8	8T	DQ1		45	3D	SA
9	9T	DQ2		46	2B	DQ19
10	8P	DQ10		47	1B	DQ20
11	7M	DQ0		48	2D	DQ28
12	9P	DQ12		49	3F	DQ18
13	8M	$\overline{CQ}(3)$		50	1D	DQ30
14	9M	DQ3		51	2F	CQ(3)
15	7K	DQ9		52	1F	DQ21
16	8K	DQ11		53	3H	DQ27
17	9K	DQ13		54	2H	DQ29
18	6L	MODE		55	1H	DQ31
19	5H	\overline{K}		56	5A	ZQ(1)
20	5G	K		57	5B	B1
21	9H	DQ4		58	5K	B2
22	8H	DQ6		59	5L	B3
23	7H	DQ8		60	4L	\overline{LBO}
24	9F	DQ14		61	1K	DQ22
25	8F	CQ(3)		62	2K	DQ24
26	9D	DQ5		63	3K	DQ26
27	7F	DQ17		64	1M	DQ32
28	8D	DQ7		65	2M	$\overline{CQ}(3)$
29	9B	DQ15		66	1P	DQ23
30	8B	DQ16		67	3M	DQ35
31	7D	SA		68	2P	DQ25
32	7C	SA		69	1T	DQ33
33	7B	SA		70	2T	DQ34
34	7A	SA		71	3R	VDD(2)
35	6D	VSS(2)		72	3T	SA
36	6C	SA		73	4R	SA
37	6A	SA		74	7U	NC

* Reserved for Mode Pin

BOUNDARY SCAN EXIT ORDER(x18)

1	5P	VDD(2)		28	5C	SA
2	5R	SA1		29	4A	SA
3	5T	SA0		30	4C	SA
4	6R	SA		31	4D	VSS(2)
5	7T	SA		32	3A	SA
6	7R	VDD(2)		33	3B	SA
7	7P	SA		34	3C	SA
8	8T	DQ1		35	3D	SA
				36	2B	DQ10
9	9P	DQ2				
10	8M	$\overline{CQ}(3)$		37	1D	DQ11
				38	2F	CQ(3)
11	7K	DQ0				
				39	3H	DQ9
12	9K	DQ3				
13	6L	MODE		40	1H	DQ12
14	5H	\overline{K}		41	5A	ZQ(1)
15	5G	K		42	5B	B1
				43	5K	B2
16	8H	DQ6		44	5L	B3
				45	4L	\overline{LBO}
17	9F	DQ4				
				46	2K	DQ15
18	7F	DQ8		47	1M	DQ13
19	8D	DQ7				
20	9B	DQ5				
				48	3M	DQ17
21	7D	SA		49	2P	DQ16
22	7C	SA		50	1T	DQ14
23	7B	SA		51	3P	SA
24	7A	SA		52	3R	VDD(2)
25	6D	VSS(2)		53	3T	SA
26	6C	SA		54	4R	SA
27	6A	SA		55	7U	NC

* Reserved for Mode Pin

NOTE :

1. If pin is connected as they should, TDO will be low. If pin is open, TDO will be high
2. This pin is place holder for higher density. TDO will be low for VSS and high for VDD
3. CQ and \overline{CQ} are outputs during boundary scan. CQ reflects the input to K and \overline{CQ} outputs the inverted value of K. It is prohibited to force CQ and \overline{CQ} . And TDO is ' X ' .(Don't Care)

SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1M x 36	3 bits	1 bits	32 bits	74 bits
2M x 18	3 bits	1 bits	32 bits	55 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit (0)
1M x 36	0000	01000 00100	XXXXXX	00001001110	1
2M x 18	0000	01001 00011	XXXXXX	00001001110	1

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	1.7	2.5	2.6	V	
Input High Level	VIH	0.65*VDD	-	VDD+0.3	V	
Input Low Level	VIL	-0.3	-	0.35*VDD	V	
Output High Voltage(I _{OH} =-2mA)	VOH	0.75*VDD	-	VDD	V	
Output Low Voltage(I _{OL} =2mA)	VOL	VSS	-	0.25*VDD	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

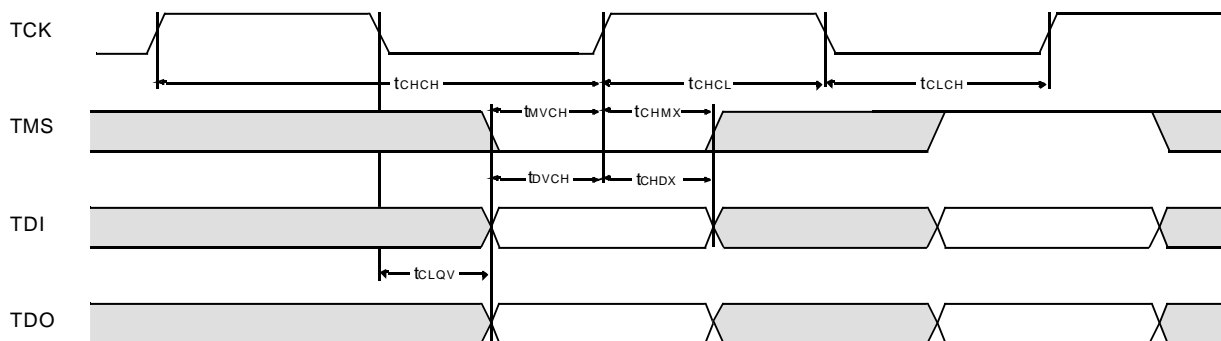
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	VIH/VIL	VDD/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		VDD/2	V	1

NOTE : 1. See SRAM AC test output load on page 5.

JTAG AC Characteristics

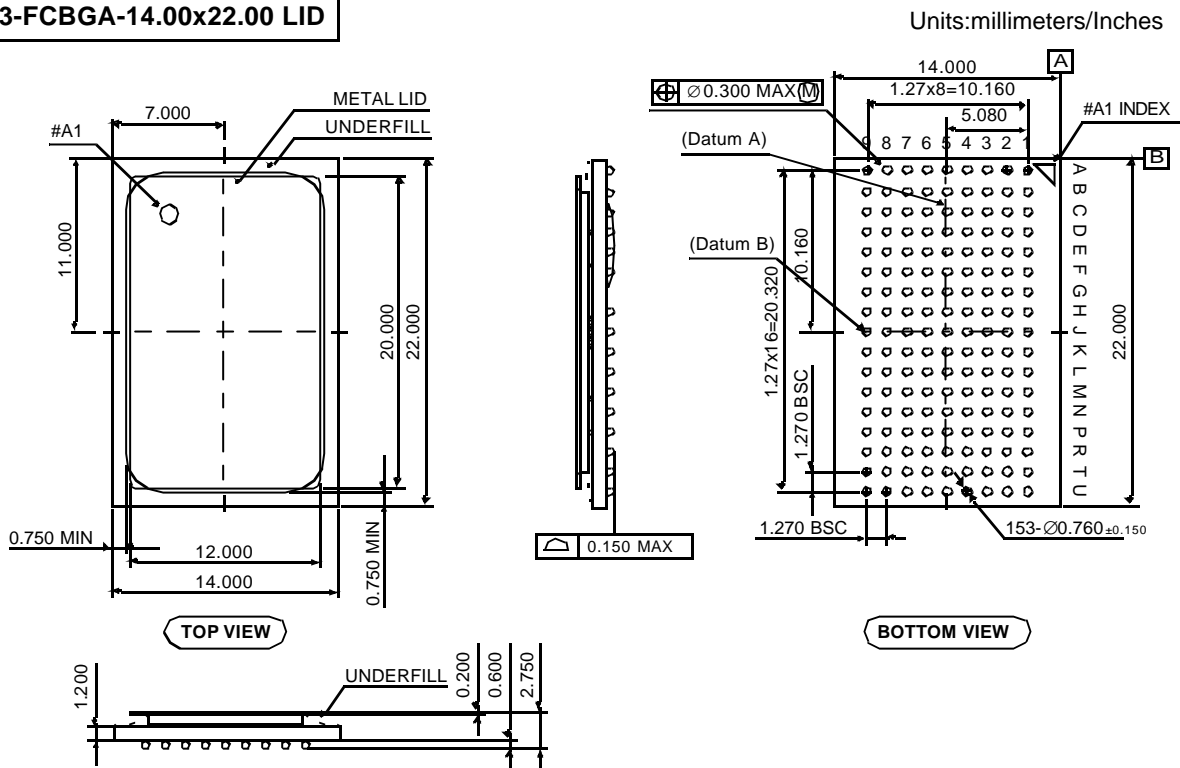
Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM



PACKAGE DIMENSIONS

153-FCBGA-14.00x22.00 LID



153 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Case	θ_{JC}	0.9	$^{\circ}\text{C}/\text{W}$	
Junction to Board	θ_{JB}	6.9	$^{\circ}\text{C}/\text{W}$	
Junction to Ambient(at air flow of 1m/sec)	θ_{JA}	16.1	$^{\circ}\text{C}/\text{W}$	
Junction to Ambient(at still air)	θ_{JA}	19.5	$^{\circ}\text{C}/\text{W}$	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times \theta_{JA}$ or $T_J = T_C + P_D \times \theta_{JC}$
 2. Strongly recommends using a heat sink because it greatly improves the ambient temperature requirement