19-4764; Rev 0; 7/98

MAXIM

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

General Description

The MAX7400/MAX7403/MAX7404/MAX7407 8th-order, lowpass, elliptic, switched-capacitor filters (SCFs) operate from a single +5V (MAX7400/MAX7403) or +3V (MAX7404/MAX7407) supply. These devices draw 2mA of supply current and allow corner frequencies from 1Hz to 10kHz, making them ideal for low-power anti-aliasing and DAC postfiltering applications. They feature a shutdown mode that reduces the supply current to just 0.2µA.

Two clocking options are available: self-clocking (through the use of an external capacitor) or external clocking for tighter cutoff-frequency control. In addition, an offset adjustment pin (OS) allows for the adjustment of the DC output level.

The MAX7400/MAX7404 provide 82dB of stopband rejection and a sharp rolloff with a transition ratio of 1.5. The MAX7403/MAX7407 provide a sharper rolloff with a transition ratio of 1.2, while still delivering 54dB of stopband rejection. The fixed response of these devices simplifies the design tasks to corner-frequency selection by setting a clock frequency. The MAX7400/MAX7403/MAX7404/MAX7407 are available in 8-pin SO and DIP packages.

Applications

ADC Anti-Aliasing

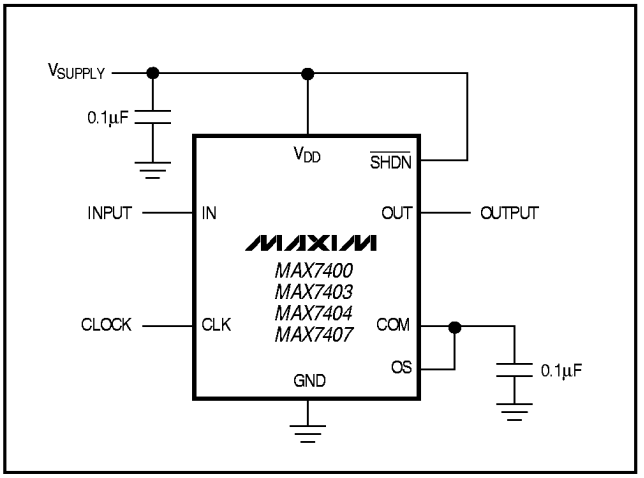
DAC Postfiltering

CT2 Base Stations

Speech Processing

Air-Bag Electronics

Typical Operating Circuit



Features

- **8th-Order Lowpass Filter**
- **Low Noise and Distortion: -82dB THD + Noise**
- **Clock-Tunable Corner Frequency (1Hz to 10kHz)**
- **Clock-to-Corner Ratio of 100:1**
- **Single-Supply Operation**
  +5V (MAX7400/MAX7403)
  +3V (MAX7404/MAX7407)
- **Low Power: 2mA (Operating Mode)**
  0.2µA (Shutdown Mode)
- **Available in 8-Pin DIP and SO Packages**
- **Low Output Offset VOS: ±5mV**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX7400CPA	0°C to +70°C	8 Plastic DIP
MAX7400CSA	0°C to +70°C	8 SO
MAX7400EPA	-40°C to +85°C	8 Plastic DIP
MAX7400ESA	-40°C to +85°C	8 SO

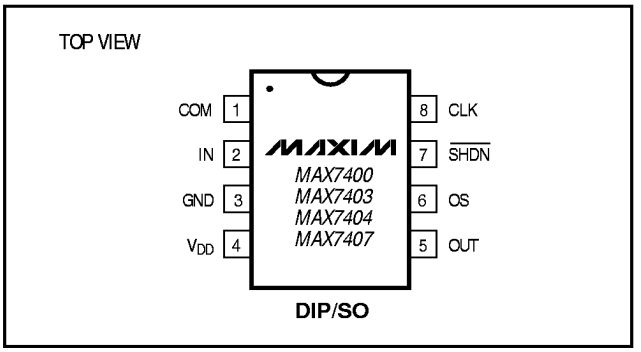
Ordering Information continued at end of data sheet.

Selector Guide

PART	FILTER RESPONSE	OPERATING VOLTAGE (V)
MAX7400	Elliptic (r = 1.5)	5
MAX7403*	Elliptic (r = 1.2)	5
MAX7404*	Elliptic (r = 1.5)	3
MAX7407*	Elliptic (r = 1.2)	3

**Future product—contact factory for availability.*

Pin Configuration



DIP/SO

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
IN, OUT, COM, OS .....-0.3V to (V_{DD} + 0.3V)
CLK, $\overline{SHDN}$ .....-0.3V to +6V
OUT Short-Circuit Duration 1sec
Continuous Power Dissipation (T_A = +70°C)
DIP (derate 9.1mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Ranges
MAX740_C_A .....0°C to +70°C
MAX740_E_A .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX7400/MAX7403

(V_{DD} = +5V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, $\overline{SHDN}$ = V_{DD}, OS = COM, 0.1µF from COM to GND, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Corner Frequency	f_C	(Note 1)			0.001 - 10		kHz
Clock-to-Corner Ratio	f_{CLK}/f_C				100:1		
Clock-to-Corner Tempco					10		ppm/°C
Output Voltage Range				0.25		V_{DD} - 0.25	V
Output Offset Voltage		IN = COM = V_{DD} / 2			±5	±25	mV
DC Insertion Gain with Output Offset Removed		COM = V_{DD} / 2 (Note 2)		-0.1	0.15	0.3	dB
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 200Hz, V_{IN} = 4Vp-p, measurement bandwidth = 22kHz	MAX7400		-82		dB
			MAX7403		-82		
OS Voltage Gain to OUT	A_{OS}				1		V/V
Input Voltage Range at OS	V_{OS}				V_{COM} ±0.1		V
COM Voltage Range	V_{COM}	Input, COM externally driven		(V_{DD} / 2) - 0.5	V_{DD} / 2	(V_{DD} / 2) + 0.5	V
		Output, COM internally biased		(V_{DD} / 2) - 0.2	V_{DD} / 2	(V_{DD} / 2) + 0.2	
Input Resistance at COM	R_{COM}			75	125		kΩ
Clock Feedthrough		T_A = +25°C			10		mVp-p
Resistive Output Load Drive	R_L			10	1		kΩ
Maximum Capacitive Load at OUT	C_L			50	500		pF
Input Leakage Current at COM		$\overline{SHDN}$ = GND, V_{COM} = 0 to V_{DD}			±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to V_{DD} - 1V (Note 3)			±0.1	±10	µA
CLOCK							
Internal Oscillator Frequency	f_{OSC}	C_{OSC} = 1000pF		29	38	48	kHz
Clock Output Current	I_{CLK}	V_{CLK} = 0 or 5V			±15	±30	µA
Clock Input	V_{IH}			V_{DD} - 0.5			V
	V_{IL}					0.5	

ELECTRICAL CHARACTERISTICS—MAX7400/MAX7403 (continued)

(V_{DD} = +5V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, $\overline{SHDN}$ = V_{DD}, OS = COM, 0.1µF from COM to GND, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	Operating mode, no load, IN = OS = COM		2	3.5	mA
Shutdown Current	I_{SHDN}	$\overline{SHDN}$ = GND, CLK driven from 0 to V_{DD}		0.2	1	µA
Power-Supply Rejection Ratio	PSRR	Measured at DC		60		dB
SHUTDOWN						
$\overline{SHDN}$ Input	V_{SDH}		V_{DD} - 0.5			V
	V_{SDL}				0.5	
$\overline{SHDN}$ Input Leakage Current		$V_{\overline{SHDN}}$ = 0 to V_{DD}		±0.1	±10	µA

ELECTRICAL CHARACTERISTICS—MAX7404/MAX7407

(V_{DD} = +3V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, OS = COM, 0.1µF from COM to GND, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Corner Frequency	f_C				0.001 - 10		kHz
Clock-to-Corner Ratio	f_{CLK}/f_C				100:1		
Clock-to-Corner Tempco					10		ppm/°C
Output Voltage Range				0.25		V_{DD} - 0.25	V
Output Offset Voltage		IN = COM = V_{DD} / 2			±5	±25	mV
DC Insertion Gain with Output Offset Removed		COM = V_{DD} / 2 (Note 2)		-0.2	0	0.2	dB
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 200Hz, V_{IN} = 2.5Vp-p, measurement bandwidth = 22kHz	MAX7404		-78		dB
			MAX7407		-78		
OS Voltage Gain to OUT	A_{OS}				1		V/V
OS Voltage Range	V_{OS}				V_{COM} ±0.1		V
COM Voltage Range	V_{COM}	COM internally biased or externally driven		(V_{DD} / 2) - 0.1	V_{DD} / 2	(V_{DD} / 2) + 0.1	V
Input Resistance at COM	R_{COM}			75	125		kΩ
Clock Feedthrough		T_A = +25°C			10		mVp-p
Resistive Output Load Drive	R_L			10	1		kΩ
Maximum Capacitive Load at OUT	C_L			50	500		pF
Input Leakage Current at COM		$\overline{SHDN}$ = GND, V_{COM} = 0 to V_{DD}			±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to V_{DD} - 1 (Note 3)			±0.1	±10	µA

ELECTRICAL CHARACTERISTICS—MAX7404/MAX7407 (continued)

(V_{DD} = +3V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, OS = COM, 0.1µF from COM to GND, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK						
Internal Oscillator Frequency	f_{OSC}	C_{OSC} = 1000pF	29	37	48	kHz
Clock Oscillator Current		V_{CLK} = 0 or 3V		±15	±30	µA
Clock Input	V_{IH}		V_{DD} - 0.5			V
	V_{IL}				0.5	
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		2.7		3.6	V
Supply Current	I_{DD}	Operating mode, no load, IN = OS = COM		2	3.5	mA
Shutdown Current	I_{SHDN}	$\overline{SHDN}$ = GND, CLK driven from 0 to V_{DD}		0.2	1	µA
Power-Supply Rejection Ratio	PSRR	Measured at DC		60		dB
SHUTDOWN						
$\overline{SHDN}$ Input	V_{SDH}		V_{DD} - 0.5			V
	V_{SDL}				0.5	
$\overline{SHDN}$ Input Leakage Current	PSRR	$V_{\overline{SHDN}}$ = 0 to V_{DD}		±0.1	±10	µA

FILTER CHARACTERISTICS—ELLIPTIC (1.5)—MAX7400/MAX7404

(V_{DD} = +5V for MAX7400, V_{DD} = +3V for MAX7404, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, $\overline{SHDN}$ = V_{DD}, V_{COM} = V_{OS} = V_{DD}/2, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Gain Relative to DC (Note 4)	f_{IN} = 0.371f_C	-0.20	-0.10	0.20	dB
	f_{IN} = 0.587f_C	-0.20	0.02	0.20	
	f_{IN} = 0.737f_C	-0.20	-0.08	0.20	
	f_{IN} = 0.868f_C	-0.20	0.06	0.20	
	f_{IN} = 0.940f_C	-0.20	-0.03	0.20	
	f_{IN} = 0.988f_C	-0.20	0.09	0.25	
	f_{IN} = 1.000f_C	-0.20	0.02	0.25	
	f_{IN} = 1.500f_C		-82	-75	
	f_{IN} = 1.601f_C		-84	-78	
	f_{IN} = 2.020f_C		-83	-78	
	f_{IN} = 4.020f_C		-85	-78	

FILTER CHARACTERISTICS—ELLIPTIC (1.2)—MAX7403/MAX7407

(V_{DD} = +5V for MAX7403, V_{DD} = +3V for MAX7407, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, $\overline{SHDN}$ = V_{DD}, V_{COM} = V_{OS} = V_{DD}/2, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Gain Relative to DC (Note 4)	f_{IN} = 0.425f_C	-0.20	-0.11	0.20	dB
	f_{IN} = 0.644f_C	-0.20	0.02	0.20	
	f_{IN} = 0.802f_C	-0.20	-0.10	0.20	
	f_{IN} = 0.895f_C	-0.20	0.03	0.20	
	f_{IN} = 0.946f_C	-0.20	-0.07	0.20	
	f_{IN} = 0.994f_C	-0.20	0.02	0.25	
	f_{IN} = 1.000f_C	-0.20	-0.10	0.25	
	f_{IN} = 1.200f_C		-54	-51	
	f_{IN} = 1.270f_C		-62	-57	
	f_{IN} = 1.530f_C		-60	-57	
	f_{IN} = 2.840f_C		-60	-57	

Note 1: The maximum f_C is defined as the clock frequency f_{CLK} = 100 x f_C, at which the peak S / (THD+N) drops to 68dB with a sinusoidal input at 0.2f_C.

Note 2: DC insertion gain is defined as ΔV_{OUT} / ΔV_{IN}.

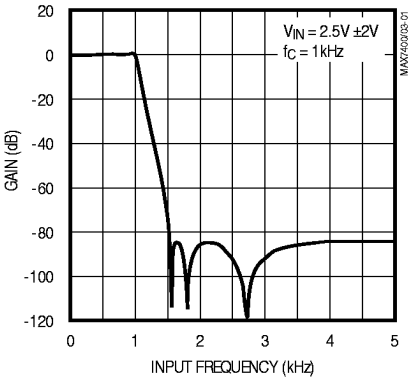
Note 3: OS voltages above V_{DD} - 1V will saturate the input and result in a 75µA typical input leakage current.

Note 4: The input frequencies, f_{IN}, are selected at the peaks and troughs of the frequency responses.

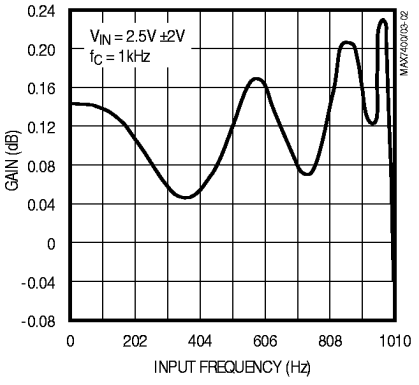
Typical Operating Characteristics

(MAX7400, V_{DD} = +5V, COM = OS, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 100kHz, T_A = +25°C, unless otherwise noted.)

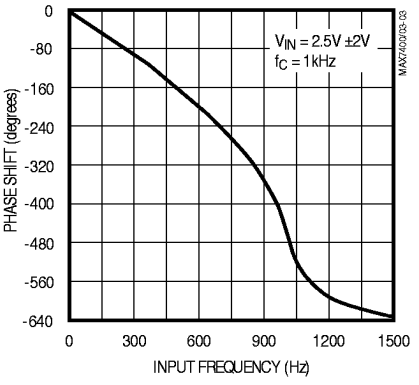
FREQUENCY RESPONSE



PASSBAND FREQUENCY RESPONSE



PHASE RESPONSE

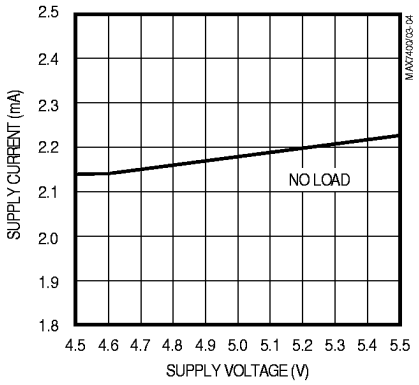


8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

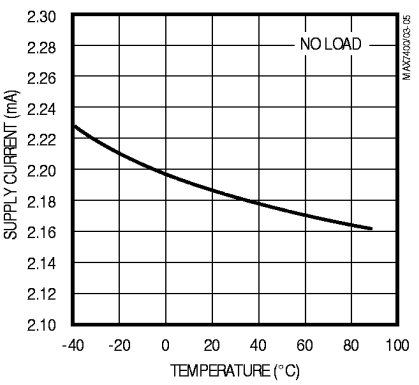
Typical Operating Characteristics (continued)

(MAX7400, V_{DD} = +5V, COM = OS, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 100kHz, T_A = +25°C, unless otherwise noted.)

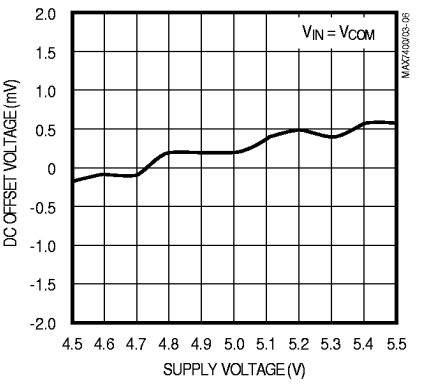
SUPPLY CURRENT vs. SUPPLY VOLTAGE



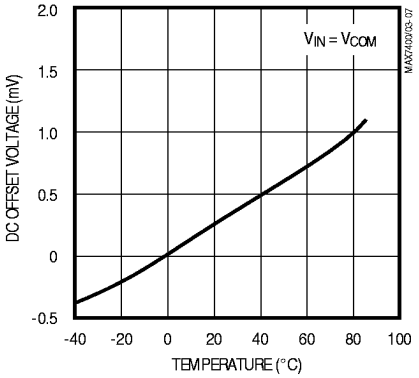
SUPPLY CURRENT vs. TEMPERATURE



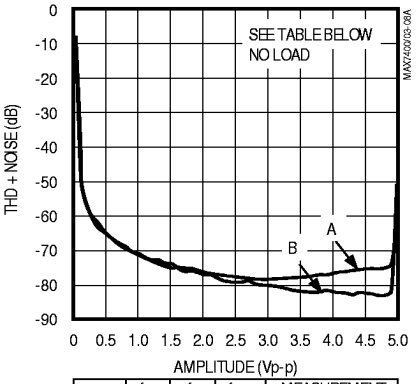
DC OFFSET VOLTAGE vs. SUPPLY VOLTAGE



DC OFFSET VOLTAGE vs. TEMPERATURE

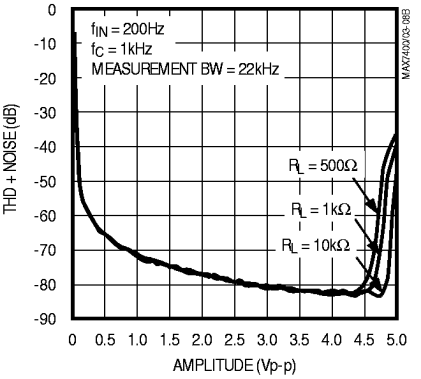


THD + NOISE vs. INPUT SIGNAL AMPLITUDE

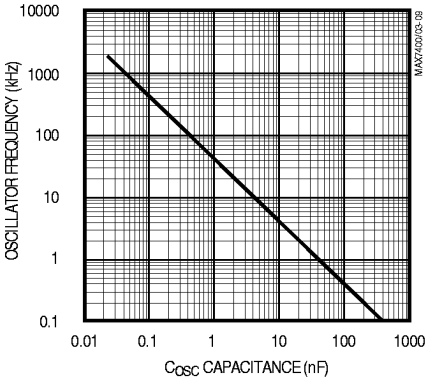


TRACE	f_{IN} (Hz)	f_C (kHz)	f_{CLK} (kHz)	MEASUREMENT BANDWIDTH (kHz)
A	1000	5	500	80
B	200	1	100	22

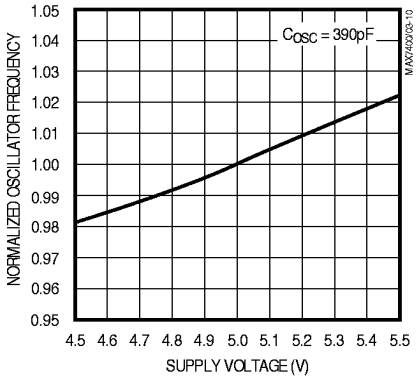
THD + NOISE vs. INPUT SIGNAL AMPLITUDE vs. RESISTIVE LOAD



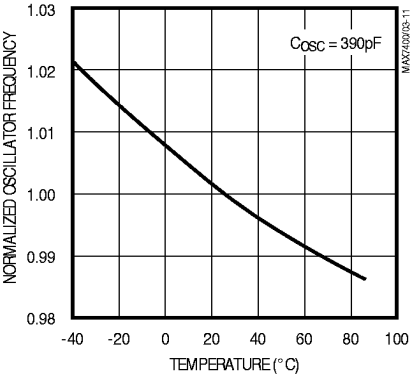
INTERNAL OSCILLATOR FREQUENCY vs. C_{OSC} CAPACITANCE



NORMALIZED INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



NORMALIZED INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	COM	Common Input Pin. Biased internally at mid-supply. Bypass to GND with a 0.1µF capacitor. To override internal biasing, drive with an external supply.
2	IN	Filter Input
3	GND	Ground
4	V_{DD}	Positive Supply Input. +5V for MAX7400/MAX7403, +3V for MAX7404/MAX7407.
5	OUT	Filter Output
6	OS	Offset Adjust Input. To adjust the output offset, bias OS externally. Connect OS to COM if no offset adjustment is needed.
7	$\overline{SHDN}$	Shutdown Input. Drive low to enable shutdown mode; drive high or connect to V_{DD} for normal operation.
8	CLK	Clock Input. To override the internal oscillator, connect to an external clock; otherwise, connect an external capacitor (C_{OSC}) from CLK to GND to set the internal oscillator frequency.

Detailed Description

The MAX7400/MAX7403/MAX7404/MAX7407 family of 8th-order, lowpass filters provides sharp rolloff with good stopband rejection. All parts operate with a 100:1 clock-to-corner frequency ratio and a 10kHz maximum corner frequency. They accept a single +5V (MAX7400/MAX7403) or +3V (MAX7404/MAX7407) supply. Figure 1 shows the functional diagram.

Most switched-capacitor filters (SFCs) are designed with biquadratic sections. Each section implements two filtering poles, and the sections can be cascaded to produce higher-order filters. The advantage of this approach is ease of design. However, this type of design is highly sensitive to component variations if any section's Q is high. The MAX7400 family uses an alternative approach, which is to emulate a passive network using switched-capacitor integrators with summing and scaling. The passive network can be synthesized using CAD programs or can be found in many filter books. Figure 2 shows a basic 8th-order ladder elliptic filter structure.

A switched-capacitor filter that emulates a passive ladder filter retains many of the same advantages. The component sensitivity of a passive ladder filter is low when compared to a cascaded biquadratic design, because each component affects the entire filter shape rather than a single pole-zero pair. In other words, a mismatched component in a biquadratic design will have a concentrated error on its respective poles, while the same mismatch in a ladder filter design will spread its error over all poles.

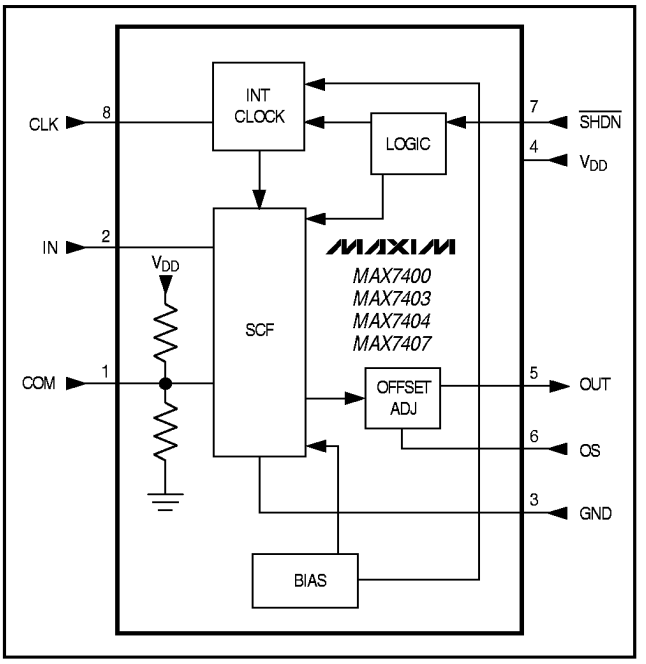


Figure 1. Functional Diagram

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

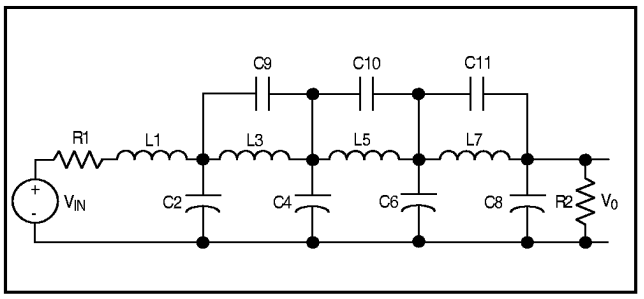


Figure 2. 8th-Order Ladder Filter Network

Elliptic Characteristics

Lowpass, elliptic filters such as the MAX7400/MAX7403/MAX7404/MAX7407 provide the steepest possible rolloff with frequency of the four most common filter types (Butterworth, Bessel, Chebyshev, and Elliptic). Figure 3 shows the 8th-order elliptic filter response. The high Q value of the poles near the passband edge combined with the stopband zeros allows for the sharp attenuation characteristic of elliptic filters, making these devices ideal for anti-aliasing and DAC postfiltering in single-supply systems (see the *Anti-Aliasing and DAC Postfiltering* section).

In the frequency domain, the first transmission zero causes the filter's amplitude to drop to a minimum level. Beyond this zero, the response rises as the frequency increases until the next transmission zero. The stopband begins at the stopband frequency, f_S. At frequencies above f_S, the filter's gain does not exceed the gain at f_S. The corner frequency, f_C, is defined as the point where the filter output attenuation falls just below the passband ripple. The transition ratio is defined as the ratio of the stopband frequency to the corner frequency:

$$r = f_S / f_C$$

The MAX7400/MAX7404 have a transition ratio of 1.5 and a typical stopband rejection of 82dB. The MAX7403/MAX7404 have a transition ratio of 1.2 (providing the steepest rolloff), a typical stopband rejection of 54dB.

Clock Signal

External Clock

The MAX7400/MAX7403/MAX7404/MAX7407 SCFs were designed for use with external clocks that have a 40% to 60% duty cycle. When using an external clock, drive the CLK pin with a CMOS gate powered from 0 to V_{DD}. Varying the rate of the external clock will adjust the corner frequency of the filter:

$$f_C = f_{CLK} / 100$$

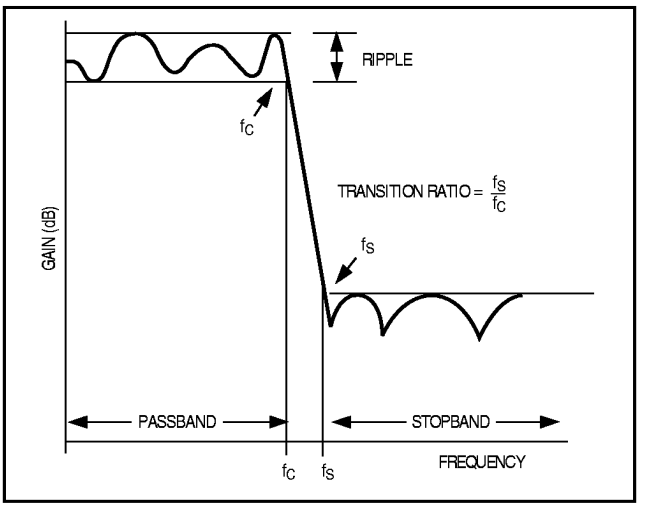


Figure 3. Elliptic Filter Response

Internal Clock

When using the internal oscillator, the capacitance (C_{OSC}) on the CLK pin determines the oscillator frequency:

$$f_{OSC}(kHz) = \frac{38 \times 10^3}{C_{OSC}};\ C_{OSC} \text{ in pF}$$

Since the capacitor value is in picofarads, the stray capacitance at CLK should be minimized so that it will not affect the internal oscillator frequency. Varying the rate of the internal oscillator adjusts the filter's corner frequency by a 100:1 clock-to-corner frequency ratio. For example, an internal oscillator frequency of 100kHz would produce a nominal corner frequency of 1kHz.

Input Impedance vs. Clock Frequencies

The MAX7400/MAX7403/MAX7404/MAX7407's input impedance is effectively that of a switched-capacitor resistor and is inversely proportional to frequency. The input impedance determined by the following equation represents the average input impedance (Table 1), since the input current is not continuous. As a rule, use a driver with an output source impedance less than 10% of the filter's input impedance. Estimate the input impedance of the filter using the following formula:

$$Z_{IN}(\Omega) = \frac{1}{(f_{CLK} \times C_{IN})}$$

where f_{CLK} = clock frequency and C_{IN} = 0.85pF. (Table 1)

Table 1. Input Impedance for Various Clock Frequencies

Z (MΩ) at 5kHz	Z (MΩ) at 50kHz	Z (MΩ) at 500kHz
235	23.5	2.35

Low-Power Shutdown Mode

These devices feature a shutdown mode that is activated by driving $\overline{SHDN}$ low. Placing the filter in shutdown mode reduces the supply current to 0.2µA (typ) and puts the output of the filter into a high-impedance state. For normal operation, drive $\overline{SHDN}$ high or connect it to V_{DD}.

Applications Information

Offset (OS) and Common-Mode (COM) Adjustment

The COM pin sets the common-mode input voltage and is internally biased at mid-supply by a resistor-divider. Bypass COM with a 0.1µF capacitor and connect the OS pin to COM. For applications where offset-adjustment or DC level shifting is required, apply an external bias voltage through a resistor-divider network to OS, as shown in Figure 4. (Note: OS should not be left unconnected). The output voltage can be represented by this equation:

$$V_{OUT} = (V_{IN} - V_{COM})_{LPF} + V_{OS}$$

$$V_{COM} = V_{DD} / 2 \text{ (typical)}$$

where (V_{IN} - V_{COM}) is lowpass filtered by the SCF, and V_{OS} is added at the output stage. See the *Electrical Characteristics* for COM and OS input voltage ranges.

Changing the voltage on COM or OS significantly from mid-supply will reduce the dynamic range.

Power Supplies

The MAX7400/MAX7403 operate from a single +5V supply. The MAX7404/MAX7407 operate from a single +3V supply. Bypass V_{DD} to GND with a 0.1µF capacitor. If dual supplies are required, connect COM to the system ground and GND to the negative supply. Figure 5 shows an example of dual-supply operation. Single-supply and dual-supply performance are equivalent. For single-supply or dual-supply operation, drive CLK and $\overline{SHDN}$ from GND (V- in dual-supply operation) to V_{DD}. For a ±2.5V supply, use the MAX7400 or MAX7403; for a ±1.5V supply, use MAX7404 or MAX7407. For ±5V dual-supply applications, use the MAX291–MAX297.

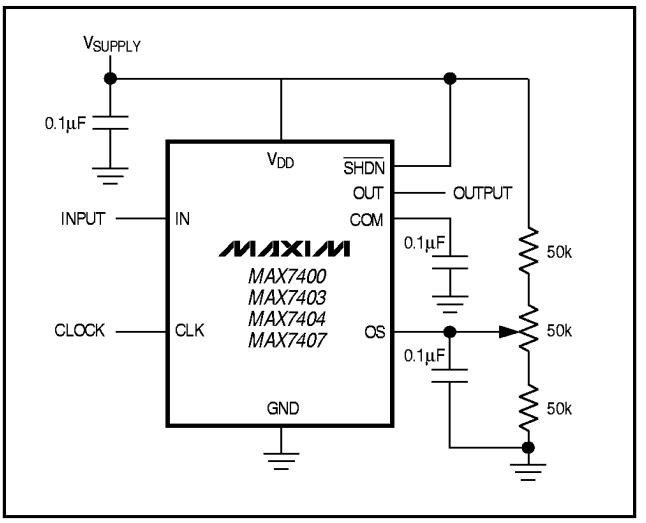


Figure 4. Offset Adjustment Circuit

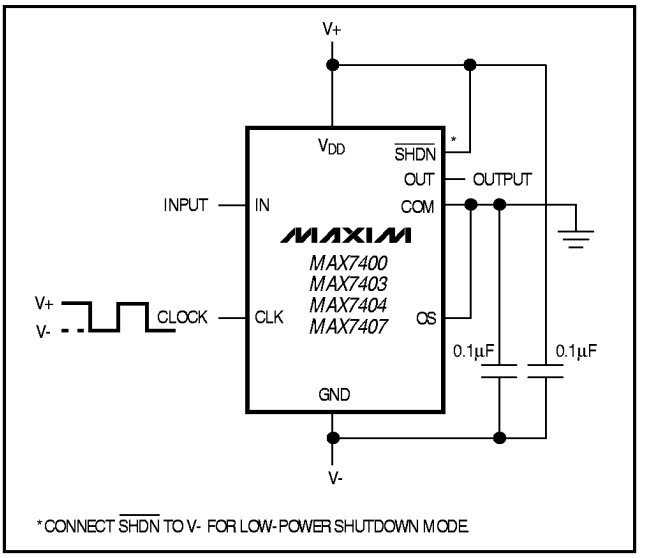


Figure 5. Dual-Supply Operation

Input Signal Amplitude Range

The ideal input signal range is determined by observing at what voltage level the total harmonic distortion plus noise is minimized for a given corner frequency. The *Typical Operating Characteristics* show Total Harmonic Distortion plus Noise Response as the input signal's peak-to-peak amplitude is varied. These measurements are made with OS and COM biased at mid-supply.

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

Anti-Aliasing and Postfiltering

When using the MAX7400/MAX7403/MAX7404/MAX7407 for anti-aliasing or DAC postfiltering, synchronize the DAC and the filter clocks. If the clocks are not synchronized, beat frequencies will alias into the passband.

The high clock-to-corner frequency ratio (100:1) also eases the requirements of pre- and post-SCF filtering. At the input, a lowpass filter prevents the aliasing of frequencies around the clock frequency into the passband. At the output, a lowpass filter attenuates the clock feedthrough.

A high clock-to-corner frequency ratio allows a simple RC lowpass filter, with the cutoff frequency set above the SCF corner frequency to provide input anti-aliasing and reasonable output clock attenuation.

Harmonic Distortion

Harmonic distortion arises from nonlinearities within the filter. Such nonlinearities generate harmonics when a pure sine wave is applied to the filter input. Table 2 lists typical harmonic distortion values for the MAX7400 with a 10kΩ load and an input signal of 4Vp-p at T_A = +25°C.

Table 2. Typical Harmonic Distortion

FILTER	f_{CLK} (kHz)	f_C (kHz)	f_{IN} (Hz)	HARMONIC DISTORTION (dB)			
				2nd	3rd	4th	5th
MAX7400	100	1	200	-89	-82	-89	-86
	500	5	1000	-89	-77	-93	-88

Chip Information

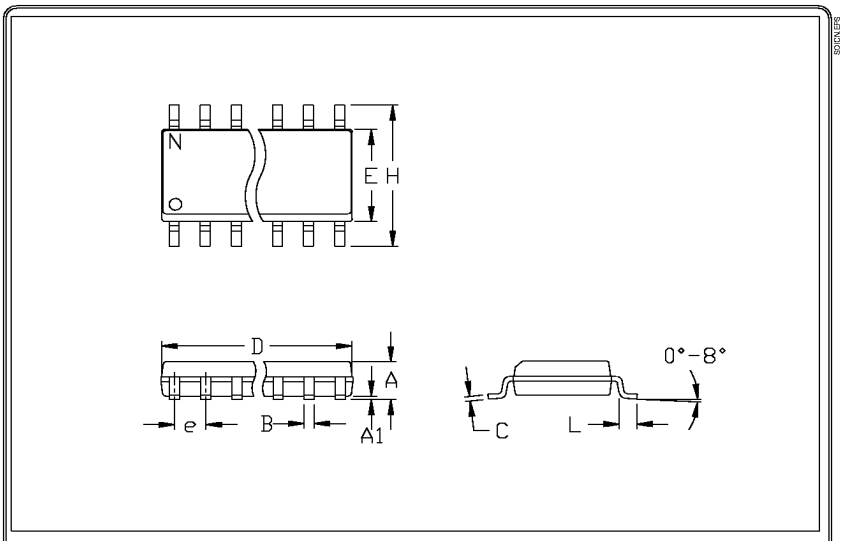
TRANSISTOR COUNT: 1116

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX7403CPA*	0°C to +70°C	8 Plastic DIP
MAX7403CSA*	0°C to +70°C	8 SO
MAX7403EPA*	-40°C to +85°C	8 Plastic DIP
MAX7403ESA*	-40°C to +85°C	8 SO
MAX7404CPA*	0°C to +70°C	8 Plastic DIP
MAX7404CSA*	0°C to +70°C	8 SO
MAX7404EPA*	-40°C to +85°C	8 Plastic DIP
MAX7404ESA*	-40°C to +85°C	8 SO
MAX7407CPA*	0°C to +70°C	8 Plastic DIP
MAX7407CSA*	0°C to +70°C	8 SO
MAX7407EPA*	-40°C to +85°C	8 Plastic DIP
MAX7407ESA*	-40°C to +85°C	8 SO

**Future product—contact factory for availability.*

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

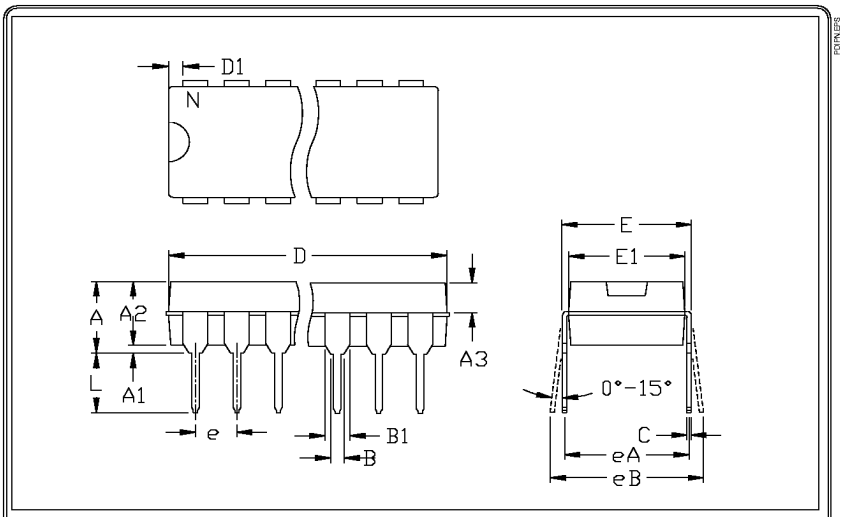
	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM — 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A (DOCUMENT CONTROL NUMBER / REV)