

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to table I: Change I_{CL} conditions from 40 V to 30 V; Rise time delay, inverting and non-inverting, change max limits from 150 to 205; Fall time delay, change non-inverting input to output, max limit from 80 to 145; Analog shutdown delay time, change max limit from 200 to 230.	87-12-10	M. A. Frye
B	Changes in accordance with NOR 5962-R056-92	91-11-27	M. A. Frye
C	Changes in accordance with NOR 5962-R234-92	92-08-10	M. A. Frye
D	Changes in accordance with NOR 5962-R122-93	93-04-02	M. A. Frye
E	Update boilerplate to add device class N. Add case outline X. Editorial changes throughout. Redrawn.-rrp	97-09-30	R. Monnin
F	Add case outline Y. Changes to 1.2.4, 1.3, and figure 1. -rrp	99-02-23	R. Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS OF SHEETS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F					
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12							
PMIC N/A	PREPARED BY Rajesh Pithadia	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216																		
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Rajesh Pithadia	MICROCIRCUIT, LINEAR, POWER DRIVER, DUAL CHANNEL, MONOLITHIC SILICON																		
	APPROVED BY Raymond Monnin																			
	DRAWING APPROVAL DATE 87-07-13	SIZE A	CAGE CODE 67268	5962-87619																
	REVISION LEVEL F	SHEET	1	OF	12															

DSCC FORM 2233
APR 97

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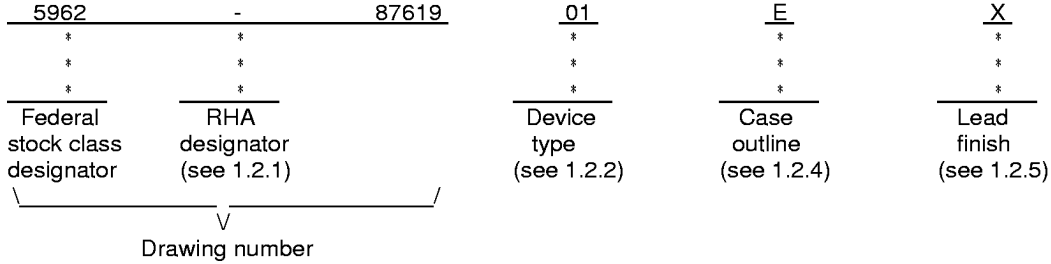
5962-E121-99

1. SCOPE

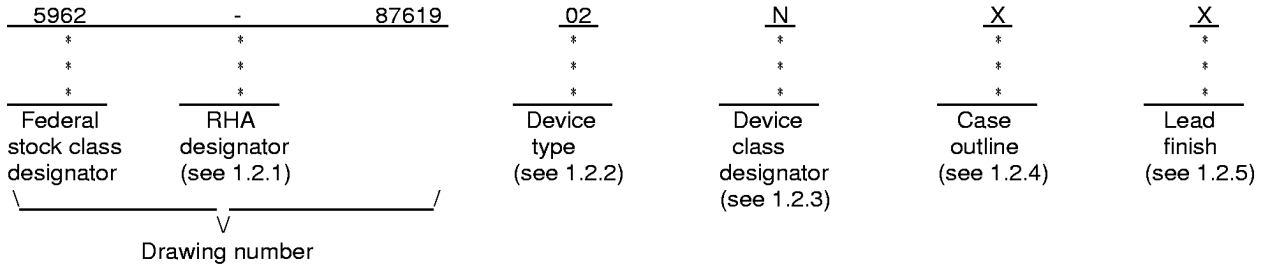
1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M or Q:



For device classes N or V:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	UC1707	Dual-channel power driver
02	UC2707	Dual-channel power driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-I-38535 with a non-traditional performance environment (encapsulated in plastic)
Q or V	Certification and qualification to MIL-PRF-38535

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1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>	<u>Document</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line	MIL-STD-1835
2	CQCC1-N20	20	Square leadless chip carrier	MIL-STD-1835
X	MS-001 BB	16	Plastic dual-in-line	JEDEC Publication 95
Y	MS-013 AA	16	Plastic SOIC	JEDEC Publication 95

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{IN})	+40 V dc	
Collector supply voltage (V_C)	+40 V dc	
Output current (each output, source or sink):			
Steady state	±500 mA	
Peak transient	±1.0 A (for cases E and 2)	
		±1.5 A (for cases X and Y)	
Capacitive discharge energy	15 µJ (for cases E and 2)	
		20 µJ (for cases X and Y)	
Digital inputs <u>2/</u>	+5.5 V dc	
Analog stop inputs	V_{IN} V dc	
Power dissipation (P_D):			
$T_A = +25^\circ\text{C}$	1 W (for cases E and 2) <u>3/</u>	
		2 W (for cases X and Y)	
$T_C = +25^\circ\text{C}$	2 W (for cases E and 2) <u>4/</u>	
		5 W (for cases X and Y)	
Storage temperature range (T_S)	-65°C to +150°C	
Lead temperature (soldering, 10 seconds)	+300°C	

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A):		
Device type 01	-55°C to +125°C
Device type 02	-25°C to +85°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Digital drive can exceed 5.5 V if input current is limited to 10 mA.

3/ Derate at 10 mW/°C above $T_A = +50^\circ\text{C}$.

4/ Derate at 16 mW/°C above $T_C = +25^\circ\text{C}$.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Publication 95 - Registered and Standard Outlines for Semiconductor Devices.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein .

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3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Block diagram(s). The block diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Marking for device class N. For PEM packages MIL-PRF-38535 marking is not required. Marking on the device shall include; a traceable date code, country of origin, pin one indicator, and manufacturers identification. In addition, the QML certification mark and the PIN as shown in 1.2 herein shall be marked on the topside of the package. Manufacturer may at their option place the QML certification mark adjacent to the PIN. In all cases, the purchase order shall reflect the SMD PIN as shown in 1.2 herein.

3.5.2 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 53 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C‡ T _A ‡ +125°C V _{IN} = V _C = 20 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
V _{IN} supply current	I _{CC(IN)}	V _{IN} = 40 V	1, 2, 3	All		15	mA
V _C supply current	I _{CC(C)}	V _C = 40 V, outputs low	1, 2, 3	All		7.5	mA
V _C leakage current	I _{CL}	V _{IO} = 0 V, V _C = 30 V	1, 2, 3	All		0.1	mA
Digital input low level voltage	V _{IL}		1, 2, 3	All		0.8	V
Digital input high level voltage	V _{IH}		1, 2, 3	All	2.2		V
Input current	I _I	V _I = 0 V	1, 2, 3	All		-1.0	mA
Input leakage current	I _{IL}	V _I = 5 V	1, 2, 3	All		0.1	mA
Output high saturation voltage, (V _C - V _O)	V _{CO(SAT)}	I _O = -50 mA	1, 2, 3	All		2.0	V
		I _O = -500 mA				2.5	
Output low saturation voltage	V _{O(SAT)}	I _O = 50 mA	1, 2, 3	All		0.4	V
		I _O = 500 mA				2.5	
Analog threshold voltage	V _{AT}	0 V‡ V _{CM} ‡ 15 V	1, 2, 3	All	100	150	mV
Input bias current	I _{IB}	V _{CM} = 0 V	1, 2, 3	All		-20	μA
Shutdown threshold voltage	V _{shutdown}	Pin 7 input	1, 2, 3	All	0.4	2.2	V
Latch disable threshold voltage	V _{disable}	Pin 3 input	1, 2, 3	All	0.8	2.2	V
Rise time delay 2/	t _{r(delay)}	Inverting input to output	9, 10, 11	01		145	ns
		Non-inverting input to output				205	
Fall time delay 2/	t _{r(delay)}	Inverting input to output	9, 10, 11	01		80	ns
		Non-inverting input to output				145	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C V _{IN} = V _C = 20 V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Rise time	t _r	Inverting input to output	C _L = 2.2 nF	9, 10, 11	01		70	ns
		Non-inverting input to output					70	
Fall time	t _f	Inverting input to output	C _L = 2.2 nF	9, 10, 11	01		70	ns
		Non-inverting input to output					70	
Analog shutdown delay time	t _{shut(A)}	Stop (+) ref. = 0 V Stop (-) input = 0 V to 0.5 V		9, 10, 11	01		190	ns
Digital shutdown delay time	t _{shut}	Shutdown (pin 7) = 2 V		9, 10, 11	01		60	ns
Functional test		See 4.4.1c		7, 8	All			

^{1/} For device type 02, -25°C ≤ T_A ≤ +85°C.

^{2/} Delay is measured to 10 percent output change.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

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Device type	01	02	01
Case outline	E	X and Y	2
Terminal number	Terminal symbol		
1	INPUT B INVERTING	INPUT B INVERTING	N/C
2	INPUT B NONINVERTING	INPUT B NONINVERTING	INPUT B INVERTING
3	LATCH DISABLE	LATCH DISABLE	INPUT B NONINVERTING
4	GROUND	GROUND	LATCH DISABLE
5	GROUND	GROUND	GROUND
6	OUTPUT A	OUTPUT A	N/C
7	SHUTDOWN	SHUTDOWN	GROUND
8	+V _{CC}	+V _{CC}	OUTPUT A
9	ANALOG STOP (+)	ANALOG STOP (+)	SHUTDOWN
10	ANALOG STOP (-)	ANALOG STOP (-)	+V _{CC}
11	OUTPUT B	OUTPUT B	N/C
12	GROUND	GROUND	ANALOG STOP (+)
13	GROUND	GROUND	ANALOG STOP (-)
14	+V _{IN}	+V _{IN}	OUTPUT B
15	INPUT A NONINVERTING	INPUT A NONINVERTING	GROUND
16	INPUT A INVERTING	INPUT A INVERTING	N/C
17	----	----	GROUND
18	----	----	V _{IN}
19	----	----	INPUT A NONINVERTING
20	----	----	INPUT A INVERTING

NOTE: All four ground terminals must be connected to a common ground.

FIGURE 1. Terminal connections.

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INVERTING	NONINVERTING	OUTPUT
H	H	L
L	H	H
H	L	L
L	L	L

OUTPUT = ~~INVERTING~~ and NONINVERTING
~~OUTPUT~~ = INVERTING and ~~NONINVERTING~~

FIGURE 2. Truth table.

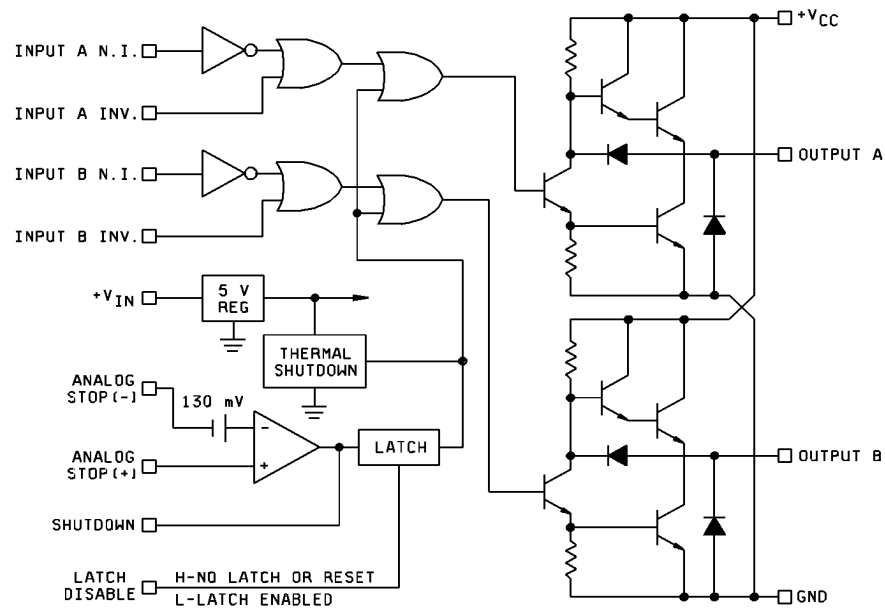


FIGURE 3. Block diagram.

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4.2.2 Additional criteria for device classes N, Q, and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5004 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 9 <u>1/</u>	1,2,3,7,9 <u>1/</u>	1,2,3,7,9 <u>1/</u>	1,2,3,7,9 <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	----	----	----	----

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-87619
		REVISION LEVEL F	SHEET 12

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-02-23

Approved sources of supply for SMD 5962-87619 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8761901EA <u>1/</u>	48726	UC1707J/883B
5962-87619012A <u>1/</u>	48726	UC1707L/883BC
5962-8761902NXB	48726	UC2707N
5962-8761902NYB	48726	UC2707DW/81429

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

48726

Vendor name
and address

Unitrode Semiconductor Corp.
7 Continental Blvd.
Merrimack, NH 03054

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.