H0541
H0542

Parallel Input
Dot Matrix LCD Driver

HUGHES
AIRCRAFT COMPANY
SEMICONDUCTOR DIVISION
Industrial Electronics Group

DESCRIPTION

Hughes 0541 and 0542 are a set of CMOS/LSI circuits which drive a dot matrix LCD display under microcomputer control. The intended display is a 5 x 7 or 5 x 8 alphanumeric dot matrix with nearly any number of characters. Other matrix displays, such as games and custom arrays, could also be driven by this set of circuits.

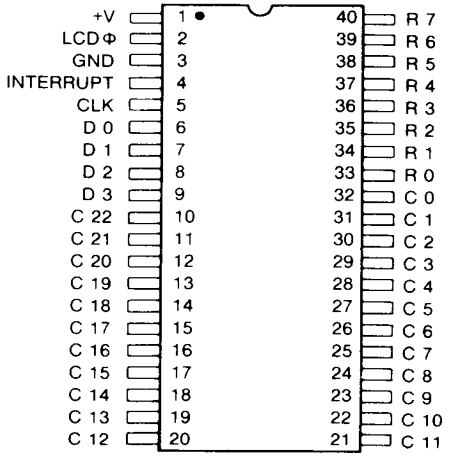
The 0541 is organized as 8 rows x 23 columns, and thus can handle up to four characters by itself. The 0542 is organized as 0 rows x 32 columns and is used in addition to the 0541 when more than 23 columns are required. Data is input 4 bit parallel to minimize the time required to load in data. This circuit drives (using a multiplexed scheme) the display with proper voltage level AC waveforms, but does not handle refresh or character encoding. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer.

The 0541 and 0542 are available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

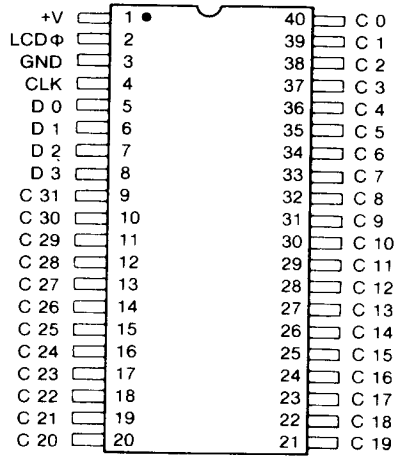
FEATURES

- Direct drive of matrix LCDs
- Cascadable for larger displays
- On chip oscillator
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and PMOS compatible inputs
- Flexible organization allows arbitrary display patterns
- Interrupt Output to request data from microcomputer

0541
PIN CONFIGURATION



0542
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

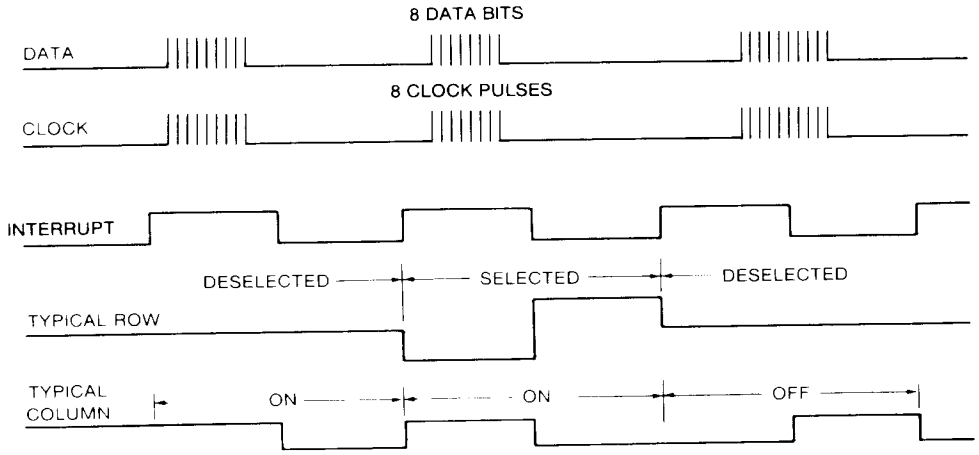
V_{DD}	−.3 to + 17 volts
Inputs	+ V_{DD} − 17 to + V_{DD} + .3 volts
Power Dissipation	250 mW
Operating Temperature	
Ceramic Package	− 55 to + 125°C
Plastic Package	− 40 to + 85°C
Storage Temperature	− 65 to + 125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

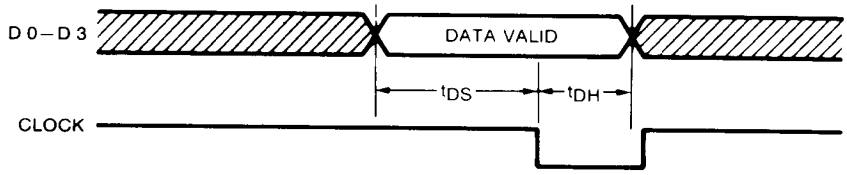
ELECTRICAL CHARACTERISTICS at T_A = + 25°C and V_{DD} = 5V unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	12	V
Supply Current	I_{DD}			600	µA
Input High Level	V_{IH}		.75V_{DD}	V_{DD}	V
Input Low Level	V_{IL}		V_{DD}−15	.25V_{DD}	V
Input Leakage	I_L			5	µA
Input Capacitance	C_I			5	pf
Row Output High	V_{OH}		V_{DD}−.05	V_{DD}	V
Row Output Low	V_{OL}		0	.05	V
Row Output Unselected	V_{OM}		.5V_{DD}−.05	.5V_{DD}+.05	V
Column Output High	V_{OH}		.68V_{DD}−.05	.68V_{DD}+.05	V
Column Output Low	V_{OL}		.32V_{DD}−.05	.32V_{DD}+.05	V
Row and Column Output Impedance	R_{ON}	I_L = 10µA		30	KΩ
Interrupt Output Impedence	R_{ON}	I_L = 100µA		1	KΩ
Clock Rate	f		DC	1.0	MHz
Data in Setup Time	t_{DS}	Data change to clock fall	300		nsec.
Data in Hold Time	t_{DH}	Clock fall to data change	150		nsec.
LCDΦ to Interrupt Output Delay	t_D		300		nsec.
LCDΦ High Level	V_{IH}		.9V_{DD}	V_{DD}	V
LCDΦ Low Level	V_{IL}		0	.1V_{DD}	V
LCDΦ Input Impendence	R_{IN}		1	3	MΩ

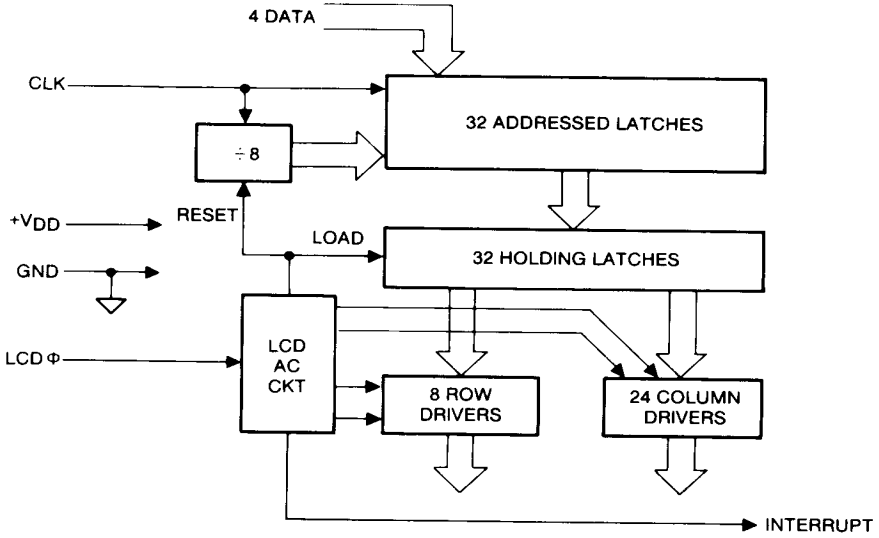
TYPICAL WAVEFORMS



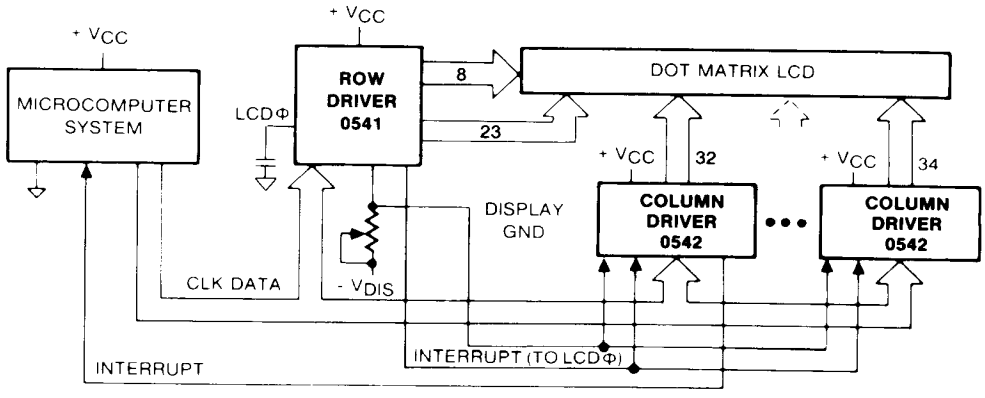
TIMING DIAGRAM



BLOCK DIAGRAM



TYPICAL SYSTEM BLOCK DIAGRAM



OPERATING NOTES

1. The addressed latches load when clock is high.
2. A logic 1 on Data In selects a row or causes a segment to be visible.
3. A parallel transfer of data from the addressed latches register to the holding latches occurs upon the rising edge of Interrupt Output. Also, the ÷8 counter is reset.
4. Row waveforms are out of phase with Interrupt Output if selected and at midpoint voltage otherwise. Levels are V_{DD}, 0, and $V_{DD}/2$.
5. Column waveforms are in phase with Interrupt Output if selected and are out of phase if not selected. Levels are .32 V_{DD} and .68 V_{DD}.
6. The intended mode of operation is as follows:
   a. Interrupt Output frequency is the minimum no flicker frequency (≈30Hz) times the number of backplanes utilized.
   b. Interrupt Output is exactly 50% duty cycle (to keep DC off the display) and is synchronized with loading the data from addressed latches to holding latches.
   c. In between each Interrupt Output rising edge, 4 bit parallel data is clocked in with 8 clock pulses for the next time slot to await the next Interrupt Output rising edge, which causes the parallel transfer.
   d. The Interrupt Output goes to the microcomputer and is treated as a refresh request, or else the microcomputer drives the LCDΦ input.
   e. Backplanes are addressed sequentially and individually.
7. The LCDΦ pin can be used in two modes, driven or oscillating. If LCDΦ is driven, the Interrupt Output will follow it. If the LCDΦ pin is allowed to oscillate, its frequency is inversely proportional to capacitance and the Interrupt Output waveform has a frequency half that of the oscillator itself. The approximate relationship is f_{out} (KHz) = 380/ c (pf). The frequency is nearly independent of supply voltage.
8. To cascade units, either connect Interrupt Output of one circuit to LCDΦ of all other circuits (thus one capacitor provides frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. Then tie all corresponding data inputs together and clock each circuit individually when its data is on the bus. In the case of two driver circuits and an 8 bit microcomputer, the clocks could be common and each Data In tied to a different line of the data bus.
9. There are two obvious signal races to be avoided:
   a. Changing data when clock is falling, and
   b. Allowing Interrupt Output rising edge to be very close to clock falling edge.
10. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
11. Input order of 0541.

Clk Pulse	1	2	3	4	5	6	7	8
Data 0	R 0	R 4	C 0	C 4	C 8	C 12	C 16	C 20
Data 0	R 1	R 5	C 1	C 5	C 9	C 13	C 17	C 21
Data 2	R 2	R 6	C 2	C 6	C 10	C 14	C 18	C 22
Data 3	R 3	R 7	C 3	C 7	C 11	C 15	C 19	

12. Input order of 0542 is similar, but starts at C0 (Pulse 1, Data 0) and ends at C 31 (Pulse 8, Data 3).

U.S.A.:
Hughes Semiconductor Division
500 Superior Avenue, Box H
Newport Beach, CA 92658-8903
Tele: (714) 759-2727 TWX: 910-596-1374 HACSSPD NPBH

EUROPE:
Hughes Microelectronics Limited
Clive House, 12/18 Queens Road, Weybridge, Surrey, England
Tele: 0932 47262 TWX: 929727
or—
Schmaedelstr. 22, 8000 Munich 60, Germany
Tele: 49-89-834-7088 Telex: 5213856 HSPD

11/85
Printed in U.S.A.