

CTCSS ENCODER/DECODER

FEATURES

- 38 CTCSS Tones + Notone
- TX/RX Audio Filters
- TX Tone Phase Reversals
- Serial or Parallel Programming

BENEFITS

- Scanning of any Channel
- Improved Sinad
- Squelch Tail Elimination
- Easy μ P Interface

APPLICATIONS

- Mobile Radio Channel Sharing
- Wireless Intercom

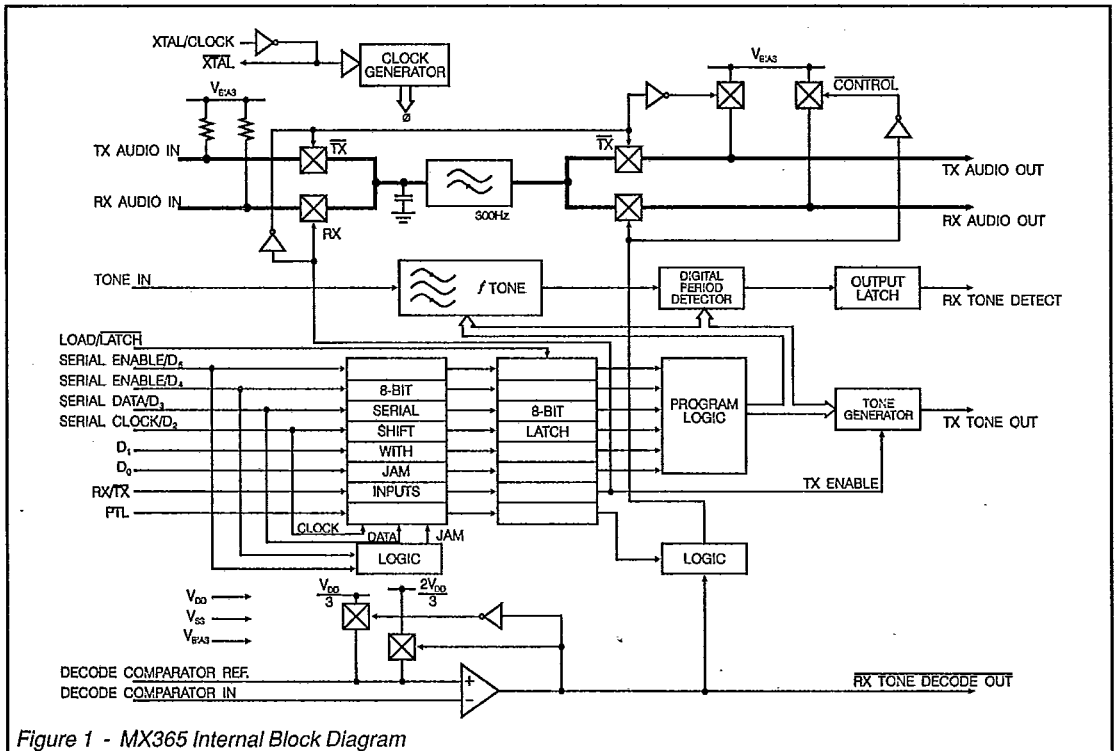
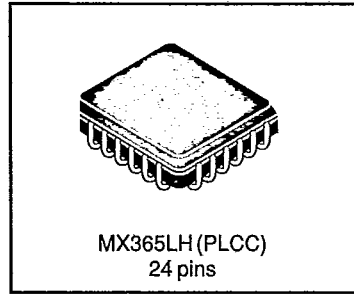
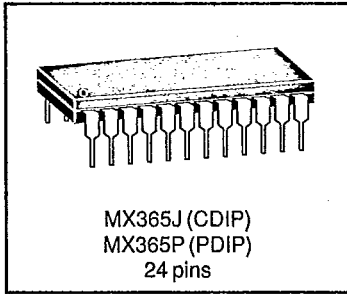


Figure 1 - MX365 Internal Block Diagram

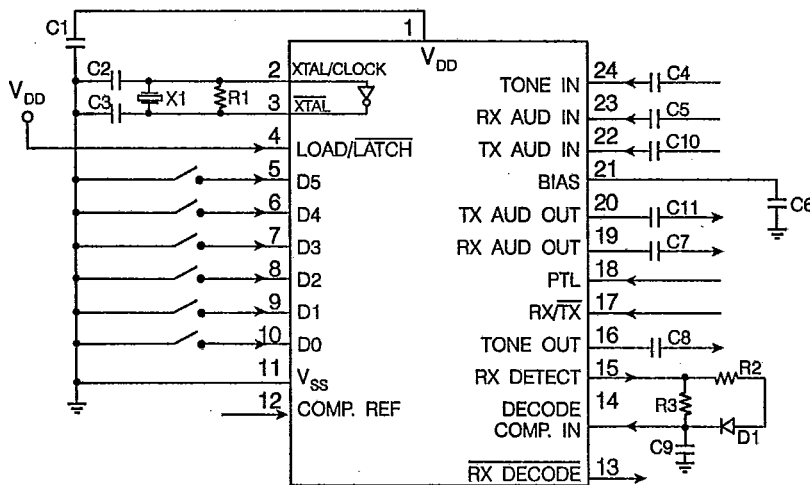
Voice on shared radio channels is multiplexed with a subaudible CTCSS tone as a means of directing messages among user groups licensed on the same RF frequency. Continuous Tone Controlled Squelch Systems (CTCSS) modulate the transmitter with a discrete tone, taken from a field of 38 in the range of 67 to 250 Hz, according to EIA standard RS-220A. Groups of radio receivers, segregated by common interest and assigned tone, demodulate the voice/tone mixture for voice messages to be heard.

The MX365 CTCSS Encoder/Decoder enhances voice/tone multiplexing with an on-chip filter that attenuates TX speech 40dB at 250Hz, while passing signals >300Hz with only ± 1 dB of ripple.

Early CTCSS designs did not filter TX speech, depending instead on the host transmitter's pre-emphasis network. At only 6dB/octave, their attenuation of speech components at the higher CTCSS tones was only a couple of dB, including talk-off.

The MX365 adds serial or parallel tone and TX/RX selection, and a new LOAD/LATCH pin. A Notone program code has been included to permit scanning channels without CTCSS. Operation of the PTL switch during TX reverses the phase of the transmitted CTCSS tone, used in some radios to eliminate squelch tails.

The MX365 is a CMOS integrated circuit requiring a single 5-volt supply and a 1MHz clock or crystal.



MX365J

Component Values

R1: 1M Ω	C1: 0.1 μ F	C5: 0.1 μ F	C9: 0.1 μ F
R2: 560k Ω	C2: 68pF	C6: 0.47 μ F	C10: 0.1 μ F
R3: 820k Ω	C3: 33pF	C7: 0.1 μ F	C11: 0.1 μ F
X1: 1MHz	C4: 0.1 μ F	C8: 0.1 μ F	D1: Small signal

Tolerances: Resistors $\pm 10\%$
Capacitors $\pm 20\%$
Xtal $\pm 0.1\%$

PIN FUNCTION TABLE

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Pin	Function
1	V_{DD} : Positive Supply.
2	Xtal/Clock : Input to the on-chip inverter used with a 1 MHz Xtal or external clock source.
3	Xtal : Output of the on-chip inverter (clock output).
4	Load/Latch : Controls 8 on-chip latches and is used to latch RX/TX, PTL, and D0-D5. This pin is internally pulled to V _{DD} . A logic "1" applied to this input puts the 8 latches in "transparent" mode. A logic "0" applied to this input puts the 8 latches in the "latched" mode. In parallel mode data is loaded and latched by a logic 1-0 transition (see Fig. 3). In serial mode data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Fig. 4).
5	D5/Serial Enable 1 : Data input D5 (in parallel mode). A logic "1" applied to this input together with a logic "0" applied to D4/Serial Enable 2 will put the device in serial mode (see Fig. 4). This pin is internally pulled to V _{DD} .
6	D4/Serial Enable 2 : Data input D4 (in parallel mode). A logic "0" applied to this input together with a logic "1" on pin 5 will place the device in serial mode (see Fig. 5). This pin is internally pulled to V _{DD} .
7	D3/Serial Data : Data input D3 (in parallel mode). In serial mode this pin becomes the serial data input for D5-D0, RX/TX and PTL (see Fig. 4). D5 is clocked first and PTL last. This pin is internally pulled to V _{DD} .
8	D2/Serial Clock : Data input D2 (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see Fig. 4). This pin is internally pulled to V _{DD} .
9	D1 : Data input D1 (in parallel mode). This pin is internally pulled to V _{DD} .
10	D0 : Data input D0 (in parallel mode). This pin is internally pulled to V _{DD} .
11	V_{SS} : Negative supply.
12	Decode Comparator Ref. : This pin is internally biased to V _{DD} /3 or 2V _{DD} /3 via 1M resistors depending on the logical state of the RX Tone Decode Out pin. RX Tone Decode Out = 1 will bias this input 2V _{DD} /3; a logic "0" will bias this input V _{DD} /3. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce "chatter" under marginal conditions.
13	RX Tone Decode Out : This is the gated output of the decode comparator. This output is used to gate the RX Audio path. A logic "0" on this pin indicates a successful decode and that the Decode Comparator Input pin is more positive than the Decode Comparator Ref. input (see Table 1).
14	Decode Comparator Input : This is the inverting input of the decode comparator. This pin is normally connected to the integrated output of the RX Tone Detect line.
15	RX Tone Detect : In RX mode this output will go to logic "1" during a successful decode. It must be externally integrated to control response and deresponse times (see Table 1).

PIN FUNCTION TABLE

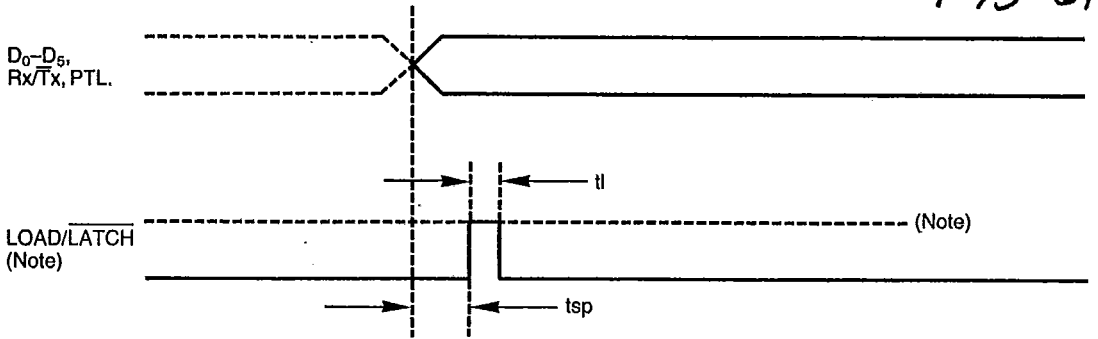
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Pin	Function
16	TX Tone Out: The CTCSS sinewave output appears on this pin under control of the RX/TX pin. This pin, when not transmitting a tone, may be biased to $V_{DD} - 0.7V$ or O/C (see Table 1). This pin is an emitter follower output with high impedance load, requiring capacitive coupling or a low impedance (<1k Ω) load to ground.
17	RX/TX: This input (in parallel mode) selects RX or TX modes (see Fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1M Ω resistor.
18	PTL: In parallel RX mode this pin operates as a "Push To Listen" function by enabling the RX audio path, thus overriding the tone squelch function. In parallel TX mode this pin reverses the phase of the transmitted CTCSS tone (used for squelch tail elimination). In serial mode this function is serially loaded (see Fig. 2).
19	RX Audio Out: This is the high pass filtered receive audio output pin. This pin outputs audio when RX Tone Decode = 0, or PTL = 1, or when Notone is programmed (see Table 2). In TX mode this pin is biased to $V_{DD}/2$.
20	TX Audio Out: This is the high pass filtered transmit audio output pin. In TX mode this pin outputs audio present at the TX Audio Input pin. In RX mode this pin is biased to $V_{DD}/2$.
21	Bias: This pin is the output of an internally generated $V_{DD}/2$ bias level and would normally be externally decoupled to V_{SS} via capacitor C7.
22	TX Audio In: This is the TX Audio input pin. In TX mode it may be prefiltered, using the TX audio path, thus helping to avoid talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. This pin is internally biased to $V_{DD}/2$.
23	RX Audio In: This is the input to the audio high pass filter in RX mode. It is internally biased to $V_{DD}/2$.
24	Tone Input: This is the input to the CTCSS tone detector. It is internally biased to $V_{DD}/2$.

PARALLEL AND SERIAL MODE TIMING DIAGRAMS

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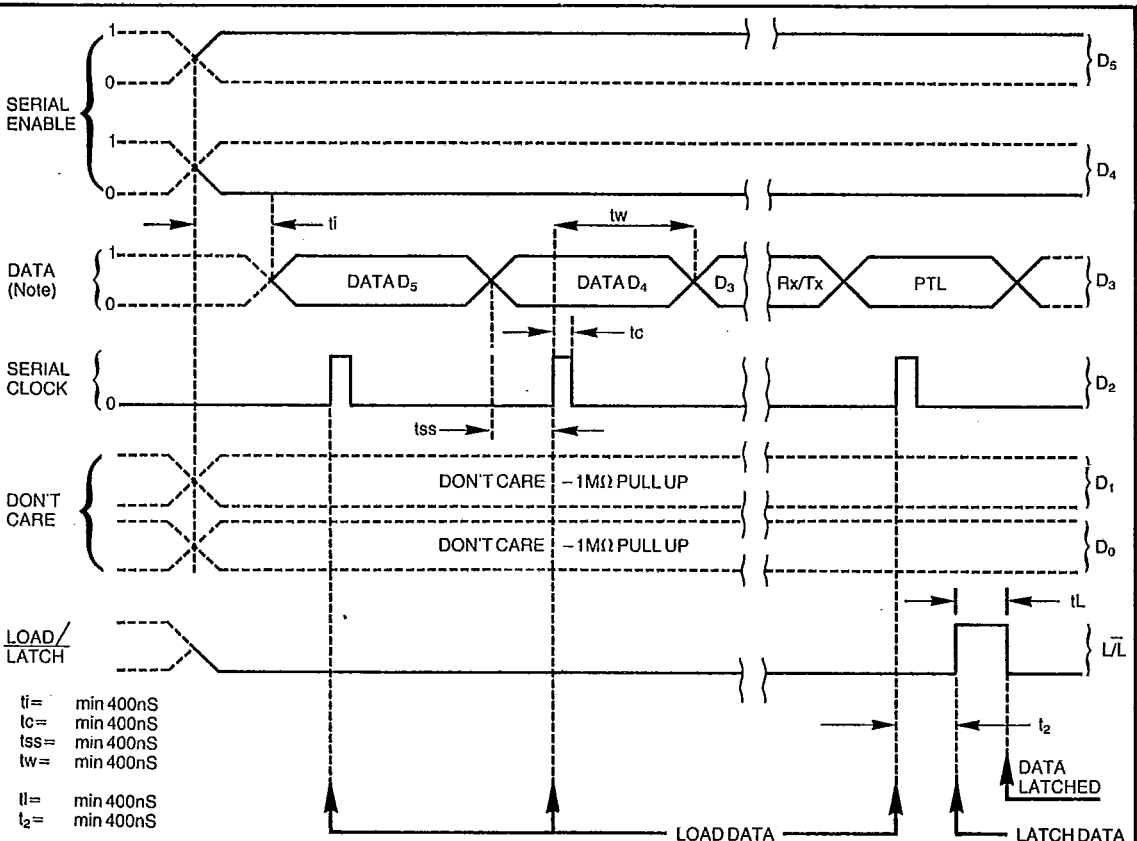
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Note: For wired, non microprocessor, applications load/latch should be connected to V_{DD}

t_i min=400ns
 t_{sp} min=400ns

FIG. 3: PARALLEL MODE
 (NOT TO SCALE)



t_i = min 400ns
 t_c = min 400ns
 t_{ss} = min 400ns
 t_w = min 400ns

t_L = min 400ns
 t_2 = min 400ns

Note 1: Serial bit 1 through bit 8= $D_5, D_4, D_3, D_2, D_1, D_0, Rx/Tx$ and PTL respectively. Load bit 1 first, bit 8 last.

FIG. 4: SERIAL MODE (NOT TO SCALE)

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Table 1 Truth table defining combinations of input/output conditions

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D ₀ -D ₅	Input Pin — Condition			Output Pin — Condition		Result/Function					
	Rx/TX	PTL	Decode Comp Input	Rx Tone Detect	Tone Decode	Tone Transmitter Enabled	Tx Tone Phase Reversed	Tx Audio Path Enabled	Tone Decoder Enabled	Rx Audio Path Enabled	Notes
Tone	0	0	x	0	1	Yes	No	Yes	No	No (bias)	1a
Tone	0	1	x	0	1	Yes	Yes	Yes	No	No (bias)	1b
No tone	0	x	x	0	1	No (o/c)	x	Yes	No	No (bias)	2
Tone	1	0	0	0	1	No (o/c)	x	No	Yes	No (bias)	3a
Tone	1	1	0	0	1	No (o/c)	x	No	Yes	Yes	3b
Tone	1	x	1	1	0	No (o/c)	x	No	Yes	Yes	4
No tone	1	x	x	x	0	No (o/c)	x	No	Yes	Yes	5

Notes:

- 1a. Normal tone transmit condition.
- 1b. Tone transmit with phase reversed.
2. 'NOTONE' programmed in Tx mode, tone transmit O/P set to $V_{DD}/2 - 0.7V$. Tx audio path enabled.
- 3a. Normal decode standby.
- 3b. Normal decode standby with PTL used to enable audio.
4. Normal 'decode of correct CTCSS tone' condition, PTL has no effect.
5. 'NOTONE' programmed in Rx mode, tone transmit O/P (o/c), Rx audio path enabled.

Table 2 Tone programming Truth table

Nominal Freq. Hz	MX365 Frequency	$\Delta f_o\%$	D ₀	D ₁	Program D ₂	Inputs D ₃	D ₄	D ₅
67.0	67.05	+ .07	1	1	1	1	1	1
71.9	71.90	0.0	1	1	1	1	1	0
74.4	74.35	- .07	0	1	1	1	1	1
77.0	76.96	- .05	1	1	1	1	0	0
79.7	79.77	+ .09	1	0	1	1	1	1
82.5	82.59	+ .10	0	1	1	1	1	0
85.4	85.38	- .02	0	0	1	1	1	1
88.5	88.61	+ .13	0	1	1	1	0	0
91.5	91.58	+ .09	1	1	0	1	1	1
94.8	94.76	- .04	1	0	1	1	1	1
97.4	97.29	-0.11	0	1	0	1	1	1
100.0	99.96	- .04	1	0	1	1	0	0
103.5	103.43	- .07	0	0	1	1	1	0
107.2	107.15	- .05	0	0	1	1	0	0
110.9	110.77	- .12	1	1	0	1	1	0
114.8	114.64	- .14	1	1	0	1	0	0
118.8	118.80	0.0	0	1	0	1	1	0
123.0	122.80	- .17	0	1	0	1	0	0
127.3	127.08	- .17	1	0	0	1	1	0
131.8	131.67	- .10	1	0	0	1	0	0
136.5	136.61	+ .08	0	0	0	1	1	0
141.3	141.32	+ .02	0	0	0	1	0	0
146.2	146.37	+ .12	1	1	1	0	1	0
151.4	151.09	- .20	1	1	1	0	0	0
156.7	156.88	+ .11	0	1	1	0	1	0
162.2	162.31	+ .07	0	1	1	0	0	0
167.9	168.14	+ .14	1	0	1	0	1	0
173.8	173.48	- .19	1	0	1	0	0	0
179.9	180.15	+ .14	0	0	1	0	1	0
186.2	186.29	+ .05	0	0	1	0	0	0
192.8	192.86	+ .03	1	1	0	0	1	0
203.5	203.65	+ .07	1	1	0	0	0	0
210.7	210.17	- .25	0	1	0	0	1	0
218.1	218.58	+ .22	0	1	0	0	0	0
225.7	226.12	+ .18	1	0	0	0	1	0
233.6	234.19	+ .25	1	0	0	0	0	0
241.8	241.08	- .30	0	0	0	0	1	0
250.3	250.28	- .01	0	0	0	0	0	0
Notone	Notone	—	0	0	0	0	0	0
Serial Input Mode			x	x	Clock	Data	0	1

SPECIFICATIONS

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ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref $V_{SS} = 0V$)	-0.3 V to $V_{DD} + 0.3 V$
Sink/Source Current (Total)	20mA
Maximum Device Dissipation	100mW
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

$$V_{DD} = 5.0V$$

$$T_{AMB} = 25^{\circ}C$$

$$0dB \text{ ref.} = 300mVrms$$

Composite signal: 0dB 1kHz test tone, -12dB noise (band limited 6kHz gaussian white noise), -20dB f_0 CTCSS tone.

Characteristics

Static Values

	See Note	Min.	Typ.	Max.	Unit
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
TX		-	3.5	-	mA
RX		-	3.5	-	mA
Tone Input Impedance		-	1	-	M Ω
Audio Input Impedance		-	1	-	M Ω
Audio Output Impedance		-	1	-	k Ω
Digital Input Impedance	1	-	1	-	M Ω
Input logic "1"	1	70% V_{DD}	-	-	V
Input logic "0"	1	-	-	30% V_{DD}	V
Logic "1" output 1' source = 0.1mA	2	80% V_{DD}	-	-	V
Logic "0" output 1' sink - 0.1mA	2	-	-	20% V_{DD}	V

Dynamic Values

Decoder

Decode Input Signal Level	3	-20	-	-	dB
Decode Response Time	3,6,7	-	-	250	ms
Deresponse Time	3,6,7	-	180	250	ms
Decode Selectivity	3	± 0.5	-	± 3	% f_0

Encoder

Tone Output Level (relative to 775mVrms)		-3	0	-	dB
Tone Frequency Accuracy (f error)		-0.3	-	+0.3	% f_0
Risetime to 90% nominal O/P:					
$f_0 > 100Hz$	4	-	15	-	ms
$f_0 < 100Hz$	4	-	45	-	ms
Tone Output Load Current		-	-	5	mA
Total Harmonic Distortion		-	2	5	%
Output Level Variation Between Tones		-	0.1	-	dB

Audio Filter

Total Harmonic Distortion	5	-	2	5	%
Output Noise Level		-	-49	-45	dB

(input a.c. short circuit, audio switch enabled)

Characteristics**See Note****Min.****Typ.****Max.****Unit****Audio Filter**

Cutoff Frequency

-

300

-

Hz

Bandpass Ripple (300-3000Hz)

5

-1

-

+1

dB

Stopband Attenuation <250Hz

5

36

40

-

dB

Passband Gain 1kHz

-

0

-

dB

Audio Switch

Isolation

5

-

60

-

dB

Serial/Parallel Inputs (See Figures 3 & 4)Parallel Set-up Time t_{sp}

400

-

-

ns

Load/Latch Pulse Width t_l

400

-

-

ns

Serial Clock Pulse Width t_c

400

-

-

ns

Serial Set-up Time t_{ss}

400

-

-

ns

Serial Clock Frequency

-

1

-

MHz

Notes:

1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite Signal Test Condition.
4. Any programming tone and $RL = 600$, $CL = 15pF$. This includes response to a phase reversal instruction.
5. 1kHz references = 0dB.
6. $f_0 > 100Hz$
(for 100 Hz $> f_0 > 67Hz$: $t = 100/f_0 Hz \times 250ms$)
7. See Figure 3.