FINAL COM'L:-10 IND:-20

PALLV16V8-10 and PALLV16V8Z-20

Low Voltage, Zero Power 20-Pin EE CMOS Universal Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3 V JEDEC compatible**
  — V_{CC} = +3.0 V to +3.6 V
- **Pin and function compatible with all 20-pin PAL® devices**
- **Electrically-erasable CMOS technology provides reconfigurable logic and full testability**
- **Direct plug-in replacement for the PAL16R8 series**
- **Designed to interface with both 3.3-V and 5-V logic**
- **Outputs programmable as registered or combinatorial in any combination**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

The PALLV16V8 is an advanced PAL device built with low-voltage, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALLV16V8 will directly replace the PAL16R8, with the exception of the PAL16C1.

The PALLV16V8Z provides zero standby power and high speed. At 30-μA maximum standby current, the PALLV16V8Z allows battery powered operation for an extended period.

The PALLV16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

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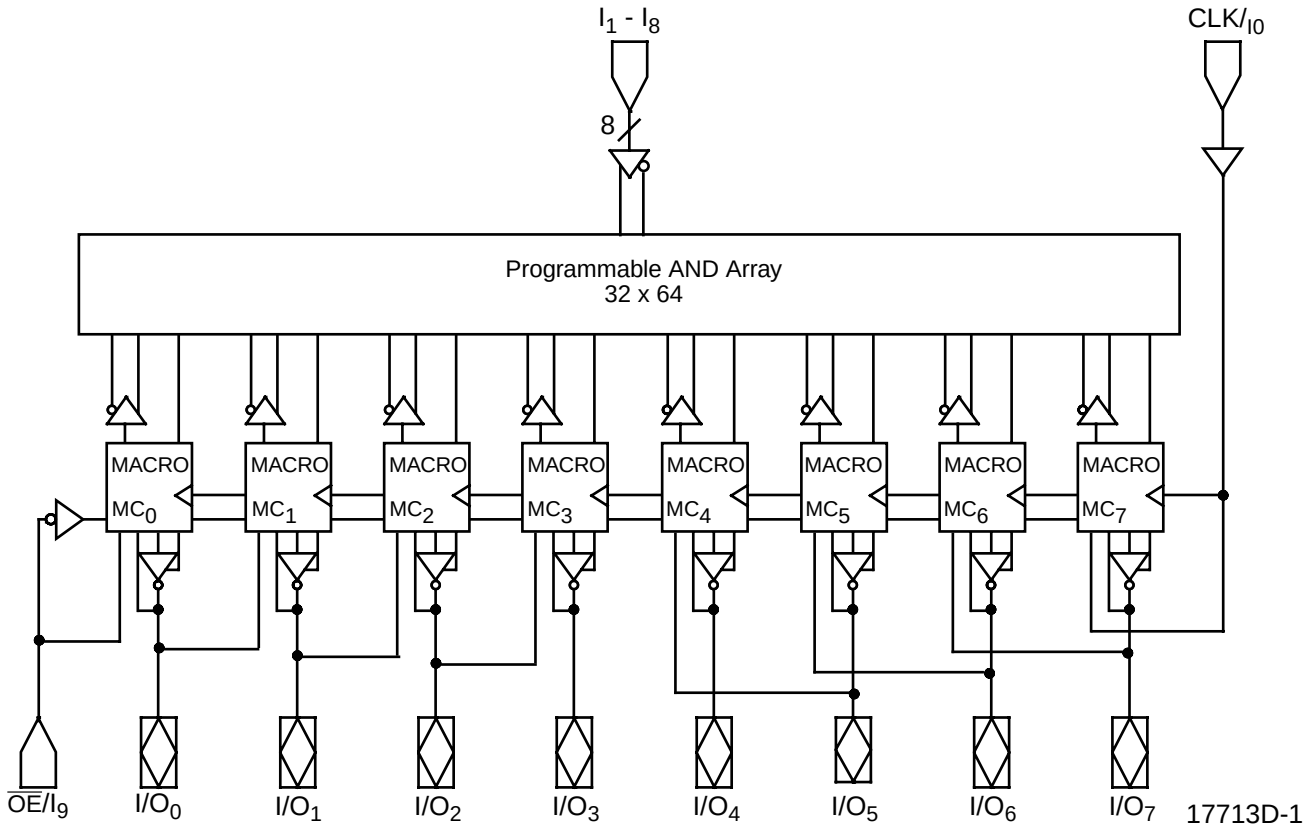
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The PALLV16V8 is a low-voltage, EE CMOS version of the PALCE16V8.

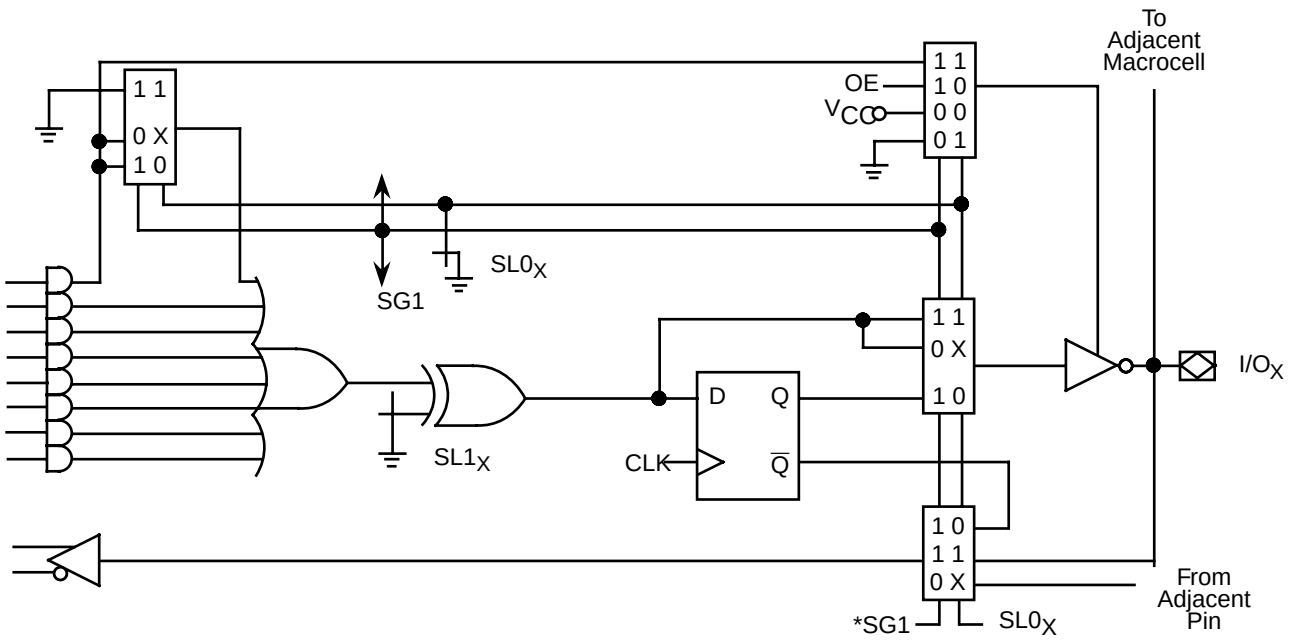
The PALLV16V8Z is a low-voltage, EE CMOS version of the PALCE16V8. In addition, the PALLV16V8Z has zero standby power and an unused product term disable feature for reduced power consumption.

The PALLV16V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0-MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALLV16V8 are automatically configured from the user's design specification. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALLV16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALLV16V8. The programmer will program the PALLV16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALLV16V8. Here the user must use the PALLV16V8 device code. This option allows full utilization of the macrocell.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.* 17713D-004

Figure 1. PALLV16V8 Macrocell

CONFIGURATION OPTIONS

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALLV16V8 will emulate a PAL16R8 family. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7,

$\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$=0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALLV16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$=0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of MC_3 and MC_4. MC_3 and MC_4 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7, and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$=1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and OE are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7, and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$=1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$=1. The output buffer is disabled. Except for MC_0 and MC_7, the feedback signal is an adjacent I/O. For MC_0 and MC_7, the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

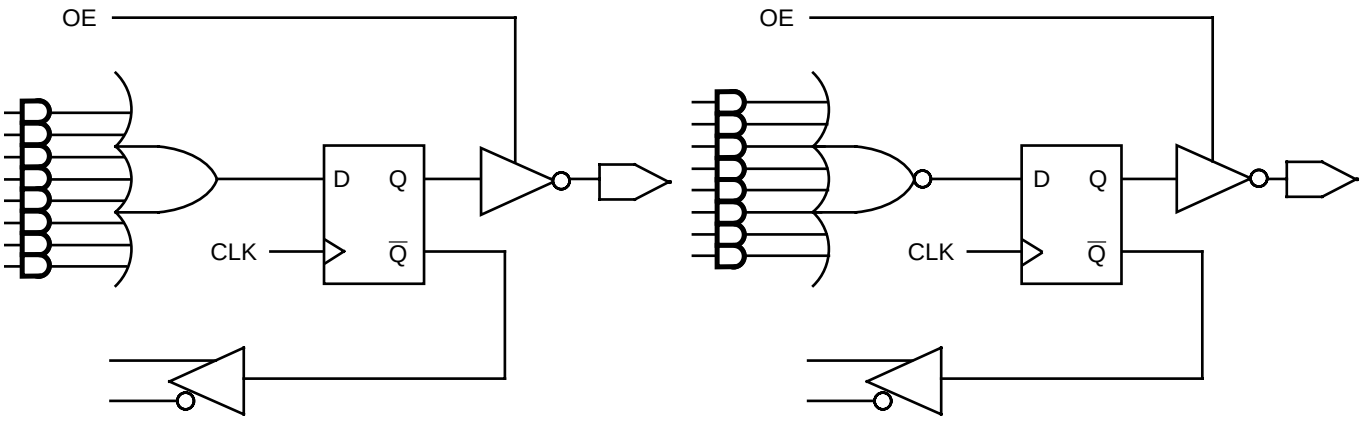
Table 1. Macrocell Configuration

SG0	SG1	$SL0_X$	Cell Configuration	Devices Emulated	SG0	SG1	$SL0_X$	Cell Configuration	Devices Emulated
Device Uses Registers					Device Uses No Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4	1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
0	1	1	Combinatorial I/O	PAL16R6, 16R4	1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
					1	1	1	Combinatorial I/O	PAL16L8

Programmable Output Polarity

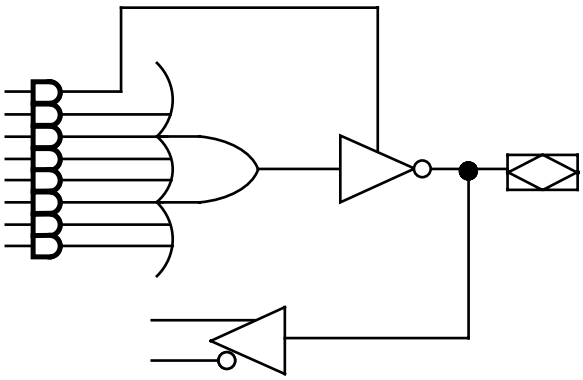
The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save “DeMorganizing” efforts.

Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.

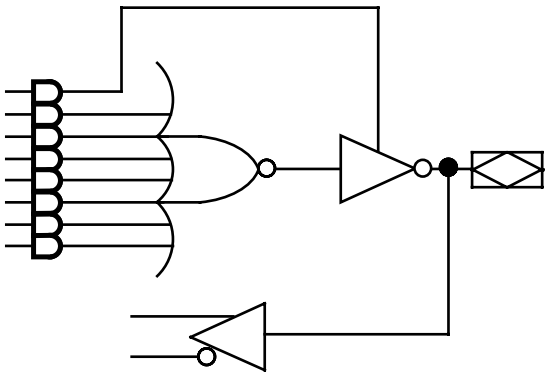


a. Registered active low

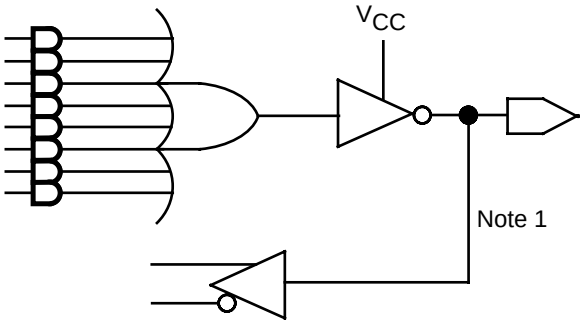
b. Registered active high



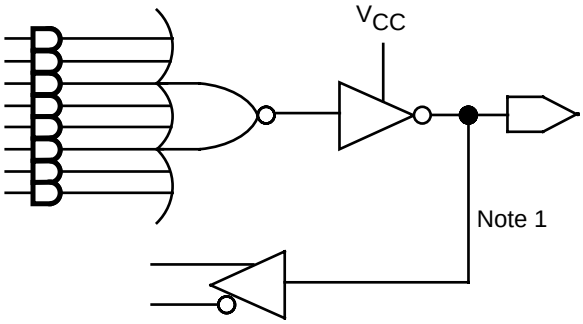
c. Combinatorial I/O active low



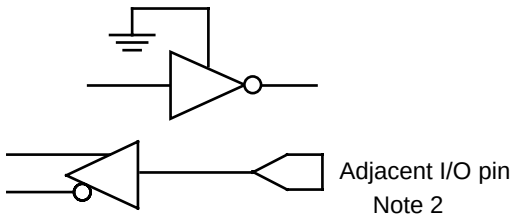
d. Combinatorial I/O active high



e. Combinatorial output active low



f. Combinatorial output active high



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g. Dedicated input

Notes:

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *The dedicated-input configuration is not available on pins 15 and 16.*

Figure 2. Macrocell Configurations

Benefits of Lower Operating Voltage

The PALLV16V8 has an operating voltage range of 3.0V to 3.6 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications. The PALLV16V8 inputs accept up to 5.5 V, so they are safe for mixed voltage design.

Because power is proportional to the square of the voltage, reduction of the supply voltage from 5.0 V to 3.3 V significantly reduces power consumption. This directly translates to longer battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3-V designs facilitate a reduction in the form factor.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation and provides a less hostile environment for board design. A lower operating voltage also reduces electromagnetic radiation noise and makes obtaining FCC approval easier.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALLV16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALLV16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

The preload function is not disabled by the security bit. This allows functional testing after the security bit is programmed.

Security Bit

A security bit is provided on the PALLV16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALLV16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALLV16V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALLV16V8 offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

Technology

The high-speed PALLV16V8Z is fabricated with Vantis' advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. This technology provides strong input-clamp diodes and a grounded substrate for clean switching.

Zero-Standby Power Mode

The PALLV16V8 features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALLV16V8Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero (I_{CC} < 30 μA). The outputs will maintain the states held before the device went into the standby mode. There is no speed penalty associated with coming out of standby mode.

When any input switches, the internal circuitry is fully enabled, and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This saving is illustrated in the I_{CC} vs. frequency graph.

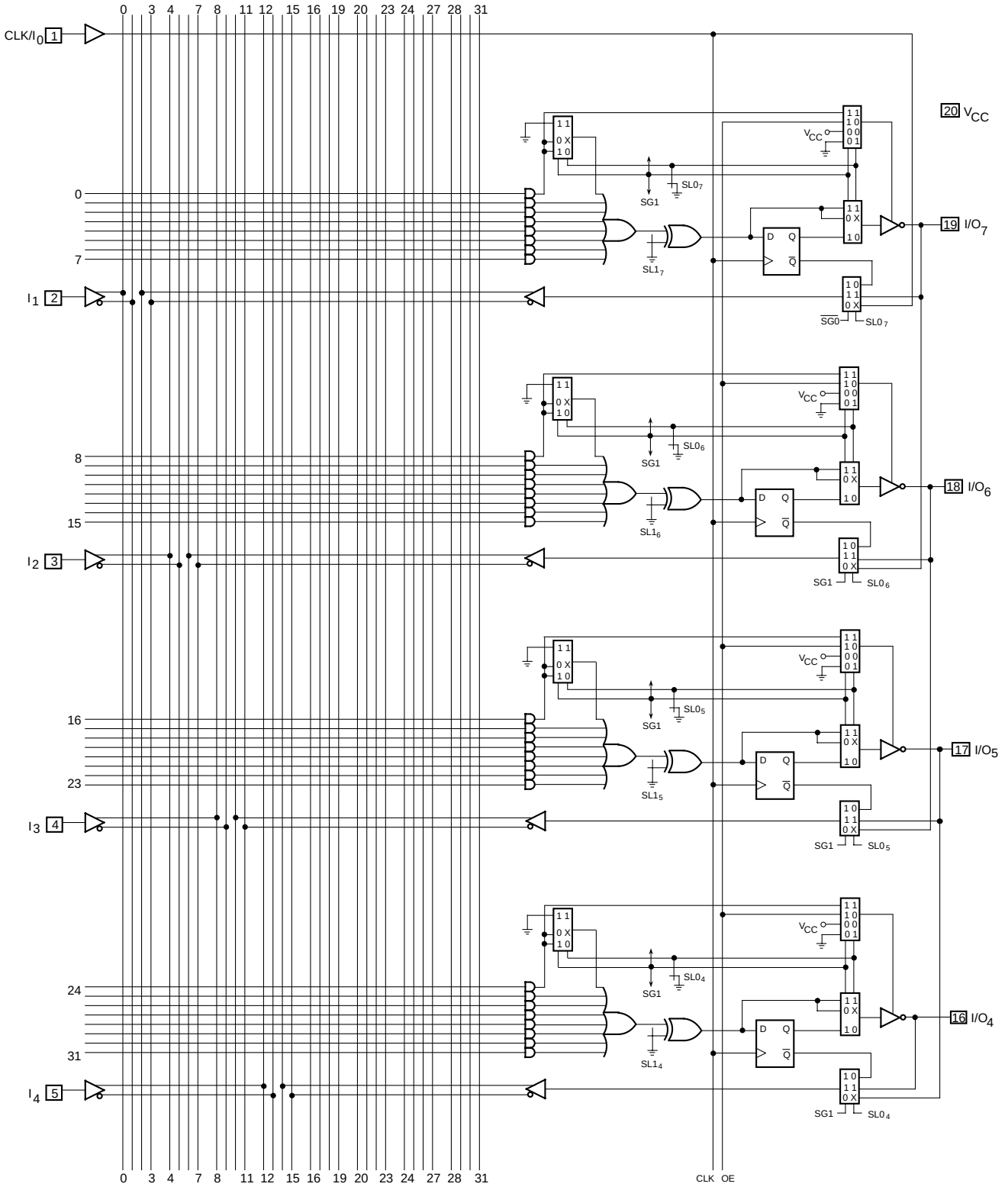
The PALLV16V8Z-20 has the free-running-clock feature. This means that if one or more registers are used, switching only the CLK will not wake up the logic array or any macrocell. The device will not be in standby mode because the CLK buffer will draw some current, but dynamic I_{CC} will typically be less than 2 mA.

Product-Term Disable

On a programmed PALLV16V8Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs. frequency graph, product-term disabling results in considerable power savings. This saving is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in a separate document entitled, *Minimizing Power Consumption with Zero-Power PLDs.*

LOGIC DIAGRAM



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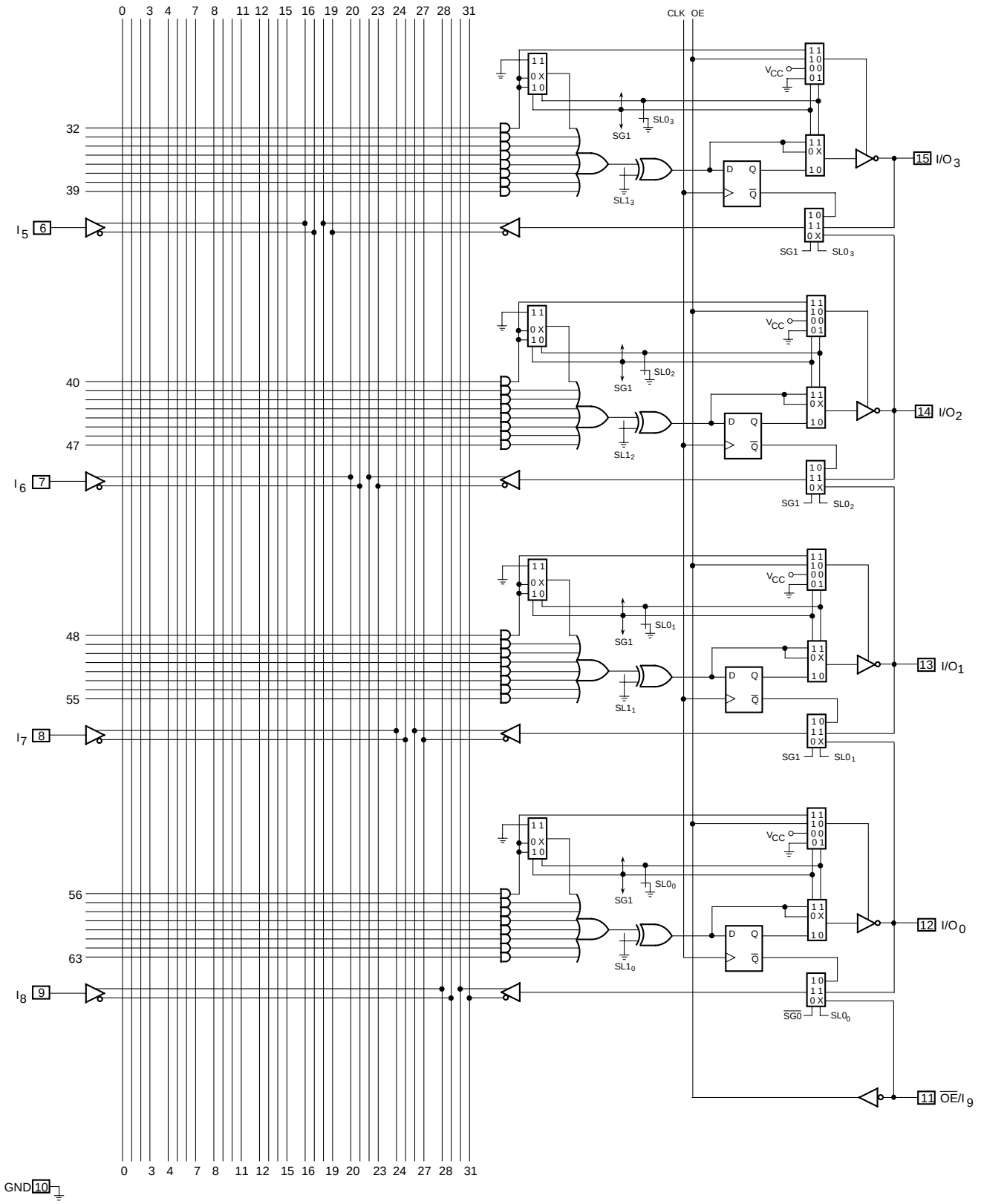
LOGIC DIAGRAM (CONTINUED)



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to 5.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2001 V

Latch-up Current
(T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = –2 mA	2.4		V
			I_{OH} = –75 mA	V_{CC} - 0.2 V		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 2 mA		0.4	V
			I_{OL} = 100 mA		0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = V_{CC}$, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		-50	-130	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz (Note 4)			55	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IL} and I_{OZL}).*
3. *Not more than one output should be shortened at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed worst case under test conditions. Refer to the I_{CC} vs. frequency graph for typical measurements.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} - 3.3 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS OVER COMMERCIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-10		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output (Note 2)				10	ns
t_S	Setup Time from Input or Feedback to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				7	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Notes 2 and 3)	External Feedback	$1/(t_S + t_{CO})$	71.4		MHz
		Internal Feedback (fCNT	$1/(t_S + t_{CF})$	83.3		MHz
		No Feedback	$1/(t_S + t_H)$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				10	ns
t_{EA}	Input to Output Enable Using Product Term Control				12	ns
t_{ER}	Input to Output Disable Using Product Term Control				12	ns

Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - tS.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to 5.5 V

DC Output or I/O
Pin Voltage . . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . . 2001 V

Latch-up Current
(T_A = -40°C to 85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . -40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground. . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = –2 mA	2.4		V
			I_{OH} = –75 µA	V_{CC} – 0.2 V		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 2 mA		0.4	V
			I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = V_{CC}$, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		-15	-75	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz (Note 4)	f = 0 MHz		30	µA
			f = 15 MHz		45	mA

Note:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed worst case under test conditions. Refer to the I_{CC} vs. frequency graph for typical measurements.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

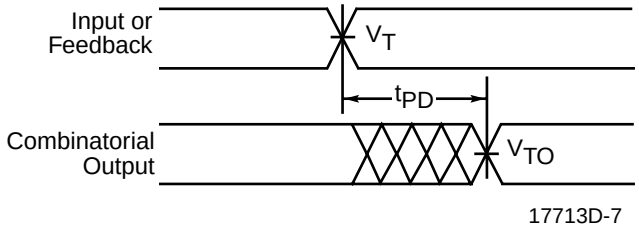
SWITCHING CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGES [1]

Parameter Symbol	Parameter Description			-20		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output (Note 2)				20	ns
t_S	Setup Time from Input or Feedback to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S + t_{CO})$	40		MHz
		Internal Feedback (fCNT)	$1/(t_S + t_{CF})$	50		MHz
		No Feedback	$1/(t_S + t_H)$	66.7		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				20	ns
t_{EA}	Input to Output Enable Using Product Term Control				20	ns
t_{ER}	Input to Output Disable Using Product Term Control				20	ns

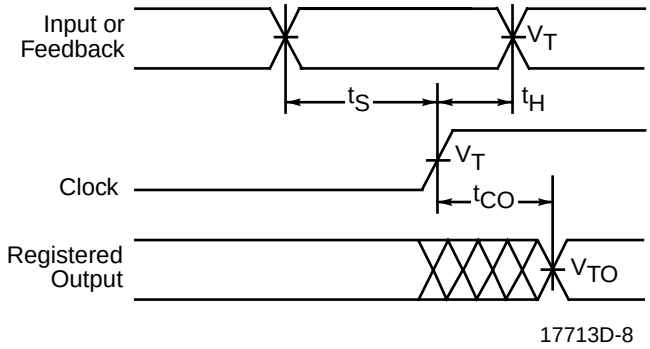
Notes:

1. *See "Switching Test Circuit" for test conditions.*
2. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be about 2 ns faster.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) - t_S.*

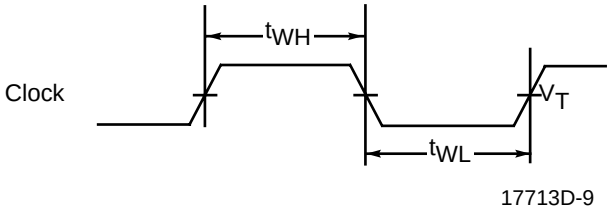
SWITCHING WAVEFORMS



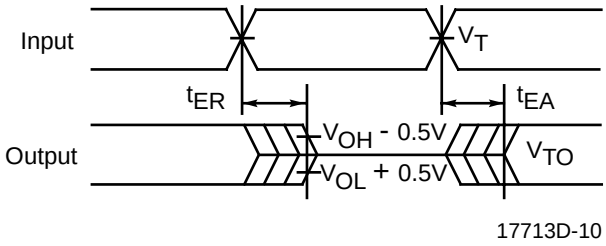
a. Combinatorial output



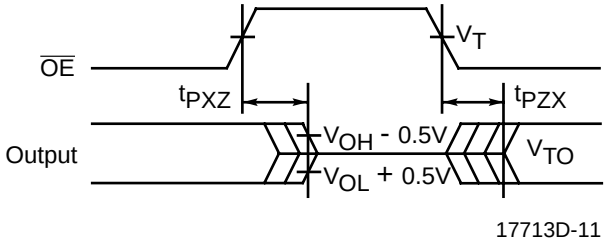
b. Registered output



c. Clock width



d. Input to output disable/enable

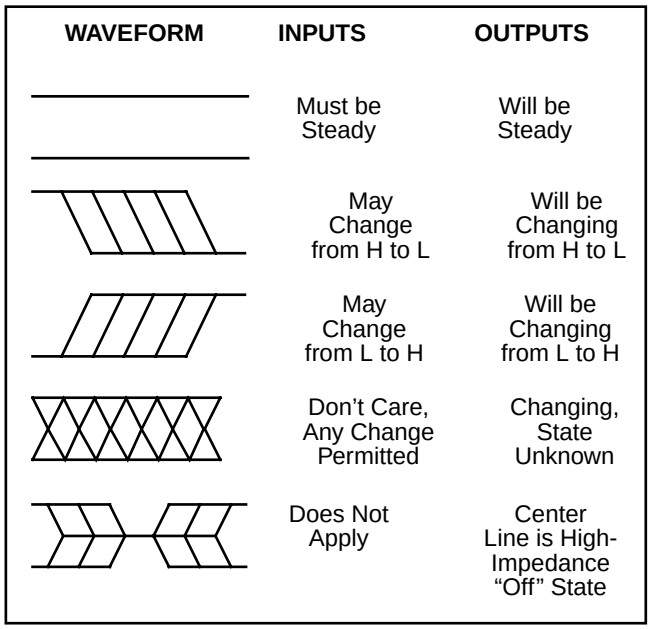


e. $\overline{OE}$ to output disable/enable

Notes:

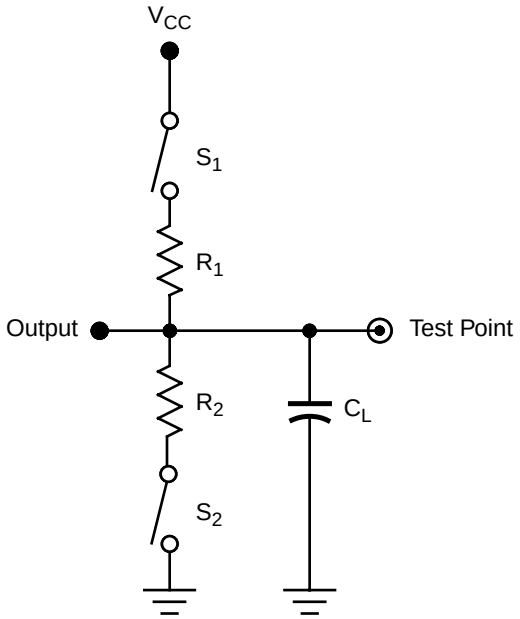
1. *V_T = 1.5 V for input signals and $V_{CC}/2$ for output signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns to 5 ns typical.*

KEY TO SWITCHING WAVEFORM



KS000010-PAL

SWITCHING TEST CIRCUIT



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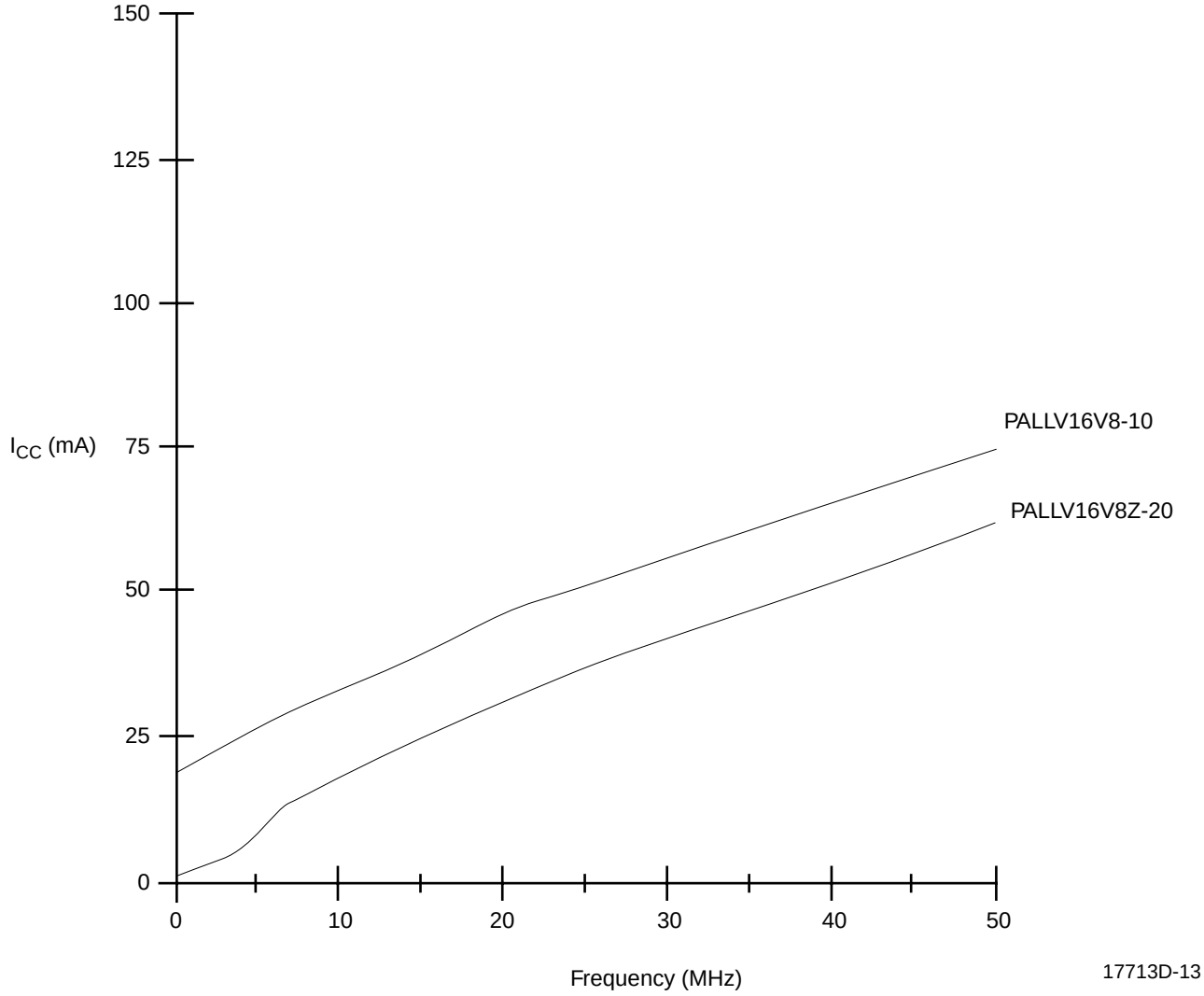
Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	1.6K	1.6K	$V_{CC}/2$
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				$V_{CC}/2$
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 3.3 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

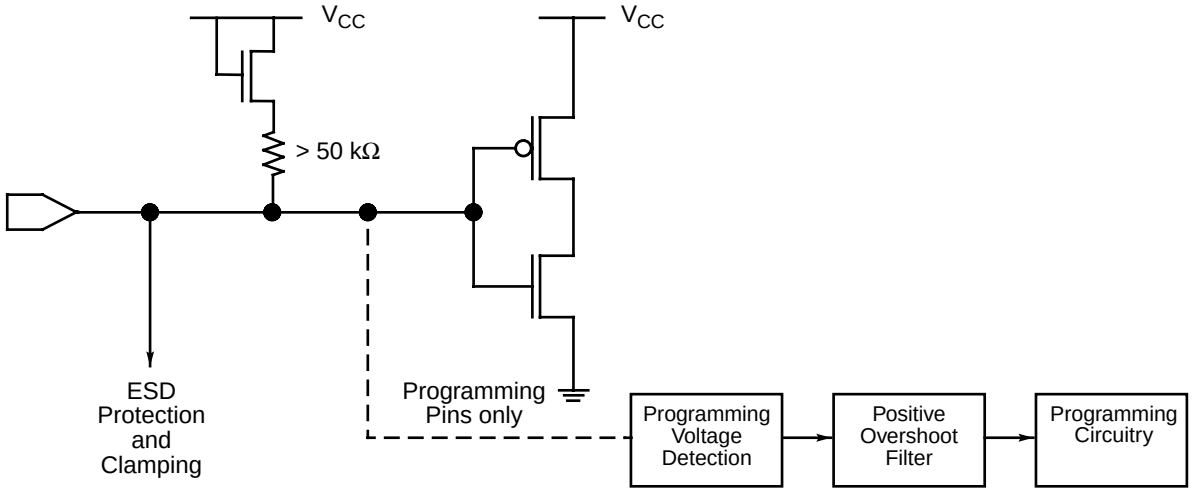
The PALLV16V8 is manufactured using Vantis' advanced electrically-erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, devices can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Value	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Max Reprogramming Cycles	Normal Programming Conditions	100	Cycles

ROBUSTNESS FEATURES

The PALLV16V8 has some unique features that make it extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input

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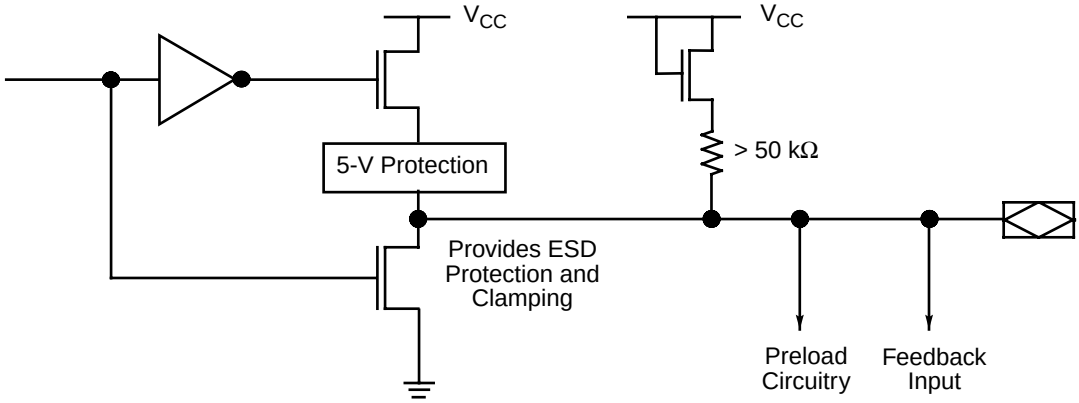

Typical Output

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POWER-UP RESET

The PALLV16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			

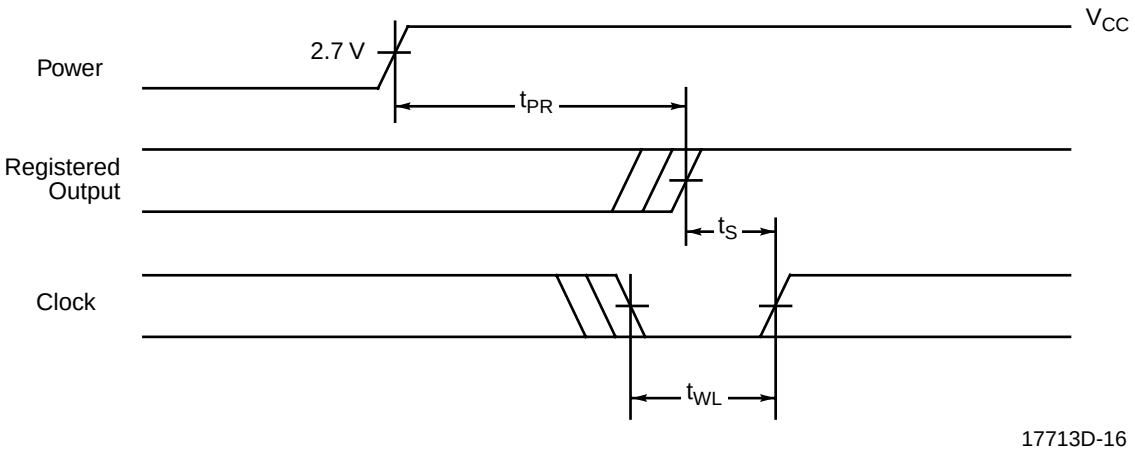


Figure 3. Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

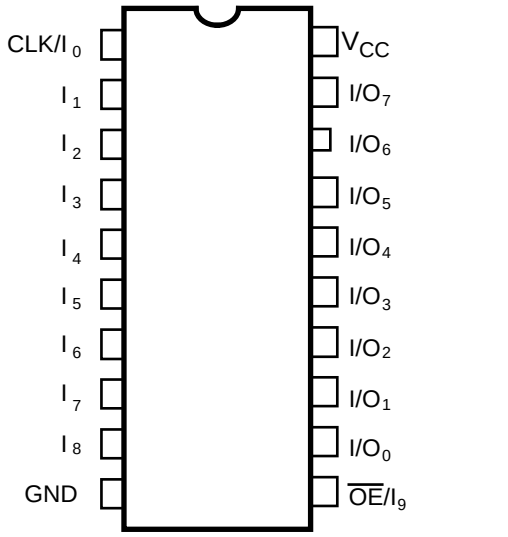
Parameter Symbol	Parameter Description		Typ		Unit
			PDIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		20	19	°C/W
θ_{ja}	Thermal impedance, junction to ambient		65	57	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	58	41	°C/W
		400 lfpm air	51	37	°C/W
		600 lfpm air	47	35	°C/W
		800 lfpm air	44	33	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location ion the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant temperature. Therefore, the measurements can only be used in a similar environment.

CONNECTION DIAGRAMS (TOP VIEW)

DIP/SOIC



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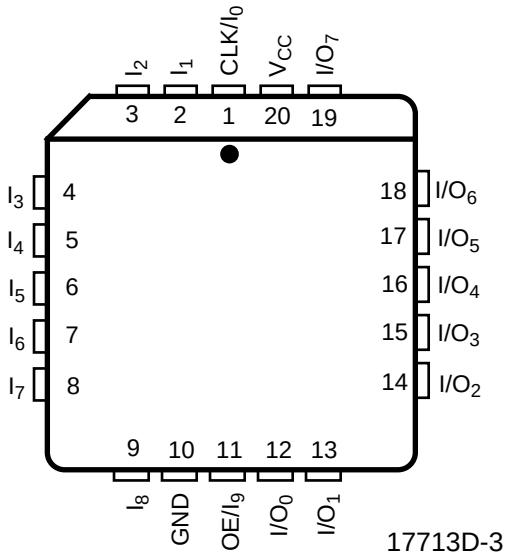
PLCC



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PIN DESIGNATIONS

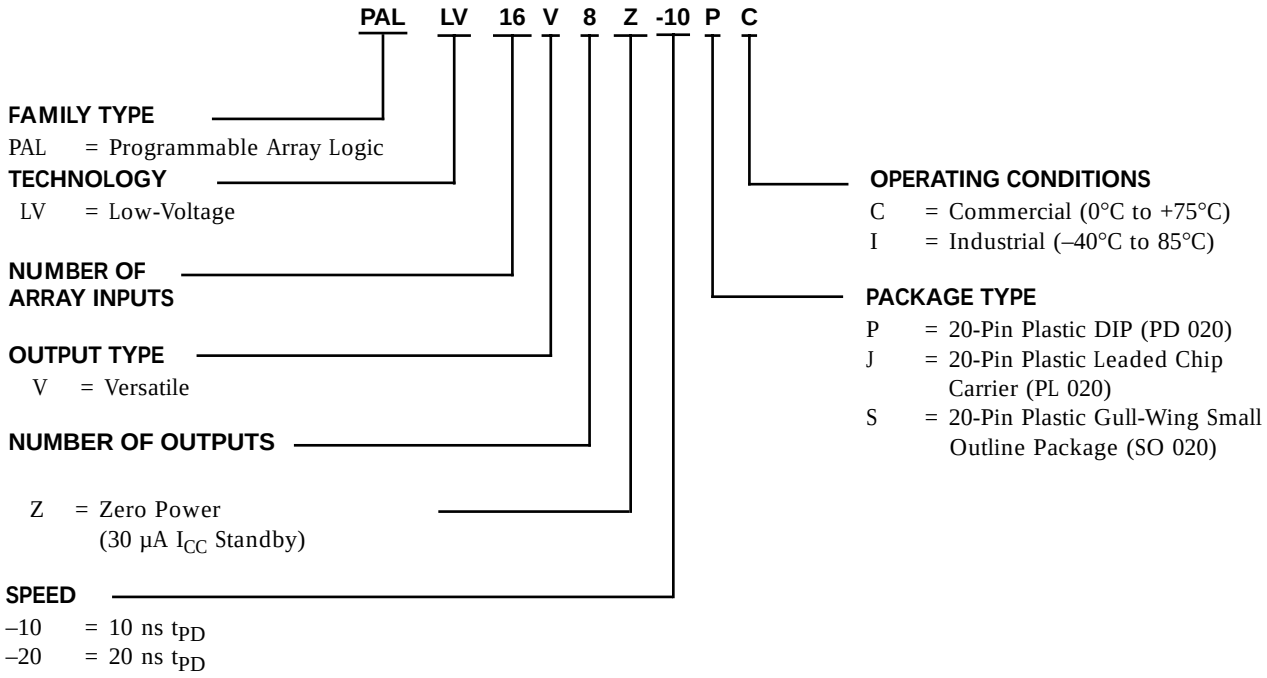
CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage

Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION

Commercial and Industrial Products

Vantis programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALLV16V8-10	PC, JC, SC
PALLV16V8Z-20	PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released