Broadband Modem Mixed Signal Front End

AD9866

FEATURES

Low cost 3.3 V CMOS MxFE™ for broadband modems
12-bit D/A converter
- **2×/4× interpolation filter**
- **200 MSPS DAC update rate**

Integrated 23 dBm line driver with 19.5 dB gain control
12-bit, 80 MSPS A/D converter
−12 dB to +48 dB low noise RxPGA (< 2.5 nV/rtHz)
Third order programmable low-pass filter
Flexible digital data path interface
- **Half- and full-duplex operation**
- **Backward compatible with AD9975 and AD9876**

Various power-down/reduction modes
Internal clock multiplier (PLL)
2 auxiliary programmable clock outputs
Available in 64-lead chip scale package or bare die

APPLICATIONS

Powerline networking
VDSL and HPNA

FUNCTIONAL BLOCK DIAGRAM

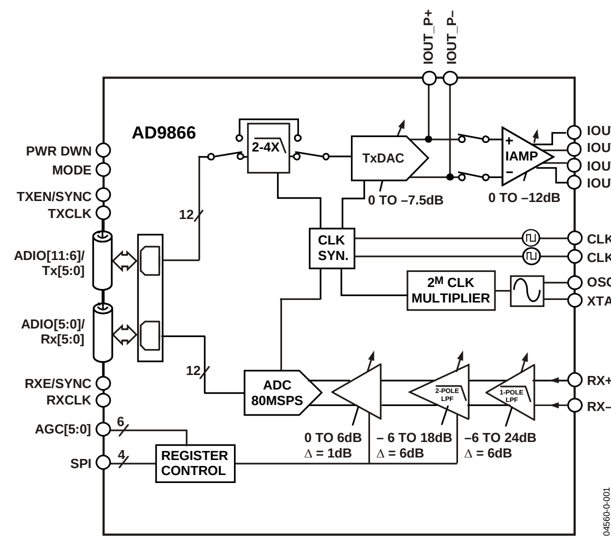

Figure 1.

GENERAL DESCRIPTION

The AD9866 is a mixed-signal front end (MxFE) IC for transceiver applications requiring Tx and Rx path functionality with data rates up to 80 MSPS. Its flexible digital interface, power saving modes, and high Tx-to-Rx isolation make it well suited for half- and full-duplex applications. The digital interface is extremely flexible allowing simple interfaces to digital back ends that support half- or full-duplex data transfers, thus often allowing the AD9866 to replace discrete ADC and DAC solutions. Power saving modes include the ability to reduce power consumption of individual functional blocks or to power down unused blocks in half-duplex applications. A serial port interface (SPI®) allows software programming of the various functional blocks. An on-chip PLL clock multiplier and synthesizer provide all the required internal clocks, as well as two external clocks from a single crystal or clock source.

The Tx signal path consists of a bypassable 2×/4× low-pass interpolation filter, a 12-bit TxDAC, and a line driver. The transmit path signal bandwidth can be as high as 34 MHz at an input data rate of 80 MSPS. The TxDAC provides differential current outputs that can be steered directly to an external load or to an internal low distortion current amplifier. The current amplifier (IAMP) can be configured as a current or voltage mode line driver (with two external npn transistors) capable of delivering in excess of 23 dBm peak signal power. Tx power can be digitally controlled over a 19.5 dB range in 0.5 dB steps.

The receive path consists of a programmable amplifier (RxPGA), a tunable low pass filter (LPF), and a 12-bit ADC. The low noise RxPGA has a programmable gain range of −12 dB to +48 dB in 1 dB steps. Its input referred noise is less than 3.3 nV/rtHz for gain settings beyond 30 dB. The receive path LPF cutoff frequency can either be set over a 15 MHz to 35 MHz range or simply bypassed. The 12-bit ADC achieves excellent dynamic performance over a 5 MSPS to 80 MSPS span. Both the RxPGA and the ADC offer scalable power consumption allowing power/performance optimization.

The AD9866 provides a highly integrated solution for many broadband modems. It is available in a space-saving 64-lead chip scale package and is specified over the commercial (−40°C to +85°C) temperature range.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

TX PATH SPECIFICATIONS

Table 1. AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%; f_{OSCIN} = 50 MHz, f_{DAC} = 200 MHz, R_{SET} = 2.0 kΩ, unless otherwise noted

Parameter	Temp	Test Level	Min	Typ	Max	Unit
TxDAC DC CHARACTERISTICS						
Resolution	Full			12		Bits
Update Rate	Full	II			200	MSPS
Full-Scale Output Current (IOUTP_FS)	Full	IV	2		25	mA
Gain Error[1]	25°C	I		±2		% FS
Offset Error	25°C	V		2		uA
Voltage Compliance Range	Full		−1		+1.5	V
TxDAC GAIN CONTROL CHARACTERISTICS						
Minimum Gain	25°C	V		−7.5		dB
Maximum Gain	25°C	V		0		dB
Gain Step Size	25°C	V		0.5		dB
Gain Step Accuracy	25°C	IV		Monotonic		
Gain Range Error	25°C	V		±2		dB
TxDAC AC CHARACTERISTICS[2]						
Fundamental				0.5		dBm
Signal-to-Noise and Distortion	Full	IV	66.6	69.2		dBc
Signal-to-Noise Ratio	Full	IV	68.4	69.8		dBc
THD	Full	IV		−79	−68.7	dBc
SFDR	Full	IV	68.5	81		dBc
IAMP DC CHARACTERISTICS						
IOUTN Full-Scale Current = IOUTN+ + IOUTN−	Full	IV	2		105	mA
IOUTG Full-Scale Current = IOUTG+ + IOUTG−	Full	IV	2		150	mA
AC Voltage Compliance Range	Full	IV	1		7	V
IAMPN AC CHARACTERISTICS[3]						
Fundamental	25°C			13		dBm
IOUTN SFDR (Third Harmonic)	Full	IV	43.3	45.2		dBc
IAMP GAIN CONTROL CHARACTERISTICS						
Minimum Gain	25°C	V		−19.5		dB
Maximum Gain	25°C	V		0		dB
Gain Step Size	25°C	V		0.5		dB
Gain Step Accuracy	25°C	IV		Monotonic		dB
IOUTN Gain Range Error	25°C	V		0.5		dB
REFERENCE						
Internal Reference Voltage[4]	25°C	I		1.23		V
Reference Error	Full	V		0.7	3.4	%
Reference Drift	Full	V		30		ppm/°C
Tx DIGITAL FILTER CHARACTERISTICS (2× INTERPOLATION)						
Latency (Relative to 1/ F_{DAC})	Full	V		43		Cycles
−0.2 dB Bandwidth	Full	V		0.2187		f_{OUT}/f_{DAC}
−3 dB Bandwidth	Full	V		0.2405		f_{OUT}/f_{DAC}
Stop-Band Rejection (0.289 F_{DAC} to 0.711 F_{DAC})	Full	V		50		dB
Tx DIGITAL FILTER CHARACTERISTICS (4× Interpolation)						
Latency (Relative to 1/ F_{DAC})	Full	V		96		Cycles
−0.2 dB Bandwidth	Full	V		0.1095		f_{OUT}/f_{DAC}

Parameter	Temp	Test Level	Min	Typ	Max	Unit
−3 dB Bandwidth	Full	V		0.1202		f_{OUT}/f_{DAC}
Stop Band Rejection (0.289 f_{OSCIN} to 0.711 f_{OSCIN})	Full	V		50		dB
PLL CLK MULTIPLIER						
OSCIN Frequency Range	Full	IV	5		80	MHz
Internal VCO Frequency Range	Full	IV	20		200	MHz
Duty Cycle	Full	II	40		60	%
OSCIN Impedance	25°C	V		100//3		MΩ//pF
CLKOUT1 Jitter[5]	25°C	III		12		ps rms
CLKOUT2 Jitter[6]	25°C	III		6		ps rms
CLKOUT1 and CLKOUT2 Duty Cycle[7]	Full	III	45		55	%

[1] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.23 V external reference and a 1 V p-p differential analog input).
[2] TxDAC IOUTFS = 20 mA, differential output with 1:1 transformer with source and load termination of 50 Ω, F_{OUT} = 5 MHz, 4× interpolation.
[3] IOUN full-scale current = 80 mA, f_{OSCIN}= 80 MHz, f_{DAC}=160 MHz, 2× interpolation.
[4] Use external amplifier to drive additional load.
[5] Internal VCO operates at 200 MHz , set to divide-by-1.
[6] Because CLKOUT2 is a divided down version of OSCIN, its jitter is typically equal to OSCIN.
[7] CLKOUT2 is an inverted replica of OSCIN, if set to divide-by-1.

RX PATH SPECIFICATIONS

Table 2. AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%; half- or full-duplex operation with CONFIG = 0 default power bias settings, unless otherwise noted

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Rx INPUT CHARACTERISTICS						
Input Voltage Span (RxPGA gain = −10 dB)	Full	III		6.33		V p-p
Input Voltage Span (RxPGA gain = +48 dB)	Full	III		8		mV p-p
Input Common-Mode Voltage	25°C	III		1.3		V
Differential Input Impedance	25°C	III		400 4.0		Ω pF
Input Bandwidth (with RxLPF Disabled, RxPGA = 0 dB)	25°C	III		53		MHz
Input Voltage Noise Density (RxPGA Gain = 36 dB, $f_{-3\ dBF}$ = 26 MHz)	25°C	III		2.7		nV/rtHz
Input Voltage Noise Density (RxPGA Gain = 48 dB, $f_{-3\ dBF}$ = 26 MHz)	25°C	III		2.4		nV/rtHz
RxPGA CHARACTERISTICS						
Minimum Gain	25°C	III		−12		dB
Maximum Gain	25°C	III		48		dB
Gain Step Size	25°C	III		1		dB
Gain Step Accuracy	25°C	III		Monotonic		dB
Gain Range Error	25°C	III		0.5		dB
RxLPF CHARACTERISTICS						
Cutoff Frequency ($f_{-3\ dBF}$) range	Full	III	15		35	MHz
Attenuation at 55.2 MHz with $f_{-3\ dBF}$ = 21 MHz	25°C	III		20		dB
Pass-Band Ripple	25°C	III		±1		dB
Settling Time to 5 dB RxPGA Gain Step @ f_{ADC} = 50 MSPS	25°C	III		20		ns
Settling Time to 60 dB RxPGA Gain Step @ f_{ADC} = 50 MSPS	25°C	III		100		ns
ADC DC CHARACTERISTICS						
Resolution	NA	NA		12		Bits
Conversion Rate	FULL	II	5		80	MSPS
RX PATH LATENCY[1]						
Full-Duplex Interface	Full	V		10.5		Cycles
Half-Duplex Interface	Full	V		10.0		Cycles

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Rx PATH COMPOSITE AC PERFORMANCE @ f_{ADC} = 50 MSPS[2]						
RxPGA Gain = 48 dB (Full-Scale = 8.0 mV p-p)						
Signal-to-Noise and Distortion (SNR)	25°C	III		43.7		dBc
Total Harmonic Distortion (THD)	25°C	III		−71		dBc
RxPGA Gain = 24 dB (Full-Scale = 126 mV p-p)						
Signal-to-Noise (SNR)	25°C	III		63.1		dBc
Total Harmonic Distortion (THD)	25°C	III		−67.2		dBc
RxPGA Gain = 0 dB (Full-Scale = 2.0 V p-p)						
Signal-to-Noise and Distortion (SINAD)	Full	IV		64.3		dBc
Total Harmonic Distortion (THD)	Full	IV		−67.3		dBc
Rx PATH COMPOSITE AC PERFORMANCE @ f_{ADC} = 80 MSPS[3]						
RxPGA Gain = 48 dB (Full-Scale = 8.0 m V p-p)						
Signal-to-Noise (SNR)	25°C	III		41.8		dBc
Total Harmonic Distortion (THD)	25°C	III		−67		dBc
RxPGA Gain = 24 dB (Full-Scale = 126 m V p-p)						
Signal-to-Noise (SNR)	25°C	III		58.6		dBc
Total Harmonic Distortion (THD)	25°C	III		−62.9		dBc
RxPGA Gain = 0 dB (Full-Scale = 2.0 V p-p)						
Signal-to-Noise (SNR)	25°C	II	61.1	62.9		dBc
Total Harmonic Distortion (THD)	25°C	II		−70.8	−60.8	dBc
Rx-to-Tx PATH FULL-DUPLEX ISOLATION						
(1 V p-p, 10 MHz Sine Wave Tx Output)						
RxPGA Gain = 40 dB						
IOUTP± Pins to RX± Pins	25°C	III		83		dBc
IOUTG± Pins to RX± Pins	25°C	III		37		dBc
RxPGA Gain = 0 dB						
IOUTP± Pins to RX± Pins	25°C	III		123		dBc
IOUTG± Pins to RX± Pins	25°C	III		77		dBc

[1]Includes RxPGA, ADC pipeline, and ADIO bus delay relative to f_{ADC}.
[2]f_{IN} = 5 MHz, AIN = −1.0 dBFS , LPF cut-off frequency set to 15.5 MHz with Reg. 0x08 = 0x80.
[3]f_{IN} = 5 MHz, AIN = −1.0 dBFS , LPF cut-off frequency set to 26 MHz with Reg. 0x08 = 0x80.

POWER SUPPLY SPECIFICATIONS

Table 3. AVDD = 3.3 V, DVDD = CLKVDD = DRVDD = 3.3 V; R_{SET} = 2 kΩ, full-duplex operation with f_{DATA} = 80 MSPS,[1] unless otherwise noted

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SUPPLY VOLTAGES						
AVDD	Full	V	3.135	3.3	3.465	V
CLKVDD	Full	V	3.0	3.3	3.6	V
DVDD	Full	V	3.0	3.3	3.6	V
DRVDD	Full	V	3.0	3.3	3.6	V
IS_TOTAL (Total Supply Current)	Full	II		406	475	mA
POWER CONSUMPTION						
I_{AVDD} + I_{CLKVDD} (Analog Supply Current)		IV		311	342	mA
I_{DVDD} + I_{DRVDD} (Digital Supply Current)	Full	IV		95	133	mA
POWER CONSUMPTION (Half-Duplex Operation with f_{DATA} = 50 MSPS)[2]						
Tx Mode						
I_{AVDD} + I_{CLKVDD}	25°C	IV		112	130	mA
I_{DVDD} + I_{DRVDD}	25°C	IV		46	49.5	mA

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Rx Mode						
$I_{AVDD} + I_{CLKVDD}$	25°C			225	253	mA
$I_{DVDD} + I_{DRVDD}$	25°C			36.5	39	mA
POWER CONSUMPTION OF FUNCTIONAL BLOCKS[1] ($I_{AVDD} + I_{CLKVDD}$)						
RxPGA and LPF	25°C	III		87		mA
ADC	25°C	III		108		mA
TxDAC	25°C	III		38		mA
IAMP (Programmable)	25°C	III	10		120	mA
Reference	25°C	III		170		mA
CLK PLL and Synthesizer	25°C	III		107		mA
MAXIMUM ALLOWABLE POWER DISSIPATION	Full	IV			1.66	W
STANDBY POWER CONSUMPTION						
IS_TOTAL (Total Supply Current)	Full			13		mA
POWER DOWN DELAY (USING PWR_DWN PIN)						
RxPGA and LPF	25°C	III		440		ns
ADC	25°C	III		12		ns
TxDAC	25°C	III		20		ns
IAMP	25°C	III		20		ns
CLK PLL and Synthesizer	25°C	III		27		ns
POWER UP DELAY (USING PWR_DWN PIN)						
RxPGA and LPF	25°C	III		7.8		μs
ADC	25°C	III		88		ns
TxDAC	25°C	III		13		μs
IAMP	25°C	III		20		ns
CLK PLL and Synthesizer	25°C	III		20		μs

[1]Default power-up settings for MODE = HIGH and CONFIG = LOW, IOUTP_FS = 20 mA, does not include IAMP's current consumption, which is application dependent.
[2]Default power-up settings for MODE = LOW and CONFIG = LOW .

DIGITAL SPECIFICATIONS

Table 4. AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%; R_{SET} = 2 kΩ, unless otherwise noted

Parameter	Temp	Test Level	Min	Typ	Max	Unit
CMOS LOGIC INPUTS						
High Level Input Voltage	Full	VI	DRVDD – 0.7			V
Low Level Input Voltage	Full	VI			0.4	V
Input Leakage Current					12	μA
Input Capacitance	Full	VI		3		pF
CMOS LOGIC OUTPUTS (C_{LOAD} = 5 pF)						
High Level Output Voltage (I_{OH} = 1 mA)	Full	VI	DRVDD – 0.7			
Low Level Output Voltage (I_{OH} = 1 mA)	Full	VI	1.2	2		
Output Rise/Fall Time (High Strength Mode and C_{LOAD} = 15 pF)	Full	VI		1.5/2.3		ns
Output Rise/Fall Time (Low Strength Mode and C_{LOAD} = 15 pF)	Full	VI		1.9/2.7		ns
Output Rise/Fall Time (High Strength Mode and C_{LOAD} = 5 pF)	Full	VI		0.7/0.7		ns
Output Rise/Fall Time (Low Strength Mode and C_{LOAD} = 5 pF)	Full	VI		1.0/1.0		ns
RESET						
Minimum Low Pulse Width (Relative to f_{ADC})			1			Clock cycles

SERIAL PORT TIMING SPECIFICATIONS

Table 5. AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, unless otherwise noted

Parameter	Temp	Test Level	Min	Typ	Max	Unit
WRITE OPERATION (See Figure 46)						
SCLK Clock Rate (f_{SCLK})	Full	IV			32	MHz
SCLK Clock High (t_{HI})	Full	IV	14			ns
SCLK Clock Low (t_{LOW})	Full	IV	14			ns
SDIO to SCLK Setup Time (t_{DS})	Full	IV	14			ns
SCLK to SDIO Hold Time (t_{DH})	Full	IV	0			ns
$\overline{\text{SEN}}$ to SCLK Setup Time (t_S)	Full	IV	14			ns
SCLK to $\overline{\text{SEN}}$ Hold Time (t_H)	Full	IV	0			ns
READ OPERATION (See Figure 47 and Figure 48)						
SCLK Clock Rate (f_{SCLK})	Full	IV			32	MHz
SCLK Clock High (t_{HI})	Full	IV	14			ns
SCLK Clock Low (t_{LOW})	Full	IV	14			ns
SDIO to SCLK Setup Time (t_{DS})	Full	IV	14			ns
SCLK to SDIO Hold Time (t_{DH})	Full	IV	0			ns
SCLK to SDIO (or SDO) Data Valid Time (t_{DV})	Full	IV			14	ns
$\overline{\text{SEN}}$ to SDIO Output Valid to Hi-Z (t_{EZ})	Full	IV		2		ns

HALF-DUPLEX DATA INTERFACE (ADIO PORT) TIMING SPECIFICATIONS

Table 6. AVDD = 3.3 V ±5%, DVDD = CLKVDD = DRVDD = 3.3 V ±10%, unless otherwise noted

Parameter	Temp	Test Level	Min	Typ	Max	Unit
READ OPERATION (See Figure 50)						
Output Data Rate	Full	II	5		80	MSPS
Three-State Output Enable Time (t_{PZL})	Full	II	80			ns
Three-State Output Disable Time (t_{PLZ})	Full	II	3			ns
Rx Data Valid Time (t_{DV})	Full	II	3			ns
Rx Data Output Delay (t_{OD})	Full	II	4			ns
WRITE OPERATION (See Figure 49)						
Input Data Rate (1× Interpolation)	Full	II	20		80	MSPS
Input Data Rate (2× Interpolation)	Full	II	10		80	MSPS
Input Data Rate (4× Interpolation)	Full	II	5		50	MSPS
Tx Data Setup Time (t_{DS})	Full	II	12.5			ns
Tx Data Hold Time (t_{DH})	Full	II	0			ns
Latch Enable Time (t_{EN})	Full	II	3			ns
Latch Disable Time (t_{DIS})	Full	II	3			ns

FULL-DUPLEX DATA INTERFACE (Tx AND Rx PORT) TIMING SPECIFICATIONS

Table 7. AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, unless otherwise noted

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Tx PATH INTERFACE (See Figure 53)						
Input Nibble Rate (2× Interpolation)	Full	II	20		160	MSPS
Input Nibble Rate (4× Interpolation)	Full	II	10		100	MSPS
Tx Data Setup Time (t_{DS})	Full	II	3			ns
Tx Data Hold Time (t_{DH})	Full	II	1			ns
Rx PATH INTERFACE (See Figure 54)						
Output Nibble Rate	Full	II	10		160	MSPS
Rx Data Valid Time (t_{DV})	Full	II	3			ns
Rx Data Hold Time (t_{DH})	Full	II	0			ns

Explanation of Test Levels

I: 100% production tested.

II: 100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.

III: Sample tested only.

IV: Parameter is guaranteed by design and characterization testing.

V: Parameter is a typical value only.

VI: 100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
ELECTRICAL	
AVDD, CLKVDD Voltage	3.9 V max
DVDD, DRVDD Voltage	3.9 V max
RX+, RX−, REFT, REFB	−0.3 V to AVDD + 0.3 V
IOUTP+, IOUTP−	−1.5 V to AVDD + 0.3 V
IOUTN+, IOUTN−, IOUTG+, IOUTG−	−0.3 V to 7 V
OSCIN, XTAL	−0.3 V to CLVDD + 0.3 VS
REFIO, REFADJ	−0.3 V to AVDD + 0.3 V
Digital Input and Output Voltage	−0.3 V to DRVDD + 0.3 V
Digital Output Current	5 mA max
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	125°C
Lead Temperature (Soldering, 10 s)	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance: 64-lead LFCSP (4-layer board).

θ_{JA} = 24°C/W (paddle soldered to ground plane, 0 LPM air).

θ_{JA} = 30.8°C/W (paddle *not* soldered to ground plane, 0 LPM air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

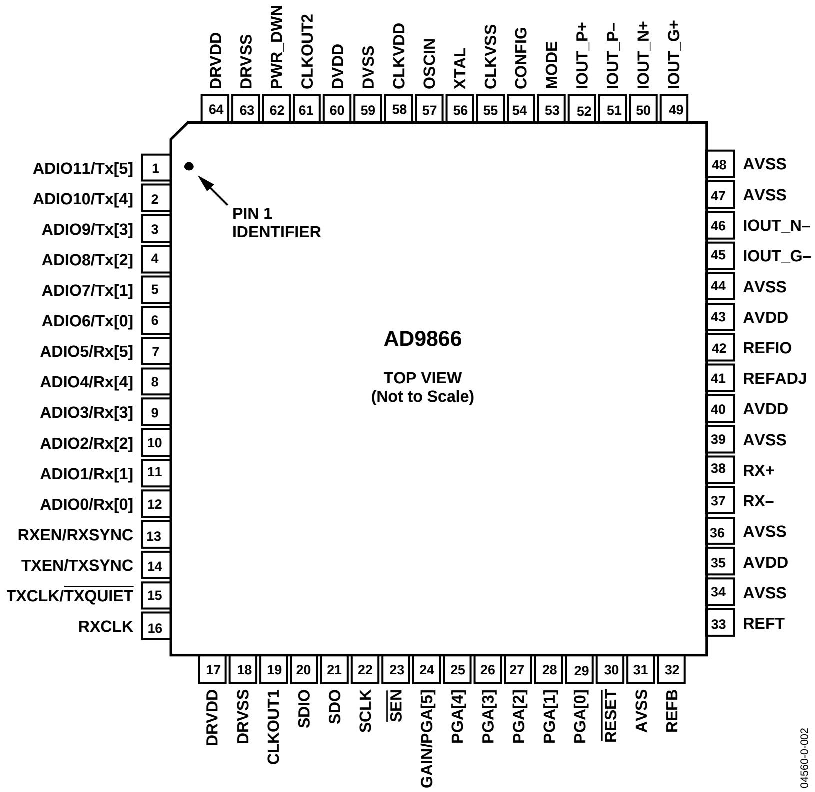

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Mode[1]	Pin Function
1	ADIO11	HD	MSB of ADIO Buffer
	Tx[5]	FD	MSB of Tx Nibble Input
2–5	ADIO10–7	HD	Bits 10–7 of ADIO Buffer
	Tx[4–1]	FD	Bits 4–1 of Tx Nibble Input
6	ADIO6	HD	Bit 6 of ADIO Buffer
	Tx[0]	FD	LSB of Tx Nibble Input
7	ADIO5	HD	Bit 5 of ADIO Buffer
	Rx[5]	FD	MSB of Rx Nibble Output
8, 9	ADIO4–3	HD	Bits 4–3 of ADIO Buffer
	Rx[4–3]	FD	Bits 4–3 of Rx Nibble Output
10	ADIO2	HD	Bit 2 of ADIO Buffer
	Rx[2]	FD	Bit 2 of Rx Nibble Output
11	ADIO1	HD	Bit 1 of ADIO Buffer
	Rx[1]	FD	Bit 1 of Rx Nibble Output
12	ADIO0	HD	LSB of ADIO Buffer
	Rx[0]	FD	LSB of Rx Nibble Output
13	RXEN	HD	ADIO Buffer Control Input
	RXSYNC	FD	Rx Data Synchronization Output
14	TXEN	HD	Tx Path Enable Input
	TXSYNC	FD	Tx Data Synchronization Input
15	TXCLK	HD	ADIO Sample Clock Input
	$\overline{\text{TXQUIET}}$	FD	Fast TxDAC/IAMP Power-Down

Pin No.	Mnemonic	Mode[1]	Pin Function
16	RXCLK	HD FD	ADIO Request Clock Input Rx and Tx Clock Output at 2 × f_{ADC}
17, 64	DRVDD		Digital Output Driver Supply Input
18, 63	DRVSS		Digital Output Driver Supply Return
19	CLKOUT1		f_{DAC}/N Clock Output (L = 1, 2, 4, or 8)
20	SDIO		Serial Port Data Input/Output
21	SDO		Serial Port Data Output
22	SCLK		Serial Port Clock Input
23	$\overline{\text{SEN}}$		Serial Port Enable Input
24	GAIN PGA[5]	FD HD or FD	Tx Data Port (Tx[5:0]) Mode Select MSB of PGA Input Data Port
25–29	PGA[4–0]	HD or FD	Bits 4–0 of PGA Input Data Port
30	$\overline{\text{RESET}}$		Reset Input (Active Low)
31, 34, 36, 39 44, 47, 48	AVSS		Analog Ground
32, 33	REFB, REFT		ADC Reference Decoupling Nodes
35, 40, 43	AVDD		Analog Power Supply Input
37, 38	RX−, RX+		Receive Path – and + Analog Inputs
41	REFADJ		TxDAC Full-Scale Current Adjust
42	REFIO		TxDAC Reference Input/Output
45	IOUT_G−		−Tx Amp Current Output_Sink
46	IOUT_N−		−Tx Mirror Current Output_Sink
49	IOUT_G+		+Tx Amp Current Output_Sink
50	IOUT_N+		+Tx Mirror Current Output_Sink
51	IOUT_P−		−TxDAC Current Output_Source
52	IOUT_P+		+TxDAC Current Output_Source
53	MODE		Digital Interface Mode Select Input LOW = HD, HIGH = FD
54	CONFIG		Power-Up SPI Register Default Setting Input
55	CLKVSS		Clock Osc./Synthesizer Supply Return
56	XTAL		Crystal Osc. Inverter Output
57	OSCIN		Crystal Osc. Inverter Input
58	CLKVDD		Clock Osc./Synthesizer Supply
59	DVSS		Digital Supply Return
60	DVDD		Digital Supply Input
61	CLKOUT2		f_{OSCIN}/L Clock Output, (L = 1, 2, or 4)
62	PWR_DWN		Power-Down Input

[1]HD = half-duplex mode; FD = full-duplex mode.

TYPICAL PERFORMANCE CHARACTERISTICS

Rx PATH TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, f_{OSCIN} = f_{ADC} = 50 MSPS, low-pass filter's $f_{-3\,dB}$ = 22 MHz, AIN = −1 dBFS, RIN = 50 Ω, half- or full-duplex interface, default power bias settings

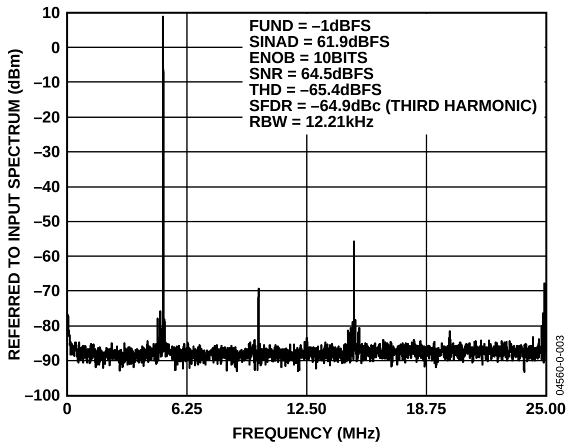

Figure 3. Spectral Plot with 4k FFT of Input Sinusoid with RxPGA = 0 dB and P_{IN} = 9 dBm

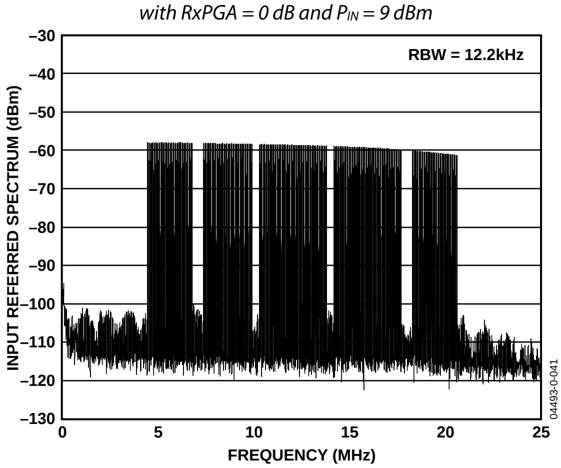

Figure 4. Spectral Plot with 4k FFT of 84-Carrier DMT Signal with PAR = 10.2 dB, P_{IN} = −33.7 dBm, and RxPGA = 36 dB

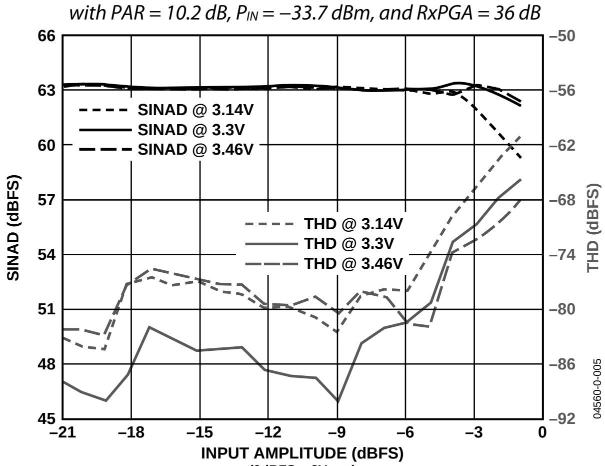

Figure 5. SINAD and THD vs. Input Amplitude and Supply (f_{IN} = 8 MHz, LPF $f_{-3\,dB}$ = 26 MHz; Rx PGA = 0 dB)

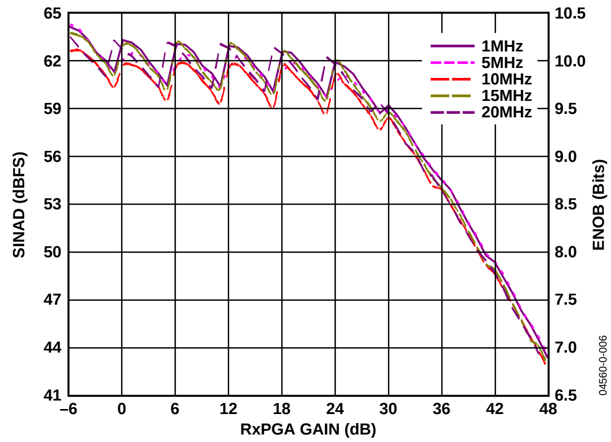

Figure 6. SINAD/ENOB vs. RxPGA Gain and Frequency

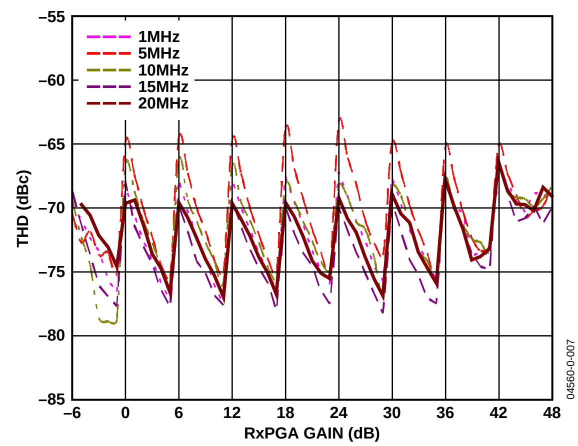

Figure 7. THD vs. RxPGA Gain and Frequency

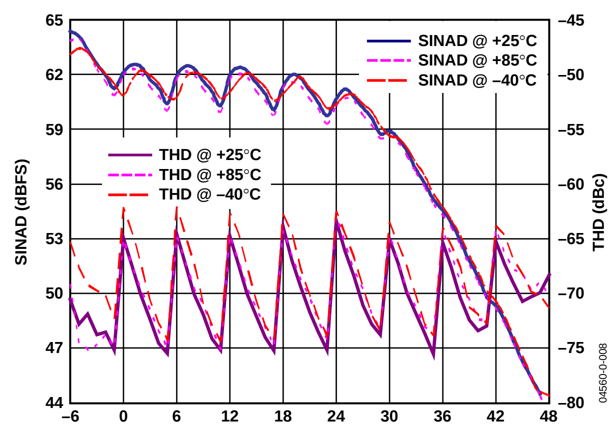

Figure 8. SINAD/THD Performance vs. RxPGA Gain and Temperature (f_{IN} = 5 MHz)

Rx Path Typical Performance Characteristics:
AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, f_{OSCIN} = f_{ADC} = 80 MSPS, low-pass filter's $f_{-3\,dB}$ = 30 MHz, AIN = −1 dBFS, RIN = 50 Ω, half- or full-duplex interface, default power bias settings

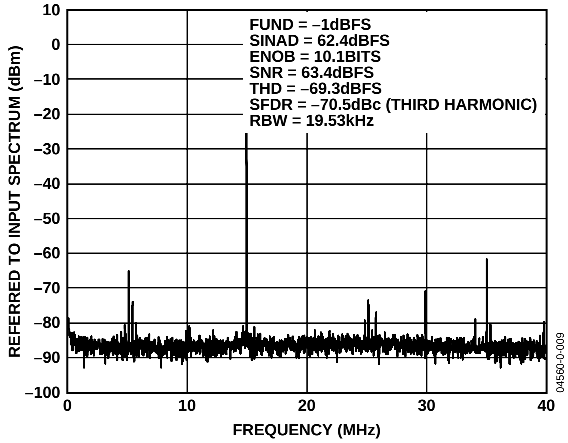

Figure 9. Spectral Plot with 4k FFT of Input Sinusoid with RxPGA = 0 dB and P_{IN} = 9 dBm

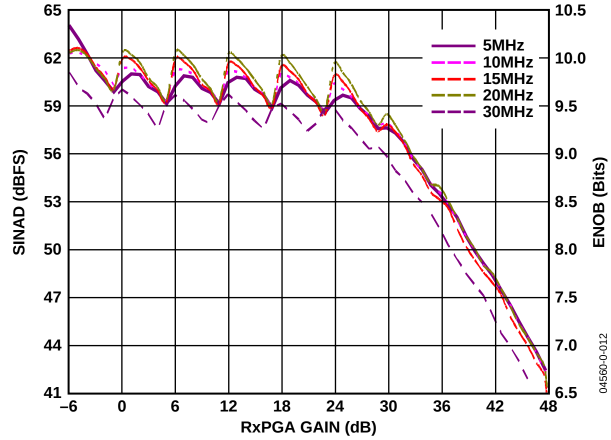

Figure 12. SINAD/ENOB vs. RxPGA Gain and Frequency

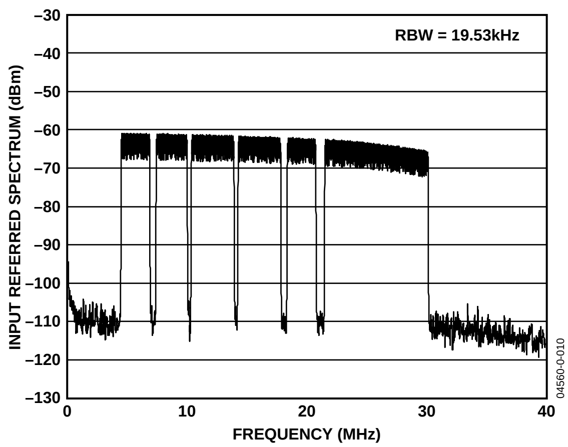

Figure 10. Spectral Plot with 4K FFT of 111-Carrier DMT Signal with PAR = 11 dB, P_{IN} = −33.7 dBm, LPF's $f_{-3\,dB}$ = 32 MHz and RxPGA = 36 dB

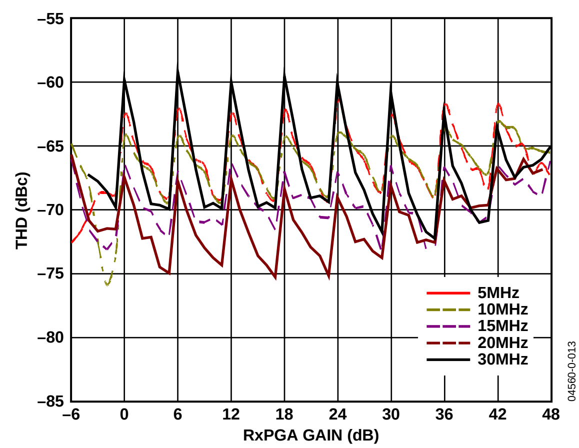

Figure 13. THD vs. RxPGA Gain and Frequency

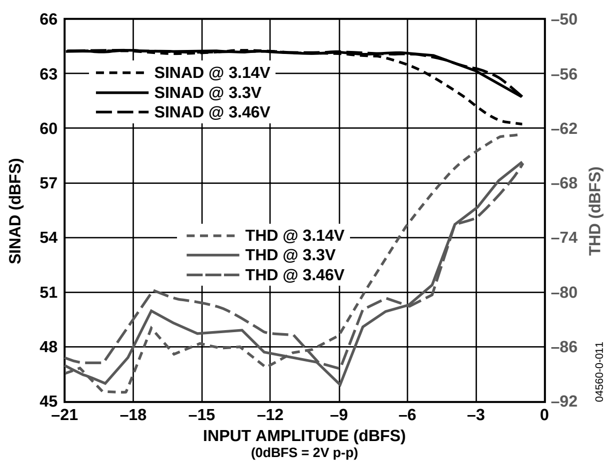

Figure 11. SINAD and THD vs. Input Amplitude and Supply (f_{IN} = 8 MHz, LPF $f_{-3\,dB}$ = 26 MHz; RxPGA = 0 dB)

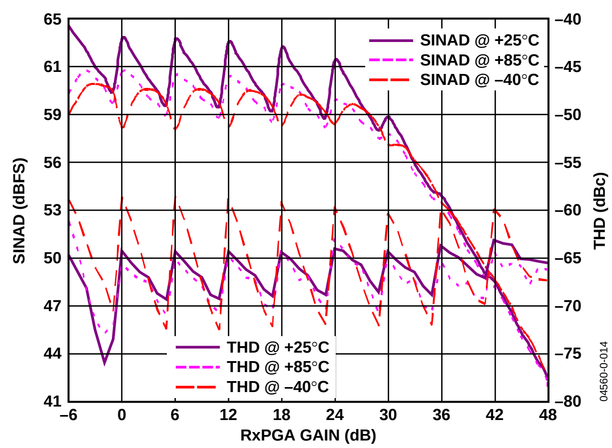

Figure 14. SINAD/THD Performance vs. RxPGA Gain and Temperature (f_{IN} = 10 MHz)

Rx Path Typical Performance Characteristics:
AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, f_{OSCIN} = f_{ADC} = 80 MSPS, low-pass filter's $f_{-3\ dB}$ = 30 MHz, AIN = −1 dBFS, RIN = 50 Ω, half- or full-duplex interface, default power bias settings

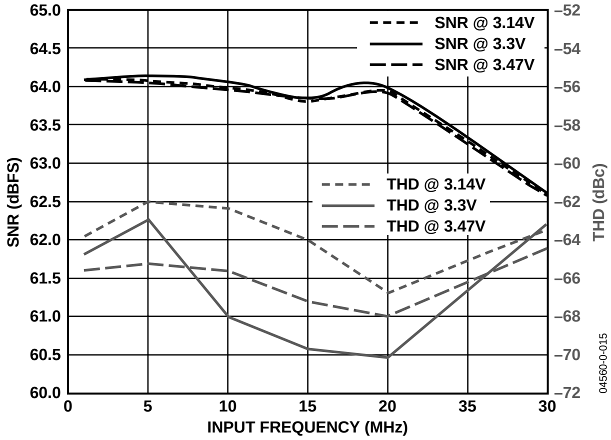

Figure 15. SNR and THD vs. Input Frequency and Supply (LPF $f_{-3\ dB}$ = 26 MHz; RxPGA = 0 dB)

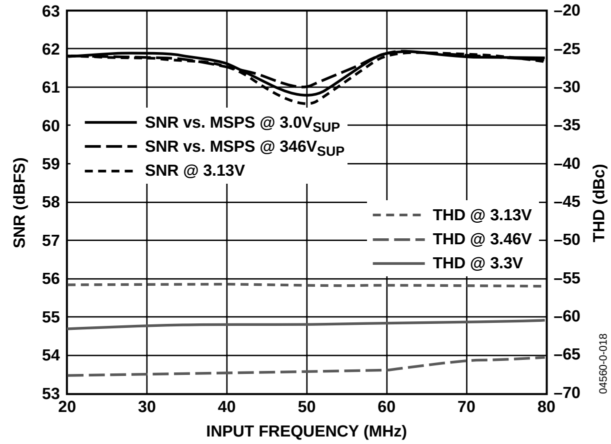

Figure 18. SNR and THD vs. Sample Rate and Supply (LPF Disabled; RxPGA = 0 dB; f_{IN} = 8 MHz)

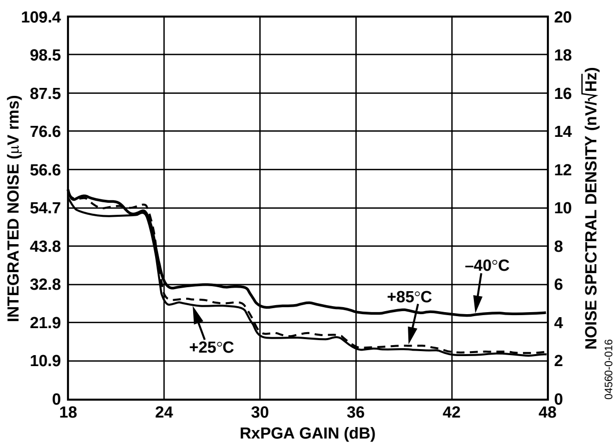

Figure 16. Input Referred Integrated Noise and Noise Spectral Density vs. RxPGA Gain (LPF $f_{-3\ dB}$ = 26 MHz)

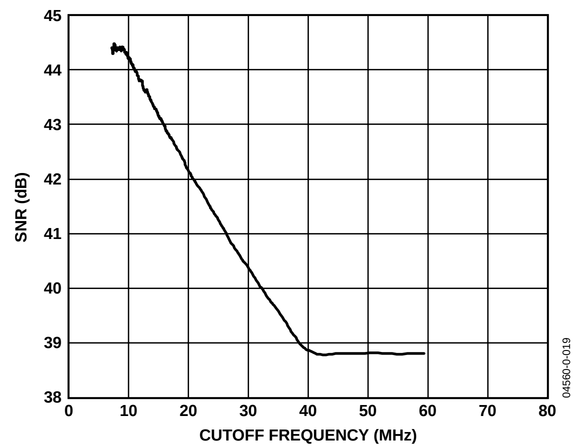

Figure 19. SNR vs. Filter Cutoff Frequency (50 MSPS; f_{IN} = 5 MHz; AIN = −1 dB; RxPGA = 48 dB)

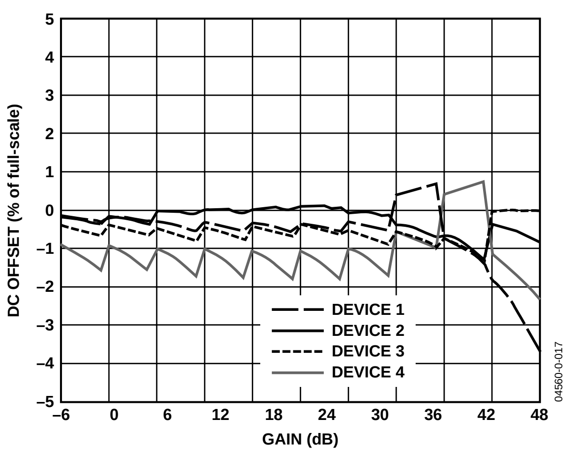

Figure 17. Rx DC Offset vs. RxPGA Gain

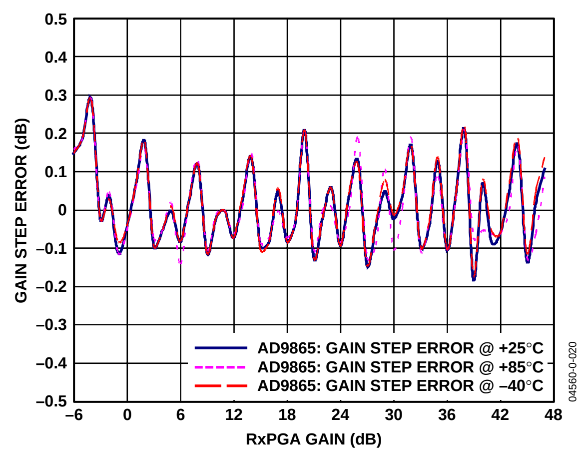

Figure 20. RxPGA Gain Step Error vs. Gain (f_{IN} = 10 MHz)

Rx Path Typical Performance Characteristics:

AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, f_{OSCIN} = f_{ADC} = 50 MSPS, low-pass filter disabled, RxPGA = 0 dB, AIN = −1 dBFS, RIN = 50 Ω, half- or full-duplex interface, default power bias settings

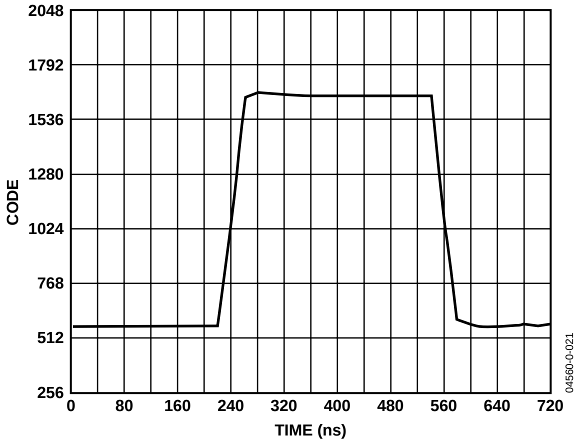

Figure 21. RxPGA Settling Time −12 dB to +48 dB Transition for DC Input (f_{ADC} = 50 MSPS, LPF Disabled)

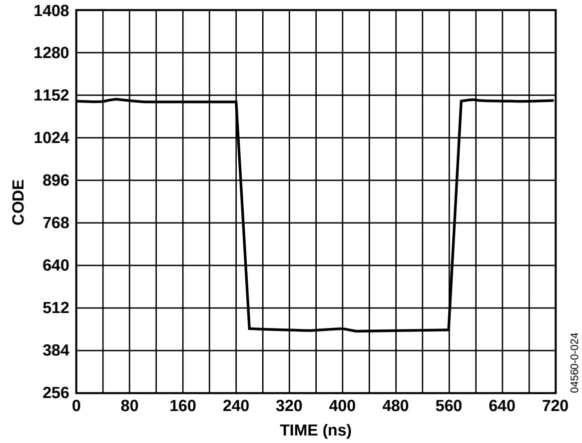

Figure 24. RxPGA Settling Time for 0 dB to +5 dB Transition for DC Input (f_{ADC} = 50 MSPS, LPF Disabled)

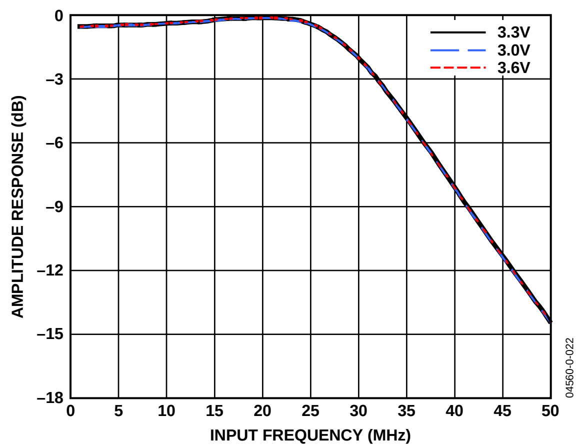

Figure 22. Rx Low-Pass Filter Amplitude Response vs. Supply (f_{ADC} = 50 MSPS, $f_{-3\ dB}$ = 33 MHz, RxPGA = 0 dB)

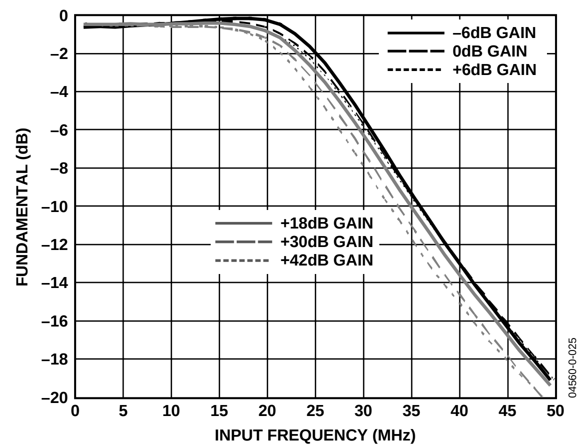

Figure 25. Rx Low-Pass Filter Amplitude Response vs. RxPGA Gain (LPF's $f_{-3\ dB}$ = 33 MHz)

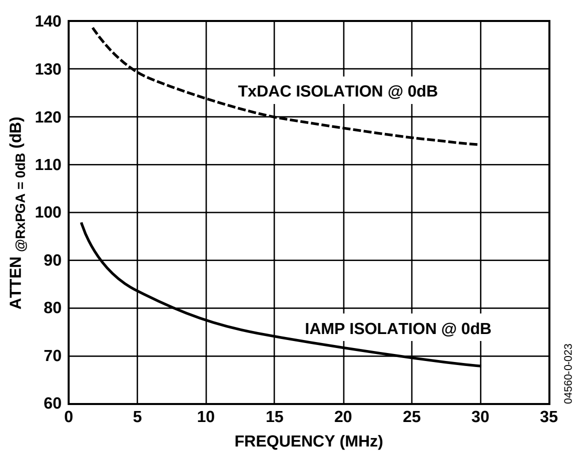

Figure 23. Rx to Tx Full-Duplex Isolation @ 0 RxPGA Setting (Note: ATTEN $_{@ RxPGA = x\ dB}$ = ATTEN $_{@ RxPGA = 0\ dB}$ − RxPGA Gain)

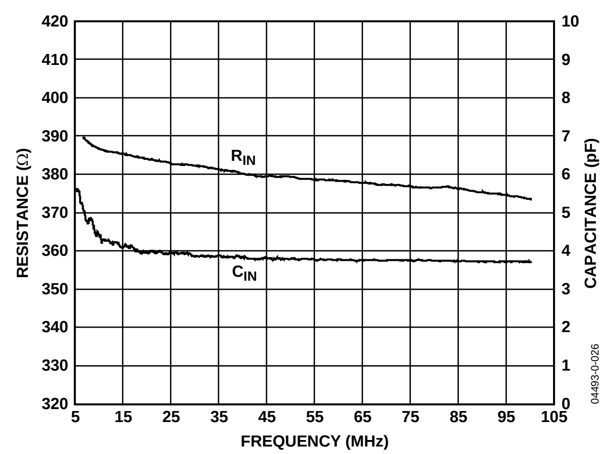

Figure 26. Rx Input Impedance vs. Frequency

TxDAC PATH TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, f_{OSCIN} = 50 MSPS and 80 MSPS, R_{SET} = 1.96 kΩ, 2:1 transformer coupled output (see Figure 63) into 50 Ω load half-or full-duplex interface, default power bias settings

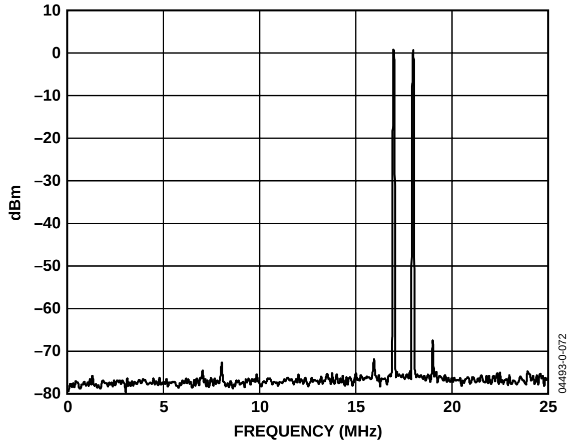

Figure 27. Dual-Tone Spectral Plot of TxDAC's Output (f_{DATA} = 50 MSPS, 4× Interpolation, 10 dBm Peak Power, F1 = 17 MHz, F2 = 18 MHz)

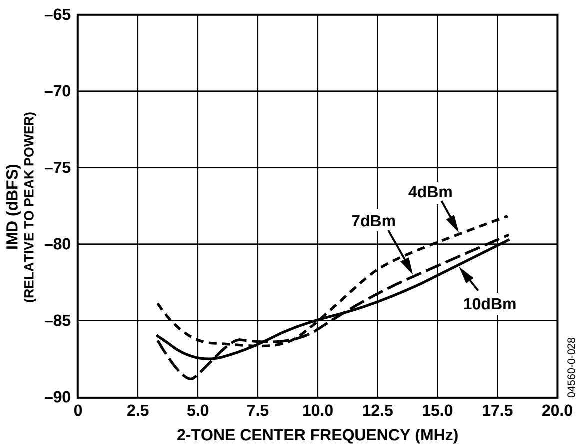

Figure 28. 2-Tone IMD Frequency Sweep vs. Peak Power with f_{DATA} = 50 MSPS, 4× Interpolation

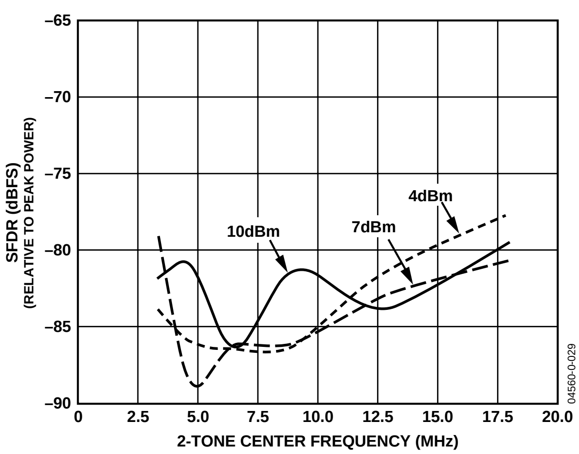

Figure 29. 2-Tone Worst Spur Frequency Sweep vs. Peak Power with f_{DATA} = 50 MSPS, 4× Interpolation

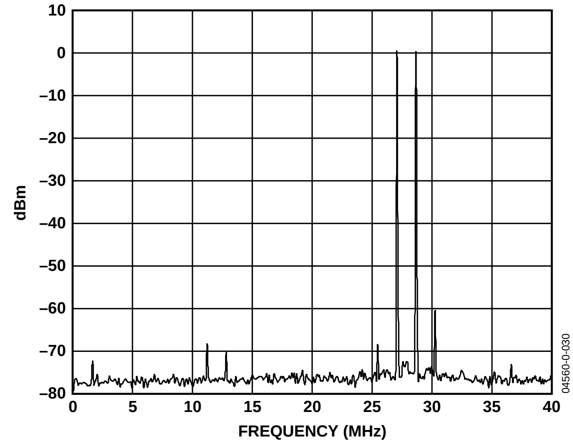

Figure 30. Dual-Tone Spectral Plot of TxDAC's Output (f_{DATA} = 80 MSPS, 2× Interpolation, 10 dBm Peak Power, F1 = 27.1 MHz, F2 = 28.7 MHz)

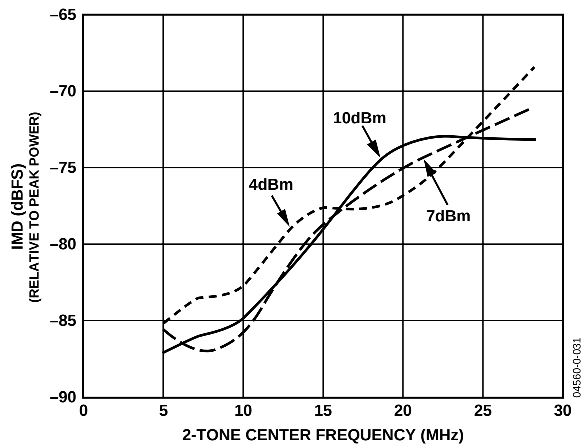

Figure 31. 2-Tone IMD Frequency Sweep vs. Peak Power with f_{DATA} = 80 MSPS, 2× Interpolation

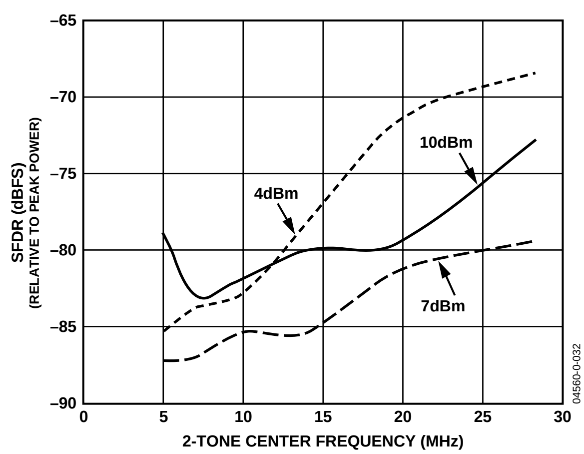

Figure 32. 2-Tone Worst Spur Frequency Sweep vs. Peak Power with f_{DATA} = 80 MSPS, 2× Interpolation

TxDAC Path Typical Performance Characteristics:
AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, f_{OSCIN} = 50 MSPS and 80 MSPS, R_{SET} = 1.96 kΩ, 2:1 transformer coupled output (see Figure 63) into 50 Ω load, half- or full-duplex interface, default power bias settings

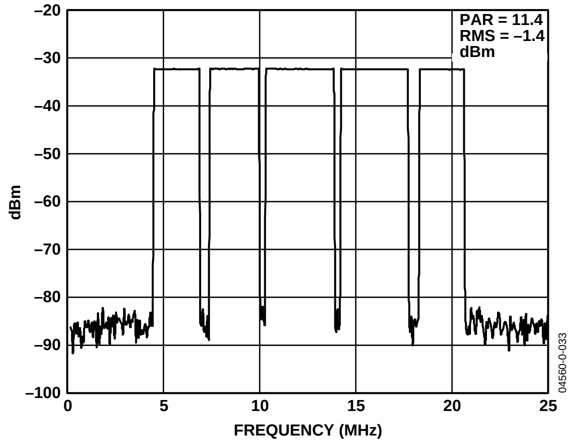

Figure 33. Spectral Plot of 84-Carrier OFDM Test Vector f_{DATA} = 50 MSPS, 4× Interpolation)

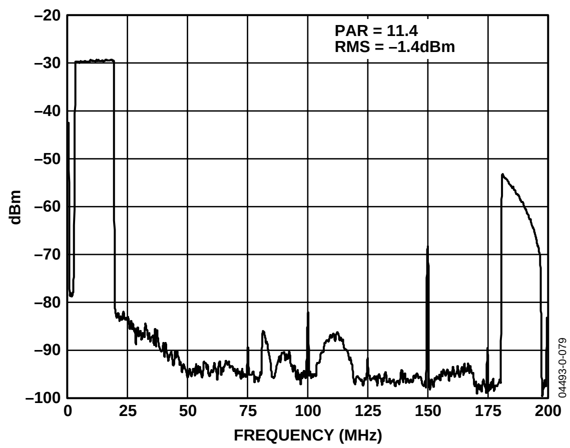

Figure 34. Wideband Spectral Plot of 88-Subcarrier OFDM Test Vector (f_{DATA} = 50 MSPS, 4× Interpolation)

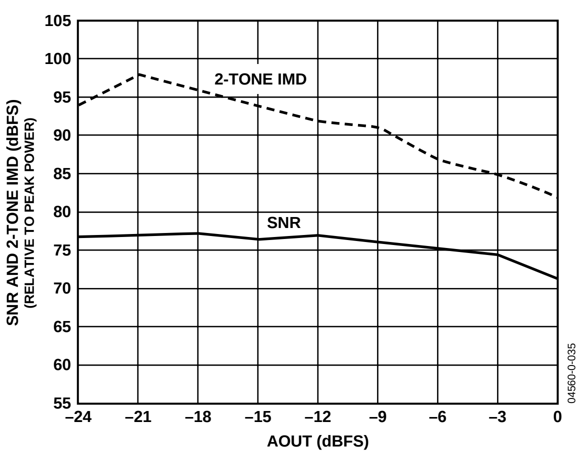

Figure 35. SNR and SFDR vs. P_{OUT} (f_{OUT} = 12.55 MHz, f_{DATA} = 50 MSPS, 4× Interpolation)

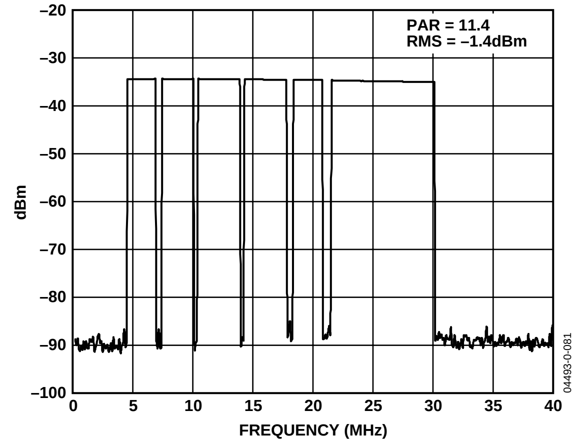

Figure 36. Spectral Plot of 111-Carrier OFDM Test Vector (f_{DATA} = 80 MSPS, 2× Interpolation)

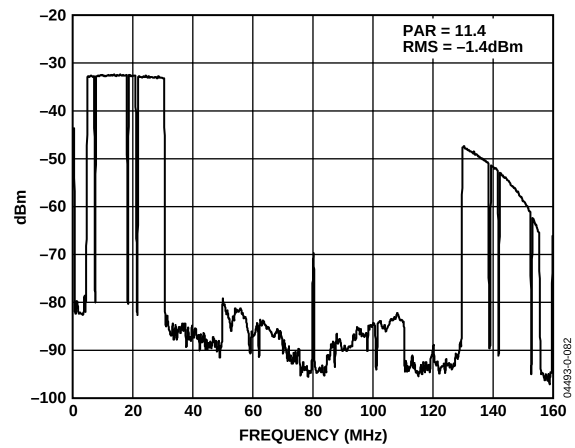

Figure 37. Wideband Spectral Plot of 111-Carrier OFDM Test Vector (f_{DATA} = 80 MSPS, 2× Interpolation)

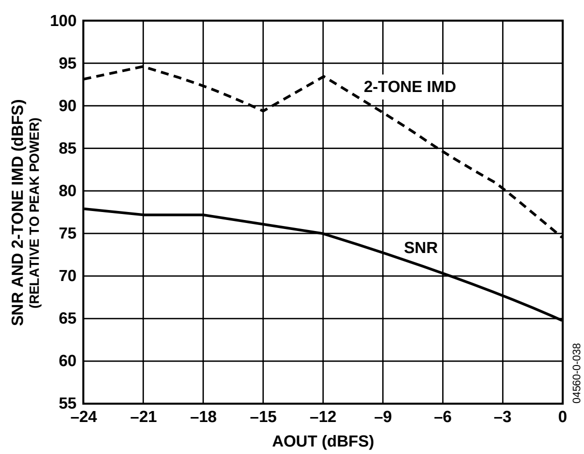

Figure 38. SNR and SFDR vs. P_{OUT} (f_{OUT} = 20 MHz, f_{DATA} = 80 MSPS, 2× Interpolation)

IAMP PATH TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, f_{OSCIN} = 50 MSPS, R_{SET} = 1.58 kΩ, 1:1 transformer coupled output (see Figure 64 and Figure 65) into 50 Ω load, half- or full-duplex interface, default power bias settings

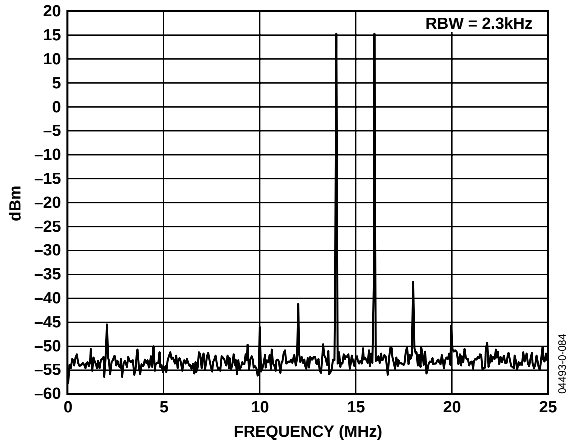

Figure 39. Dual-Tone Spectral Plot of IAMPN Output (IAMP Settings of I = 12.5 mA, N = 4, G = 0, 2:1 Transformer into 75 Ω Loader, VCM = 4.8 V)

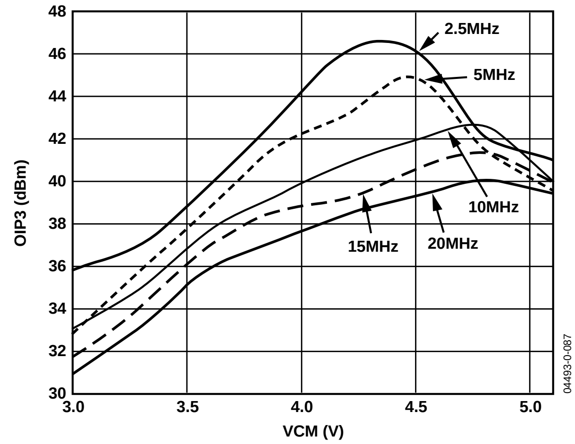

Figure 42. IOUTN Third-Order Intercept vs. Common-Mode Voltage (IAMP Settings of I = 12.5 mA, N = 4, G = 0, 2:1 Transformer into 75 Ω Load)

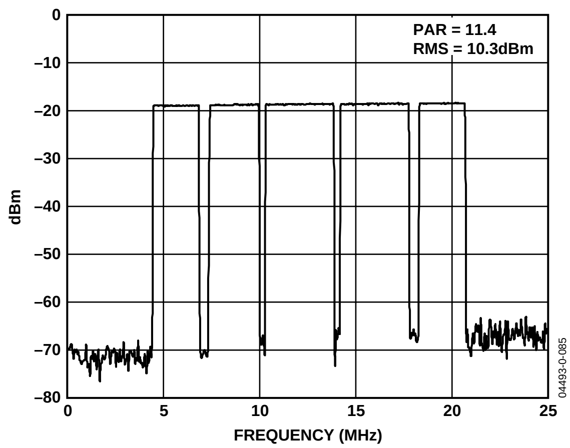

Figure 40. Spectral Plot of 84-Carrier OFDM Test Vector Using IAMPN in Current Mode Configuration (IAMP Settings of I = 10 mA, N = 4, G = 0; VCM = 4.8 V)

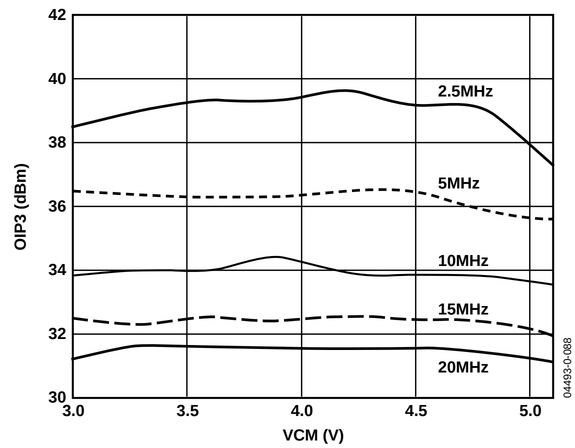

Figure 43. IOUTG Third-Order Intercept vs. Common-Mode Voltage (IAMP Settings of I = 4.25 mA, N = 0, G = 6, 2:1 Transformer into 75 Ω Load)

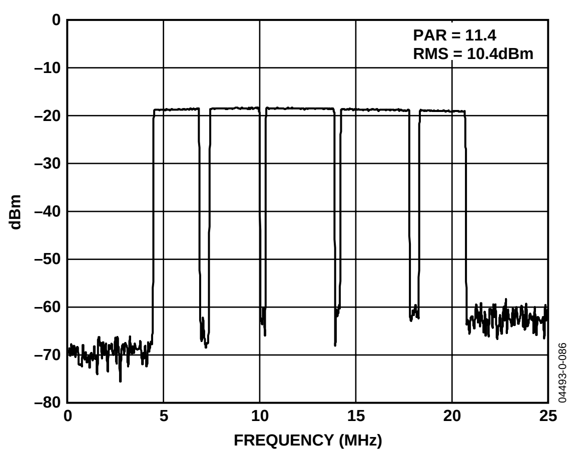

Figure 41. Spectral Plot of 84-Carrier OFDM Test Vector Using IAMP in Voltage Mode Configuration with AVDD = 5 V (PBR951 Transistors, IAMP Settings of I = 6 mA, N = 2, G = 6)

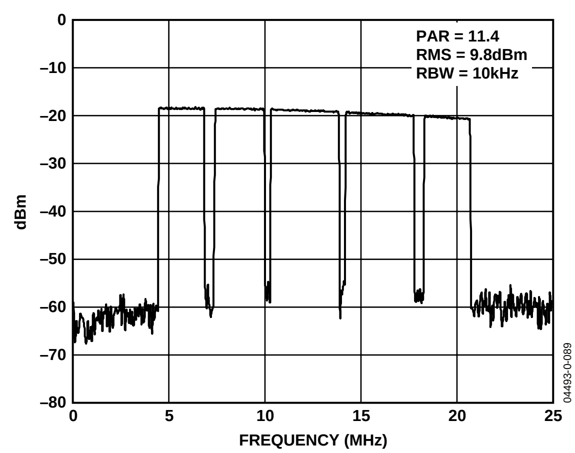

Figure 44. Spectral Plot of 84-Carrier OFDM Test Vector Using IAMP in Voltage Mode Configuration with AVDD = 3.3 V (PBR951 Transistors, IAMP Settings of I = 6 mA, N = 2, G = 6)

SERIAL PORT

Table 10. SPI Register Mapping

Address (Hex) [1]	Bit Break-down	Description	Width	Power-Up Default Value: MODE = 0 (Half-Duplex) CONFIG = 0	MODE = 0 (Half-Duplex) CONFIG = 1	MODE = 1 (Full-Duplex) CONFIG = 0	MODE = 1 (Full-Duplex) CONFIG = 1	Comments
SPI PORT CONFIGURATION AND SOFTWARE RESET								
0x00	(7)	4-Wire SPI	1	0	0	0	0	Default SPI configuration is 3-wire, MSB first.
	(6)	LSB First	1	0	0	0	0	
	(5)	S/W Reset	1	0	0	0	0	
POWER CONTROL REGISTERS (via PWR_DWN pin)								
0x01	(7)	Clock Syn.	1	0	0	0	0	PWR_DWN = 0 Default setting is for all blocks powered on.
	(6)	TxDAC/IAMP	1	0	0	0	0	
	(5)	Tx Digital	1	0	0	0	0	
	(4)	REF	1	0	0	0	0	
	(3)	ADC CML	1	0	0	0	0	
	(2)	ADC	1	0	0	0	0	
	(1)	PGA Bias	1	0	0	0	0	
	(0)	RxPGA	1	0	0	0	0	
0x02	(7)	CLK Syn.	1	0	0	0	1*	PWR_DWN = 1 Default setting* is for all functional blocks powered down except PLL. *MODE = CONFIG = 1 Setting has PLL powered down with OSCIN input routed to RXCLK output.
	(6)	TxDAC/IAMP	1	1	1	1	1	
	(5)	Tx Digital	1	1	1	1	1	
	(4)	REF	1	1	1	1	1	
	(3)	ADC CML	1	1	1	1	1	
	(2)	ADC	1	1	1	1	1	
	(1)	PGA Bias	1	1	1	1	1	
	(0)	RxPGA	1	1	1	1	1	
HALF-DUPLEX POWER CONTROL								
0x03	(7:3)	Tx OFF Delay	5	0xFF	0xFF	N/A	N/A	Default setting is for TXEN input to control power on/off of Tx/Rx path. Tx driver delayed by 31 $1/f_{DATA}$ clock cycles.
	(2)	Rx _TXEN	1					
	(1)	Tx PWRDN	1					
	(0)	Rx PWRDN	1					
PLL CLOCK MULTIPLIER/SYNTHESIZER CONTROL								
0x04	(5)	Duty Cycle Enable	1	0	0	0	0	Default setting is Duty Cycle Restore disabled, ADC CLK from OSCIN input, and PLL multiplier × 2 setting. *PLL multiplier × 4 setting.
	(4)	f_{ADC} from PLL	1	0	0	0	0	
	(3:2)	PLL Divide-N	2	00	00	00	00	
	(1:0)	PLL Multiplier-M	2	01	10*	01	01	
0x05	(2)	OSCIN to RXCLK	1	0	0	0	1*	Full-duplex RXCLK normally at nibble rate. *Exception on power-up.
	(1)	Invert RXCLK	1	0	0	0	0	
	(0)	Disabled RXCLK	1	0	0	0	0	
0x06	(7:6)	CLKOUT2 Divide	2	10	10	10	10	Default setting is CLKOUT2 and CLKOUT1 enabled with divide-by-2. *CLKOUT1 and CLKOUT2 disabled.
	(5)	CLKOUT2 Invert	1	0	0	0	0	
	(4)	CLKOUT2 Disable	1	0	0	0	1*	
	(3:2)	CLKOUT1 Divide	2	10	10	10	10	
	(1)	CLKOUT1 Invert	1	0	0	0	0	
	(0)	CLKOUT1 Disable	1	0	0	0	1*	

Address (Hex) [1]	Bit Break-down	Description	Width	Power-Up Default Value: MODE = 0 (Half-Duplex), CONFIG = 0	MODE = 0 (Half-Duplex), CONFIG = 1	MODE = 1 (Full-Duplex), CONFIG = 0	MODE = 1 (Full-Duplex), CONFIG = 1	Comments
Rx PATH CONTROL								
0x07	(5)	Initiate Offset Cal.	1	0	0	0	0	Default setting has LPF ON and Rx path at nominal power bias setting. *Rx path to low power.
	(4)	Rx Low Power	1	0	1*	0	1*	
	(0)	Rx Filter ON	1	1	1	1	1	
0x08	(7:0)	Rx Filter Tuning Cut-off Frequency	8	0x80	0x61*	0x80	0x80	Refer to Low-Pass Filter section.
Tx/Rx PATH GAIN CONTROL								
0x09	(6)	Use SPI Rx Gain	1	0x00	0x00	0x00	0x00	Default setting is for hardware Rx gain code via PGA or Tx data port.
	(5:0)	Rx Gain Code	6					
0x0A	(6)	Use SPI Tx Gain	1	0x7F	0x7F	0x7F	0x7F	Default setting is for Tx gain code via SPI control.
	(5:0)	Tx Gain Code	6					
Tx AND Rx PGA CONTROL								
0x0B	(6)	PGA Code for Tx	1	0	0	0	0	Default setting is RxPGA control active. *Tx port with GAIN strobe (AD9875/AD9876 compatible). ** 3-bit RxPGA gain map (AD9975 compatible).
	(5)	PGA Code for Rx	1	1	1	1	1	
	(3)	Force GAIN strobe	1	0	0	0	0	
	(2)	Rx Gain on Tx Port	1	0	0	1*	1*	
	(1)	3-Bit RxPGA Port	1	0	1**	0	0	
Tx DIGITAL FILTER AND INTERFACE								
0x0C	(7:6)	Interpolation Factor	2	01	00	01	01	Default setting is 2× interpolation with LPF response. Data format is straight binary for half-duplex and twos complement for full-duplex interface. *Full-duplex only.
	(4)	Invert TXEN/TXSYNC	1	0	0	0	0	
	(2)	LS Nibble First*	1	N/A	N/A	0	0	
	(1)	TXCLK neg. edge	1	0	0	0	0	
	(0)	Twos complement	1	0	0	1	1	
Rx INTERFACE AND ANALOG/DIGITAL LOOPBACK								
0x0D	(7)	Analog Loopback	1	0	0	0	0	Data format is straight binary for half-duplex and twos complement for full-duplex interface. Analog loopback: ADC Rx data fed back to TxDAC. Digital loopback: Tx input data to Rx output port. *Full-duplex only.
	(6)	Digital Loopback*	1	0	0	0	0	
	(5)	Rx Port 3-State	1	N/A	N/A	0	0	
	(4)	Invert RXEN/RXSYNC	1	0	0	0	0	
	(2)	LS Nibble First*	1	N/A	N/A	0	0	
	(1)	RXCLK neg. edge	1	0	0	0	0	
	(0)	Twos complement	1	0	0	1	1	
DIGITAL OUTPUT DRIVE STRENGTH, TxDAC OUTPUT, AND REV ID								
0x0E	(7)	Low Drive Strength	1	0	0	0	0	Default setting is for high drive strength and IAMP enabled.
	(0)	TxDAC Output	1	0	0	0	0	
0x0F	(3:0)	REV ID Number	4	0x00	0x00	0x00	0x00	
Tx IAMP GAIN AND BIAS CONTROL								
0x10	(7)	Select Tx Gain	1	0x44	0x44	0x44	0x44	Secondary path G1 = 0, 1, 2, 3, 4. Primary path N = 0, 1, 2, 3, 4.
	(6:4)	G1	3					
	(2:0)	N	3					
0x11	(6:4)	G2	3	0x62	0x62	0x62	0x62	Secondary path stages: G2 = 0 to 1.50 in 0.25 steps and G3 = 0 to 6.
	(2:0)	G3	3					

Address (Hex) [1]	Bit Break-down	Description	Width	Power-Up Default Value: MODE = 0 (Half-Duplex) CONFIG = 0	MODE = 0 (Half-Duplex) CONFIG = 1	MODE = 1 (Full-Duplex) CONFIG = 0	MODE = 1 (Full-Duplex) CONFIG = 1	Comments
0x12	(6:4)	Stand_Secondary	3	0x01	0x01	0x01	0x01	Standing current of primary and secondary path.
	(2:0)	Stand_Primary	3					
0x13	(7:5)	CPGA Bias Adjust	3	0x00	0x00	0x00	0x00	Current bias setting for Rx path's functional blocks. Refer to Page 41.
	(4:3)	SPGA Bias Adjust	2					
	(2:0)	ADC Bias Adjust	4					

[1]Bits that are undefined should always be assigned a 0.

REGISTER MAP DESCRIPTION

The AD9866 contains a set of programmable registers described in Table 10 that can be used to optimize its numerous features, interface options, and performance parameters from its default register settings. Registers pertaining to similar functions have been grouped together and assigned adjacent addresses to minimize the update time when using the multibyte serial port interface (SPI) read/write feature. Bits that are undefined within a register should be assigned a 0 when writing to that register.

The default register settings were intended to allow some applications to operate without the use of an SPI. The AD9866 can be configured to support a half- or full-duplex digital interface via the MODE pin with each interface having two possible default register settings determined by the setting of the CONFIG pin.

For instance, applications that need to use only the Tx or Rx path functionality of the AD9866 can configure it for a half-duplex interface (MODE = 0) and use the TXEN pin to select between the Tx or Rx signal path with the unused path remaining in a reduced power state. The CONFIG pin can be used to select the default interpolation ratio of the Tx path and RxPGA gain mapping.

SERIAL PORT INTERFACE (SPI)

The serial port of the AD9866 has 3- or 4-wire SPI capability allowing read/write access to all registers that configure the device's internal parameters. Registers pertaining to the SPI are listed in Table 11. The default 3-wire serial communication port consists of a clock (SCLK), serial port enable ($\overline{\text{SEN}}$), and a bidirectional data (SDIO) signal. $\overline{\text{SEN}}$ is an active low control gating read and write cycles. When $\overline{\text{SEN}}$ is high, SDO and SDIO are three-stated. The inputs to SCLK, $\overline{\text{SEN}}$, and SDIO contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about VDDH/2. The SDO pin remains three-stated in a 3-wire SPI interface.

Table 11. SPI Registers Pertaining to SPI Options

Address (Hex)	Bit	Description
0x00	(7)	Enable 4-wire SPI
	(6)	Enable SPI LSB first

A 4-wire SPI can be enabled by setting the 4-wire SPI bit high, causing the output data to appear on the SDO pin instead of on the SDIO pin. The SDIO pin serves as an input only, throughout the read operation. Note that the SDO pin is active only during the transmission of data and remains three-stated at any other time.

An 8-bit instruction header must accompany each read and write operation. The instruction header is shown in Table 12. The MSB is a R/$\overline{\text{W}}$ indicator bit with logic high indicating a read operation. The next two bits, N1 and N0, specify the number of bytes (one to four bytes) to be transferred during the data transfer cycle. The remaining five bits specify the address bits to be accessed during the data transfer portion. The data bits immediately follow the instruction header for both read and write operations.

Table 12. Instruction Header Information

MSB						LSB	
17	16	15	14	13	12	11	10
R/W	N1	N0	A4	A3	A2	A1	A0

The AD9866 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. Figure 45 illustrates how the serial port words are built for the MSB first and LSB first modes. The bit order is controlled by the SPI LSB first bit (Register 0, Bit 6). The default value is 0, MSB first. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the last address to be accessed. The AD9866 automatically decrements the address for each successive byte required for the multibyte communication cycle.

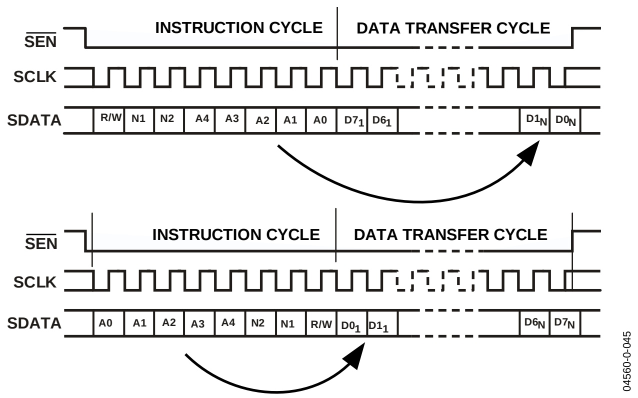

Figure 45. SPI Timing, MSB First (Upper) and LSB First (Lower)

When the SPI LSB first bit is set high, the serial port interprets both instruction and data bytes LSB first. Multibyte data transfers in LSB format can be completed by writing an instruction byte that includes the register address of the first address to be accessed. The AD9866 automatically increments the address for each successive byte required for the multibyte communication cycle.

Figure 46 illustrates the timing requirements for a write operation to the SPI port. After the serial port enable ($\overline{\text{SEN}}$) signal goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of the clock (SCLK). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the SDIO pin on the rising edge of the next eight clock cycles. If a multibyte communication cycle is specified, the destination address is decremented (MSB first) and another eight bits of data are shifted in. This process repeats itself until all the bytes specified in the instruction header (N1, N0 bits) are shifted in. $\overline{\text{SEN}}$ must remain low during the data transfer operation, only going high after the last bit is shifted in.

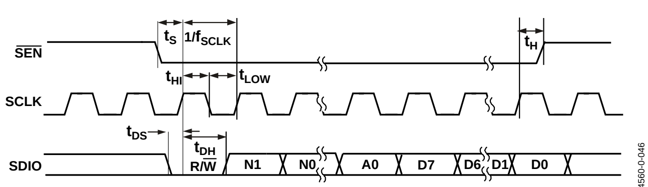

Figure 46. SPI Write Operation Timing

Figure 47 illustrates the timing for a 3-wire read operation to the SPI port. After $\overline{\text{SEN}}$ goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of SCLK. A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the SDIO pin on the falling edges of the next eight clock cycles. If a multibyte communication cycle is specified in the instruction header, a similar process as previously described for a multibyte SPI write operation applies. The SDO pin remains three-stated in a 3-wire read operation.

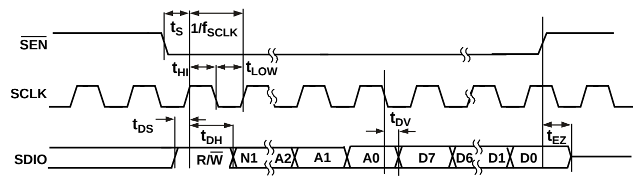

Figure 47. SPI 3-Wire Read Operation Timing

Figure 48 illustrates the timing for a 4-wire read operation to the SPI port. The timing is similar to the 3-wire read operation with the exception that data appears at the SDO pin, while the SDIO pin remains high impedance throughout the operation. The SDO pin is an active output only during the data transfer phase and remains three-stated at all other times.

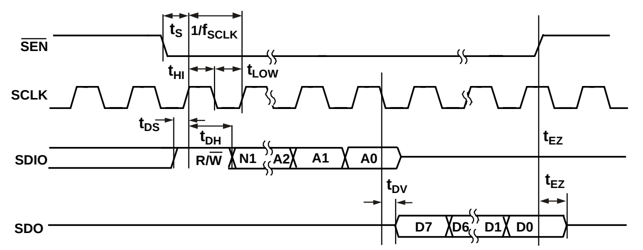

Figure 48. SPI 4-Wire Read Operation Timing

DIGITAL INTERFACE

The digital interface port is configurable for half-duplex or full-duplex operation by pin-strapping the MODE pin low or high, respectively. In half-duplex mode, the digital interface port becomes a 10-bit bidirectional bus called the ADIO port. In full-duplex mode, the digital interface port is divided into two 6-bit ports called Tx[5:0] and Rx[5:0] for simultaneous Tx and Rx operations. In this mode, data is transferred between the ASIC and AD9866 in 6-bit nibbles. The AD9866 also features a flexible digital interface for updating the RxPGA and TxPGA gain registers via a 6-bit PGA port or Tx[5:0] port for fast updates, or via the SPI port for slower updates. See the RXPGA Control section.

HALF-DUPLEX MODE

The half-duplex mode functions as follows when the MODE pin is tied low. The bidirectional ADIO port is typically shared in burst fashion between the transmit path and receive path. Two control signals, TXEN and RXEN, from a DSP (or digital ASIC) control the bus direction by enabling the ADIO port's input latch and output driver, respectively. Two clock signals, TXCLK and RXCLK, are used to latch the Tx input data and clock the Rx output data, respectively. The ADIO port can also be disabled by setting TXEN and RXEN low (default setting), thus allowing it to be connected to a shared bus.

Internally, the ADIO port consists of an input latch for the Tx path in parallel with an output latch with three-state outputs for the Rx path. TXEN is used to enable the input latch; RXEN is used to three-state the output latch. A five-sample-deep FIFO is used on the Tx and Rx paths to absorb any phase difference between the AD9866's internal clocks and the externally supplied clocks (TXCLK, RXCLK). The ADIO bus accepts input data-words into the transmit path when the TXEN pin is high, the RXEN pin is low, and a clock is present on the TXCLK pin, as shown in Figure 49.

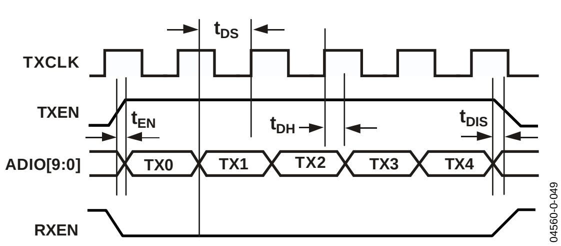

Figure 49. Transmit Data Input Timing Diagram

The Tx interpolation filter(s) following the ADIO port can be flushed with zeros, if the clock signal into the TXCLK pin is present for 33 clock cycles after TXEN goes low. Note that the data on the ADIO bus is irrelevant over this interval.

The output from the receive path is driven onto the ADIO bus when the RXEN pin is high, and a clock is present on the RXCLK pin. While the output latch is enabled by RXEN, valid data appears on the bus after a 6-clock-cycle delay due to the internal FIFO delay. Note that Rx data is not latched back into the Tx path, if TXEN is high during this interval with TXCLK present. The ADIO Bus becomes three-stated once the RXEN pin returns low. Figure 50 illustrates the receive path output timing.

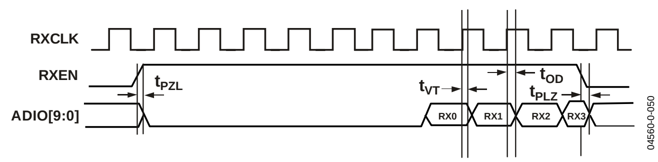

Figure 50. Receive Data Output Timing Diagram

To add flexibility to the digital interface port, several programming options are available in the SPI registers. These options are listed in Table 13. The default Tx and Rx data input formats are straight binary, but can be changed to twos complement. The default TXEN and RXEN settings are active high, but can be set to opposite polarities, thus allowing them to share the same control. In this case, the ADIO port can still be placed onto a shared bus by disabling its input latch via the control signal, and disabling the output driver via the SPI register. The clock timing can be independently changed on the transmit and receive paths by selecting either the rising or falling clock edge as the validating/sampling edge of the clock. Lastly, the output driver's strength can be reduced for lower data rate applications.

Table 13. SPI Registers for Half-Duplex Interface

Address (Hex)	Bit	Description
0x0C	(4)	Invert TXEN
	(1)	TXCLK negative edge
	(0)	Twos complement
0x0D	(5)	Rx port three-state
	(4)	Invert RXEN
	(1)	RXCLK negative edge
	(0)	Twos complement
0x0E	(7)	Low digital drive strength

The half-duplex interface can be configured to act like a slave or a master to the digital ASIC. An example of a slave configuration is shown in Figure 51. In this example, the AD9866 accepts all the clock and control signals from the digital ASIC. Because the sampling clocks for the DAC and ADC are derived internally from the OSCIN signal, it is required that the TXCLK and RXCLK signals be at exactly the same frequency as the OSCIN signal. The phase relationships among the TXCLK, RXCLK, and OSCIN signals can be arbitrary. If the digital ASIC cannot provide a low jitter clock source to OSCIN, consider using the AD9866 to generate the clock for its DAC and ADC and pass the desired clock signal to the digital ASIC via CLKOUT1 or CLKOUT2.

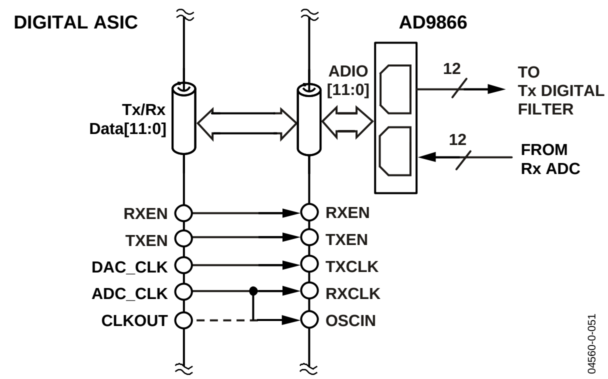

Figure 51. Example of a Half -Duplex Digital Interface with AD9866 Serving as the Slave

Figure 52 shows a half-duplex interface with the AD9866 acting as the master, generating all the required clocks. CLKOUT1 provides a clock equal to the bus data rate that is fed to the ASIC as well as back to the TXCLK and RXCLK inputs. This interface has the advantage of reducing the digital ASIC's pin count by three. The ASIC needs only to generate a bus control signal that controls the data flow on the bidirectional bus.

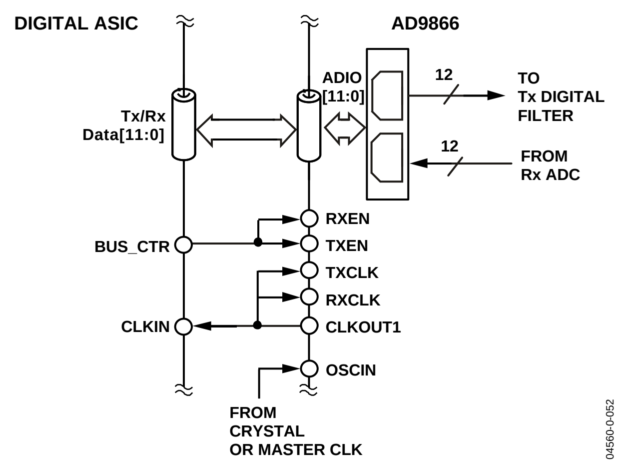

Figure 52. Example of a Half -Duplex Digital Interface with AD9866 Serving as the Master

FULL-DUPLEX MODE

The full-duplex mode interface is selected when the MODE pin is tied high. It can be used for full- or half-duplex applications. The digital interface port is divided into two 6-bit ports called Tx[5:0] and Rx[5:0], allowing simultaneous Tx and Rx operations for full-duplex applications. In half-duplex applications, the Tx[5:0] port can also be used to provide a fast update of the RxPGA (AD9876 backward compatible) during an Rx operation. This feature is enabled by default and can be used to reduce the required pin count of the ASIC (refer to RxPGA Control section for more detail).

In either application, Tx and Rx data are transferred between the ASIC and AD9866 in 6-bit (or 5-bit) nibbles at twice the internal input/output word rates of the Tx interpolation filter and ADC. Note that the TxDAC update rate *must not* be less than the nibble rate. Therefore, the 2× or 4× interpolation filter must be used with a full-duplex interface.

The AD9866 acts as the master, providing RXCLK as an output clock that is used for the timing of both the Tx[5:0] and Rx[5:0] ports. RXCLK always runs at the nibble rate and can be inverted or disabled via an SPI register. Because RXCLK is derived from the clock synthesizer, it remains active, provided that this functional block remains powered on. A buffered version of the signal appearing at OSCIN can also be directed to RXCLK by setting Bit 2 of Reg. 0x05. This feature allows the AD9866 to be completely powered down (including the clock synthesizer) while serving as the master.

The Tx[5:0] port operates in the following manner with the SPI register default settings. Two consecutive nibbles of the Tx data are multiplexed together to form a 10-bit data-word in twos complement format. The clock appearing on the RXCLK pin is a buffered version of the internal clock used by the Tx[5:0] port's input latch with a frequency that is always twice the ADC sample rate ($2 \times f_{ADC}$). Data from the Tx[5:0] port is read on the rising edge of this sampling clock, as illustrated in the timing diagram shown in Figure 53.

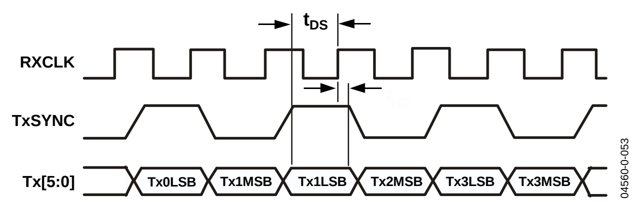

Figure 53. Tx[5:0] Port Full-Duplex Timing Diagram

The TXSYNC signal is used to indicate to which word a nibble belongs. The first nibble of every word is read while TXSYNC is low as the most significant nibble. The second nibble of that same word is read on the following TXSYNC high level as the least significant nibble. If TXSYNC is low for more than one clock cycle, the last transmit data is read continuously until TXSYNC is brought high for the second nibble of a new transmit word. This feature can be used to flush the interpolator filters with zeros. Note that the GAIN signal must be kept low during a Tx operation.

The Rx[5:0] port operates in the following manner with the SPI register default settings. Two consecutive nibbles of the Rx data are multiplexed together to form a 10-bit data-word in twos complement format. The Rx data is valid on the rising edge of RXCLK, as illustrated in the timing diagram shown in Figure 54. The RXSYNC signal is used to indicate to which word a nibble belongs. The first nibble of every word is transmitted while RXSYNC is low as the most significant nibble. The second nibble of that same word is transmitted on the following RXSYNC high level as the least significant nibble.

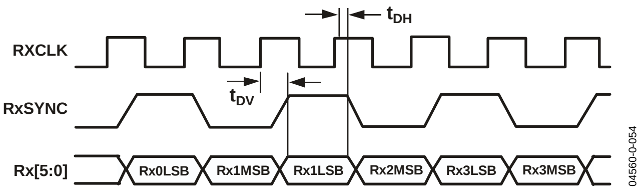

Figure 54. Full-Duplex Rx Port Timing

To add flexibility to the full-duplex digital interface port, several programming options are available in the SPI registers. These options are listed in Table 14. The timing for the Tx[5:0] and/or Rx[5:0] ports can be independently changed by selecting either the rising or falling clock edge as the sampling/validating edge of the clock. Inverting RXCLK (via Bit 1 or Reg. 0x0D) affects both the Rx and Tx interface, because they both use RXCLK.

Table 14. SPI Registers for Full-Duplex Interface

Address (Hex)	Bit	Description
0x05	(2)	OSCIN to RXCLK
	(1)	Invert RXCLK
	(0)	Disable RXCLK
0x0B	(2)	Rx gain on Tx port
0x0C	(4)	Invert TXSYNC
	(3)	Tx 5/5 nibble
	(2)	LS nibble first
	(1)	TXCLK negative edge
	(0)	Twos complement
0x0D	(5)	Rx port three-state
	(4)	Invert RXSYNC
	(3)	Rx 5/5 nibble
	(2)	LS nibble first
	(1)	RXCLK negative edge
	(0)	Twos complement
0x0E	(7)	Low drive strength

The default Tx and Rx data input formats are twos complement, but can be changed to straight binary. The default TXSYNC and RXSYNC settings can be changed such that the first nibble of the word appears while TXSYNC, RXSYNC, or both are high. Also, the least significant nibble can be selected as the first nibble of the word (LS nibble first). The output driver strength can also be reduced for lower data rate applications.

Figure 55 shows a possible digital interface between an ASIC and the AD9866. The AD9866 serves as the master generating the required clocks for the ASIC. This interface requires that the ASIC reserve 16 pins for the interface, assuming a 6-bit nibble width and the use of the Tx port for RxPGA gain control. Note that the ASIC pin allocation can be reduced by 3, if a 5-bit nibble width is used and the gain (or gain strobe) of the RxPGA is controlled via the SPI port.

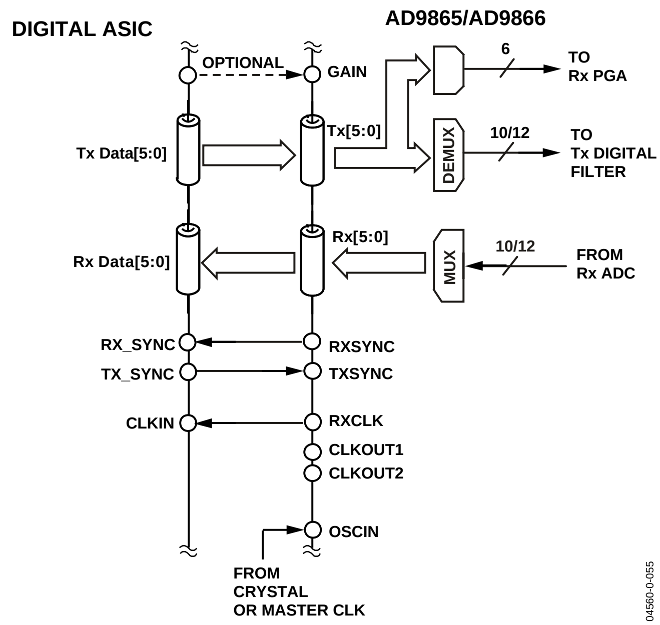

Figure 55. Example of a Full-Duplex Digital Interface with Optional RxPGA Gain Control via Tx[5:0]

RxPGA CONTROL

The AD9866 contains a digital PGA in the Rx path that is used to extend the dynamic range. The RxPGA can be programmed over a −12 dB to +48 dB with 1 dB resolution using a 6-bit word, and with a 0 dB setting corresponding to a 2 V p-p input signal. The 6-bit word is fed into a LUT that is used to distribute the desired gain over three amplification stages within the Rx path. Upon power-up, the RxPGA gain register is set to its minimum gain of −12 dB. The RxPGA gain mapping is shown in Figure 56. Table 15 lists the SPI registers pertaining to the RxPGA.

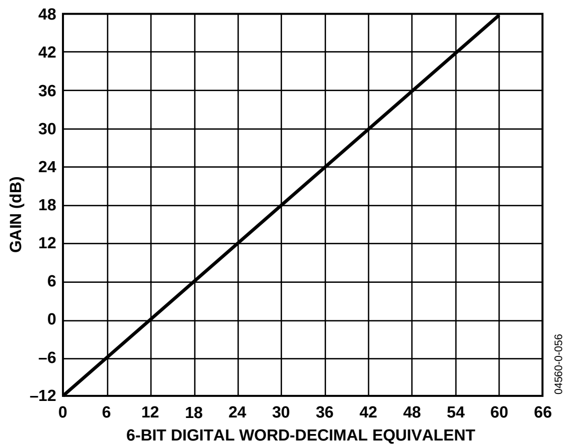

Figure 56. Digital Gain Mapping of RxPGA

Table 15. SPI Registers RxPGA Control

Address (Hex)	Bit	Description
0x09	(6)	Enable RxPGA update via SPI
	(5:0)	RxPGA gain code
0x0B	(6)	Select TxPGA via PGA[5:0]
	(5)	Select RxPGA via PGA[5:0]
	(3)	Enable software GAIN strobe – full-duplex
	(2)	Enable RxPGA update via Tx[5:0] – full-duplex
	(1)	3-bit RxPGA gain mapping – half-duplex

The RxPGA gain register can be updated via the Tx[5:0] port, the PGA[5:0] port, or the SPI port. The first two methods allow fast updates of the RxPGA gain register and should be considered for digital AGC functions requiring a fast closed-loop response. The SPI port allows direct update and readback of the RxPGA gain register via Reg. 0x09 with an update rate limited to 1.6 MSPS (with SCLK = 32 MHz). Note that Bit 6 of Reg. 0x09 must be set for a read or write operation.

Updating the RxPGA via the Tx[5:0] port is an option only in full-duplex mode.[1] In this case, a high level on the GAIN pin[2] with Tx SYNC low programs the PGA setting on either the rising edge or falling edge of RXCLK, as shown in Figure 57. The GAIN pin must be held high, TxSYNC must be held low, and GAIN data must be stable for one or more clock cycles to update the RxPGA gain setting. A low level on the GAIN pin enables data to be fed to the digital interpolation filter. This interface should be considered when upgrading existing designs from the AD9876 MxFE product or half-duplex applications trying to minimize an ASIC's pin count.

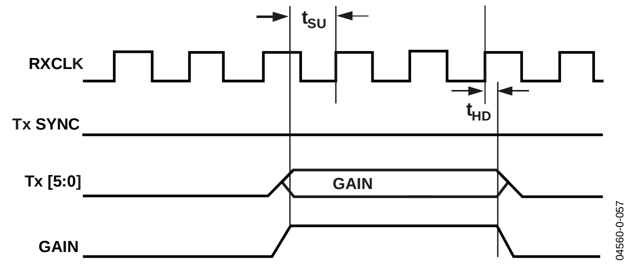

Figure 57. Updating RxPGA via Tx[5:0] in Full-Duplex Mode

Updating the RxPGA (or TxPGA) via the PGA[5:0] port is an option for both the half-duplex[3] and full-duplex interfaces. The PGA port consists of an input buffer that passes the 6-bit data appearing at its input directly to the RxPGA (or TxPGA) gain register with no gating signal required. Bit 5 or Bit 6 of Reg. 0x0B is used to select whether the data updates the RxPGA or TxPGA gain register. In applications that switch between RxPGA and TxPGA gain control via PGA[5:0], be careful that the RxPGA (or TxPGA) is not inadvertently loaded with the wrong data during a transition. In the case of an RxPGA to TxPGA transition, first deselect the RxPGA gain register, update the PGA[5:0] port with the desired TxPGA gain setting, and then select the TxPGA gain register.

The RxPGA also offers an alternative 3-bit word gain mapping option[4] that provides a −12 dB to +36 dB span in 8 dB increments as shown in Table 16. The 3-bit word is directed to PGA[5:3] with PGA[5] being the MSB. This feature is backward compatible with the AD9975 MxFE and allows direct interfacing to the CX11647 or INT5130 HomePlug 1.0 PHYs.

Table 16. PGA Timing for AD9975 Backward Compatible Mode

Digital Gain Setting		
PGA[5:3]	Decimal	Gain (dB)
000	0	−12
001	1	−12
010	2	−4
011	3	4
100	4	12
101	5	20
110	6	28
111	7	36

[1] Default setting for full-duplex mode (MODE = 1) .
[2] The GAIN strobe can also be set in software via Reg. 0x0B, Bit 3 for continuous updating. This eliminates the requirement for external GAIN signal, reducing the ASIC pin count by 1.

[3] Default setting for half-duplex mode (MODE = 0).
[4] Default setting for MODE = 0 and CONFIG =1.

TxPGA CONTROL

The AD9866 also contains a digital PGA in the Tx path distributed between the TxDAC and IAMP. The TxPGA is used to control the peak current from the TxDAC and IAMP over a 7.5 dB and 19.5 dB span, respectively, with 0.5 dB resolution. A 6-bit word is used to set the TxPGA attenuation according to the mapping shown in Figure 58. The TxDAC gain mapping is applicable only when Bit 0 of Reg. 0x0E is set, and only the 4 LSBs of the 6-bit gain word are relevant.

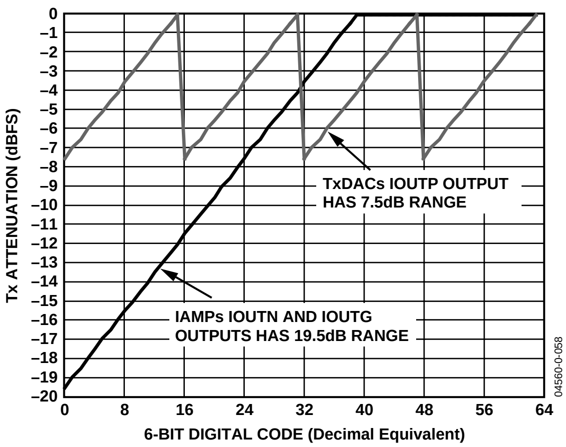

Figure 58. Digital Gain Mapping of TxPGA

The TxPGA register can be updated via the PGA[5:0] port or SPI port. The first method should be considered for fast updates of the TxPGA register. Its operation is similar to the description in the RxPGA Control section. The SPI port allows direct update and readback of the TxPGA register via Reg. 0x0A with an update rate limited to 1.6 MSPS (SCLK = 32 MHz). Bit 6 of Reg 0x0A must be set for a read or write operation. Table 17 lists the SPI registers pertaining to the TxPGA. The TxPGA control register default setting is for minimum attenuation (0 dBFS) with the PGA[5:0] port disabled for Tx gain control.

Table 17. SPI Registers TxPGA Control

Address (Hex)	Bit	Description
0x0A	(6)	Enable TxPGA update via SPI
	(5:0)	TxPGA gain code
0x0B	(6)	Select TxPGA via PGA[5:0]
	(5)	Select RxPGA via PGA[5:0]
0x0E	(0)	TxDAC output (IAMP disabled)

TRANSMIT PATH

The AD9866 (or AD9865) transmit path consists of a selectable digital 2×/4× interpolation filter, a 12-bit (or 10-bit) TxDAC, and a current-output amplifier (IAMP), as shown in Figure 59. Note that the additional two bits of resolution offered by the AD9866 (vs. the AD9865) result in a 10 dB to 12 dB reduction in the pass-band noise floor. The digital interpolation filter relaxes the Tx analog filtering requirements by simultaneously reducing the images from the DAC reconstruction process while increasing the analog filter's transition band. The digital interpolation filter can also be bypassed, resulting in lower digital current consumption.

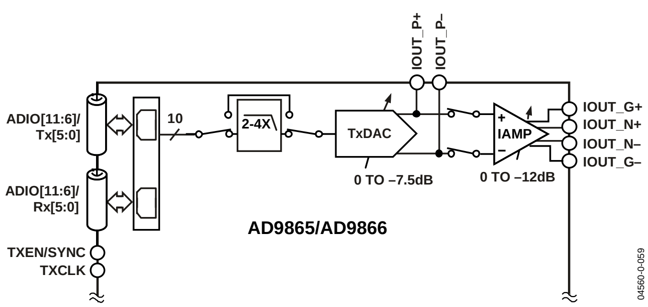

Figure 59. Functional Block Diagram of Tx Path

DIGITAL INTERPOLATION FILTERS

The input data from the Tx port can be fed into a selectable 2×/4× interpolation filter or directly into the TxDAC (for a half-duplex only). The interpolation factor for the digital filter is set via SPI Reg. 0x0C with the settings shown in Table 18. The maximum input word rate, f_{DATA}, into the interpolation filter is 80 MSPS; the maximum DAC update rate is 200 MSPS. Therefore, applications with input word rates at or below 50 MSPS can benefit from 4× interpolation, while applications with input word rates between 50 MSPS and 80 MSPS can benefit from 2× interpolation.

Table 18. Interpolation Factor Set via SPI Reg. 0x0C

Bits [7:6]	Interpolation Factor
00	4
01	2
10	1 (half-duplex only)
11	Do not use

The interpolation filter consists of two cascaded half-band filter stages with each stage providing 2× interpolation. The first stage filter consists of 43 taps. The second stage filter, operating at the higher data rate, consists of 11 taps. The normalized wide band and pass-band filter responses (relative f_{DATA}) for the 2× and 4× low-pass interpolation filters are shown in Figure 60 and Figure 61, respectively. Note that these responses also include the inherent sinc(x) from the TxDAC reconstruction process and can be used to estimate any post analog filtering requirements.

The pipeline delays of the 2× and 4× filter responses are 21.5 and 24 clock cycles, respectively, relative to f_{DATA}. The filter delay is also taken into consideration for applications configured for a half-duplex interface with the half-duplex power-down mode enabled. This feature allows the user to set a programmable delay that powers down the TxDAC and IAMP only after the last Tx input sample has propagated through the digital filter. See the Power Control section for more details.

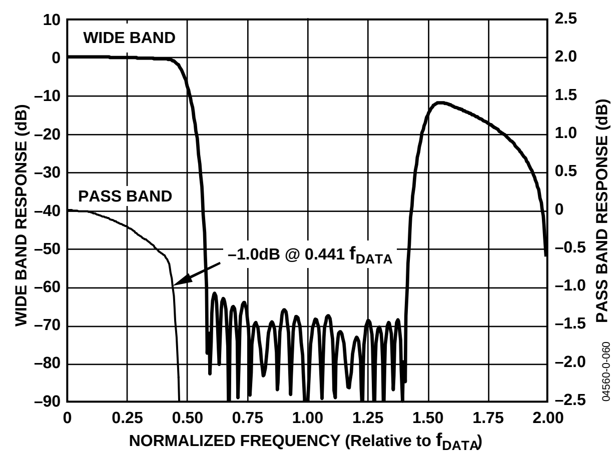

Figure 60. Frequency Response of 2× Interpolation Filter (Normalized to f_{DATA})

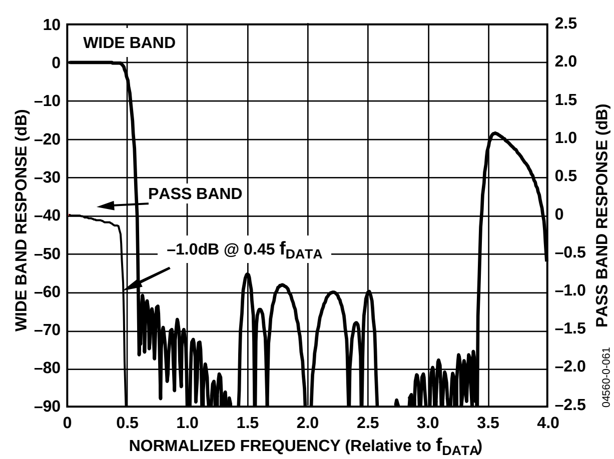

Figure 61. Frequency Response of 4× Interpolation Filter (Normalized to f_{DATA})

TxDAC AND IAMP ARCHITECTURE

The Tx path contains a TxDAC along with a current amplifier, IAMP. The TxDAC reconstructs the output of the interpolation filter and sources a differential current output that can either be directed to an external load or fed into the IAMP for further amplification. The TxDAC's and IAMPS's peak current outputs are digitally programmable over a 0 to −7.5 dB and 0 to −19.5 dB range, respectively, in 0.5 dB increments. Note that this assumes default register settings for Reg. 0x10 and Reg. 0x11.

Applications demanding the highest spectral performance and/or lowest power consumption can use the TxDAC output directly. The TxDAC is capable of delivering a peak signal power-up to 10 dBm while maintaining respectable linearity performance, as shown in Figure 27 through Figure 38. For power-sensitive applications requiring the highest Tx power efficiency, the TxDAC's full-scale current output can be reduced to as low as 2 mA and its load resistors sized to provide a suitable voltage swing that can be amplified by a low power op-amp-based driver.

Most applications requiring higher peak signal powers (up to 23 dBm) should consider using the IAMP. The IAMP can be configured as a current source for loads having a well defined impedance (50 Ω or 75 Ω systems) or a voltage source (with the addition of a pair of npn transistors) for poorly defined loads having varying impedance (such as power lines).

Figure 62 shows the equivalent schematic of the TxDAC and IAMP. The TxDAC provides a differential current output appearing at IOUTP+ and IOUTP−. It can be modeled as a differential current source generating a signal-dependent ac current, when ΔI_S has a peak current of I along with two dc current sources, sourcing a standing current equal to I. The full-scale output current, IOUTFS, is equal to the sum of these standing current sources (IOUTFS = 2*I).

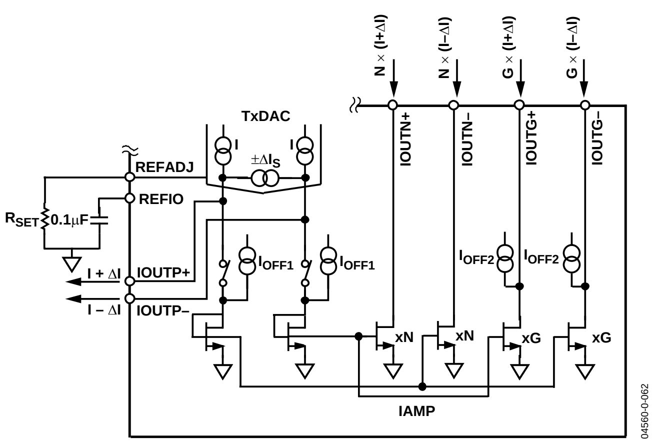

Figure 62. Equivalent Schematic of TxDAC and IAMP

The value of I is determined by the R_{SET} value at the REFADJ pin along with the Tx path's digital attenuation setting. With 0 dB attenuation, the value of I is

$$I = 16 * (1.23 / R_{SET})$$

Equation 1.

For example, an R_{SET} value of 1.96 kΩ results in I equal to 10.0 mA with IOUTFS equal to 20.0 mA. Note that the REFIO pin provides a nominal band gap reference voltage of 1.23 V and should be decoupled to analog ground via a 0.1 µF capacitor.

The differential current output of the TxDAC is always connected to the IOUTP pins, but can be directed to the IAMP by setting Bit 0 of Reg 0x0E. As a result, the IOUTP pins *must* remain completely open, if the IAMP is to be used. The IAMP contains two sets of current mirrors that are used to replicate the TxDAC's current output with a selectable gain. The first set of current mirrors is designated as the primary path, providing a gain factor of N that is programmable from 0 to 4 in steps of 1 via Bits 2:0 of Reg. 0x10 with a default setting of N = 4. Bit 7 of this register *must* be set to overwrite the default settings of this register. This differential path exhibits the best linearity performance (see Figure 42) and is available at the IOUTN+ and IOUTN− pins. The maximum peak current per output is 100 mA and occurs when the TxDAC's standing current, I, is set for 12.5 mA (IOUTFS = 25 mA).

The second set of current mirrors is designated as the secondary path providing a gain factor of G that is programmable from 0 to 36 via Bits 6:4 of Reg. 0x10 and Bits 6:0 of Reg. 0x11 with a default setting of G = 12. This differential path is intended to be used in the voltage mode configuration to bias the external *npn* transistors, because it exhibits degraded linearity performance (see Figure 43) relative to the primary path . It is capable of sinking up to 180 mA of peak current into either its IOUTG+ or IOUTG− pins. The secondary path actually consists of 3 gain stages (G1, G2, and G3), which are individually programmable as shown in Table 19. While many permutations may exist to provide a fixed gain of G, the linearity performance of a secondary path remains relatively independent of the various individual gain settings that are possible to achieve a particular overall gain factor.

Both sets of mirrors sink current, because they originate from NMOS devices. Therefore, each output pin requires a dc current path to a positive supply. Although the voltage output of each output pin can swing between 0.5 and 7 V, optimum ac performance is typically achieved by limiting the ac voltage swing with a dc bias voltage set between 4 to 5 V. Lastly, both the standing current, I, and the ac current, ΔI_S, from the TxDAC are amplified by the gain factor (N and G) with the total standing current drawn from the positive supply being equal to

$$2 * (N + G) * I$$

Programmable current sources I_{OFF1} and I_{OFF2} via Reg. 0x12 can be used to improve the primary and secondary path mirrors' linearity performance under certain conditions by increasing their signal-to-standing current ratio. This feature provides a marginal improvement in distortion performance under large signal conditions when the peak ac current of the reconstructed waveform frequently approaches the dc standing current within the TxDAC (0 to −1 dBFS sine wave) causing the internal mirrors to turn off. However, the improvement in distortion performance diminishes as the crest factor (peak-to-rms ratio) of the ac signal increases. Most applications can disable these current sources (set to 0 mA via Reg. 0x12) to reduce the IAMP's current consumption.

Table 19. SPI Registers for TxDAC and IAMP

Address (Hex)	Bit	Description
0x0E	(0)	TxDAC output
0x10	(7)	Enable current mirror gain settings
	(6:4)	Secondary path first stage gain of 0 to 4 with Δ = 1
	(3)	Not used
	(2:0)	Primary path NMOS gain of 0 to 4 with Δ = 1
0x11	(7)	Don't care
	(6:4)	Secondary path second stage gain of 0 to 1.5 with Δ = 0.25
	(3)	Not used
	(2:0)	Secondary path third stage gain of 0 to 5 with Δ = 1
0x12	(6:4)	IOFF2, secondary path standing current
	(2:0)	IOFF1, primary path standing current

Tx PROGRAMMABLE GAIN CONTROL

TxPGA functionality is also available to set the peak output current from the TxDAC or IAMP. The TxDAC and IAMP are digitally programmable via the PGA[5:0] port or SPI over a 0 dB to −7.5 dB and 0 dB to −19.5 dB range, respectively, in 0.5 dB increments.

The TxPGA can be considered as two cascaded attenuators with the TxDAC providing 7.5 dB range in 0.5 dB increments, and the IAMP providing 12 dB range in 6 dB increments. As a result, the IAMP's composite 19.5 dB span is valid only if Reg. 0x10 remains at its default setting of 0x44. Modifying this register setting corrupts the LUT and results in an invalid gain mapping.

TxDAC OUTPUT OPERATION

The differential current output of the TxDAC can be directed to the IOUTP+ and IOUTP− pins by setting Bit 0 of Reg. 0x0E. Any load connected to these pins must be ground referenced to provide a dc path for the current sources. Figure 63 shows the outputs of the TxDAC driving a doubly terminated 1:1 transformer with its center-tap tied to ground. The peak-to-peak voltage, V p-p, across R_L (and IOUT+ to IOUT−) is equal to $2*I*(R_L//R_S)$. With I = 10 mA and $R_L = R_S = 50\ \Omega$, V p-p is equal to 0.5 V with 1 dBm of peak power being delivered to R_L and 1 dBm being dissipated in R_S.

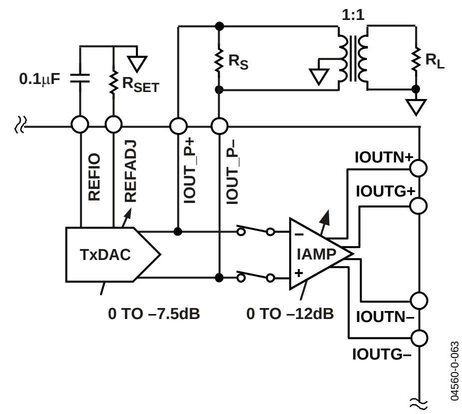

Figure 63. TxDAC Output Directly via Center-Tap Transformer

The TxDAC is capable of delivering up to 10 dBm peak power to a load, R_L. To increase the peak power for a fixed standing current, one must increase V p-p across IOUTP+ and −IOUTP− by increasing one or more of the following parameters: R_S, R_L (if possible), and/or the turns ratio, N, of transformer. For example, the removal of R_S and the use of a 2:1 impedance ratio transformer in the previous example results in 10 dBm of peak power capabilities to the load. Note that increasing the power output capabilities of the TxDAC reduces the distortion performance due to the higher voltage swings seen at IOUTP+ and IOUTP−. See Figure 27 through Figure 38 for performance plots on the TxDAC's ac performance. Optimum distortion performance can typically be achieved by:

- Limiting the peak positive V_{IOUTP+} and V_{IOUTP-} to 0.8 V to avoid onset of TxDAC's output compression. (TxDAC's voltage compliance is around 1.2 V.)
- Limiting V p-p seen at IOUTP+ and IOUTP− to less than 1.6 V.

Applications demanding higher output voltage swings and power drive capabilities can benefit from using the IAMP.

IAMP CURRENT MODE OPERATION

The IAMP can be configured for the current mode operation as shown in Figure 64 for loads remaining relatively constant. In this mode, the primary path mirrors should be used to deliver the signal-dependent current to the load via a center-tapped transformer, because it provides the best linearity performance. Because the mirrors exhibit a high output impedance, they can be easily back-terminated (if required).

For peak signal currents ($IOUT_{PK}$ up to 50 mA), only the primary path mirror gain should be used for optimum distortion performance and power efficiency. The primary path's gain should be set to 4, with the secondary path's gain stages set to 0 (Reg. 0x10 = 0x84). The TxDAC's standing current, I, can be set between 2.5 mA and 12.5 mA with the IOUTP outputs left open. The IOUTN outputs should be connected to the transformer, with the IOUTG (and IOUTP) outputs left open for optimum linearity performance. The transformer[1] should be specified to handle the dc standing current, I_{BIAS}, drawn by the IAMP. Also, because I_{BIAS} remains signal independent, a series resistor (not shown) can be inserted between AVDD and the transformer's center-tap to reduce the IAMP's common-mode voltage, V_{CM}, and reduce the power dissipation on the IC. The V_{CM}, bias should not exceed 5.0 V and the power dissipated in the IAMP alone is as follows:

$$P_{IAMP} = 2 * (N + G) * I * V_{CM}$$

Equation 2.

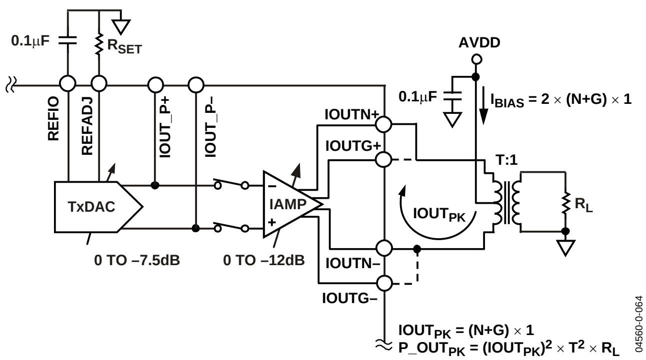

Figure 64. Current Mode Operation

A step-down transformer[1] with a turn ratio, T, can be used to increase the output power, P_OUT, delivered to the load. This causes the output load, R_L, to be reflected back to the IAMP's differential output by T^2 resulting in a larger differential voltage swing seen at the IAMP's output. For example, the IAMP can deliver 24 dBm of peak power to a 50 Ω load, if a 1.41:1 step-down transformer is used. This results in 5 V p-p voltage swings appearing at IOUTN+ and IOUTN− pins. Figure 42 shows how the third order intercept point, OIP3, of the IAMP varies as a function of common-mode voltage over a 2.5 MHz to 20.0 MHz span with a 2-tone signal having a peak power of approximately 24 dBm with $IOUT_{PK}$ = 50 mA.

For applications requiring an $IOUT_{PK}$ exceeding 50 mA, set the secondary's path to deliver the additional current to the load. IOUTG+ and IOUTN+ should be shorted as well as IOUTG− and IOUTN−. If $IOUT_{PK}$ represents the peak current to be delivered to the load, then the current gain in the secondary path, G, can be set by the following equation:

$$G = IOUT_{PK} / 12.5 - 4$$

Equation 3.

The linearity performance becomes limited by the secondary mirror path's distortion.

IAMP VOLTAGE MODE OPERATION

The voltage mode configuration is shown in Figure 65. This configuration is suited for applications having a poorly defined load that can vary over a considerable range. A low impedance voltage driver can be realized with the addition of two external RF bipolar npn transistors (Phillips PBR951) and resistors. In this configuration, the current mirrors in the primary path (IOUTN outputs) feed into scaling resistors, R, generating a differential voltage into the bases of the npn transistors. These transistors are configured as source followers with the secondary path current mirrors appearing at IOUTG+ and IOUTG− providing a signal-dependent bias current. Note that the IOUTP outputs *must* remain open for proper operation.

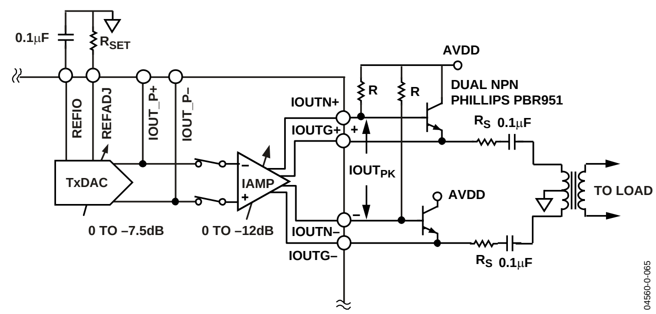

Figure 65. Voltage Mode Operation

The peak differential voltage signal developed across the npn's bases is as follows:

$$VOUT_{PK} = R * (N * I)$$

Equation 4.

where:

N is the gain setting of the primary mirror.

I is the standing current of the TxDAC defined in Equation 1.

The common-mode bias voltage seen at IOUTN+ and IOUTN− is approximately AVDD − $VOUT_{PK}$, while the common-mode voltage seen at IOUTG+ and IOUTG− is approximately the npn's V_{BE} drop below this level (AVDD − $VOUT_{PK}$ − 0.65). In the voltage mode configuration, the total power dissipated within the IAMP is as follows :

$$P_{IAMP} = 2 * I * \{(AVDD - VOUTPK) * N + (AVDD - VOUT_{PK} - 0.65) * G\}$$

Equation 5.

The emitters of the npn transistors are ac-coupled to the transformer[1] via a 0.1 µF blocking capacitor and series resistor of 1Ω to 2 Ω. Note that protection diodes are not shown for clarity purposes, but should be considered, if interfacing to a power or phone line.

[1] The B6080 and BX6090 transformers from Pulse Engineering are worthy of consideration for current and voltage modes.

The amount of standing and signal-dependent current used to bias the npn transistors is dependent on the peak current, $IOUT_{PK}$, required by the load. If the load is variable, determine the worst case, $IOUT_{PK}$, and add 3 mA of margin to ensure that the npn transistors remain in the active region during peak load currents. The gain of the secondary path, G, and the TxDAC's standing current, I, can be set using the following equation:

$$IOUT_{PK} + 3mA = G * I$$

Equation 6.

The voltage output driver exhibits a high output impedance, if the bias currents for the npn transistors are removed. This feature is advantageous in half-duplex applications (for example, power lines) in which the Tx output driver must go into a high impedance state while in Rx mode. If the AD9866 is configured for the half-duplex mode (MODE = 0), the IAMP, TxDAC, and interpolation filter are automatically powered down after a Tx burst (via TXEN), thus placing the Tx driver into a high impedance state while reducing its power consumption.

IAMP CURRENT CONSUMPTION CONSIDERATIONS

The Tx path's analog current consumption is an important consideration when determining its contribution to the overall on-chip power dissipation. This is especially the case in full-duplex applications, where the power dissipation can exceed the maximum limit of 1.66 W, if the IAMP's $IOUT_{PK}$ is set to high. The analog current consumption includes the TxDAC's analog supply (Pin 43) along with the standing current from the IAMP's outputs. Equation 2 and Equation 5 can be used to calculate the power dissipated in the IAMP for the current and voltage mode configuration. Figure 66 shows the current consumption for the TxDAC and IAMP as a function of the TxDAC's standing current, I, when only the IOUTN outputs are used. Figure 67 shows the current consumption for the TxDAC and IAMP as a function of the TxDAC's standing current, I, when the IOUTN and IOUTG outputs are used. Both figures are with the default current mirror gain settings of N = 4 and G = 12.

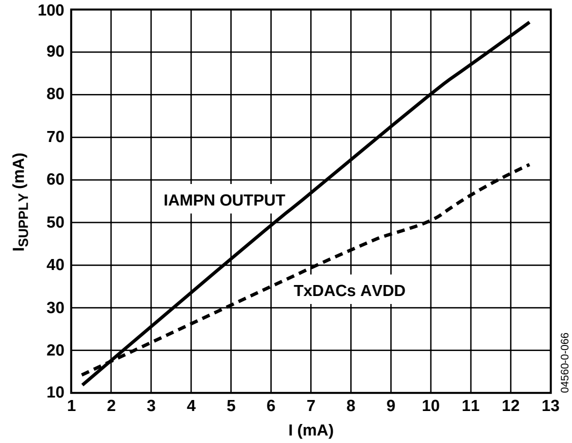

Figure 66. Current Consumption of TxDAC and IAMP in Current Mode Operation with IOUTN Only (Default IAMP Settings)

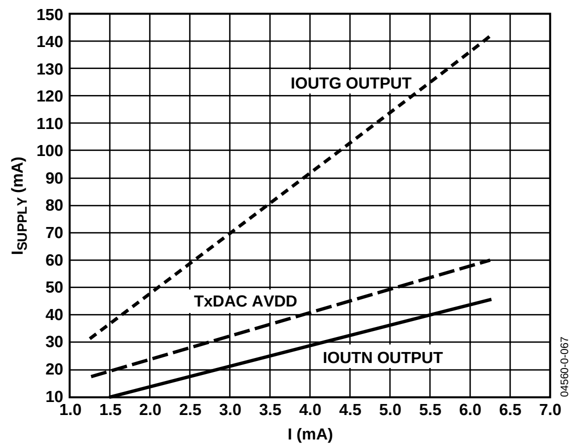

Figure 67. Current Consumption of TxDAC and IAMP in Current Mode Operation with IOUTN Only (Default IAMP Settings)

RECEIVE PATH

The receive path block diagram for the AD9866 (or AD9865) is shown in Figure 68. The receive signal path consists of a 3-stage RxPGA, a 3-pole programmable LPF, and a 12-bit (or 10-bit) ADC. Note that the additional 2 bits of resolution offered by the AD9866 (vs. the AD9865) result in a 3 dB to 5 dB lower noise floor depending on the RxPGA gain setting and LPF cutoff frequency. Also working in conjunction with the receive path is an offset correction circuit. These blocks are discussed in detail in the following sections. Note that the power consumption of the RxPGA can be modified via Reg. 0x13 as discussed in the Power Control and Dissipation section.

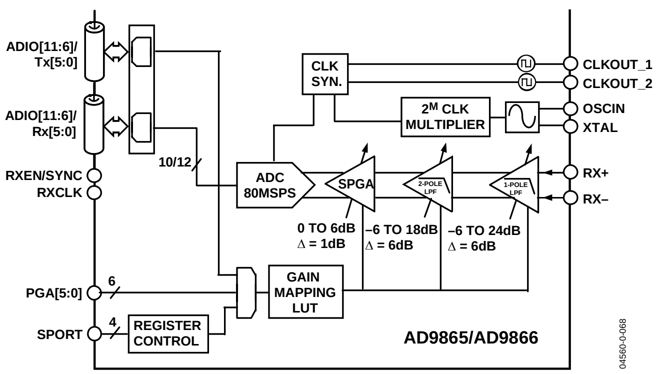

Figure 68. Functional Block Diagram of Rx Path

RX PROGRAMMABLE GAIN AMPLIFIER

The RxPGA has a digitally programmable gain range from −12 dB to +48 dB with 1 dB resolution via a 6-bit word. Its purpose is to extend the dynamic range of the Rx path such that the input of the ADC is presented with a signal that scales within its fixed 2 V input span. There are multiple ways of setting the RxPGA's gain as discussed in the RxPGA Control section, as well as an alternative 3-bit gain mapping having a range of −12 dB to +36 dB with 8 dB resolution.

The RxPGA is comprised of two sections: a continuous time PGA (CPGA) for course gain and a switched capacitor PGA (SPGA) for fine gain resolution. The CPGA consists of two cascaded gain stages providing a gain range from −12 dB to +42 dB with 6 dB resolution. The first stage features a low noise preamplifier (< 3.0 nV/rtHz), thereby eliminating the need for an external preamplifier. The SPGA provides a gain range from 0 dB to 6 dB with 1 dB resolution. A look-up table (LUT) is used to select the appropriate gain setting for each stage.

The nominal differential input impedance of the RxPGA input appearing at the device RX+ and RX– input pins is 400 Ω//4 pF (±20%) and remains relatively independent of gain setting. The PGA input is self-biased at a 1.3 V common-mode level allowing maximum input voltage swings of ±1.5 V at RX+ and RX–. AC coupling the input signal to this stage via coupling capacitors (0.1 μF) is recommended to ensure that any external dc offset does not get amplified with high RxPGA gain settings, potentially exceeding the ADC input range.

To limit the RxPGA's self-induced input offset, an offset cancellation loop is included. This cancellation loop is automatically performed upon power-up and can also be initiated via SPI. During calibration, the RxPGA's first stage is internally shorted, and each gain stage set to a high gain setting. A digital servo loop slaves a calibration DAC, which forces the Rx input offset to be within ±32 LSB for this particular high gain setting. Although the offset varies for other gain settings, the offset is typically limited to ±5% of the ADC's 2 V input span. Note that the offset cancellation circuitry is intended to reduce the voltage offset attributed to only the RxPGA's input stage, not any dc offsets attributed to an external source.

The gain of the RxPGA should be set to minimize clipping of the ADC while utilizing most of its dynamic range. The maximum peak-to-peak differential voltage that does not result in clipping of the ADC is shown in Figure 69. While the graph suggests that maximum input signal for a gain setting of −12 dB is 8.0 V p-p, the maximum input voltage into the PGA should be limited to less than 6 V p-p to prevent turning on ESD protection diodes. For applications having higher maximum input signals, consider adding an external resistive attenuator network. While the input sensitivity of the Rx path is degraded by the amount of attenuation on a dB-to-dB basis, the low noise characteristics of the RxPGA provide some design margin such that the external line noise remains the dominant source.

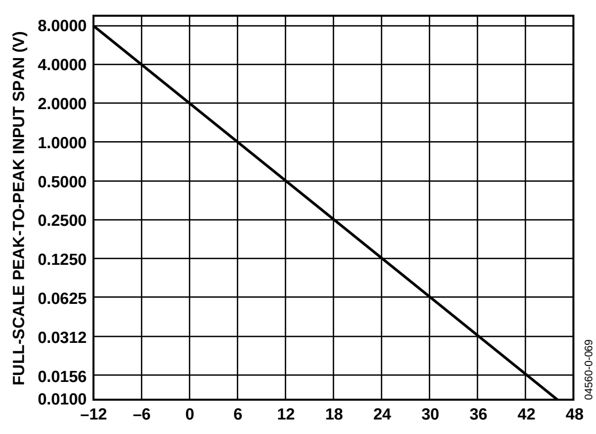

Figure 69. Maximum Peak-to-Peak Input vs. RxPGA Gain Setting that Does Not Result in ADC Clipping

LOW-PASS FILTER

The low-pass filter (LPF) provides a third order response with a cut-off frequency that is typically programmable over a 15 MHz to 35 MHz span. Figure 68 shows that the first real pole is implemented within the first CPGA gain stage, and the complex pole pair is implemented in the second CPGA gain stage. Capacitor arrays are used to vary the different R-C time constants within these two stages in a manner that changes the cut-off frequency while preserving the normalized frequency response. Because absolute resistor and capacitor values are process-dependent, a calibration routine lasting less than 100 µs automatically occurs each time the target cut-off frequency register (Reg. 0x08) is updated, ensuring a repeatable cut-off frequency from device to device.

Although the default setting specifies that the LPF be active, it can also be bypassed providing a nominal $f_{-3\,dB}$ of 55 MHz. Table 20 shows the SPI registers pertaining to the LPF.

Table 20. SPI Registers for Rx Low-Pass Filter

Address (Hex)	Bit	Description
0x07	(0)	Enable Rx LPF
0x08	(7:0)	Target value

The normalized wideband gain response is shown in Figure 70. The normalized pass-band gain and group delay responses are shown in Figure 71. The normalized cut-off frequency, $f_{-3\,dB}$, results in −3 dB attenuation. Also, the actual group delay time (GDT) response can be calculated given a programmed cut-off frequency using the following equation:

$$Actual\,GDT = Normalized\;\;GDT\,/(2.45 * f_{-3dB})$$

Equation 7.

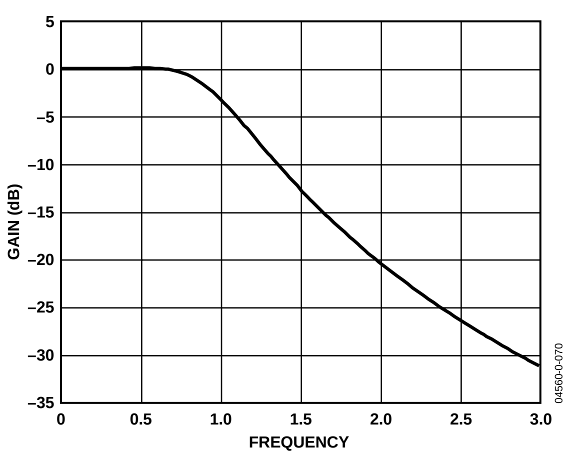

Figure 70. LPF's Normalized Wideband Gain Response

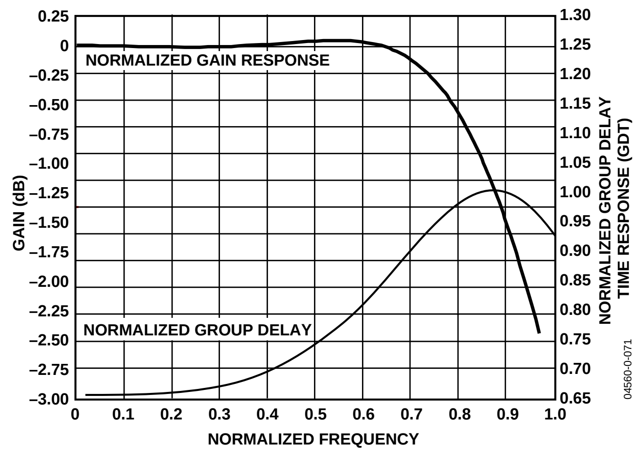

Figure 71. LPF's Normalized Pass-Band Gain and Group Delay Responses

The −3 dB cut-off frequency, $f_{-3\,dB}$, is programmable by writing an 8-bit word, referred to as the target, to Reg. 0x08. The cut-off frequency is a function of the ADC sample rate, f_{ADC}, and to a lesser extent RxPGA gain setting (in dB). Figure 72 shows how the frequency response, $f_{-3\,dB}$, varies as a function of the RxPGA gain setting.

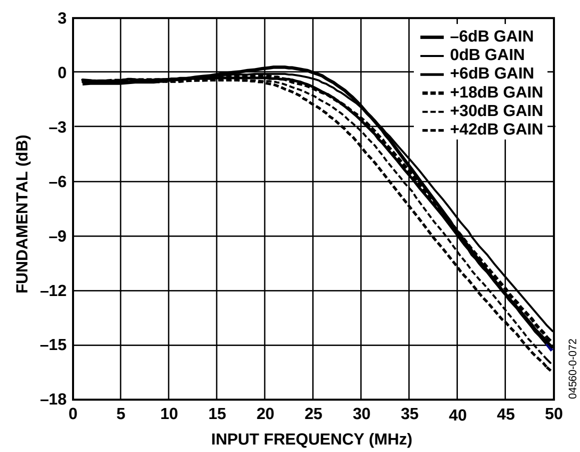

Figure 72. Effects of RxPGA Gain on LPF Frequency Response ($f_{-3\,dB}$ = 32 MHz (@ 0 dB and f_{ADC} = 80 MSPS)

The following formula[1] can be used to estimate $f_{-3\,dB}$ for a RxPGA gain setting of 0 dB:

$$f_{-3dB\_0dB} = (128\,/\,target) * (f_{ADC}\,/\,80) * (f_{ADC}\,/\,30 + 23.83)$$

Equation 8.

Figure 73 compares the measured and calculated $f_{-3\,dB}$ using this formula.

[1]Empirically derived for a $f_{-3\,dB}$ range of 15 MHz to 35 MHz and f_{ADC} of 40 MSPS to 80 MSPS with an RxPGA = 0 dB.

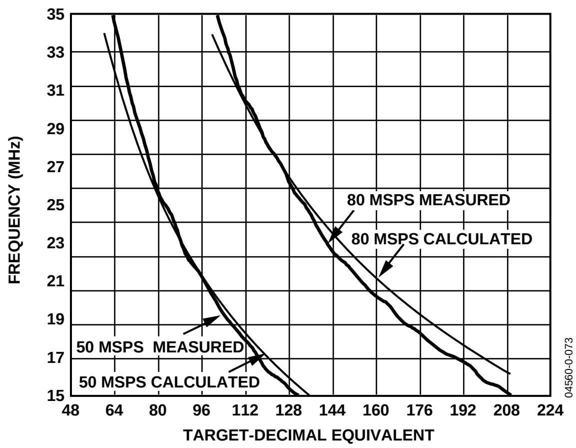

Figure 73. Measured and Calculated $f_{-3\ dB}$ vs. Target Value for f_{ADC} = 50 MSPS and 80 MSPS

The following scaling factor can be applied to the previous formula to compensate for the RxPGA gain setting on $f_{-3\ dB}$:

$$Scale\ Factor = 1 - (RxPGA\ \ in\ \ dB)/382$$

Equation 9.

This scaling factor reduces the calculated $f_{-3\ dB}$ as the RxPGA is increased. Applications that need to maintain a minimum cut-off frequency, $f_{-3\ dB\_MIN}$, for all RxPGA gain settings should first determine the scaling factor for the highest RxPGA gain setting to be used. Next, the $f_{-3\ dB\_MIN}$ should be divided by this scale factor to normalize to the 0 dB RxPGA gain setting ($f_{-3\ dB\_0\ dB}$). Equation 8 can then be used to calculate the target value.

The LPF frequency response shows a slight sensitivity to temperature, as shown in Figure 74. Applications sensitive to temperature drift can recalibrate the LPF by rewriting the target value to Reg. 0x08.

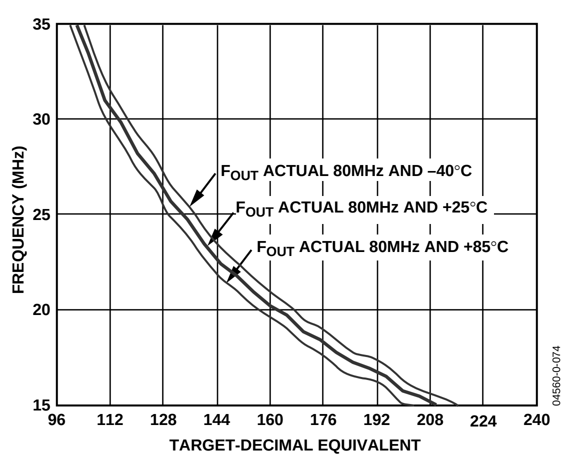

Figure 74. Temperature Drift of $f_{-3\ dB}$ for f_{ADC} = 80 MSPS and RxPGA = 0 dB

ANALOG TO DIGITAL CONVERTER (ADC)

The AD9866 features a 12-bit analog-to-digital converter (ADC) capable of up to 80 MSPS. Referring to Figure 68, the ADC is driven by the SPGA stage, which performs both the sample-and-hold and the fine gain adjust functions. A buffer amplifier (not shown) isolates the last CPGA gain stage from the dynamic load presented by the SPGA stage. The full-scale input span of the ADC is 2 V p-p, with the full-scale input span into the SPGA adjustable from 1 V to 2 V in 1 dB increments, depending on the PGA gain setting.

A pipelined multistage ADC architecture is used to achieve high sample rates while consuming low power. The ADC distributes the conversion over several smaller A/D subblocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage on each clock edge. The ADC typically performs best when driven internally by a 50% duty cycle clock. This is especially the case when operating the ADC at high sample rate (55 MSPS to 80 MSPS) and/or lower internal bias levels, which adversely affect interstage settling time requirements.

The ADC sampling clock path also includes a duty cycle restorer circuit, which ensures that the ADC gets a near 50% duty cycle clock even when presented with a clock source with poor symmetry (35/65). This circuit should be enabled, if the ADC sampling clock is a buffered version of the reference signal appearing at OSCIN (see the Clock Synthesizer section) and if this reference signal is derived from an oscillator or crystal whose specified symmetry cannot be guaranteed to be within 45/55 (or 55/45). This circuit can remain disabled, if the ADC sampling clock is derived from a divided down version of the clock synthesizer's VCO, because this clock is near 50%.

The ADC's power consumption can be reduced by 25 mA, with minimal effect on its performance, by setting Bit 4 of Reg. 0x07. Alternative power bias settings are also available via Reg. 0x13, as discussed in the Power Control and Dissipation section. Lastly, the ADC can be completely powered down for half-duplex operation, further reducing the AD9866's peak power consumption.

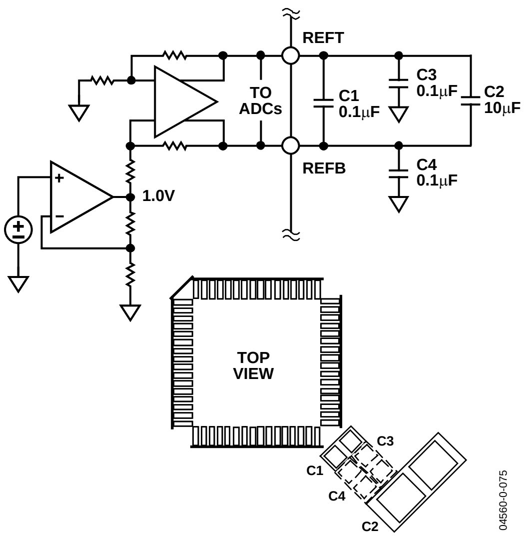

Figure 75. ADC Reference and Decoupling

The ADC has an internal voltage reference and reference amplifier as shown in Figure 75. The internal band gap reference generates a stable 1 V reference level that is converted to a differential 1 V reference centered about mid-supply (AVDD/2). The outputs of the differential reference amplifier are available at the REFT and REFB pins and *must* be properly decoupled for optimum performance. The REFT and REFB pins are conveniently situated at the corners of the CSP package such that C1 (0603 type) can be placed directly across its pins. C3 and C4 can be placed underneath C1, and C2 (10 µF tantalum) can be placed furthest from the package.

Table 21. SPI Registers for Rx ADC

Address (Hex)	Bit	Description
0x04	(5)	Duty cycle restore circuit
	(4)	ADC clock from PLL
0x07	(4)	ADC low power mode
0x13	(2:0)	ADC power bias adjust

AGC TIMING CONSIDERATIONS

When implementing a digital AGC timing loop, it is important to consider the Rx path latency and settling time of the Rx path in response to a change in gain setting. Figure 21 and Figure 24 show the RxPGA's settling response to a 60 dB and 5 dB change in gain setting when using the Tx[5:0] or PGA[5:0] port. While the RxPGA settling time may also show a slight dependency on the LPF's cutoff frequency, the ADC's pipeline delay along with the ADIO bus interface presents a more significant delay. The amount of delay or latency depends on whether a half- or full-duplex is selected. An impulse response at the RxPGA's input can be observed after 10.0 ADC clock cycles ($1/f_{ADC}$) in the case of a half-duplex interface and 10.5 ADC clock cycles in the case of a full-duplex interface. This latency along with the RxPGA settling time should be considered to ensure stability of the AGC loop.

CLOCK SYNTHESIZER

The AD9866 generates all its internal sampling clocks, as well as two user-programmable clock outputs appearing at CLKOUT1 and CLKOUT2, from a single reference source as shown in Figure 76. The reference source can be either a fundamental frequency or an overtone quartz crystal connected between OSCIN and XTAL with the parallel resonant load components as specified by the crystal manufacturer. It can also be a TTL-level clock applied to OSCIN with XTAL left unconnected.

The data rate, f_{DATA}, for the Tx and Rx data paths must always be equal. Therefore, the ADC's sample rate, f_{ADC}, is always equal to f_{DATA}, while the TxDAC update rate is a factor of 1, 2, or 4 of f_{DATA}, depending on the interpolation factor selected. The data rate refers to the word rate and should not be confused with the nibble rate in full-duplex interface.

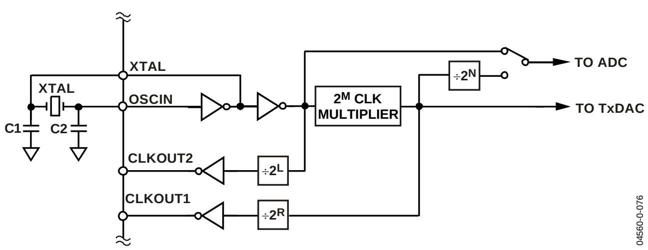

Figure 76. Clock Oscillator and Synthesizer

The 2^M CLK multiplier contains a PLL (with integrated loop filter) and VCO capable of generating an output frequency that is a multiple of 1, 2, 4, or 8 of its input reference frequency, f_{OSCIN}, appearing at OSCIN. The input frequency range of f_{OSCIN} is between 20 MHz and 80 MHz, while the VCO can operate over a 40 MHz to 200 MHz span. For the best phase noise/jitter characteristics, it is advisable to operate the VCO with a frequency between 100 MHz and 200 MHz. The VCO output drives the TxDAC directly such that its update rate, f_{DAC}, is related to f_{OSCIN} by the following equation:

$$f_{DAC} = 2^{M*} f_{OSCIN}$$

Equation 10.

where $M = 0, 1, 2$, or 3.

M is the PLL's multiplication factor set in Reg. 0x04. The value of M is determined by the Tx path's word rate, f_{DATA}, and digital interpolation factor, F, as shown in the following equation:

$$M = \log_2 (F * f_{DATA} / f_{OSCIN})$$

Equation 11.

Note that, if the reference frequency appearing at OSCIN is chosen to be equal to the AD9866's Tx and Rx path's word rate, then M is simply equal to $\log_2(F)$.

The clock source for the ADC can be selected in Reg. 0x04 as a buffered version of the reference frequency appearing at OSCIN (default setting) or a divided version of the VCO output (f_{DAC}). The first option is the default setting and most desirable, if f_{OSCIN} is equal to the ADC sample rate, f_{ADC}. This option typically results in the best jitter/phase noise performance for the ADC sampling clock. The second option is suitable in cases where f_{OSCIN} is a factor of 2 or 4 less than the f_{ADC}. In this case, the divider ratio, N, is chosen such that the divided down VCO output, f_{DAC}, is equal to the ADC sample rate, as shown in the following equation:

$$f_{DAC} = 2^{(M-N)} * f_{OSCIN}$$

Equation 12.

where $N = 0, 1$, or 2.

Figure 77 shows the degradation in phase noise performance imparted onto the ADC's sampling clock for different VCO output frequencies. In this case, a 25 MHz, 1 V p-p sinewave was used to drive OSCIN and the PLL's M and N factor were selected to provide an f_{ADC} of 50 MHz for a VCO operating frequency of 50, 100, and 200 MHz. The RxPGA input was driven with a near full-scale, 12.5 MHz input signal with a gain setting of 0 dB. Operating the VCO at the highest possible frequency results in the best narrow and wideband phase noise characteristics. For comparison purposes, the clock source for the ADC was taken directly from OSCIN when driven by a 50 MHz square wave.

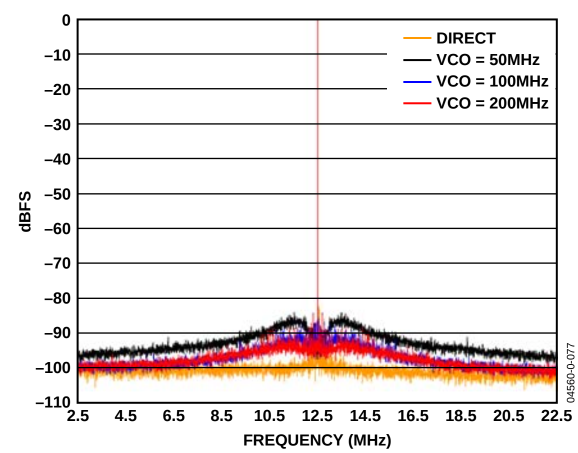

Figure 77. Comparison of Phase Noise Performance when ADC Clock Source Is Derived from Different VCO Output Frequencies

The CLK synthesizer also has two clock outputs appearing at CLKOUT1 and CLKOUT2. They are programmable via Reg. 0x06. Both outputs can be inverted or disabled. The voltage levels appearing at these outputs are relative to DRVDD and remain active during a hardware or software reset. Table 22 shows the SPI registers pertaining to the clock synthesizer.

CLKOUT1 is a divided version of the VCO output and can be set to be a submultiple integer of f_{DAC} ($f_{DAC}/2^R$, where R = 0, 1, 2, or 3). Because this clock is actually derived from the same set of dividers used within the PLL core, it is phase-locked to them such that its phase relationship relative to the signal appearing at OSCIN (or RXCLK)can be determined upon power-up. Also, this clock has near 50% duty cycle, because it is derived from the VCO. As a result, CLKOUT1 should be selected before CLKOUT2 as the primary source for system clock distribution.

CLKOUT2 is a divided version of the reference frequency, f_{OSCIN}, and can be set to be a submultiple integer of f_{OSCIN} ($f_{OSCIN}/2^L$, where L = 0, 1, or 2). With L set to 0, the output of CLKOUT2 is a delayed version of the signal appearing at OSCIN, exhibiting the same duty cycle characteristics. With L set to 1 or 2, the output of CLKOUT2 is a divided version of the OSCIN signal, exhibiting a near 50% duty cycle, but without having a deterministic phase relationship relative to CLKOUT1 (or RXCLK).

Table 22. SPI Registers for CLK Synthesizer

Address (Hex)	Bit	Description
0x04	(4)	ADC CLK from PLL
	(3:2)	PLL divide factor (P)
	(1:0)	PLL multiplication factor (M)
0x06	(7:6)	CLKOUT2 divide number
	(5)	CLKOUT2 invert
	(4)	CLKOUT2 disable
	(3:2)	CLKOUT1 divide number
	(1)	CLKOUT1 invert
	(0)	CLKOUT1 disable

POWER CONTROL AND DISSIPATION

POWER-DOWN

The AD9866 provides the ability to control the power-on state of various functional blocks. The state of the PWRDWN pin along with the contents of Reg. 0x01 and Reg. 0x02 allow two user-defined power settings that are pin selectable. The default settings[1] are such that Reg. 0x01 has all blocks powered on (all bits 0), while Reg. 0x02 has all blocks powered down excluding the PLL such that the clock signal remains available at CLKOUT1 and CLKOUT2. When the PWRDWN pin is low, the functional blocks corresponding to the bits in Reg. 0x01 are powered down. When the PWRDWN is high, the functional blocks corresponding to the bits in Reg. 0x02 are powered down. PWRDWN immediately affects the designated functional blocks with minimum digital delay.

Table 23. SPI Registers Associated with Power-Down and Half-Duplex Power Savings

Address (Hex)	Bit	Description	Comments
0x01	(7)	PLL	PWRDWN = 0
	(6)	TxDAC/IAMP	
	(5)	TX Digital	Default setting is all functional blocks powered on.
	(4)	REF	
	(3)	ADC CML	
	(2)	ADC	
	(1)	PGA BIAS	
	(0)	Rx PGA	
0x02	(7)	PLL	PWRDWN = 1
	(6)	TxDAC/IAMP	
	(5)	TX Digital	Default setting is all functional blocks powered off excluding PLL.
	(4)	REF	
	(3)	ADC CML	
	(2)	ADC	
	(1)	PGA BIAS	
	(0)	Rx PGA	
0x03	(7:3)	Tx OFF Delay	Half-duplex power savings.
	(2)	Rx PWRDWN via TXEN	
	(1)	Enable Tx PWRDWN	
	(0)	Enable Rx PWRDWN	

[1] With MODE = 1 and CONFIG = 1, Reg. 0x02 default settings are with all blocks powered off, with RXCLK providing a buffered version of the signal appearing at OSCIN. This setting results in the lowest power consumption upon power-up while still allowing AD9865 to generate the system clock via a crystal.

HALF-DUPLEX POWER SAVINGS

Significant power savings can be realized in applications having a half-duplex protocol allowing only the Rx or Tx path to be operational at any instance. The power-savings method depends on whether the AD9866 is configured for a full- or half-duplex interface. Functional blocks having fast power on/off times for the Tx and Rx path are controlled by the following bits: TxDAC/IAMP, Tx Digital, ADC, and RxPGA.

In the case of a full-duplex digital interface (MODE = 1), one can set Reg. 0x01 to 0x60 and Reg. 0x02 to 0x05 (or vice versa) such that the AD9866's Tx and Rx path are never powered on simultaneously. The PWRDWN pin can then be used to control what path is powered on, depending on the burst type. During a Tx burst, the Rx path's PGA and ADC blocks can typically be powered down within 100 ns, while the Tx paths DAC, IAMP, and digital filter blocks are powered up within 0.5 μs. For an Rx burst, the Tx path's can be powered down within 100 ns, while the Rx circuitry is powered up within 2 μs.

The $\overline{\text{TXQUIET}}$ pin can also be used with the full-duplex interface to quickly power down the IAMP and disable the interpolation filter by setting this pin low. This is meant to maintain backward compatibility with the AD9875/AD9876 MxFEs with the exception that the TxDAC remains powered if its IOUTP outputs are used. In most applications, the interpolation filter needs to be flushed with 0s before or after being powered down. This ensures that, upon power-up, the TxDAC (and IAMP) have a negligible differential dc offset, thus preventing spectral splatter due to an impulse transient.

Applications using a half-duplex interface (MODE = 0) can benefit from an additional power savings feature made available in Reg. 0x03. This register is effective only for a half-duplex interface. Besides providing power savings for half-duplex applications, this feature allows the AD9866 to be used in applications that need only its Rx (or Tx) path functionality through pin-strapping, making a serial port interface (SPI) optional. This feature also allows the PWRDWN pin to retain its default function as a master power control, as defined in Table 10.

The default settings for Reg. 0x03 provide fast power control of the functional blocks in the Tx and Rx signal paths (outlined above) using the TXEN pin. The TxDAC still remains powered on in this mode, while the IAMP is powered down. Significant current savings are typically realized when the IAMP is powered down.

For a Tx burst, the falling edge of TXEN is used to generate an internal delayed signal for powering down the Tx circuitry. Upon receipt of this signal, power-down of the Tx circuitry occurs within 100 ns. The user-programmable delay for the Tx path power-down is meant to match the pipeline delay of the last Tx burst sample such that power-down of the TxDAC and IAMP does not impact its transmission. A 5-bit field in Reg. 0x03 sets the delay from 0 to 31 TXCLK clock cycles, with the default being 31 (0.62 µs with f_{TxCLK} = 50 MSPS). The digital interpolation filter is automatically flushed with midscale samples prior to power-down, if the clock signal into the TXCLK pin is present for 33 additional clock cycles after TXEN returns low. For an Rx burst, the rising edge of TXEN is used to generate an internal signal (with no delay) that powers up the Tx circuitry within 0.5 µs.

The Rx path power-on/power-off can be controlled by either TXEN or RXEN by setting Bit 2 of Reg. 0x03. In the default setting, the falling edge of TXEN powers up the Rx circuitry within 2 µs, while the rising edge of TXEN powers down the Rx circuitry within 0.5 µs. If RXEN is selected as the control signal, then its rising edge powers up the Rx circuitry and the falling edge powers it down. It is possible to disable the fast power-down of the Tx and/or Rx circuitry by setting Bit 1 and/or Bit 0 to 0.

POWER REDUCTION OPTIONS

The power consumption of the AD9866 can be significantly reduced from its default setting by optimizing the power consumption versus performance of the various functional blocks in the Tx and Rx signal path. On the Tx path, minimum power consumption is realized when the TxDAC output is used directly and its standing current, I, is reduced to as low as 1 mA. Although a slight degradation in THD performance results at reduced standing currents, it often remains adequate for most applications, because the op amp driver typically limits the overall linearity performance of the Tx path. The load resistors used at the TxDAC outputs (IOUTP+ and IOUTP−) can be increased to generate an adequate differential voltage that can be further amplified via a power efficient op amp based driver solution. Figure 78 shows how the supply current for the TxDAC (Pin 43) is reduced from 55 mA to 14 mA as the standing current is reduced from 12.5 mA to 1.25 mA. Further Tx power savings can be achieved by bypassing or reducing the interpolation factor of the digital filter as shown in Figure 79.

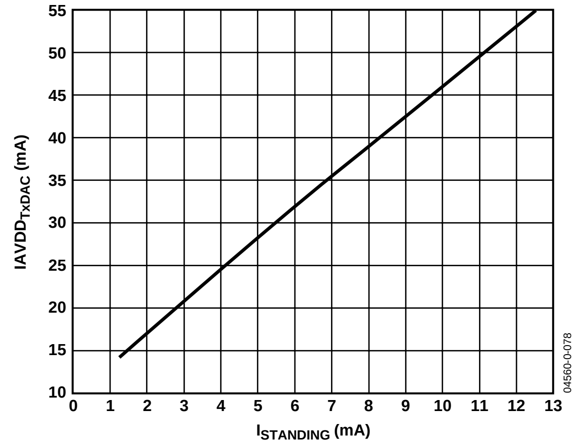

Figure 78. Reduction in TxDAC's Supply Current vs. Standing Current

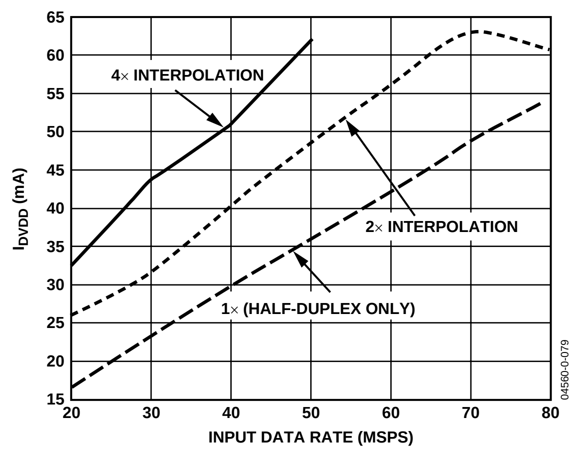

Figure 79. Digital Supply Current Consumption vs. Input Data Rate (DVDD = DRVDD =3.3 V and $f_{OUT} = f_{DATA}/10$)

Power consumption on the Rx path can be achieved by reducing the bias levels of the various amplifiers contained within the RxPGA and ADC. As previously noted, the RxPGA consists of two CPGA amplifiers and one SPGA amplifier. The bias levels of each of these amplifiers along with the ADC can be controlled via Reg. 0x13 as shown in Table 24. The default setting for 0x13 is 0x00.

Table 24. SPI Register for RxPGA and ADC Biasing

Address (Hex)	Bit	Description
0x07	(4)	ADC low power
0x13	(7:5)	CPGA bias adjust
	(4:3)	SPGA bias adjust
	(2:0)	ADC power bias adjust

Because the CPGA processes signals in the continuous time domain, its performance versus bias setting remains mostly independent of the sample rate. Table 25 shows how the typical current consumption seen at AVDD (Pins 35 and 40) varies as a function of Bits (7:5), while the remaining bits are maintained at their default setting of 0. Only four of the possible settings result in any reduction in current consumption relative to the default setting. Reducing the bias level typically results in a degradation in the THD versus frequency performance as shown in Figure 80 due to a reduction of the amplifier's unity gain bandwidth, while the SNR performance remains relatively unaffected.

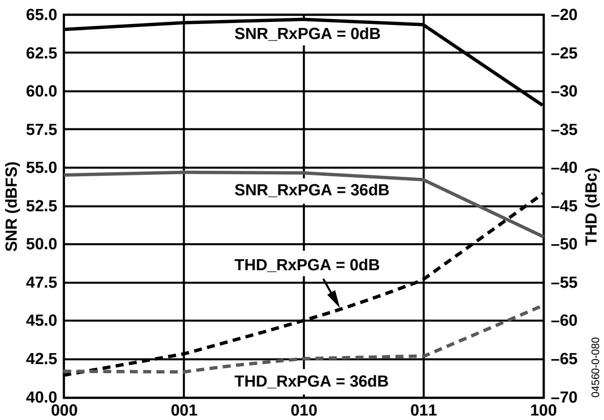

Figure 80. THD vs. f_{IN} Performance and RxPGA Bias Settings (000,001,010,100 with RxPGA = 0 and +36 dB and AIN = −1 dBFS, LPF set to 26 MHz and f_{ADC} = 50 MSPS)

Table 25. Analog Supply Current vs. CPGA Bias Settings at f_{ADC} = 65 MSPS

Bit 7	Bit 6	Bit 5	Δ mA
0	0	0	0
0	0	1	−27
0	1	0	−42
0	1	1	−51
1	0	0	−55
1	0	1	27
1	1	0	69
1	1	1	27

The SPGA is implemented as a switched capacitor amplifier. Therefore, its performance versus bias level is mostly dependent on the sample rate. Figure 81 shows how the typical current consumption seen at AVDD (Pins 35 and 40) varies as a function of bits (4:3) and sample rate, while the remaining bits are maintained at their default setting of 0. Figure 81 shows how the SNR and THD performance is affected for a 10 MHz sine wave input as the ADC sample rate is swept from 20 MHz to 80 MHz.

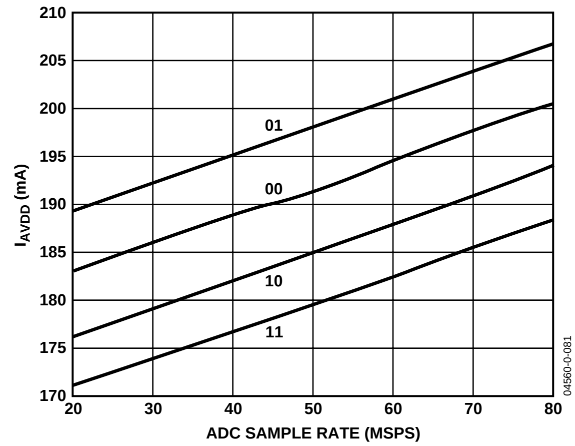

Figure 81. AVDD Current vs. SPGA Bias Setting and Sample Rate

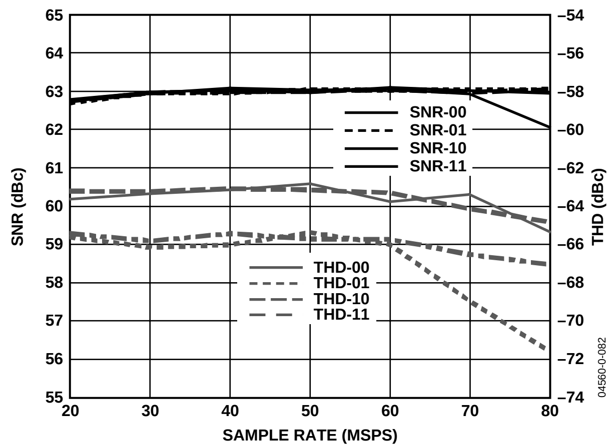

Figure 82. SNR and THD Performance vs. f_{ADC} and SPGA Bias Setting with RxPGA = 0 dB, f_{IN} = 10 MHz. AIN = −1 dBFS

The ADC is based on a pipeline architecture with each stage consisting of a switched capacitor amplifier. Therefore, its performance versus bias level is also mostly dependent on the sample rate. Figure 83 shows how the typical current consumption seen at AVDD (Pins 35 and 40) varies as a function of bits (2:0) and sample rate, while the remaining bits are maintained at their default setting of 0. Setting Bit 4 or Reg. 0x07 corresponds to the 011 setting, and the settings of 101 and 111 result in higher current consumption. Figure 84 shows how the SNR and THD performance are affected for a 10 MHz sine wave input for the lower power settings as the ADC sample rate is swept from 20 MHz to 80 MHz.

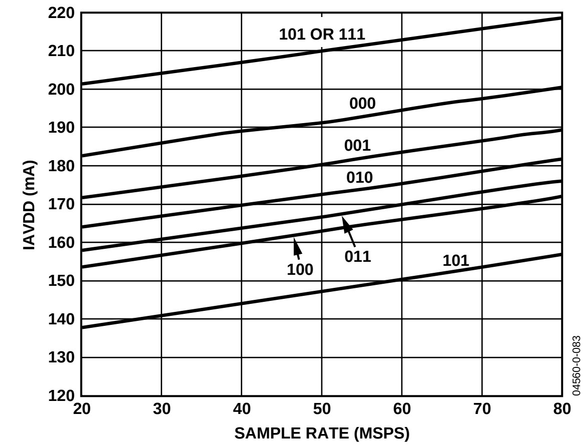

Figure 83. AVDD Current vs. ADC Bias Setting and Sample Rate

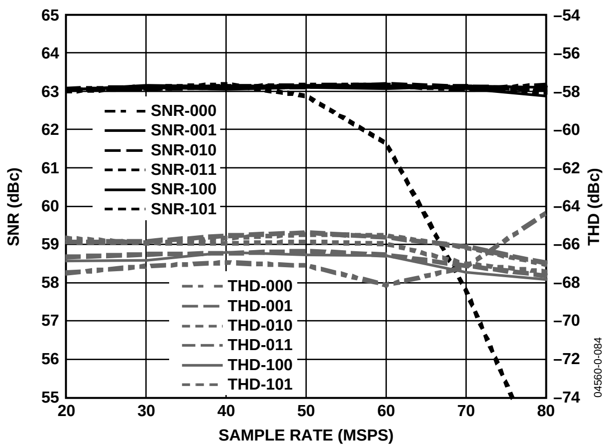

Figure 84. SNR and THD Performance vs. f_{ADC} and SPGA Bias Setting with RxPGA = 0 dB, f_{IN} = 10 MHz, AIN = −1 dBFS

A sine wave input is a standard and convenient method of analyzing the performance of a system. However, the amount of power reduction that is possible is application dependent, based on the nature of the input waveform (such as frequency content, peak-to-rms ratio), the minimum ADC sample, and the minimum acceptable level of performance. As a result, it is advisable that power-sensitive applications optimize the power bias setting of the Rx path using an input waveform that is representative of the application.

POWER DISSIPATION

The power dissipation of the AD9866 can become quite high in full-duplex applications in which the Tx and Rx paths are simultaneously operating with nominal power bias settings. In fact, some applications desiring to use the IAMP may need to either reduce its peak power capabilities or reduce the power consumption of the Rx path, so that the device's maximum allowable power consumption, P_{MAX}, is not exceeded.

P_{MAX} is specified at 1.66 W to ensure that the die temperature does not exceed 125°C at an ambient temperature of 85°C. This specification is based on the 64-pin LFSCP having a thermal resistance, θ_{JA}, of 24°C/W with its heat slug soldered. (The θ_{JA} is 30.8°C/W, if the heat slug remains unsoldered.) If a particular application's maximum ambient temperature, T_A, falls below 85°C, the maximum allowable power dissipation can be determined by the following equation:

$$P_{MAX} = 1.66 + (85 - T_A)/24$$

Equation 13.

Assuming that the IAMP's common-mode bias voltage is operating off the same analog supply as the AD9866, the following equation can be used to calculate the maximum total current consumption, I_{MAX}, of the IC:

$$I_{MAX} = (P_{MAX} - P_{IAMP})/3.47$$

Equation 14.

With an ambient temperature of up to 85°C, I_{MAX} is 478 mA.

If the IAMP is operating off a different supply or in the voltage mode configuration, first calculate the power dissipated in the IAMP, P_{IAMP}, using Equation 2 or Equation 5, and then recalculate I_{MAX}, using the following equation:

$$I_{MAX} = (P_{MAX} - P_{IAMP})/3.47$$

Equation 15.

Figure 78, Figure 79, Figure 81, and Figure 83 can be used to calculate the current consumption of the Rx and Tx paths for a given setting.

MODE SELECT UPON POWER-UP AND RESET

The AD9866 power-up state is determined by the logic levels appearing at the MODE and CONFIG pins. The MODE pin is used to select a half- or full-duplex interface by pin strapping it low or high, respectively. The CONFIG pin is used in conjunction with the MODE pin to determine the default settings for the SPI registers as outlined in Table 10.

The intent of these particular default settings is to allow some applications to avoid using the SPI (disabled by pin-strapping $\overline{\text{SEN}}$ high), thereby reducing the implementation cost. For example, setting MODE low and CONFIG high configures the AD9866 to be backward compatible with the AD9975, while setting MODE high and CONFIG low makes it backward compatible with the AD9875. Other applications must use the SPI to configure the device.

A hardware ($\overline{\text{RESET}}$ pin) or software (Bit 5 of Reg. 0x00) reset can be used to place the AD9866 into a known state of operation as determined by the state of the MODE and CONFIG pins. A dc offset calibration and filter tuning routine is also initiated upon a hardware reset, but not with a software reset. Neither reset method flushes the digital interpolation filters in the Tx path. Refer to the Half-Duplex Mode and Full-Duplex Mode sections for information on flushing the digital filters.

A hardware reset can be triggered by pulsing the $\overline{\text{RESET}}$ pin low for a minimum of 50 ns. The SPI registers are instantly reset to their default settings upon $\overline{\text{RESET}}$ going low, while the dc offset calibration and filter tuning routine is initiated upon $\overline{\text{RESET}}$ returning high. To ensure sufficient power-on time of the various functional blocks, $\overline{\text{RESET}}$ returning high should occur no less than 10 ms upon power-up. If a digital reset signal from a microprocessor reset circuit (such as ADM1818) is not available, a simple R-C network referenced to DVDD can be used to hold $\overline{\text{RESET}}$ low for approximately 10 ms upon power-up.

ANALOG AND DIGITAL LOOP-BACK TEST MODES

The AD9866 features analog and digital loop-back capabilities that can assist in system debug and final test. Analog loop-back routes the digital output of the ADC back into the Tx data path prior to the interpolation filters such that the Rx input signal can be monitored at the output of the TxDAC or IAMP. As a result, the analog loop-back feature can be used for a half- or full-duplex interface, to allow testing of the functionality of the entire IC (excluding the digital data interface).

For example, the user can configure the AD9866 with similar settings as the target system, inject an input signal (sinusoidal waveform) into the Rx input, and monitor the quality of the reconstructed output from the TxDAC or IAMP to ensure a minimum level of performance. In this test, the user can also exercise the RxPGA as well as validate the attenuation characteristics of the RxLPF. Note that the RxPGA gain setting should be selected such that the input does not result in clipping of the ADC.

Digital loop-back can be used to test the full-duplex digital interface of the AD9866. In this test, data appearing on the Tx[5:0] port is routed back to the Rx[5:0] port, thereby confirming proper bus operation. The Rx port can also be three-stated for half- and full-duplex interfaces.

Table 26. SPI Registers for Test Modes

Address (Hex)	Bit	Description
0x0D	(7)	Analog loop-back
	(6)	Digital loop-back
	(5)	Rx port three-state

PCB DESIGN CONSIDERATIONS

Although the AD9866 is a mixed-signal device, the part should be treated as an analog component. The on-chip digital circuitry has been specially designed to minimize the impact of its digital switching noise on the MxFE's analog performance.

To achieve the best performance, the power, grounding, and layout recommendations in this section should be followed. Assembly instructions for the micro-lead frame package can be found in an application note from Amkor at: http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf.

COMPONENT PLACEMENT

If the three following guidelines of component placement are followed, chances for getting the best performance from the MxFE are greatly increased. First, manage the path of return currents flowing in the ground plane so that high frequency switching currents from the digital circuits do not flow on the ground plane under the MxFE or analog circuits. Second, keep noisy digital signal paths and sensitive receive signal paths as short as possible. Third, keep digital (noise generating) and analog (noise susceptible) circuits as far away from each other as possible.

To best manage the return currents, pure digital circuits that generate high switching currents should be closest to the power supply entry. This keeps the highest frequency return current paths short and prevents them from traveling over the sensitive MxFE and analog portions of the ground plane. Also, these circuits should be generously bypassed at each device, which further reduces the high frequency ground currents. The MxFE should be placed adjacent to the digital circuits, such that the ground return currents from the digital sections do not flow in the ground plane under the MxFE.

The AD9866 has several pins that are used to decouple sensitive internal nodes. These pins are REFIO, REFB, and REFT. The decoupling capacitors connected to these points should have low ESR and ESL. These capacitors should be placed as close to the MxFE as possible (see Figure 75) and be connected directly to the analog ground plane. The resistor connected to the REFADJ pin should also be placed close to the device and connected directly to the analog ground plane.

POWER PLANES AND DECOUPLING

While the AD9866 evaluation board demonstrates a very good power supply distribution and decoupling strategy, it can be further simplified for many applications. The board has four layers: two signal layers, one ground plane, and one power plane. While the power plane on the evaluation board is split into multiple analog and digital subsections, a permissible alternative would be to have AVDD and CLKVDD share the same analog 3.3 V power plane. A separate analog plane/supply may be allocated to the IAMP, if its supply voltage differs from the 3.3 V required by AVDD and CLKVDD. On the digital side, DVDD and DRVDD can share the same 3.3 V digital power plane. This digital power plane brings the current used to power the digital portion of the MxFE and its output drivers. This digital plane should be kept from going underneath the analog components.

The analog and digital power planes allocated to the MxFE may be fed from the same low noise voltage source; however, they should be decoupled from each other to prevent the noise generated in the digital portion of the MxFE from corrupting the AVDD supply. This can be done by using ferrite beads between the voltage source and the respective analog and digital power planes with a low ESR, bulk decoupling capacitor on the MxFE side of the ferrite. Each of the MxFE's supply pins (AVDD, CLKVDD, DVDD, and DRVDD) should also have a dedicated low ESR, ESL decoupling capacitors. The decoupling capacitors should be placed as close to the MxFE supply pins as possible.

GROUND PLANES

The AD9866 evaluation board uses a single serrated ground plane to help prevent any high frequency digital ground currents from coupling over to the analog portion of the ground plane. The digital currents affiliated with the high speed data bus interface (Pins 1–16) have the highest potential of generating problematic high frequency noise. A ground serration that contains these currents should reduce the effects of this potential noise source.

The ground plane directly underneath the MxFE should be continuous and uniform. The 64-lead LFCSP package is designed to provide excellent thermal conductivity. This is partly achieved by incorporating an exposed die paddle on the bottom surface of the package. However, to take full advantage of this feature, the PCB must have features to effectively conduct heat away from the package. This can be achieved by incorporating thermal pad and thermal vias on the PCB. While a thermal pad provides a solderable surface on the top surface of the PCB (to solder the package die paddle on the board), thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat.

Lastly, all ground connections should be made as short as possible. This results in the lowest impedance return paths and the quietest ground connections.

SIGNAL ROUTING

The digital Rx and Tx signal paths should be kept as short as possible. Also, the impedance of these traces should have a controlled characteristic impedance of about 50 Ω. This prevents poor signal integrity and the high currents that can occur during undershoot or overshoot caused by ringing. If the signal traces cannot be kept shorter than about 1.5 inches, series termination resistors (33 Ω to 47 Ω) should be placed close to all digital signal sources. It is a good idea to series-terminate all clock signals at their source, regardless of trace length.

The receive RX+ and RX− signals are the most sensitive signals on the entire board. Careful routing of these signals is essential for good receive path performance. The RX+ and RX− signals form a differential pair and should be routed together as a pair. By keeping the traces adjacent to each other, noise coupled onto the signals appears as common mode and is largely rejected by the MxFE receive input. Keeping the driving point impedance of the receive signal low and placing any low-pass filtering of the signals close to the MxFE further reduces the possibility of noise corrupting these signals.

EVALUATION BOARD

An evaluation board is available for the AD9865 and AD9866. The digital interface to the evaluation board can be configured for a half- or full-duplex interface. Two 40-pin and one 26-pin male right angle headers (0.100 inches) provide easy interfacing to test equipment such as digital data capture boards, pattern generators, or custom digital evaluation boards (FPGA, DSP, or ASIC). The reference clock source can originate from an external generator, crystal oscillator, or crystal. Software and an interface cable are included to allow for programming of the SPI registers via a PC.

The analog interface on the evaluation board provides a full analog front-end reference design for power line applications. It includes a power line socket, line transformer, protection diodes, and passive filtering components. An auxiliary path allows independent monitoring of the ac power line. The evaluation board allows complete optimization of power line reference designs based around the AD9865 or AD9866.

Alternatively, the evaluation board allows independent evaluation of the TxDAC, IAMP, and Rx paths via SMA connectors. The IAMP can be easily configured for a voltage or current mode interface via jumper settings. The TxDAC's performance can be evaluated directly or via an optional dual op amp driver stage. The Rx path includes a transformer and termination resistor, allowing for a calibrated differential input signal to be injected into its front end.

More information on the AD9866 evaluation board can be found at:
http://www.analog.com/Analog_Root/productPage/productHome/0%2C2121%2CAD9866%2C00.html.

OUTLINE DIMENSIONS

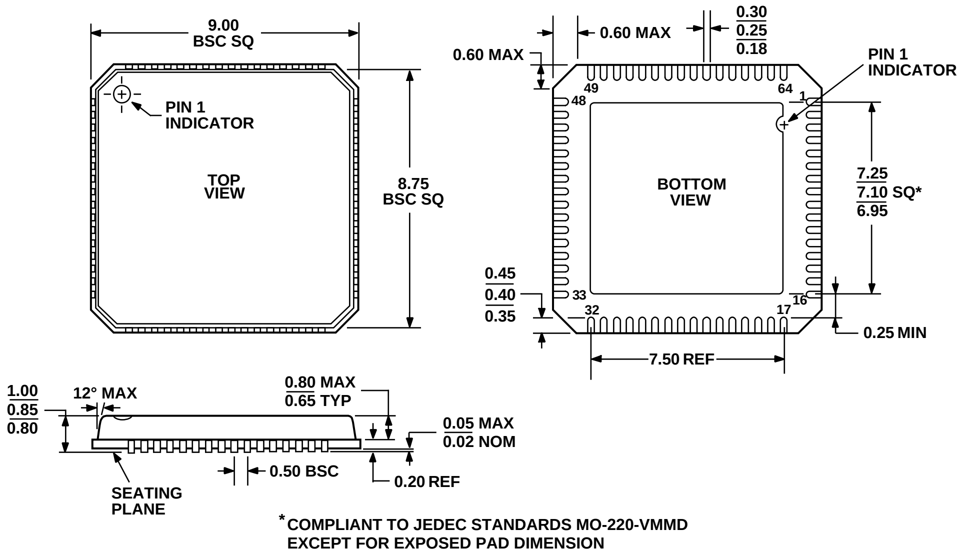

Figure 85. 64-Lead Lead Frame Chip Scale Package (LFCSP)
[CP-64-3]
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9866BCP	–40°C to +85°C	64-Lead LFCSP	CP-64-3
AD9866BCPRL	–40°C to +85°C	64-Lead LFCSP	CP-64-3
AD9866CHIPS	–40°C to +85°C	Chip	
AD9866-EB	25°C	Evaluation Board	

NOTES