AZC199-02S

Low Capacitance High ESD Level Protection Array For High Speed I/O Port

Features

- ESD Protect for 2 high-speed I/O lines
- Provide ESD protection for each line to
  IEC 61000-4-2,(ESD) (contact/air) ±16kV
  IEC 61000-4-4 (EFT) Level-3, 55A (5/50ns)
  IEC 61000-4-5 (Lightning) 5A (8/20μs)
- For low operating voltage applications: 5V, 4.2V, 3.3V, 2.5V etc.
- Low capacitance : 1.6pF typical
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS diode
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- **Video Graphics Cards**
- **Digital Visual Interface (DVI)**
- USB2.0 Power and Data lines protection
- Notebook and PC Computers
- Monitors and Flat Panel Displays

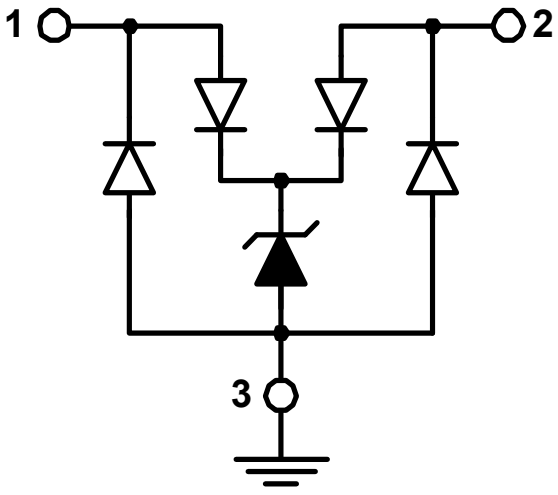
Description

AZC199-02S is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZC199-02S has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

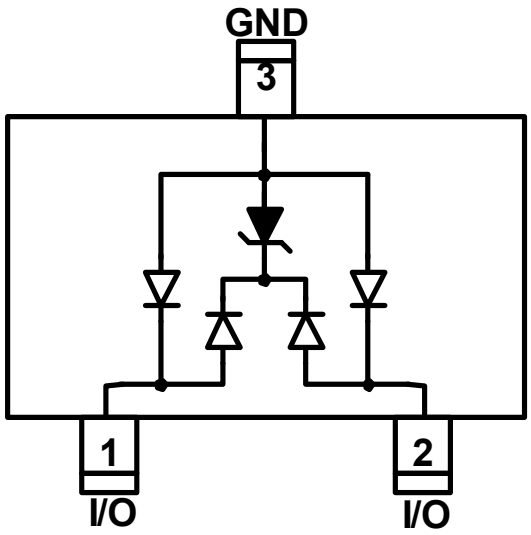
AZC199-02S is a unique design which includes ESD rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to ground line. The internal unique design of clamping cell prevents over-voltage on the data line, protecting any downstream components.

AZC199-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



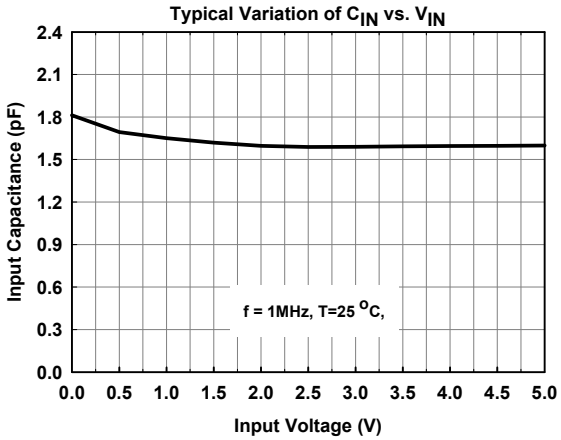
JEDEC SOT23-3L (Top View)

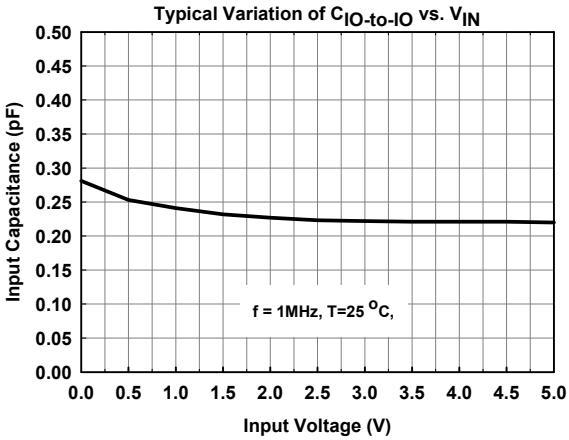
SPECIFICATIONS

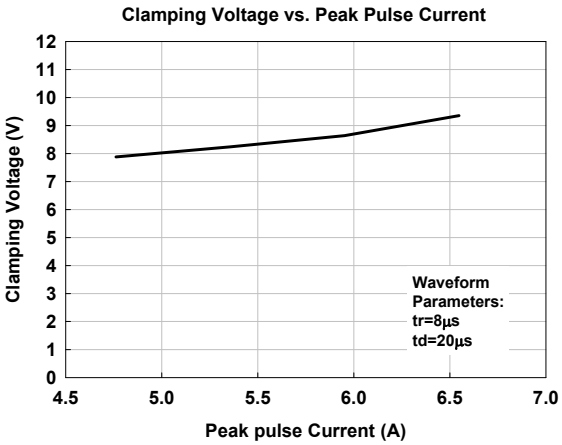
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs)	I_{PP}	5	**A**
Operating Supply Voltage	V_{DC}	6	**V**
ESD per IEC 61000-4-2 (Air/Contact)	V_{ESD}	±16	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +85	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	**V**

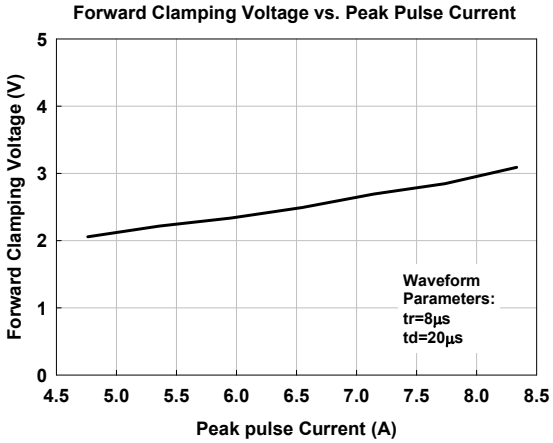
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Leakage Current	I_{Leak}	$V_{pin1\ or\ pin2}$ = 5V, V_{Pin3} = 0V, T=25 °C			1	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, Pin 1/2 to Pin 3	7		10	**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C, Pin 3 to Pin1/2		0.85	1.1	**V**
ESD Clamping Voltage	V_{clamp}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Pin 1/2 to Pin 3		11		**V**
ESD Dynamic Turn on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+6kV,T=25 °C, Contact mode, Pin 1/2 to Pin 3		0.3		**Ω**
Lightning Clamping Voltage	$V_{lightning}$	I_{PP}=5A, tp=8/20μs, T=25 °C Pin 1/2 to Pin 3		8.5		**V**
Channel Input Capacitance	C_{IN}	V_{pin3}=0V,**$V_{pin1\ or\ 2}$=2.5V**, f=1MHz,T=25°C, Pin 1/2 to Pin 3		1.6	1.9	**pF**
Channel to Channel Input Capacitance	C_{CROSS}	V_{pin3} =0V, **$V_{pin1\ or\ 2}$=2.5V**, f=1MHz, T=25°C, Between Pin 1 and Pin 2		0.23	0.28	**pF**
Variation of Channel Input Capacitance	$\triangle C_{IN}$	V_{pin3} =0V, **$V_{pin1\ or\ 2}$=2.5V**, f=1MHz, T=25°C, (Pin 1 to Pin 3)–(Pin 2 to Pin 3)		0.06	0.08	**pF**

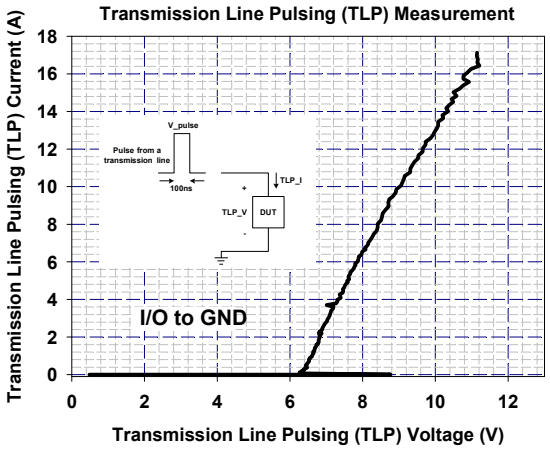
Typical Characteristics











Applications Information

The AZC199-02S is designed to protect two lines against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZC199-02S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and 2. The pin 3 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZC199-02S should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZC199-02S.
- Place the AZC199-02S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

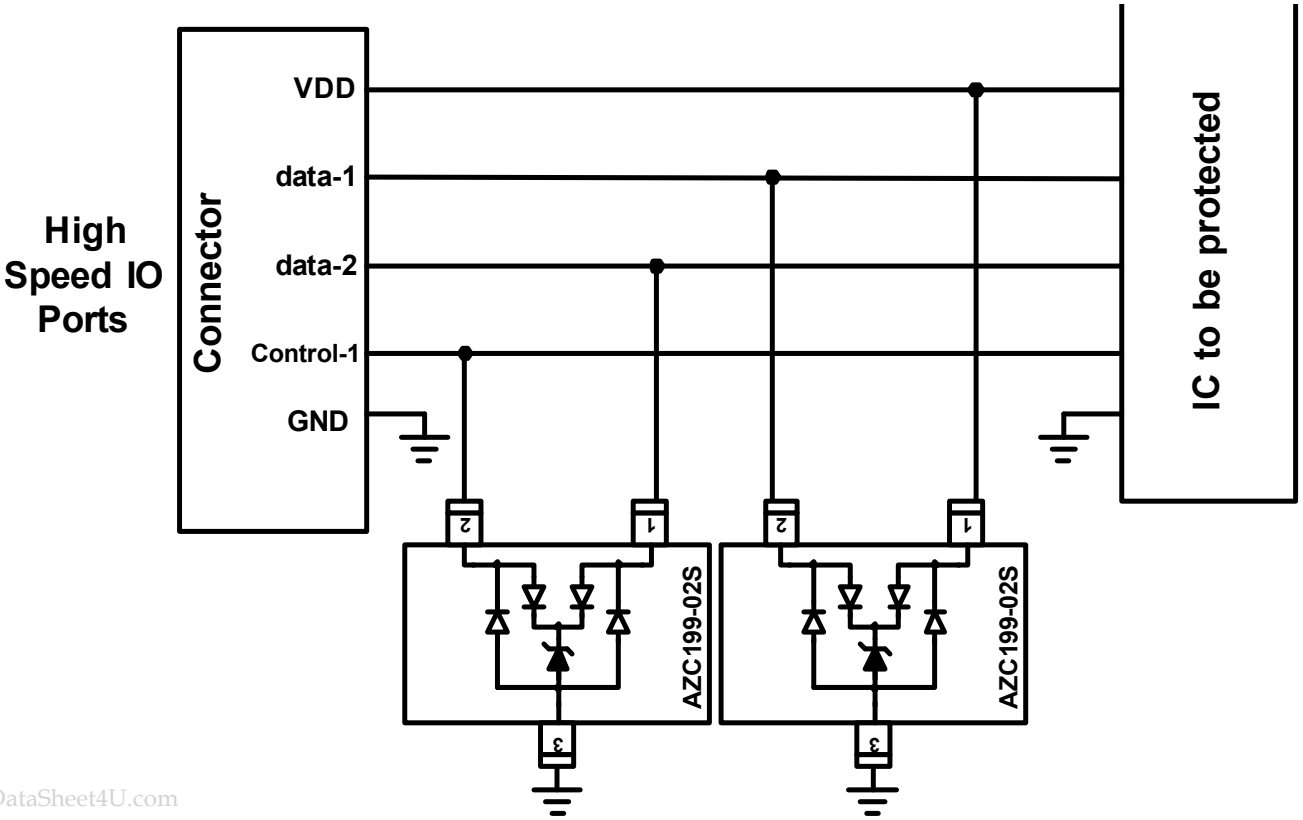


Fig. 1

Fig. 2 shows another simplified example of using AZC199-02S to protect the control lines, high speed data lines, and power lines from ESD transient stress.

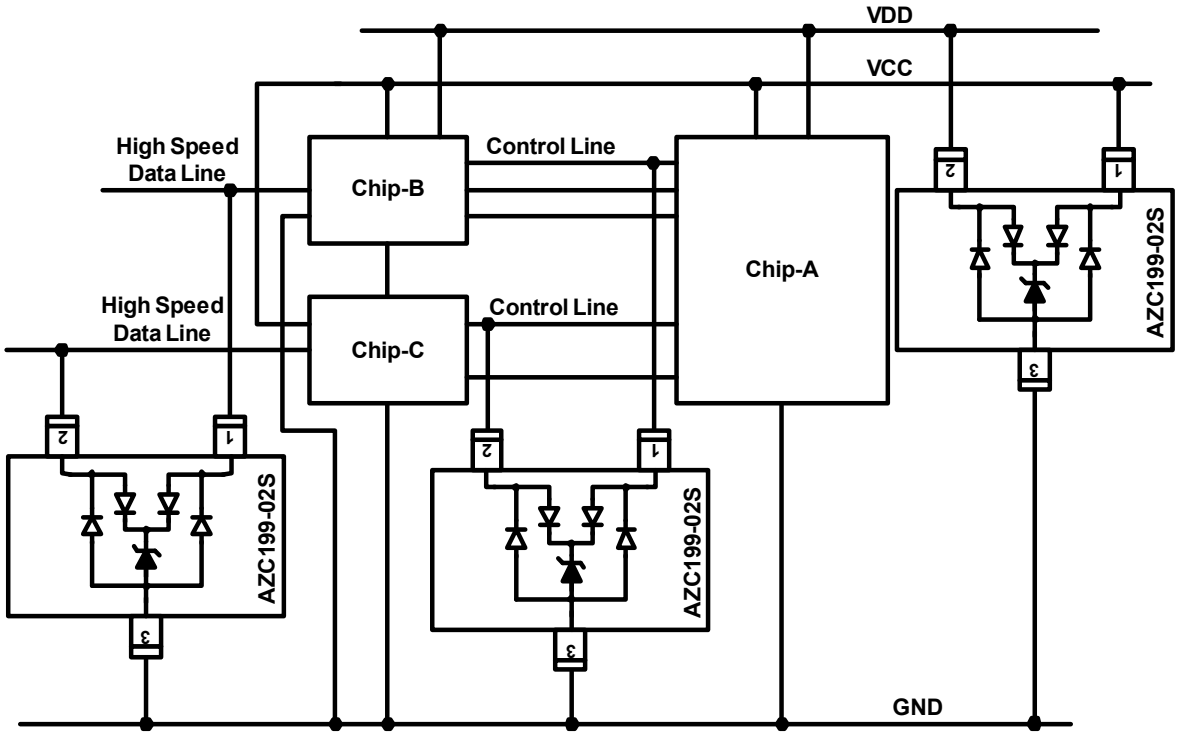
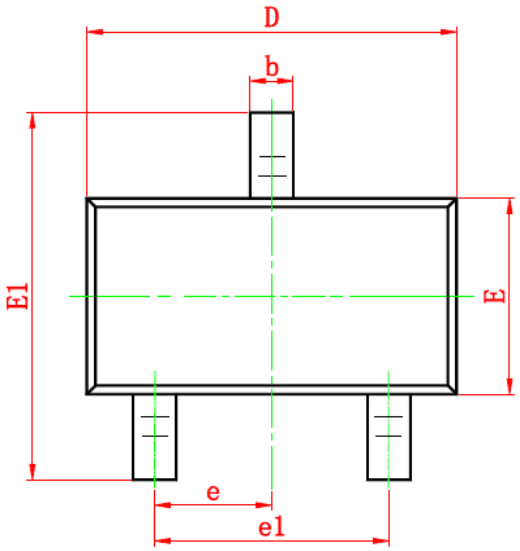


Fig. 2

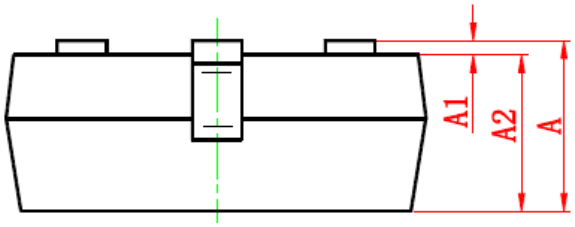
Mechanical Details

SOT23-3L PACKAGE DIAGRAMS

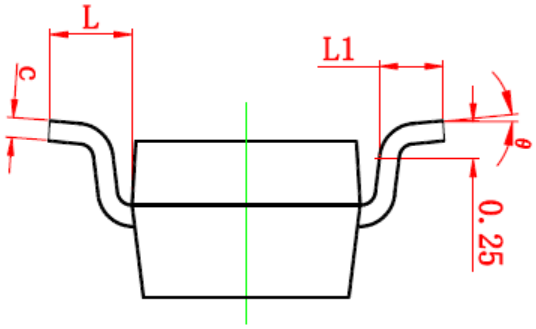
TOP VIEW



SIDE VIEW



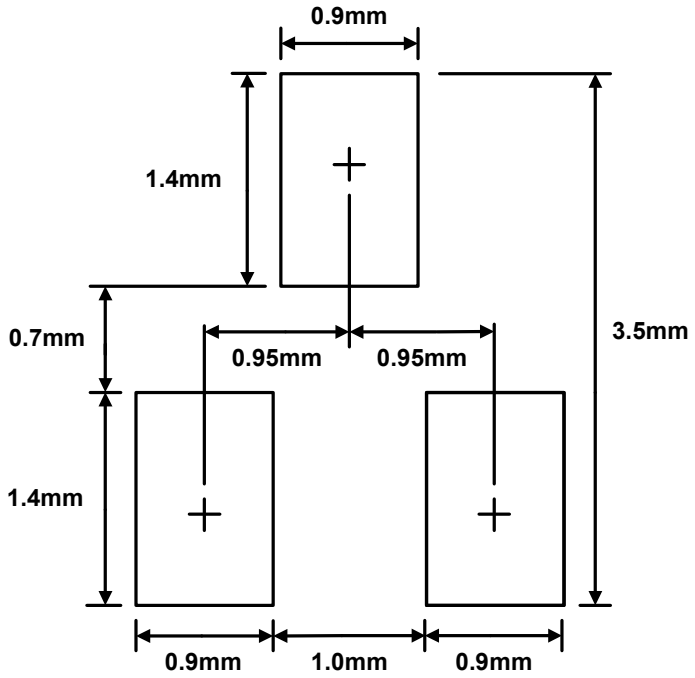
END VIEW



PACKAGE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°

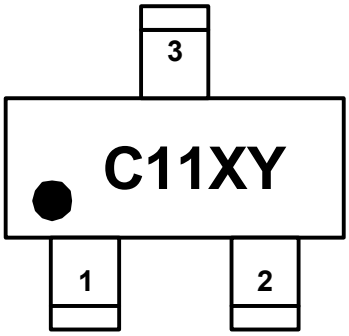
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



C11 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZC199-02S	C11XY

Revision History

Revision	Modification Description
Revision 2009/03/12	Initial Formal Release.