GM16C450/82C50A
ASYNCHRONOUS COMMUNICATIONS ELEMENT

General Description

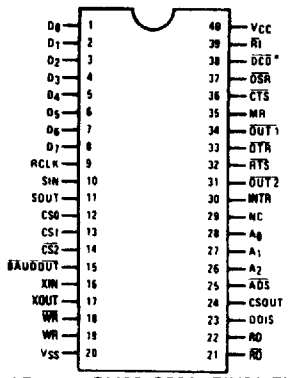
The GM16C450 is an improved specification version of the GM82C50A Asynchronous Communications Element (ACE). The improved specifications ensure compatibility with state-of-the-art CPUs. Functionally, the GM16C450 is equivalent to the GM82C50A.
The GM16C450 and GM82C50A each function as a serial data input/output interface in a microcomputer system. The functional conifguration of the ACEs is programmed by the system software via a 3-state 8-bit bidirectional data bus; this includes the on-board baud rate generator.
The ACE performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the ACE, as well as any error conditions (parity, overrun, framing or break interrupt).
The ACE includes a programmable baud generator that is capable of dividing the timing reference clock input by a divisor between 1 and (2 to the power of 16 - 1), and producing a 16x clock for driving the internal transmitter logic. Provisions are also include to use this 16x clock to drive the receiver logic. Also included in the ACE is a complete modem control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.
In additional, the GM16C450/GM82C50A runs at a maximum speed of 16 MHz.

Features

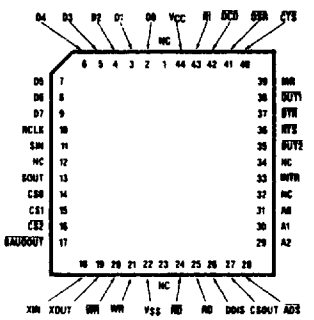
- Easily interfaces to most popular microprocessors
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from serial data stream
- Full double-buffering eliminates need for precise synchronization
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud generator allows division of any input clock by 1 to (2 to the power of 16 - 1) and generates the internal 16x clock
- Independent receiver clock input
- Moderm control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$ and $\overline{DCD}$)
- Fully programmable serial interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1-, 1.5- or 2-stop bit generation
  - Baud generation (DC to 56k baud)
- False start bit detection
- Complete status reporting capabilities
- 3-state TTL drive capabilities for bidirectional
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
  - Fully prioritized interrupt system controls
- Compatible with PS/2 system speed data bus and control bus
- Line break generation and detection

Pin Configuration

Dual-In-Line Package



PLCC Package



*On the GM82 C50A, PIN38(PIN42 on the PLCC PACKAGE) is also called $\overline{RLSD}$

1.0 Absolute Maximum Ratings

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	700 mW

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

2.0 DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	GM16C450		GM82C50A		Units
			Min	Max	Min	Max	
V_{ILX}	Clock Input Low Voltage		−0.5	0.8	−0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input Low Voltage		−0.5	0.8	−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all (Note 2)		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0 mA (Note 2)	2.4		2.4		V
I_{CC}(AV)	Avg. Power Supply Current (V_{CC})	V_{CC} = 5.25V, T_A = 25°C No Loads on output SIN, DSR, DCD, CTS, RI = 2.4V All other inputs = 0.4V Baud Rate Generator at 4 MHz Baud Rate at 50k		10		10	mA
I_{IL}	Input Leakage	V_{CC} = 5.25V, V_{SS} = 0V All other pins floating.		±10		±10	µA
I_{CL}	Clock Leakage	V_{IN} = 0V, 5.25V		±10		±10	µA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 5.25V, V_{SS} = 0V V_{OUT} = 0V, 5.25V 1) Chip deselected 2) WRITE mode, chip selected		±20		±20	µA
V_{ILMR}	MR Schmitt V_{IL}			0.8		0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		2.0		V

Capacitance T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{XIN}	Clock Input Capacitance	f_C = 1 MHz Unmeasured pins returned to V_{SS}		15	20	pF
C_{XOUT}	Clock Output Capacitance			20	30	pF
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			10	20	pF

Note 1: Inputs on the CMOS parts are TTL compatible outputs on the CMOS parts drive to GND and V_{CC}

Note 2: Does not apply to XOUT

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Conditions	GM 16C450		GM 82C50A		Units
			Min	Max	Min	Max	
t_{ADS}	Address Strobe Width		60		90		ns
t_{AH}	Address Hold Time		0		0		ns
t_{AR}	RD, $\overline{RD}$ Delay from Address	(Note 1)	60		80		ns
t_{AS}	Address Setup Time		60		90		ns
t_{AW}	WR, $\overline{WR}$ Delay from Address	(Note 1)	60		80		ns
t_{CH}	Chip Select Hold Time		0		0		ns
t_{CS}	Chip Select Setup Time		60		90		ns
t_{CSC}	Chip Select Output Delay from Select	@100 pF loading (Note 1)		100		125	ns
t_{CSR}	RD, $\overline{RD}$ Delay from Chip Select	(Note 1)	50		80		ns
t_{CSW}	WR, $\overline{WR}$ Delay from Select	(Note 1)	50		80		ns
t_{DH}	Data Hold Time		40		60		ns
t_{DS}	Data Setup Time		40		90		ns
t_{HZ}	RD, $\overline{RD}$ to Floating Data Delay	@100 pF loading (Note 3)	0	100	0	100	ns
t_{MR}	Master Reset Pulse Width		5		10		μs
t_{RA}	Address Hold Time from RD, $\overline{RD}$	(Note 1)	20		20		ns
t_{RC}	Read Cycle Delay		175		500		ns
t_{RCS}	Chip Select Hold Time from RD, $\overline{RD}$	(Note 1)	20		20		ns
t_{RD}	RD, $\overline{RD}$ Strobe Width		125		175		ns
t_{RDD}	RD, $\overline{RD}$ to Driver Disable Delay	@100 pF loading (Note 3)		60		75	ns
t_{RVD}	Delay from RD, $\overline{RD}$ to Data	@100 pF loading		125		175	ns
t_{WA}	Address Hold Time from WR, $\overline{WR}$	(Note 1)	20		20		ns
t_{WC}	Write Cycle Delay		200		500		ns
t_{WCS}	Chip Select Hold Time from WR, $\overline{WR}$	(Note 1)	20		20		ns
t_{WR}	WR, $\overline{WR}$ Strobe Width		100		175		ns
t_{XH}	Duration of Clock High Pulse	External Clock (3.1 MHz Max.)	140		140		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (3.1 MHz Max.)	140		140		ns
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$		360		755		ns
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$		360		755		ns
Baud Generator							
N	Baud Divisor		1	$2^{16}-1$	1	$2^{16}-1$	
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		125		250	ns
t_{BLD}	Baud Output Negative Edge Del. ,	100 pF Load		125		250	ns
t_{HW}	Baud Output Up Time	$f_X = 3$ MHz, ÷3, 100 pF Load	330		330		ns
t_{LW}	Baud Output Down Time	$f_X = 2$ MHz, ÷2, 100 pF Load	425		425		ns
Receiver							
t_{RINT}	Delay from RD, $\overline{RD}$ (RD RBR or RD LSR) to Reset Interrupt	100 pF Load		1		1	μs
t_{SCD}	Delay from RCLK to Sample Time			2		2	μs
t_{SINT}	Delay from Stop to Set Interrupt			1		1	RCLK Cycles (Note 2)

Note 1: Applicable only when $\overline{ADS}$ is tied low. **Note 2:** RCLK is equal to t_{XH} and t_{XL}

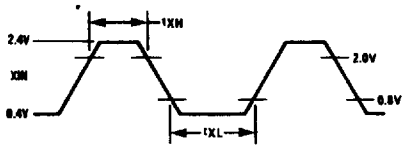
Note 3: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ (Continued)

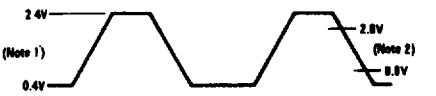
Symbol	Parameter	Conditions	GM16C450		GM82C50A		Units
			Min	Max	Min	Max	
Transmitter							
t_{HR}	Delay from WR, $\overline{WR}$ (WR THR) to Reset Interrupt	100 pF Load		175		1000	ns
t_{IR}	Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	100 pF Load		250		1000	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	8	24	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to Interrupt		16	32	16	32	BAUDOUT Cycles
t_{STI}	Delay from Stop to Interrupt (THRE)		8	8	8	8	BAUDOUT Cycles
Modem Control							
t_{MDO}	Delay from WR, $\overline{WR}$ (WR MCR) to Output	100 pF Load		200		1000	ns
t_{RIM}	Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)	100 pF Load		250		1000	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load		250		1000	ns

4.0 Timing Waveforms (All timings are referenced to valid 0 and valid 1)

External Clock Input (3.1 MHz Max.)



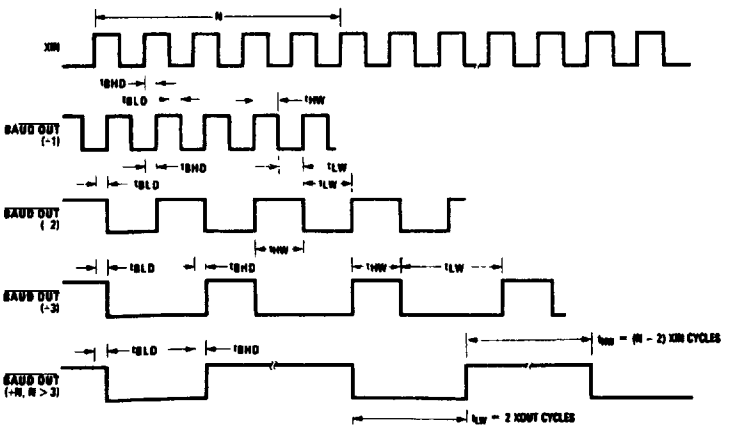
AC Test Points



Note 1: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.

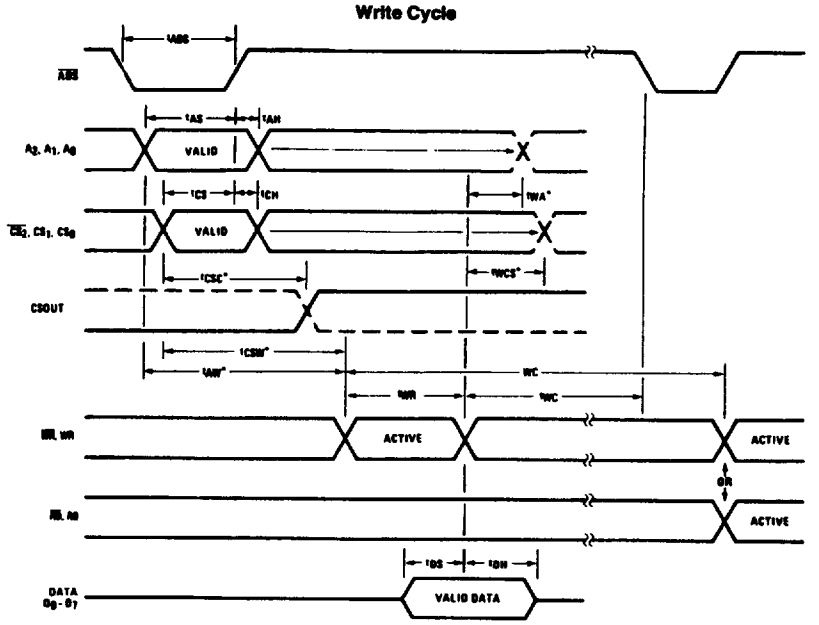
Note 2: The 2.0V and 0.8V levels are the voltages at which the timing tests are made.

$\overline{BAUDOUT}$ Timing



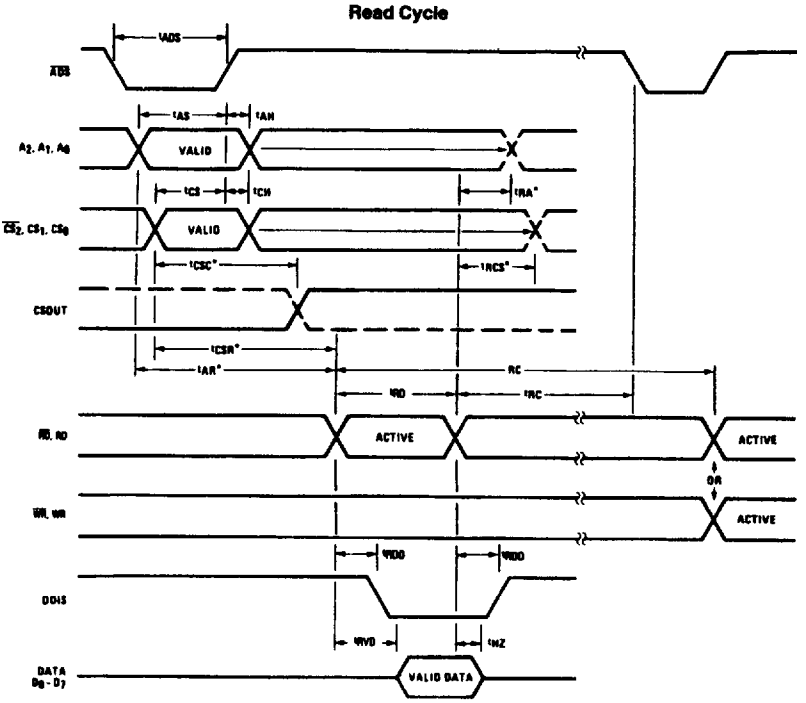
4.0 Timing Waveforms (Continued)

Write Cycle



*Applicable Only When $\overline{ADS}$ is Tied Low.

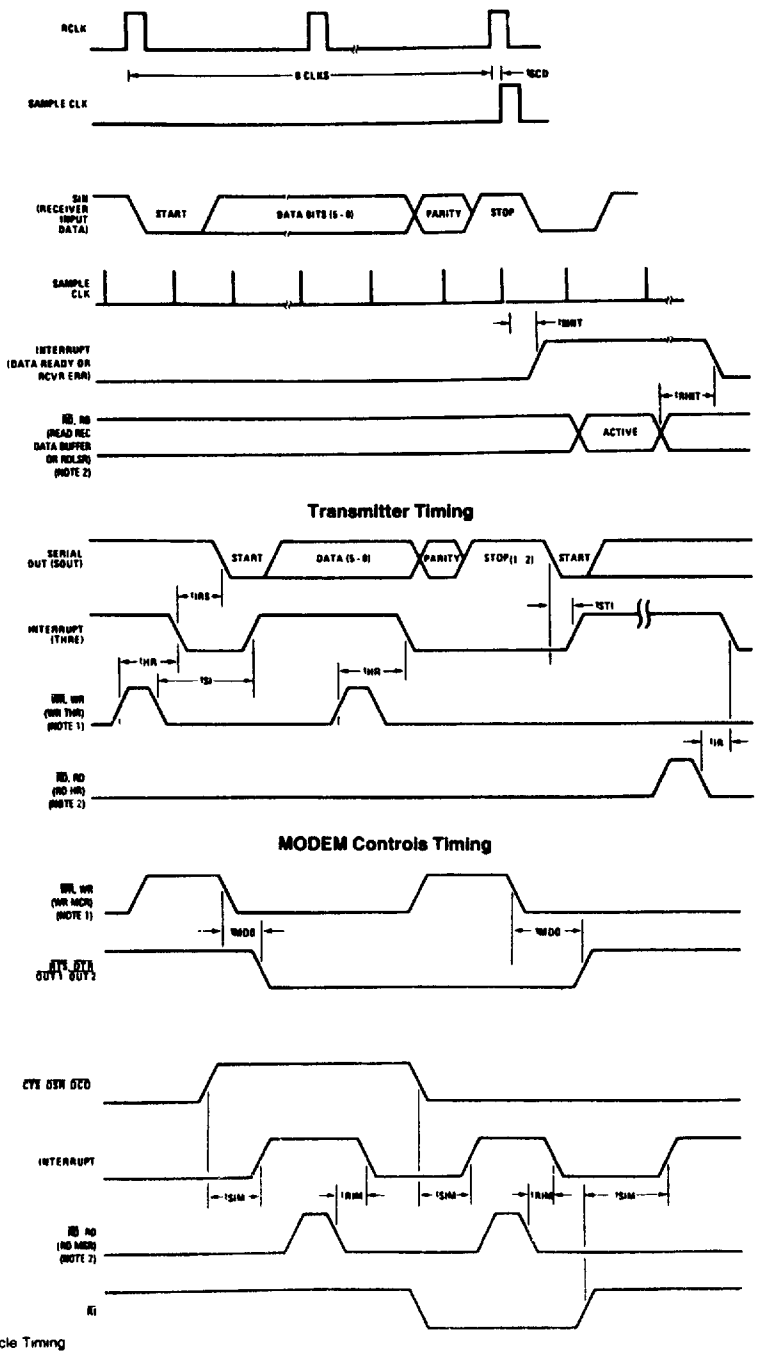
Read Cycle



*Applicable Only When $\overline{ADS}$ is Tied Low

4.0 Timing Waveforms (Continued)

Receiver Timing



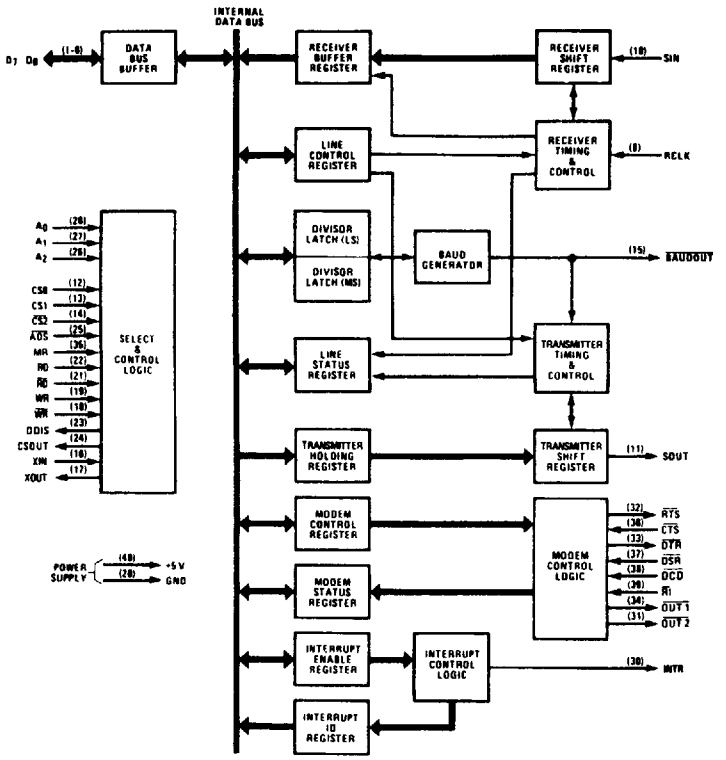
Transmitter Timing

MODEM Controls Timing

Note 1: See Write Cycle Timing

Note 2: See Read Cycle Timing

5.0 Block Diagram



Note: Applicable pinout numbers are included within parenthesis

6.0 Pin Descriptions

The following describes the function of all ACE pins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

6.1 INPUT SIGNALS

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12–14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. This enables communication between the ACE and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If $\overline{ADS}$ is always low, valid chip selects should stabilize according to the t_{CSW} parameter.

Read (RD, $\overline{RD}$), Pins 22 and 21: When RD is high or $\overline{RD}$ is low while the chip is selected, the CPU can read status information or data from the selected ACE register

Note: Only an active RD or $\overline{RD}$ input is required to transfer data from the UART during a read operation Therefore, tie either the RD input permanently low or the $\overline{RD}$ input permanently high, when it is not used

Write (WR, $\overline{WR}$), Pins 19 and 18: When WR is high or $\overline{WR}$ is low while the chip is selected, the CPU can write control words or data into the selected ACE register.

Note: Only an active WR or $\overline{WR}$ input is required to transfer data to the UART during a write operation Therefore, tie either the WR input permanently low or the $\overline{WR}$ input permanently high, when it is not used.

Address Strobe ($\overline{ADS}$), Pin 25: The positive edge of an active Address Strobe ($\overline{ADS}$) signal latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals.

Note: An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low

Register Select (A0, A1, A2), Pins 26–28: Address signals connected to these 3 inputs select a ACE register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain ACE registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

6.0 Pin Descriptions (Continued)

Register Addresses

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals (SOUT, INTR, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to Table I.) This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis.

Receiver Clock (RCLK), Pin 9: This input is the 16 × baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: When low, this indicates that the MODEM or data set is ready to exchange data. The $\overline{CTS}$ signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled

Data Set Ready ($\overline{DSR}$), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link with the ACE. The $\overline{DSR}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled

Data Carrier Detect ($\overline{DCD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register Bit 7 is the complement of the $\overline{DCD}$ signal Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input **signal** has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled

V_{CC}, Pin 40: + 5V supply.

V_{SS}, Pin 20: Ground (0V) reference.

6.2 OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, this informs the MODEM or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

Request to Send ($\overline{RTS}$), Pin 32: When low, this informs the MODEM or data set that the ACE is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

Output 1 ($\overline{OUT\ 1}$), Pin 34: This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the XMOS parts this will achieve TTL levels.

Output 2 ($\overline{OUT\ 2}$), Pin 31: This user-designated output can be set to an active low, by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the XMOS parts this will achieve TTL levels.

Chip Select Out (CSOUT), Pin 24: When high, it indicates that the chip has been selected by active, CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1 CSOUT goes low when the UART is deselected

Driver Disable (DDIS), Pin 23: This goes low whenever the CPU is reading data from the UART It can disable or control the direction of a data bus transceiver between the CPU and the ACE (see Typical Interface for a High Capacity Data Bus)

Baud Out ($\overline{BAUDOUT}$), Pin 15: This is the 16 × clock signal from the transmitter section of the UART The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip

6.0 Pin Descriptions (Continued)

Interrupt (INTR), Pin 30: This goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Line Status; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: This is the composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation or when the transmitter is idle.

6.3 INPUT/OUTPUT SIGNALS

Data (D_7–D_0) Bus, Pins 1–8: This bus is comprised of eight TRI-STATE input/output lines. The bus provides bidirectional communications between the ACE and the CPU. Data, control words, and status information are transferred via the D_7–D_0 Data Bus.

External Clock Input/Output (XIN, XOUT) Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the UART. When a crystal oscillator or a clock signal is provided, it drives the ACE via XIN (see typical oscillator network illustration).

7.0 Connection Diagrams

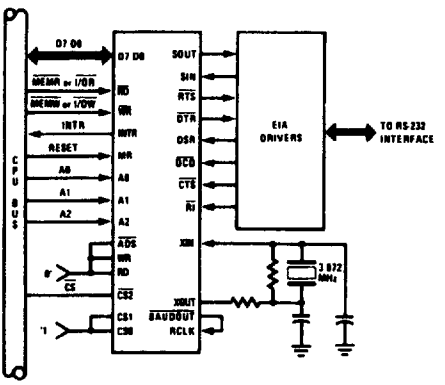


TABLE I. UART Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	**0000** 0000 (Note 1)
Interrupt Identification Register	Master Reset	**0000 0**001
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	**0000** 0000
Line Status Register	Master Reset	**0**110 0000
MODEM Status Register	Master Reset	XXXX 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High

Note 1: Boldface bits are permanently low

Note 2: Bits 7–4 are driven by the input signals