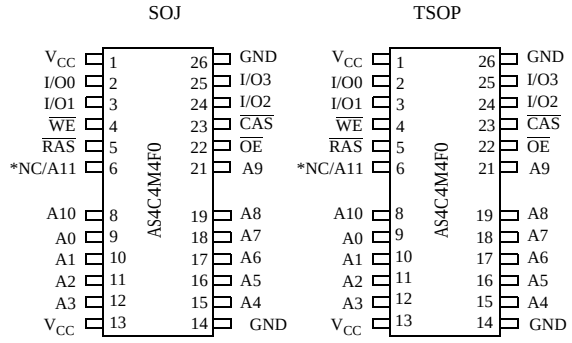
5V 4M×4 CMOS DRAM (fast page mode)

Features

- Organization: 4,194,304 words × 4 bits
- High speed
  - 50/60 ns $\overline{RAS}$ access time
  - 25/30 ns column address access time
  - 12/15 ns $\overline{CAS}$ access time
- Low power consumption
  - Active: 908 mW max
  - Standby: 5.5 mW max, CMOS I/O
- Fast page mode
- Refresh
  - 4096 refresh cycles, 64 ms refresh interval for AS4C4M4F0
  - 2048 refresh cycles, 32 ms refresh interval for AS4C4M4F1
  - $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh or self-refresh
- TTL-compatible, three-state I/O
- JEDEC standard package
  - 300 mil, 24/26-pin SOJ
  - 300 mil, 24/26-pin TSOP
- Latch-up current ≥ 200 mA
- ESD protection ≥ 2000 mV
- Industrial and commercial temperature available

Pin arrangement



*NC on 2K refresh version; A11 on 4K refresh version

Pin designation

Pin(s)	Description
A0 to A11	Address inputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
I/O0 to I/O3	Input/output
$\overline{OE}$	Output enable
V_{CC}	Power
GND	Ground

DRAM

Selection guide

	Symbol	AS4C4M4F0-50 AS4C4M4F1-50	AS4C4M4F0-60 AS4C4M4F1-60	Unit
Maximum $\overline{RAS}$ access time	t_{RAC}	50	60	ns
Maximum column address access time	t_{CAA}	25	30	ns
Maximum $\overline{CAS}$ access time	t_{CAC}	12	15	ns
Maximum output enable ($\overline{OE}$) access time	t_{OEA}	13	15	ns
Minimum read or write cycle time	t_{RC}	85	100	ns
Minimum fast page mode cycle time	t_{PC}	25	30	ns
Maximum operating current	I_{CC1}	135	120	mA
Maximum CMOS standby current	I_{CC5}	1.0	1.0	mA

Functional description

The AS4C4M4F0 and AS4C4M4F1 are high performance 16-megabit CMOS Dynamic Random Access Memory (DRAM) devices organized as 4,194,304 words × 4 bits. The devices are fabricated using advanced CMOS technology and innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels. The Alliance 16Mb DRAM family is optimized for use as main memory in PC, workstation, router and switch applications.

These devices feature a high speed page mode operation where read and write operations within a single row (or page) can be executed at very high speed by toggling column addresses within that row. Row and column addresses are alternately latched into input buffers using the falling edge of $\overline{RAS}$ and $\overline{CAS}$ inputs respectively. Also, $\overline{RAS}$ is used to make the column address latch transparent, enabling application of column addresses prior to $\overline{CAS}$ assertion.

Refresh on the 4096 address combinations of A0 to A11 must be performed every 64 ms using:

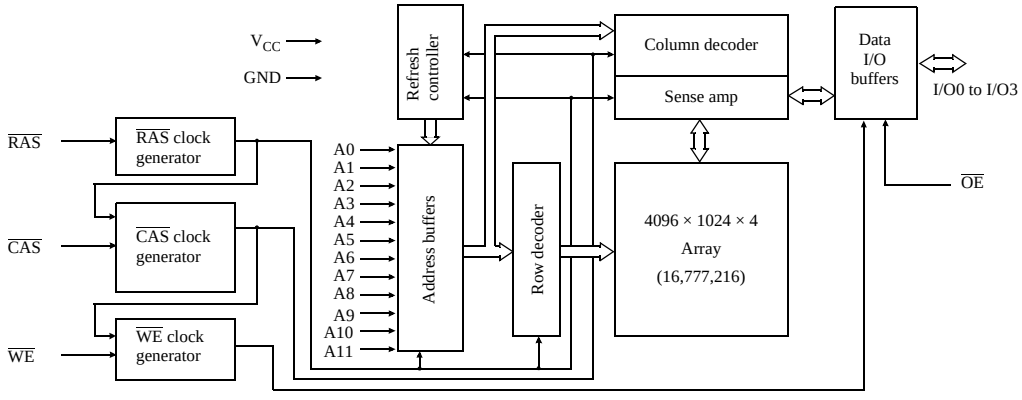
- $\overline{RAS}$-only refresh: $\overline{RAS}$ is asserted while $\overline{CAS}$ is held high. Each of the 4096 rows must be strobed. Outputs remain high impedence.
- Hidden refresh: $\overline{CAS}$ is held low while $\overline{RAS}$ is toggled. Refresh address is generated internally. Outputs remain low impedence with previous valid data.
- $\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR): $\overline{CAS}$ is asserted prior to $\overline{RAS}$. Refresh address is generated internally. Outputs are high-impedence ($\overline{OE}$ and $\overline{WE}$ are don't care).
- Normal read or write cycles refresh the row being accessed.
- Self-refresh cycles

Refresh on the 2048 address combinations of A0 to A10 must be performed every 32 ms using:

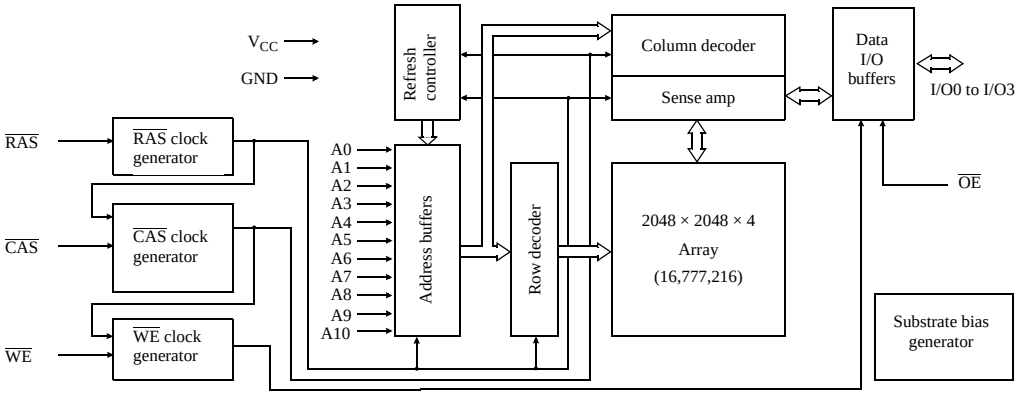
- $\overline{RAS}$-only refresh: $\overline{RAS}$ is asserted while $\overline{CAS}$ is held high. Each of the 2048 rows must be strobed. Outputs remain high impedence.
- Hidden refresh: $\overline{CAS}$ is held low while $\overline{RAS}$ is toggled. Refresh address is generated internally. Outputs remain low impedence with previous valid data.
- $\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR): $\overline{CAS}$ is asserted prior to $\overline{RAS}$. Refresh address is generated internally. Outputs are high-impedence ($\overline{OE}$ and $\overline{WE}$ are don't care).
- Normal read or write cycles refresh the row being accessed.
- Self-refresh cycles

The AS4C4M4F0 and AS4C4M4F1 are available in the standard 24/26-pin plastic SOJ and 24/26-pin plastic TSOP packages. The AS4C4M4F0 and AS4C4M4F1 operate with a single power supply of 5V ± 0.5V and provide TTL compatible inputs and outputs.

Logic block diagram for 4K refresh



Logic block diagram for 2K refresh



Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V_{CC}	4.5	5.0	5.5	V
		GND	0.0	0.0	0.0	V
Input voltage		V_{IH}	2.4	–	V_{CC}	V
		V_{IL}	–0.5†	–	0.8	V
Ambient operating temperature	Commercial	T_A	0	–	70	°C
	Industrial		-40	–	85	

†V_{IL} min -3.0V for pulse widths less than 5 ns. Recommended operating conditions apply throughout this document unlesss otherwise specified.

DRAM

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage	V_{in}	-1.0	+7.0	V
Input voltage (DQs)	V_{DQ}	-1.0	V_{CC} + 0.5	V
Power supply voltage	V_{CC}	-1.0	+7.0	V
Storage temperature (plastic)	T_{STG}	-55	+150	°C
Soldering temperature × time	T_{SOLDER}	–	260 × 10	°C × sec
Power dissipation	P_D	–	1	W
Short circuit output current	I_{out}	–	50	mA

DC electrical characteristics

			-50		-60			
Parameter	Symbol	Test conditions	Min	Max	Min	Max	Unit	Notes
Input leakage current	I_{IL}	$0V \le V_{in} \le +5.5V$, Pins not under test = 0V	-5	+5	-5	+5	µA	
Output leakage current	I_{OL}	D_{OUT} disabled, $0V \le V_{out} \le +5.5V$	-5	+5	-5	+5	µA	
Operating power supply current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Address cycling; t_{RC}=min	–	135	–	120	mA	1,2
TTL standby power supply current	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}	–	2.0	–	2.0	mA	
Average power supply current, $\overline{RAS}$ refresh mode or CBR	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ V_{IH}, t_{RC} = min of $\overline{RAS}$ low after $\overline{XCAS}$ low.	–	120	–	110	mA	1
Fast page mode average power supply current	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{HPC} = min	–	130	–	120	mA	1, 2
CMOS standby power supply current	I_{CC5}	$\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V	–	1.0	–	1.0	mA	
Output voltage	V_{OH}	I_{OUT} = -5.0 mA	2.4	–	2.4	–	V	
	V_{OL}	I_{OUT} = 4.2 mA	–	0.4	–	0.4	V	
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	120	–	110	mA	
Self refresh current	I_{CC7}	$\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ ≤ 0.2V, $\overline{WE}$ = $\overline{OE}$ ≥ V_{CC} - 0.2V, all other inputs at 0.2V or V_{CC} - 0.2V	–	0.6	–	0.6	mA	

DRAM

AC parameters common to all waveforms

		-50		-60			
Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
t_{RC}	Random read or write cycle time	80	–	100	–	ns	
t_{RP}	$\overline{RAS}$ precharge time	30	–	40	–	ns	
t_{RAS}	$\overline{RAS}$ pulse width	50	10K	60	10K	ns	
t_{CAS}	$\overline{CAS}$ pulse width	8	10K	10	10K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	15	35	15	43	ns	6
t_{RAD}	$\overline{RAS}$ to column address delay time	12	25	12	30	ns	7
t_{RSH}	$\overline{CAS}$ to $\overline{RAS}$ hold time	10	–	10	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CAS}$ hold time	40	–	50	–	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	5	–	ns	
t_{ASR}	Row address setup time	0	–	0	–	ns	
t_{RAH}	Row address hold time	8	–	10	–	ns	
t_T	Transition time (rise and fall)	1	50	1	50	ns	4,5
t_{REF}	Refresh period	–	64	–	64	ms	3
t_{CP}	$\overline{CAS}$ precharge time	8	–	10	–	ns	
t_{RAL}	Column address to $\overline{RAS}$ lead time	25	–	30	–	ns	
t_{ASC}	Column address setup time	0	–	0	–	ns	
t_{CAH}	Column address hold time	8		10	–	ns	

Read cycle

		-50		-60			
Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
t_{RAC}	Access time from $\overline{RAS}$	–	50	–	60	ns	6
t_{CAC}	Access time from $\overline{CAS}$	–	12	–	15	ns	6,13
t_{AA}	Access time from address	–	25	–	30	ns	7,13
t_{RCS}	Read command setup time	0	–	0	–	ns	
t_{RCH}	Read command hold time to $\overline{CAS}$	0	–	0	–	ns	9
t_{RRH}	Read command hold time to $\overline{RAS}$	0	–	0	–	ns	9

Write cycle

		-50		-60			
Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
t_{WCS}	Write command setup time	0	–	0	–	ns	11
t_{WCH}	Write command hold time	10	–	10	–	ns	11
t_{WP}	Write command pulse width	10	–	10	–	ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	10	–	10	–	ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	8	–	10	–	ns	
t_{DS}	Data-in setup time	0	–	0	–	ns	12
t_{DH}	Data-in hold time	8	–	10	–	ns	12

Read-modify-write cycle

		-50		-60			
Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
t_{RWC}	Read-write cycle time	113	–	135	–	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay time	67	–	77	–	ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay time	32	–	35	–	ns	11
t_{AWD}	Column address to $\overline{WE}$ delay time	42	–	47	–	ns	11

Refresh cycle

		-50		-60			
Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$)	5	–	5	–	ns	3
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$)	8	–	10	–	ns	3
t_{RPC}	$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ precharge time (CBR counter test)	10		10	–	ns	

Fast page mode cycle

		-50		-60			
Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
t_{CPA}	Access time from $\overline{CAS}$ precharge	–	28	–	35		13
t_{RASP}	$\overline{RAS}$ pulse width	50	100K	60	100K		
t_{PC}	Read-write cycle time	30	–	35	–		
t_{CP}	$\overline{CAS}$ precharge time (fast page)	10	–	10	–		
t_{PCM}	Fast page mode RMW cycle	80	–	85	–		
t_{CRW}	Page mode $\overline{CAS}$ pulse width (RMW)	12	–	15	–		

Output enable

		-50		-60			
Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
t_{CLZ}	$\overline{CAS}$ to output in Low Z	0	–	0	–	ns	8
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	8	–	10	–	ns	
t_{OEA}	$\overline{OE}$ access time	–	13	–	15	ns	
t_{OED}	$\overline{OE}$ to data delay	13	–	15	–	ns	
t_{OEZ}	Output buffer turnoff delay from $\overline{OE}$	0	13	0	15	ns	8
t_{OEH}	$\overline{OE}$ command hold time	10	–	10	–	ns	
t_{OLZ}	$\overline{OE}$ to output in Low Z	0	–	0	–	ns	
t_{OFF}	Output buffer turn-off time	0	13	0	15	ns	8,10

Self refresh cycle

Std		-50		-60			
Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
t_{RASS}	$\overline{RAS}$ pulse width (CBR self refresh)	100	–	100	–	µs	
t_{RPS}	$\overline{RAS}$ precharge time (CBR self refresh)	90	–	105	–	ns	
t_{CHS}	$\overline{CAS}$ hold time (CBR self refresh)	8	–	10	–	ns	

Notes

1 I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on frequency.
2 I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3 An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).
4 AC Characteristics assume t_T = 2 ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF, V_{IL} (min) ≥ GND and V_{IH} (max) ≤ V_{CC}.
5 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
7 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
8 Assumes three state test load (5 pF and a 380 Ω Thevenin equivalent).
9 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10 t_{OFF} (max) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels. t_{OFF} is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
11 t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12 These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-write cycles.
13 Access time is determined by the longest of t_{CAA} or t_{CAC} or t_{CPA}
14 $t_{ASC} \geq t_{CP}$ to achieve t_{PC} (min) and t_{CPA} (max) values.
15 These parameters are sampled and not 100% tested.
16 These characteristics apply to AS4C4M4F0 5V devices.

AC test conditions

- Access times are measured with output reference levels of V_{OH} = 2.4V and V_{OL} = 0.4V,
  V_{IH} = 2.4V and V_{IL} = 0.8V
- Input rise and fall times: 2 ns

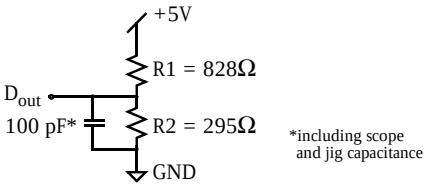


Figure A: Equivalent output load (AS4C4M4E0)

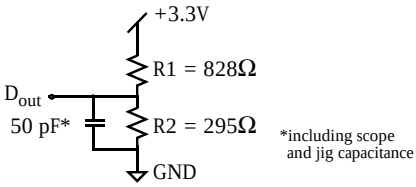
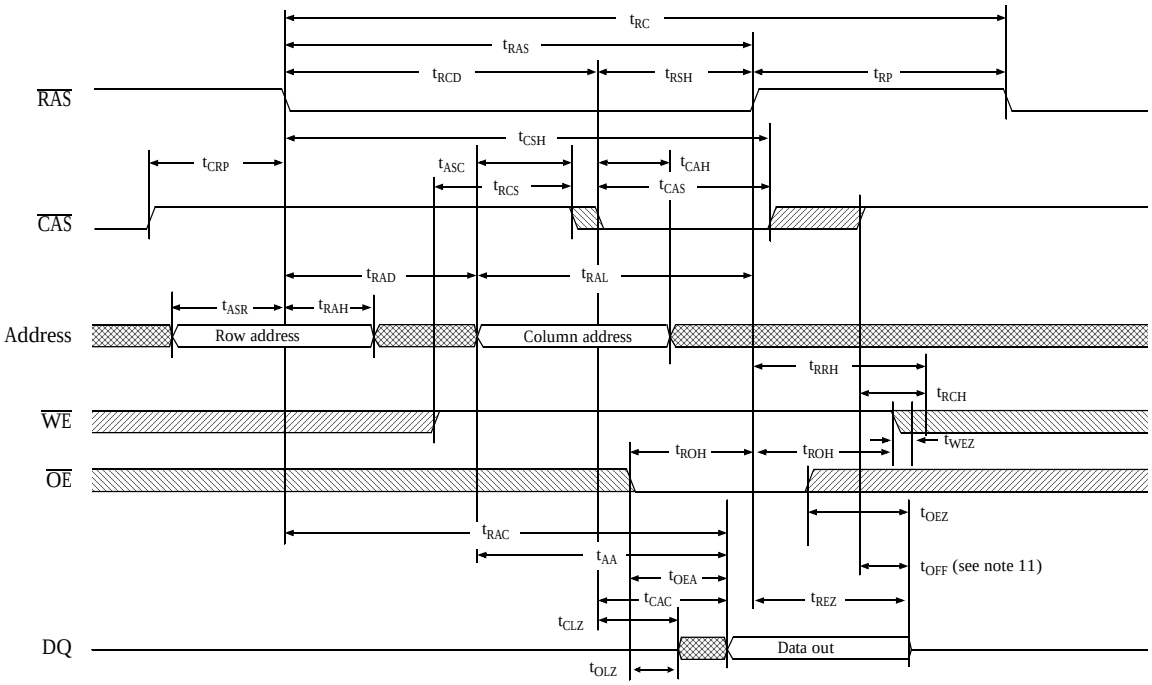


Figure B: Equivalent output load (AS4LC4M4E0)

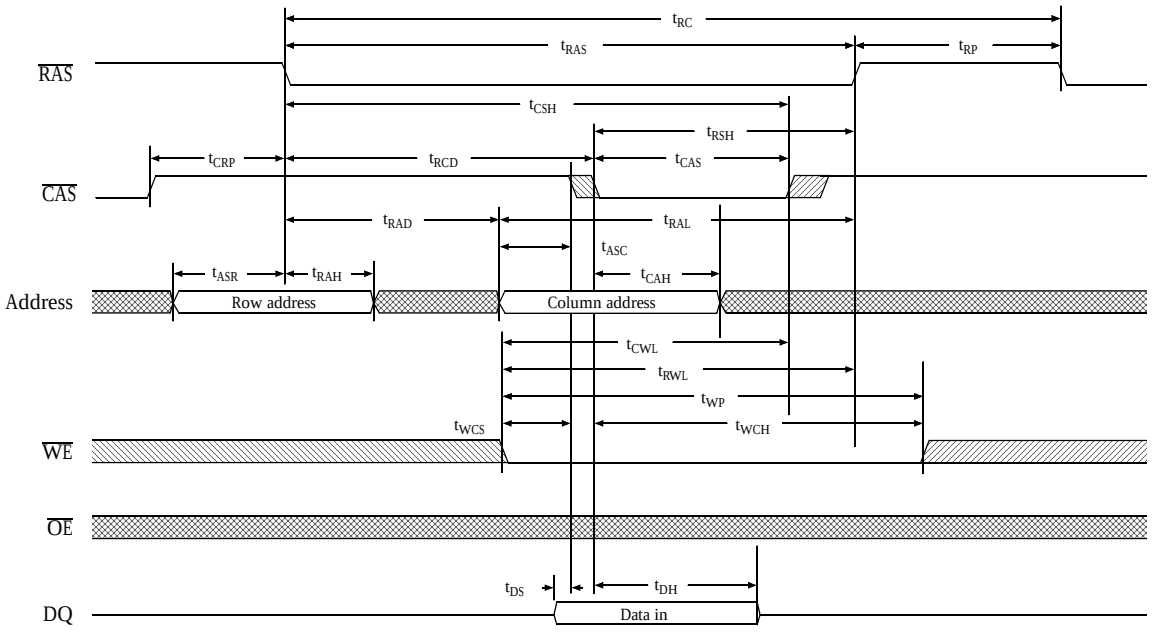
Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform



Early write waveform



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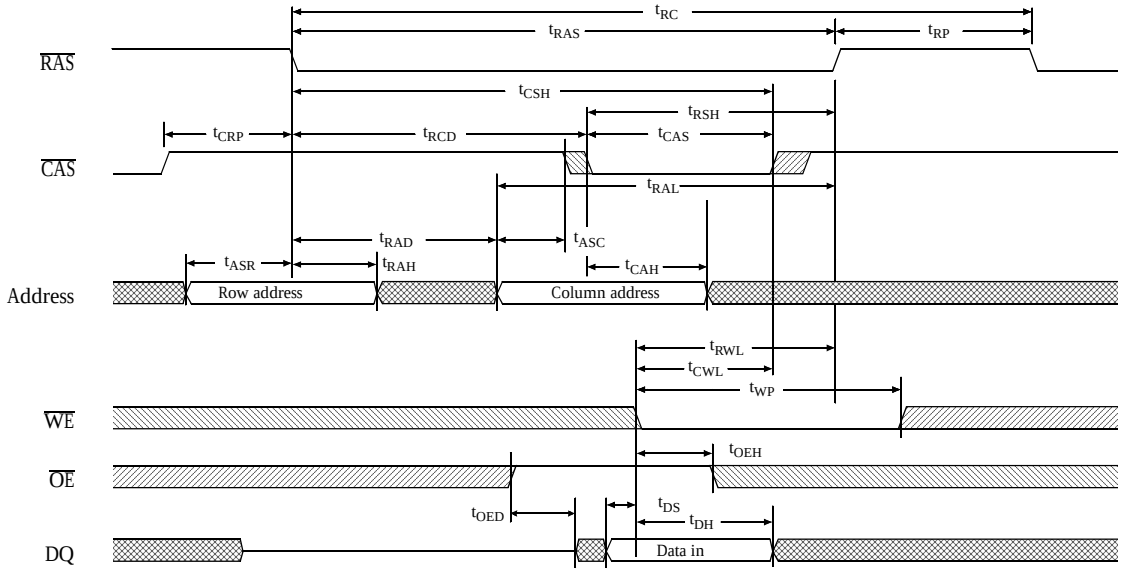
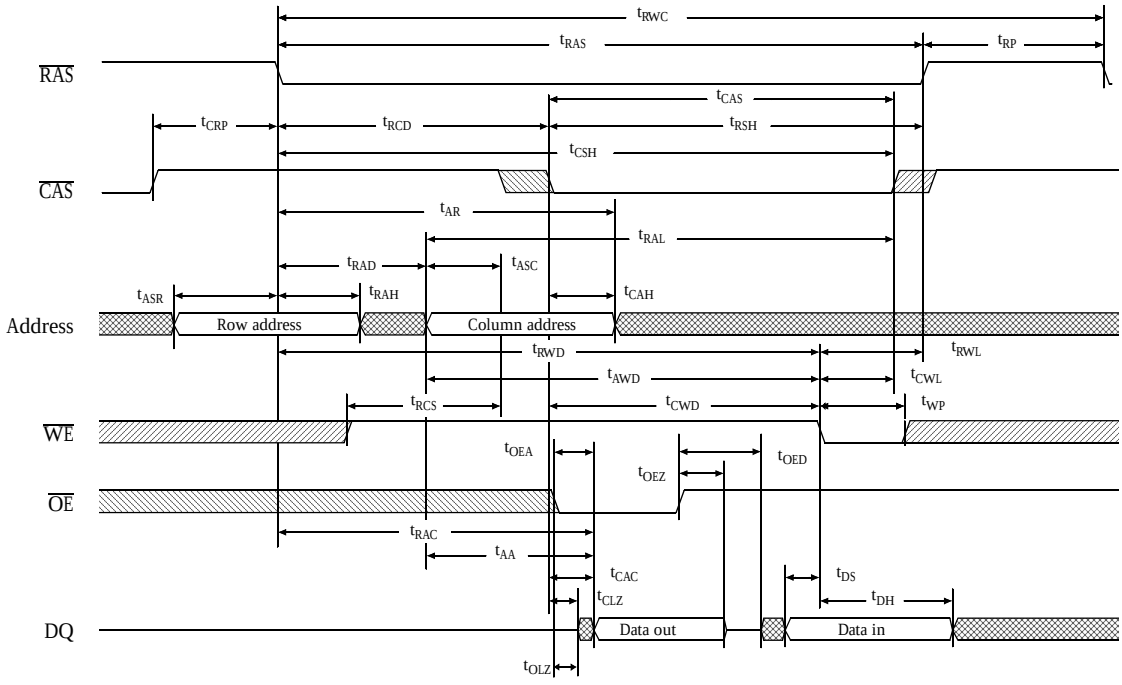
Write waveform

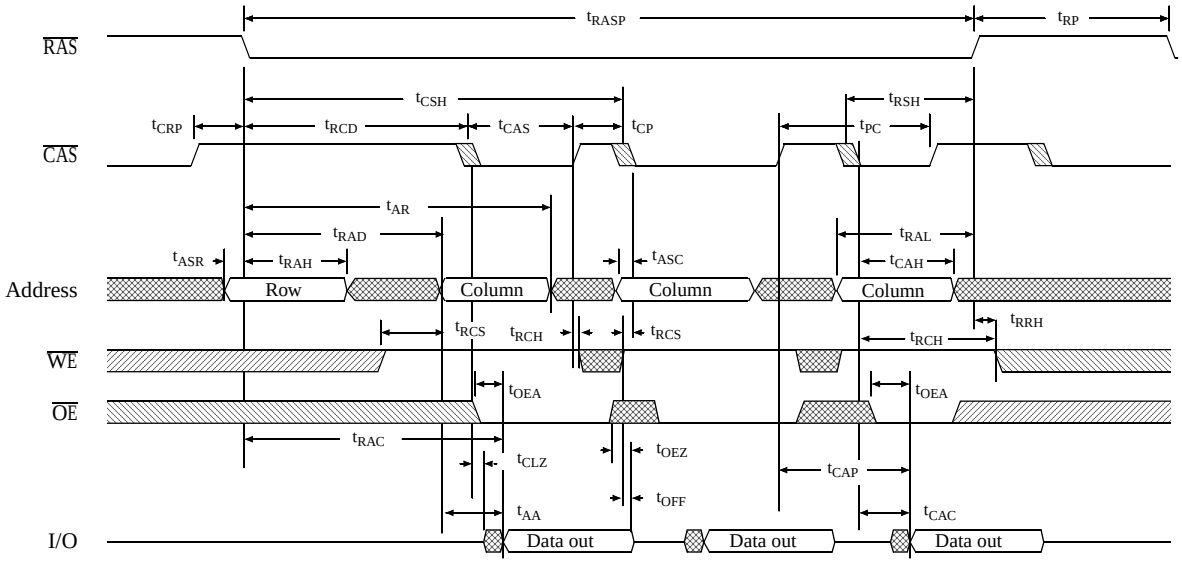
$\overline{OE}$ controlled



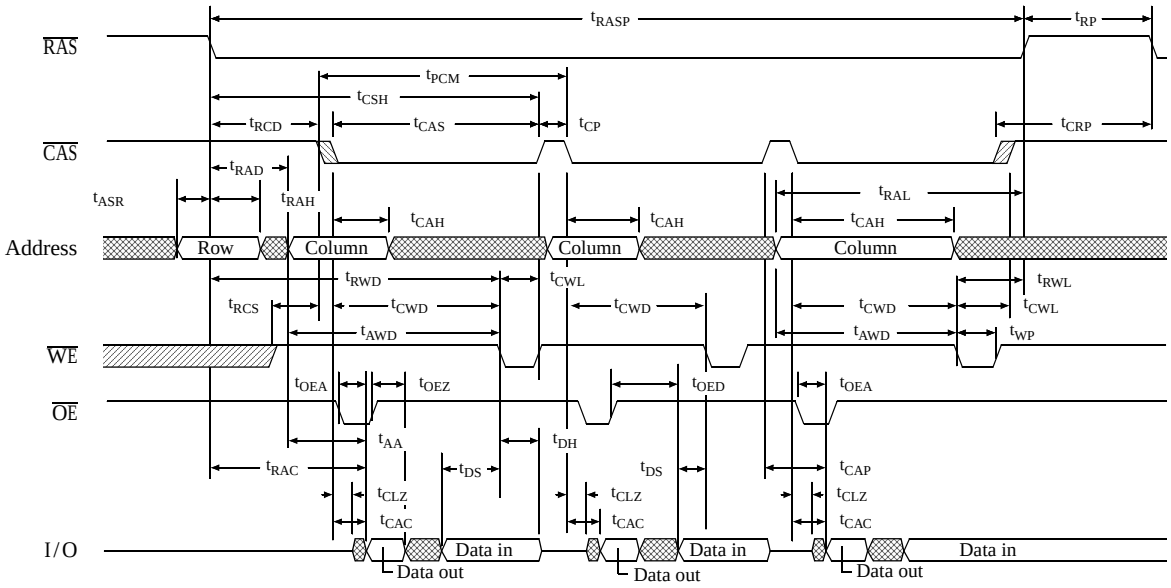
Read-modify-write waveform



Fast page mode read waveform



Fast page mode byte write waveform



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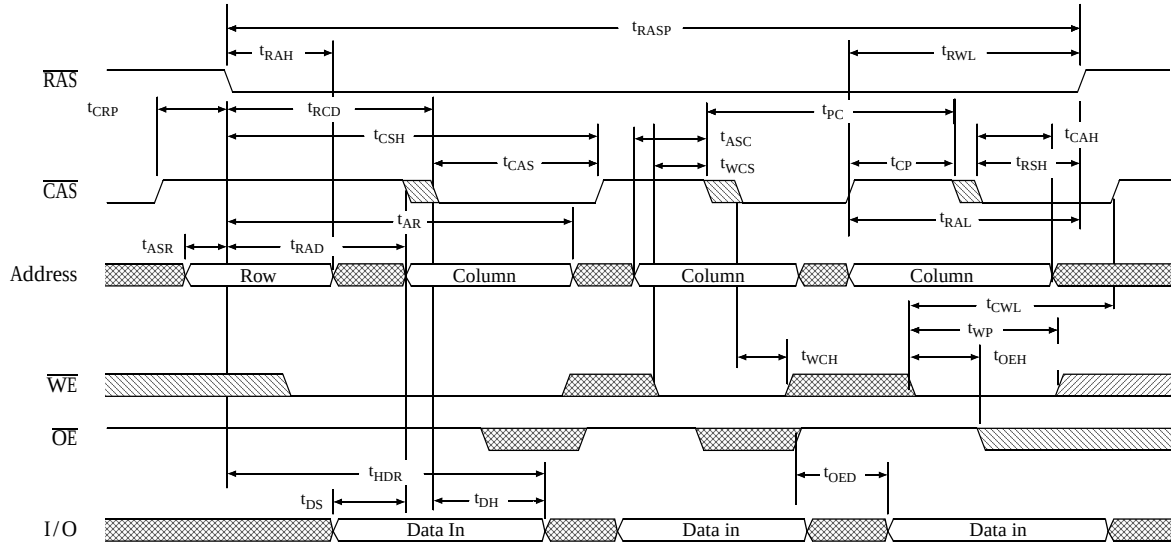
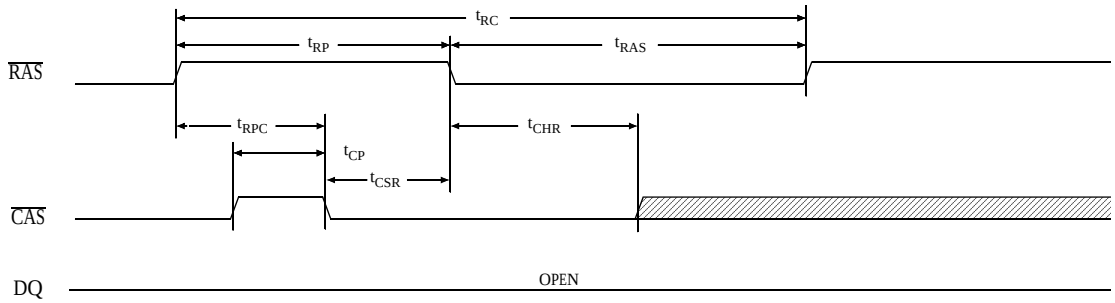
Fast page mode early write waveform



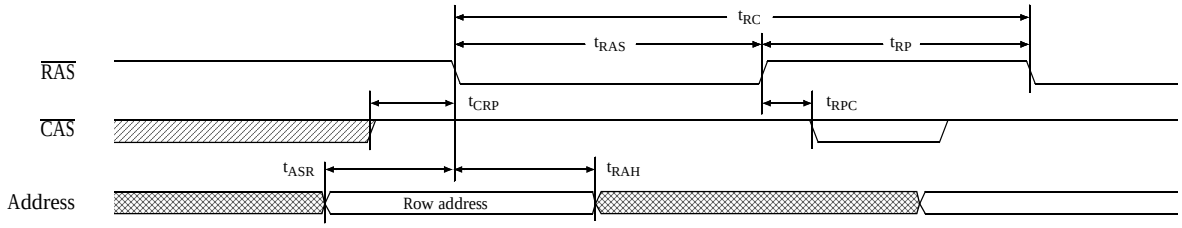
CAS before RAS refresh waveform

$\overline{WE}$ = A = V_{IH} or V_{IL}

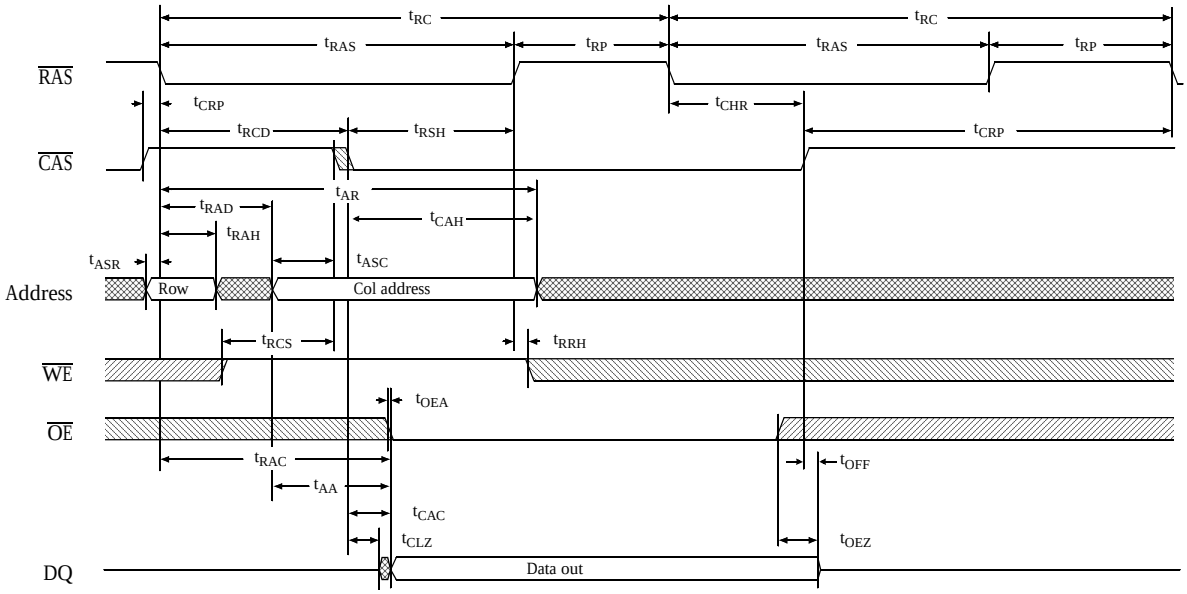


RAS only refresh waveform

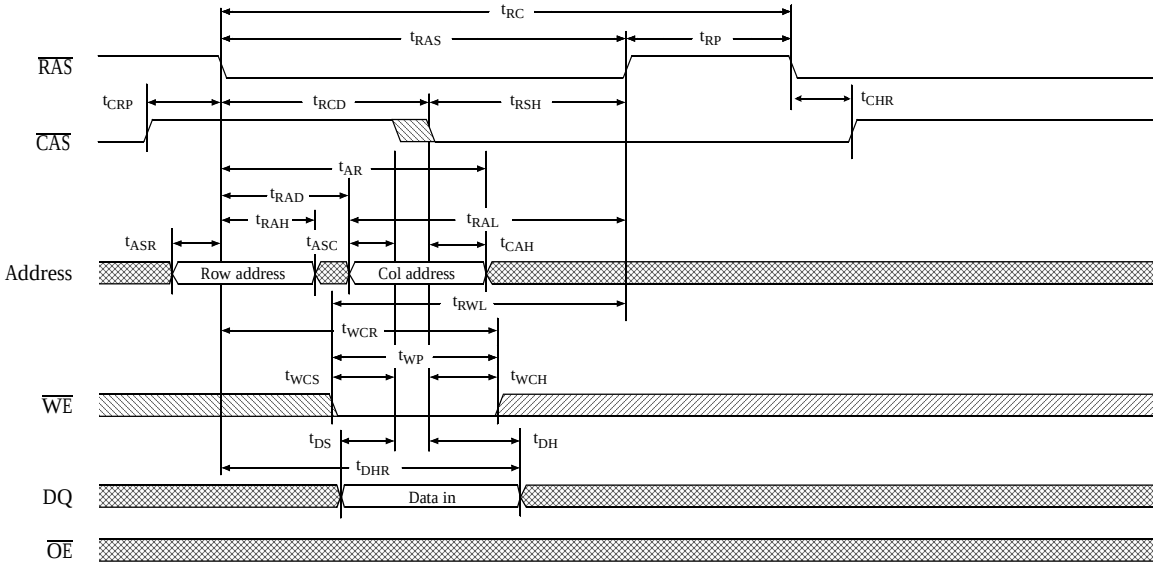
$\overline{WE}$ = $\overline{OE}$ = V_{IH} or V_{IL}



Hidden refresh waveform (read)



Hidden refresh waveform (write)



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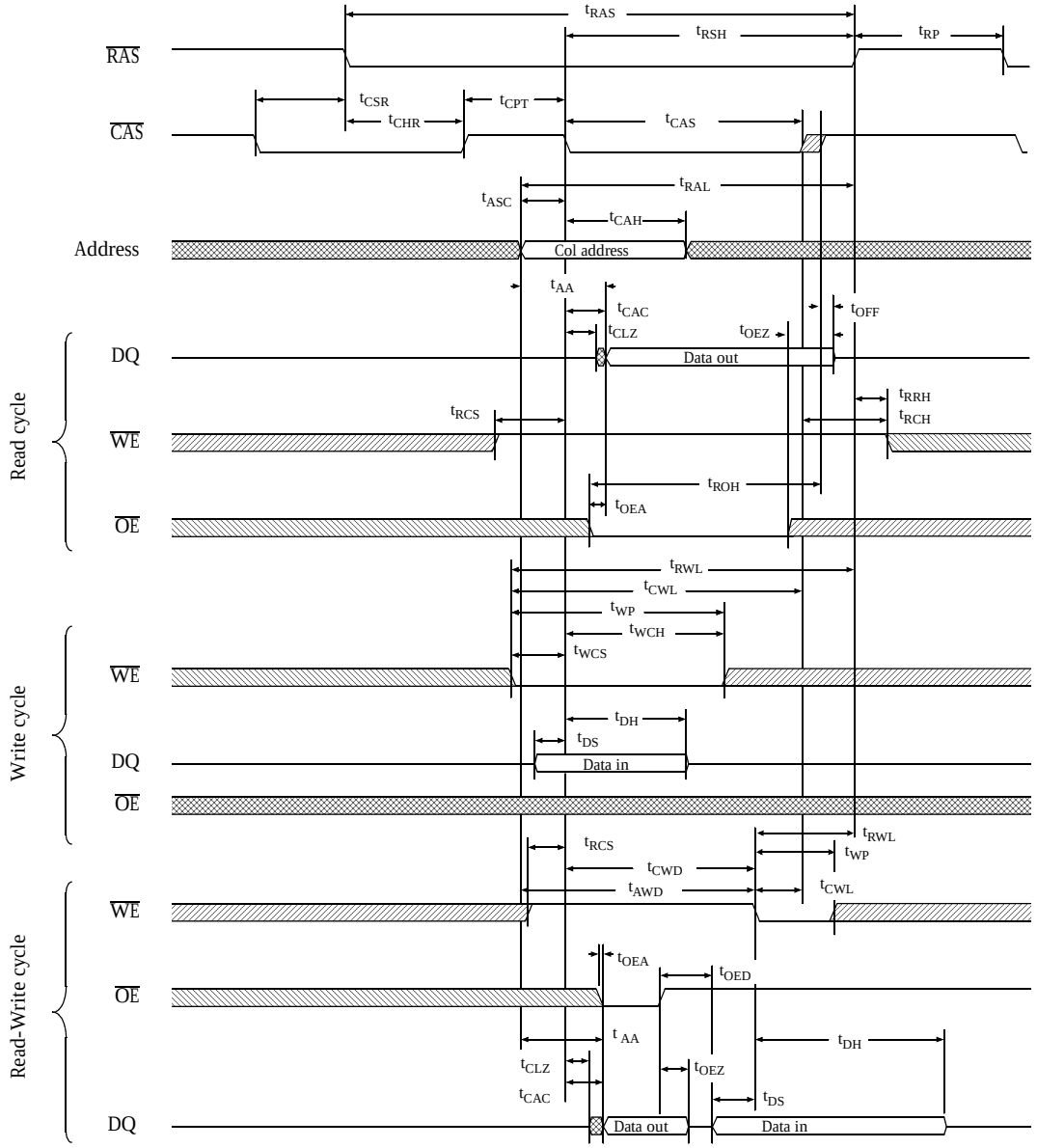
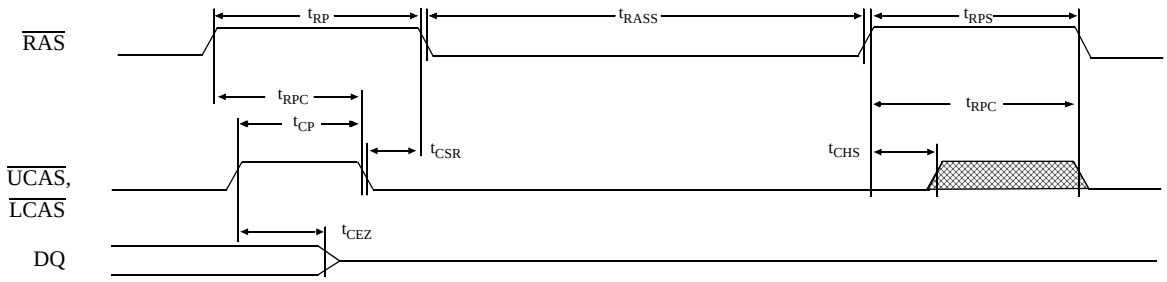
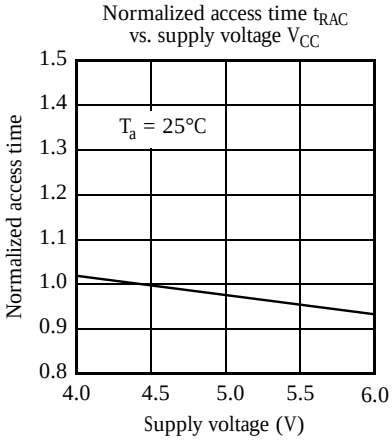
CAS before RAS refresh counter test waveform

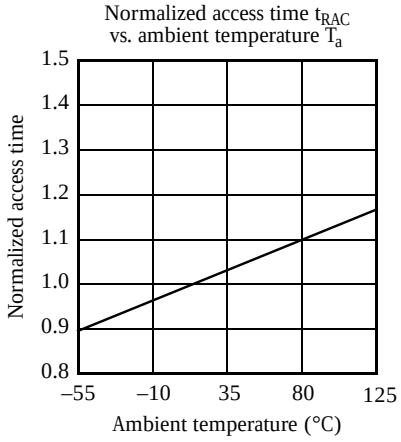


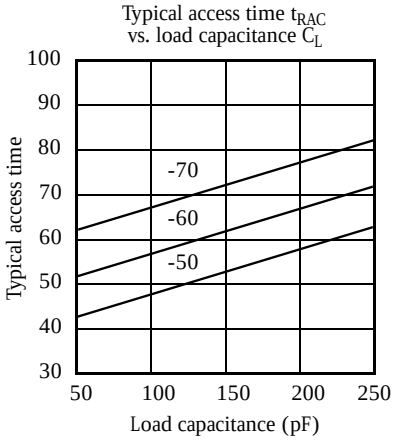
CAS-before-RAS self refresh cycle

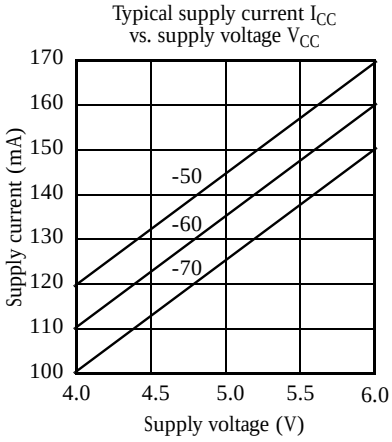


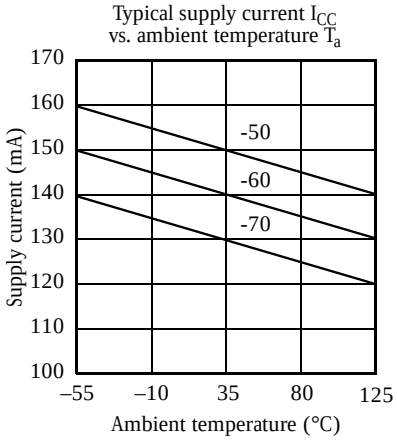
Typical DC and AC characteristics

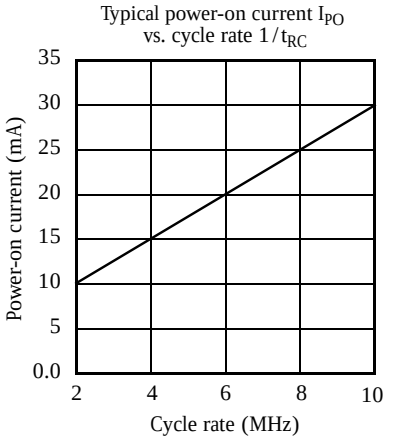




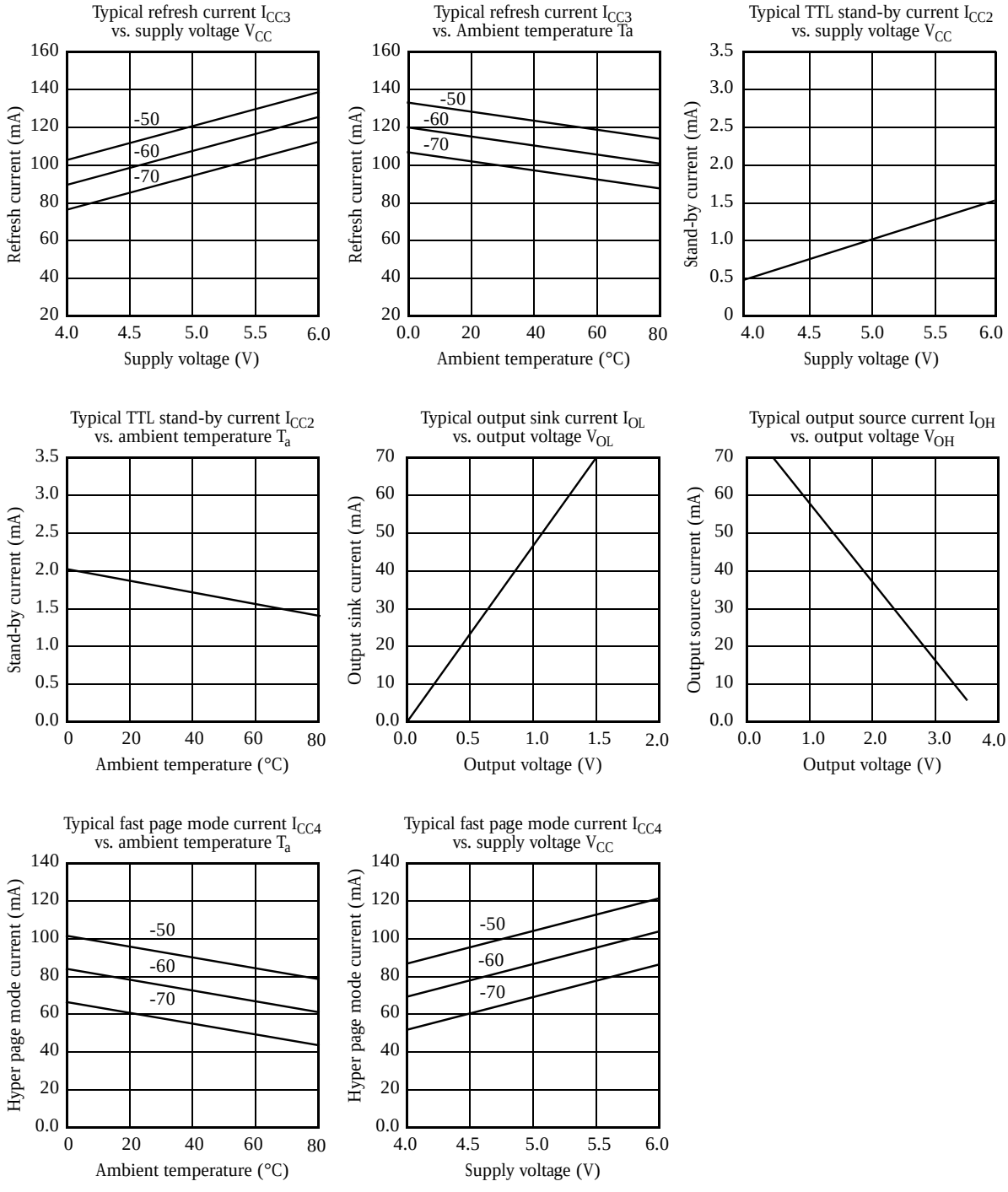








DRAM


Typical refresh current I_{CC3} vs. supply voltage V_{CC}
Refresh current (mA)
160
140
120
100
80
60
40
20
-50
-60
-70
4.0
4.5
5.0
5.5
6.0
Supply voltage (V)
Typical refresh current I_{CC3} vs. Ambient temperature Ta
Refresh current (mA)
160
140
120
100
80
60
40
20
-50
-60
-70
0.0
20
40
60
80
Ambient temperature (°C)
Typical TTL stand-by current I_{CC2} vs. supply voltage V_{CC}
Stand-by current (mA)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
4.0
4.5
5.0
5.5
6.0
Supply voltage (V)
Typical TTL stand-by current I_{CC2} vs. ambient temperature T_a
Stand-by current (mA)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0
20
40
60
80
Ambient temperature (°C)
Typical output sink current I_{OL} vs. output voltage V_{OL}
Output sink current (mA)
70
60
50
40
30
20
10
0.0
0.0
0.5
1.0
1.5
2.0
Output voltage (V)
Typical output source current I_{OH} vs. output voltage V_{OH}
Output source current (mA)
70
60
50
40
30
20
10
0.0
0.0
1.0
2.0
3.0
4.0
Output voltage (V)
Typical fast page mode current I_{CC4} vs. ambient temperature T_a
Hyper page mode current (mA)
140
120
100
80
60
40
20
0.0
-50
-60
-70
0
20
40
60
80
Ambient temperature (°C)
Typical fast page mode current I_{CC4} vs. supply voltage V_{CC}
Hyper page mode current (mA)
140
120
100
80
60
40
20
0.0
-50
-60
-70
4.0
4.5
5.0
5.5
6.0
Supply voltage (V)

Capacitance [15]

f = 1 MHz, T_a = Room temperature

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN1}	A0 to A9	V_{in} = 0V	5	pF
	C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	7	pF
DQ capacitance	C_{DQ}	DQ0 to DQ15	V_{in} = V_{out} = 0V	7	pF

AS4C4M4F0 ordering information

Package \ $\overline{RAS}$ access time		50 ns	60 ns
Plastic SOJ, 300 mil, 24/26-pin	5V	AS4C4M4F0-50JC AS4C4M4F0-50JI	AS4C4M4F0-60JC AS4C4M4F0-60JI
Plastic TSOP, 300 mil, 24/26-pin	5V	AS4C4M4F0-50TC AS4C4M4F0-50TI	AS4C4M4F0-60TC AS4C4M4F0-60TI

AS4C4M4F1 ordering information

Package \ $\overline{RAS}$ access time		50 ns	60 ns
Plastic SOJ, 300 mil, 24/26-pin	5V	AS4C4M4F1-50JC AS4C4M4F1-50JI	AS4C4M4F1-60JC AS4C4M4F1-60JI
Plastic TSOP, 300 mil, 24/26-pin	5V	AS4C4M4F1-50TC AS4C4M4F1-50TI	AS4C4M4F1-60TC AS4C4M4F1-60TI

AS4C4M4F0/F1 family part numbering system

AS4	C	4M4	F0/F1	–XX	X	X
DRAM prefix	C = 5V CMOS	4M×4	F0=4K refresh F1=2K refresh	$\overline{RAS}$ access time	Package: J = SOJ 300 mil, 24/26 T = TSOP 300 mil, 24/26	Temperature range C=Commercial, 0°C to 70 °C I=Industrial, -40°C to 85°C