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GENERAL DESCRIPTION

The EM23C8200 series is a 5V only, 8M-bit, Read Only Memory. It is organized as 1M x 8 bits (byte mode) or as 512K x 16 bit (word mode) depending on $\overline{BYTE}$ (pin 32) voltage level. EM23C8200 has a static standby mode, and has an access time of 100/120/150/200ns. it is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

EM23C8200 offers automatic power-down, with power down controlled by the chip (CE/$\overline{CE}$) input. When CE/$\overline{CE}$ is not selected, the device automatically powers down and remains in a low-power standby mode as long as CE/$\overline{CE}$ stays in the unselected mode.

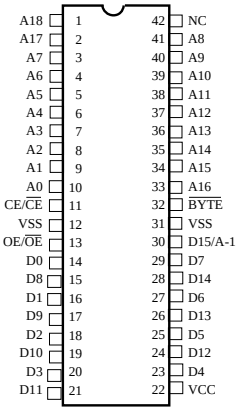
The OE/$\overline{OE}$ inputs as well as CE/$\overline{CE}$ input may be programmed either active High or Low.

FEATURES

- Switchable configuration.
- 1M x 8 (byte mode)
  512K x 16 (word mode)
- Single +5V power supply.
- Fast access time : 100/120/150/200 ns.
- Totally static operation.
- Completely TTL compatible.
- Operating current : 60 mA.
- Standby current : 100 μA
- Package:
  EM23C8200EP, - 42 pins 600 mil DIP
  EM23C8200EM, - 44 pins 500 mil SOP.

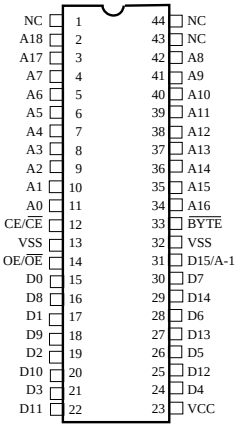
PIN ASSIGNMENTS

EM23C8200EP



PDIP

EM23C8200EM



SOP

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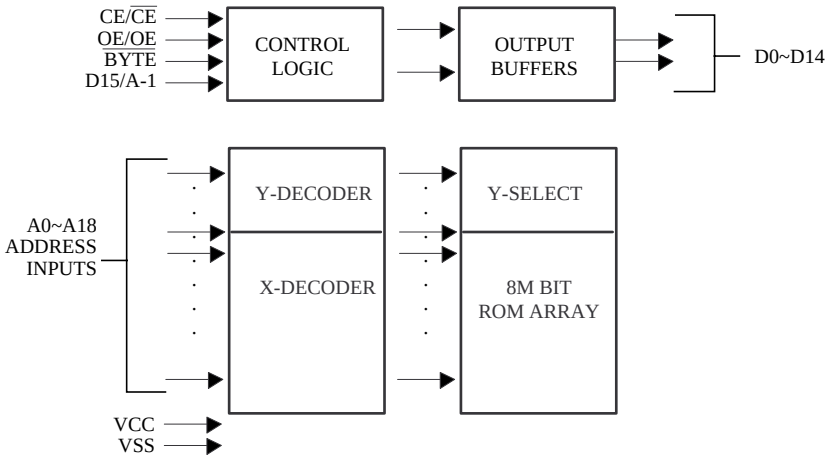
BLOCK DIAGRAM



PIN DESCRIPTIONS

Symbol	Function
A0~A18	Address input
D0~D14	Data output
CE/$\overline{CE}$	Chip enable input
OE/$\overline{OE}$	Output enable input
$\overline{BYTE}$	Word/byte selection
D15/A-1	D15 (word mode) / LSB addr. (byte mode)
V_{CC}	Power Supply pin (+5V)
V_{SS}	Ground pin

FUNCTION DESCRIPTIONS

BYTE MODE ($\overline{BYTE}$ =V_{SS})

MODE	$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	D0-D7	SUPPLY CURRENT	NOTE
Non selected	H	X	X	High Z	Standby (I_{CC2})	1
Selected/Non output	L	L/H	X	High Z	Operating (I_{CC1})	1
Selected	L	H/L	A-1 input	DOUT	Operating (I_{CC1})	1

WORD MODE ($\overline{BYTE}$ =V_{CC})

MODE	$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	D0-D14	SUPPLY CURRENT	NOTE
Non selected	H	X	High Z	High Z	Standby (I_{CC2})	1
Selected/Non output	L	L/H	High Z	High Z	Operating (I_{CC1})	1
Selected	L	H/L	DOUT	DOUT	Operating (I_{CC1})	1

NOTE1 : X=H or L

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ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Rating
Operating temperature	T_{OPR}		0 to 70°C
Storage temperature	T_{STR}		-65°C to 125°C
Input voltage	V_{IN}		- 0.5V to 7.0V
Output voltage	V_{OUT}		- 0.5V to 7.0V
Supply voltage	V_{CC}		- 0.5V to 7.0V
Power Dissipation			1.0W

* NOTICE : Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not imlied. Exposure to absoute maximum rating conditions for extended period may affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A=0~70°C)

Parameter	Sym.	Condition	Min.	Max.	Unit	Note
Output "High" voltage	V_{OH}	I_{OH} = -1.0mA	2.4		V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1mA		0.4	V	
Input "High" voltage	V_{IH}		2.2	V_{CC}+0.3	V	
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input leakage current	I_{LI}	V_{IN} = 0V to 5.5V		10	μA	
Output leakage current	I_{LO}	V_{OUT}=0V to 5.5V		10	μA	
Power-down supply current	I_{CC3}	$\overline{CE}$ > V_{CC}-0.2V		100	μA	
Standby supply current	I_{CC2}	$\overline{CE}$ = V_{IH}		2	mA	
Operating supply current	I_{CC1}			60	mA	1

CAPACITANCE T_A=25°C, f=1.0 MHz (Note 2)

Parameter	Sym.	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		10	pF
Output capacitance	C_{OUT}	V_{OUT}=0V		10	pF

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A=0~70°C)

Parameter	Sym.	8200-10		8200-12		8200-15		8200-20		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Cycle time	t_{CYC}	100		120		150		200		ns	
Address access time	t_{ACC}		100		120		150		200	ns	
Output hold time after address change	t_{OH}	10		10		10		10		ns	
Chip enable access time	t_{ACE}		100		120		150		200	ns	
Output enable/chip select access time	t_{AOE}		60		70		80		90	ns	
Output low Z delay	t_{LZ}	0		0		0		0		ns	Note 3
Output high Z delay	t_{LH}		70		70		70		70	ns	Note 4
$\overline{BYTE}$ access time	t_{BHA}		100		120		150		200	ns	
$\overline{BYTE}$ output hold time	t_{OHB}	0		0		0		0		ns	
$\overline{BYTE}$ output delay time	t_{BHZ}		70		70		70		70	ns	
$\overline{BYTE}$ output set time	t_{BLZ}	10		10		10		10		ns	

Note: 1. Measured with device selected at f=5 MHz and output unloaded.
2. This parameter is periodcally sampled and is not 100% tested.
3. Output low-impedance delay (tlZ) is measured from $\overline{CE}$ going low.
4. Output high-impedance delay (tHZ) is measured from $\overline{CE}$ going high.

AC TEST CONDITIONS

Input pulse levels	0.4V TO 2.4V
Input rise and fall time	10 ns
Input timing level	1.5 V
Output timing level	0.8V and 2.0V
Output load	See figure 1

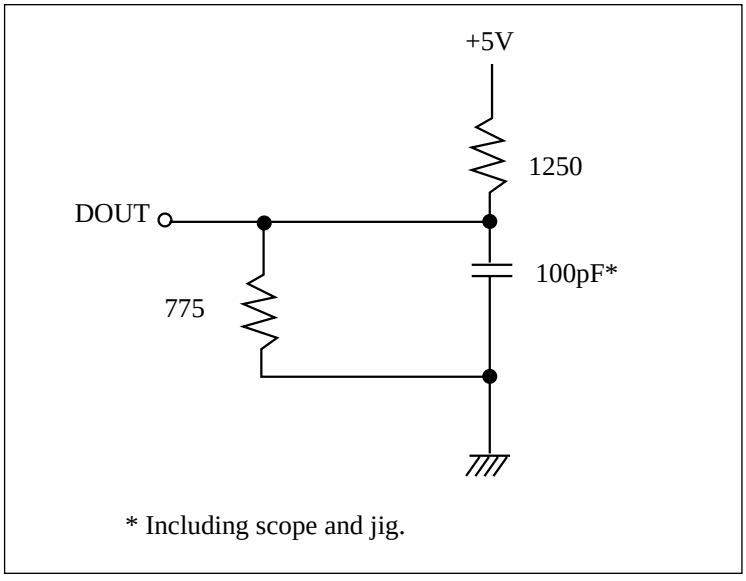

FIG.1 output load circuit

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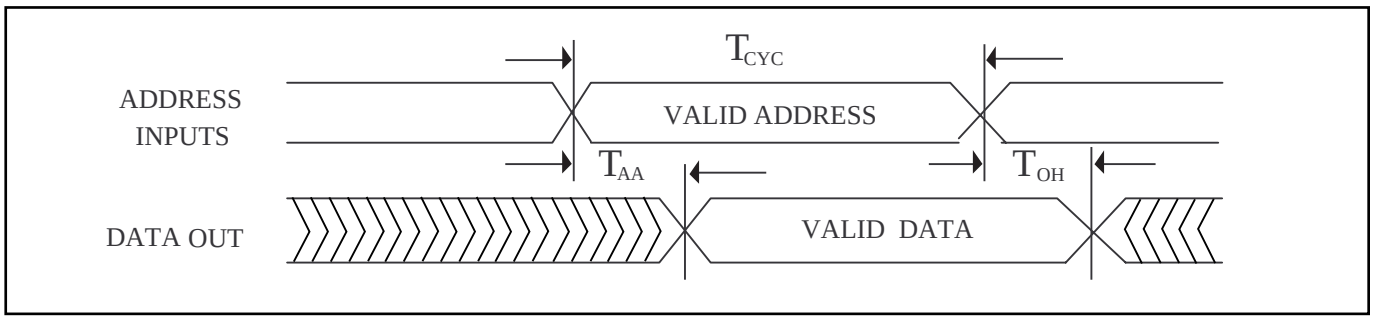
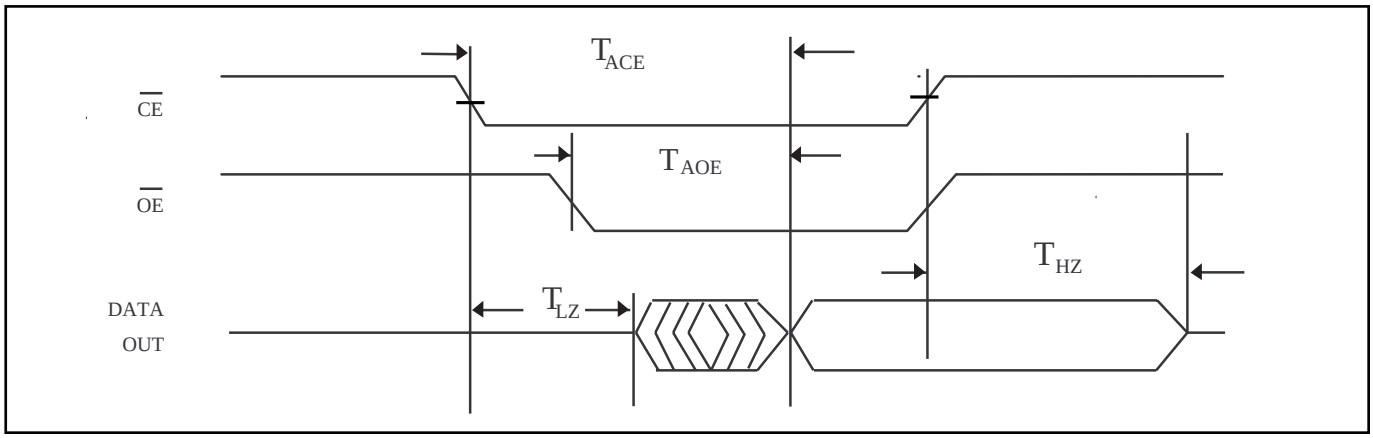
TIMING DIAGRAM

Propagation delay from address ($\overline{CE}$/$\overline{OE}$=Active)



Propagation delay from chip enable (Address vaild)



Propagation delay from chip enable (Address valid)