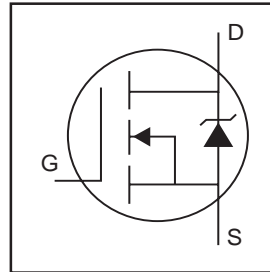


Features

- | Advanced Process Technology
- | Ultra Low On-Resistance
- | Dynamic dv/dt Rating
- | 175°C Operating Temperature
- | Fast Switching
- | Repetitive Avalanche Allowed up to Tjmax

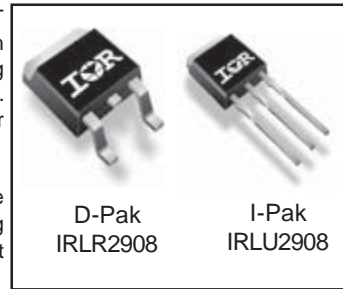


$V_{DSS} = 80V$
$R_{DS(on)} = 28m\Omega$
$I_D = 30A$

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, low R θ JC, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	39	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig. 9)	28	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	30	
I_{DM}	Pulsed Drain Current ①	150	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	120	W
	Linear Derating Factor	0.77	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	180	mJ
$E_{AS} (tested)$	Single Pulse Avalanche Energy Tested Value ⑦	250	
I_{AR}	Avalanche Current ①	See Fig.12a,12b,15,16	A
E_{AR}	Repetitive Avalanche Energy ⑥		mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.3	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

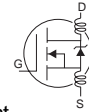
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	80	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.085	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	22.5	28	mΩ	$V_{GS} = 10V, I_D = 23A$ ④
		—	25	30		$V_{GS} = 4.5V, I_D = 20A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	35	—	—	S	$V_{DS} = 25V, I_D = 23A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	22	33	nC	$I_D = 23A$
Q_{gs}	Gate-to-Source Charge	—	6.0	9.1		$V_{DS} = 64V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	11	17		$V_{GS} = 4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 40V$
t_r	Rise Time	—	95	—		$I_D = 23A$
$t_{d(off)}$	Turn-Off Delay Time	—	36	—		$R_G = 8.3\Omega$
t_f	Fall Time	—	55	—		$V_{GS} = 4.5V$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1890	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	260	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	35	—		$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	1920	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	170	—		$V_{GS} = 0V, V_{DS} = 64V, f = 1.0\text{MHz}$
$C_{oss\text{ eff.}}$	Effective Output Capacitance	—	310	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 64V$



Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	39	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	150		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 23A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	75	110	ns	$T_J = 25^\circ\text{C}, I_F = 23A, V_{DD} = 25V$
Q_{rr}	Reverse Recovery Charge	—	210	310	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes ① through ⑧ are on page 11

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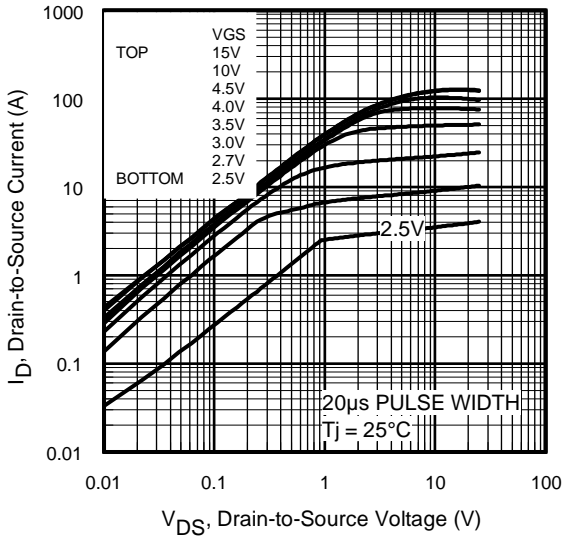


Fig 1. Typical Output Characteristics

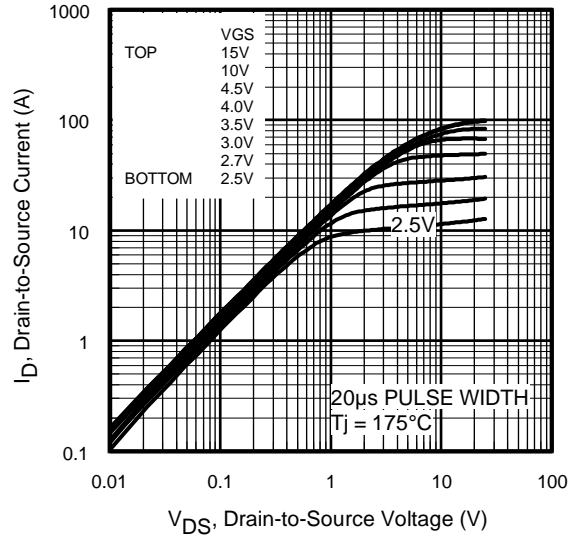


Fig 2. Typical Output Characteristics

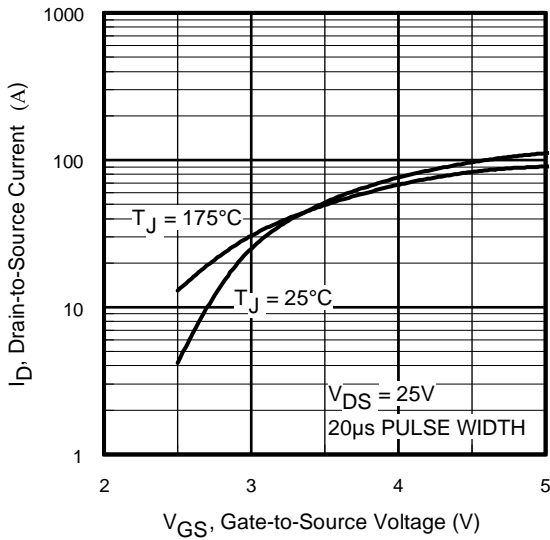


Fig 3. Typical Transfer Characteristics

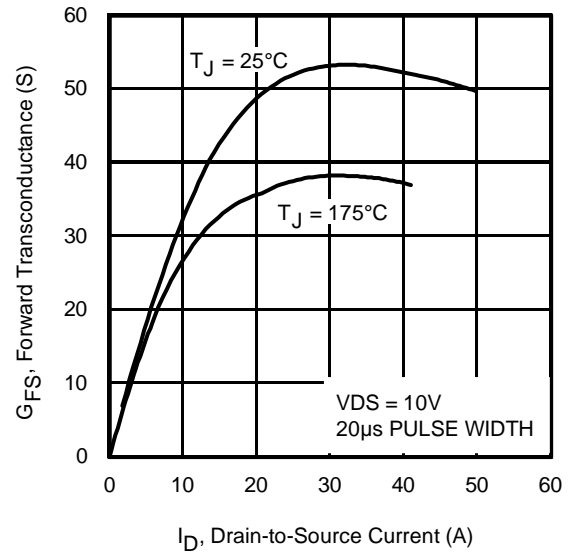


Fig 4. Typical Forward Transconductance vs. Drain Current

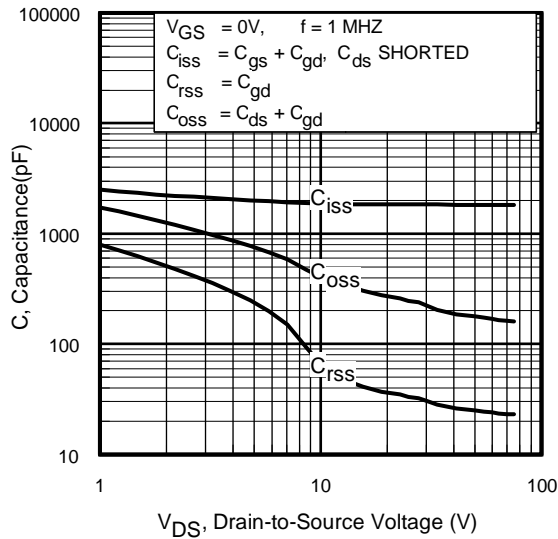


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

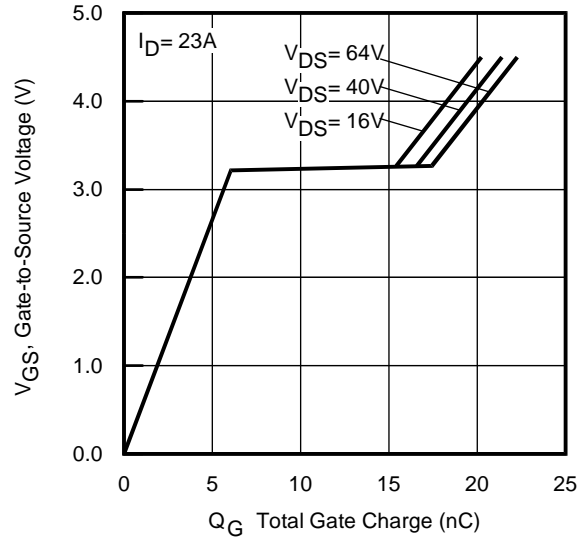


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

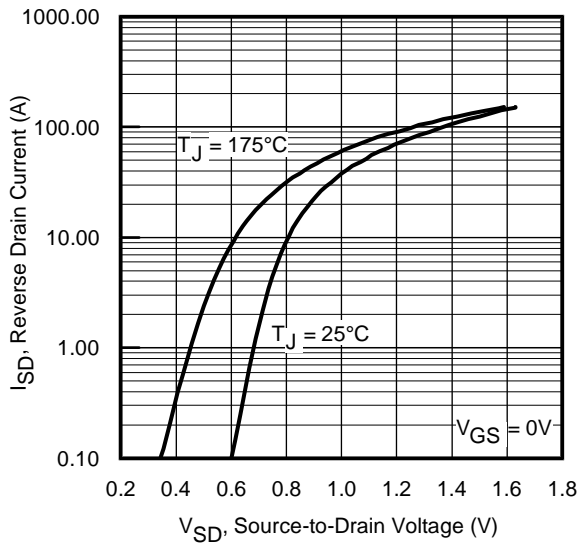


Fig 7. Typical Source-Drain Diode Forward Voltage

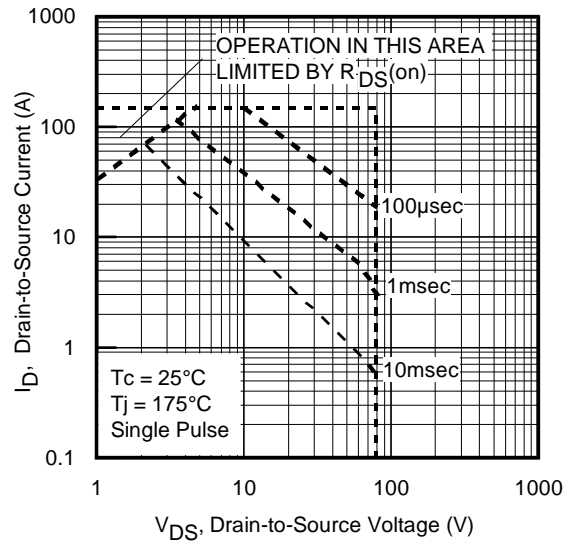


Fig 8. Maximum Safe Operating Area

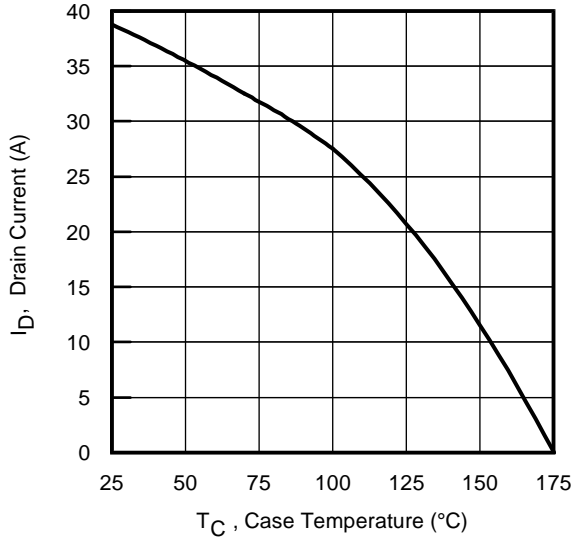


Fig 9. Maximum Drain Current vs. Case Temperature

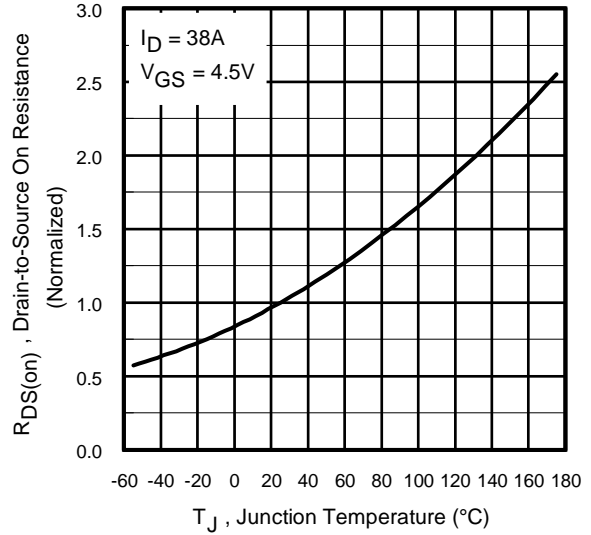


Fig 10. Normalized On-Resistance vs. Temperature

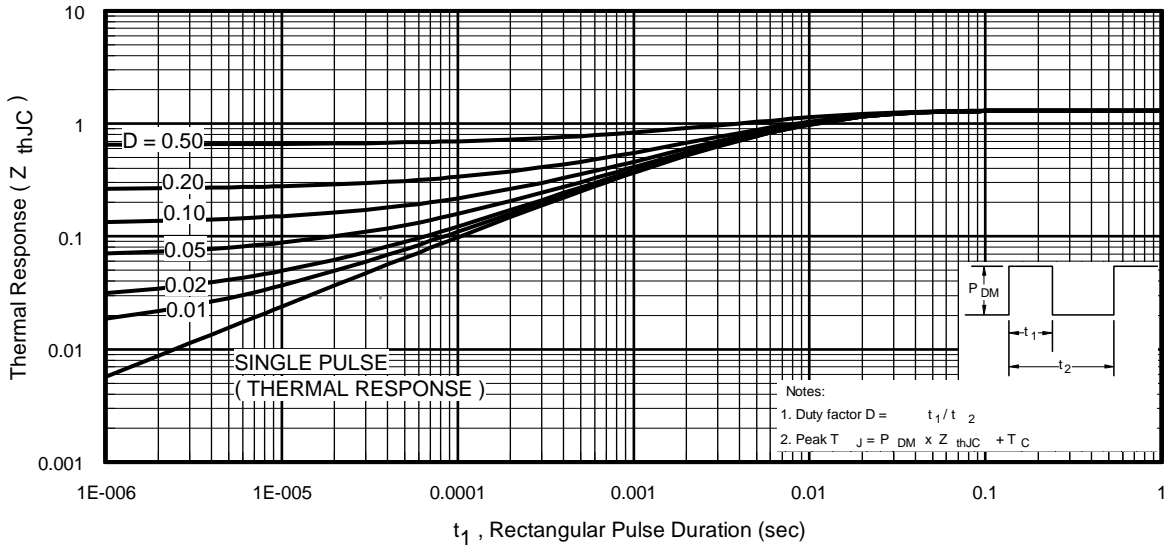


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

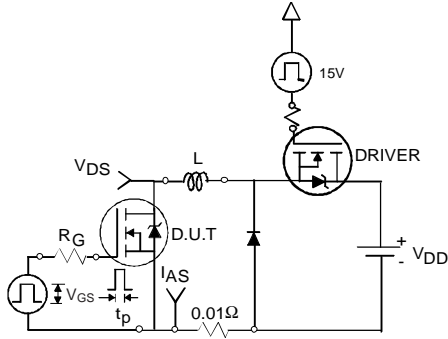


Fig 12a. Unclamped Inductive Test Circuit

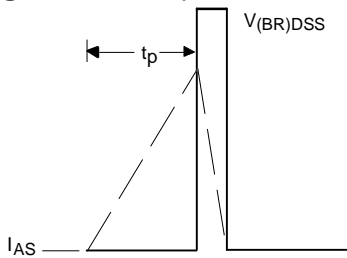


Fig 12b. Unclamped Inductive Waveforms

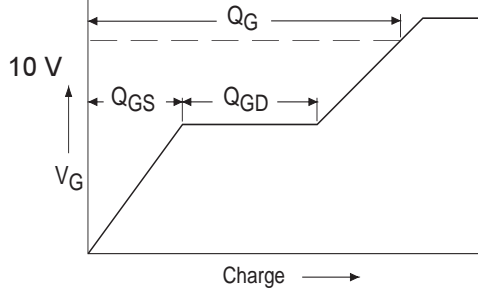


Fig 13a. Basic Gate Charge Waveform

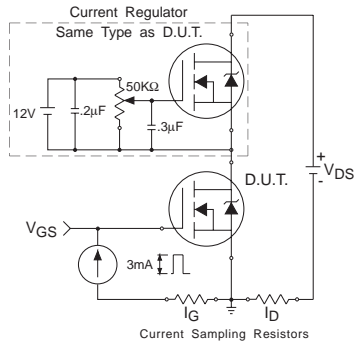


Fig 13b. Gate Charge Test Circuit

6

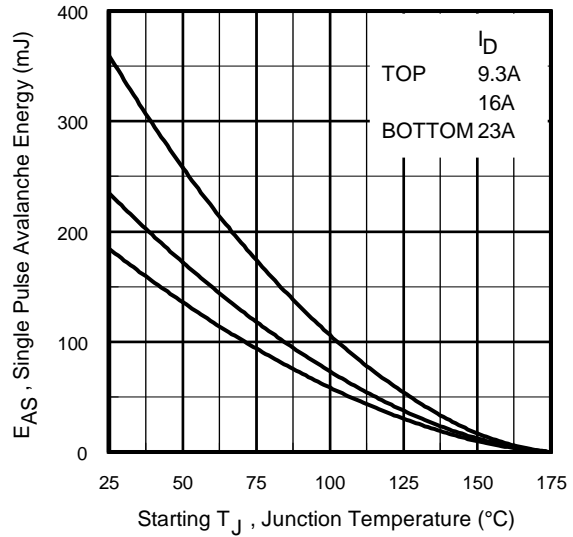


Fig 12c. Maximum Avalanche Energy vs. Drain Current

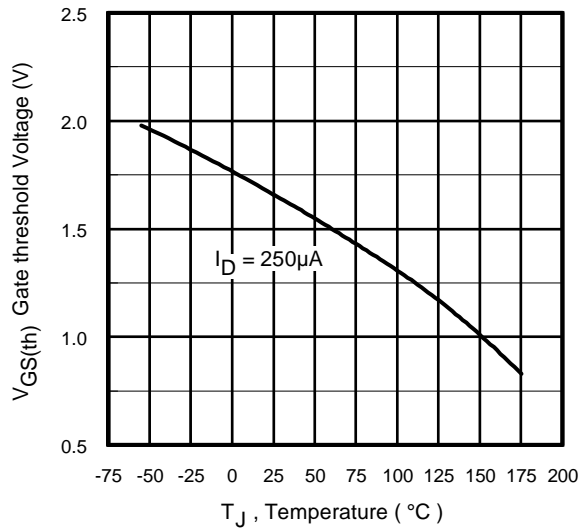


Fig 14. Threshold Voltage vs. Temperature

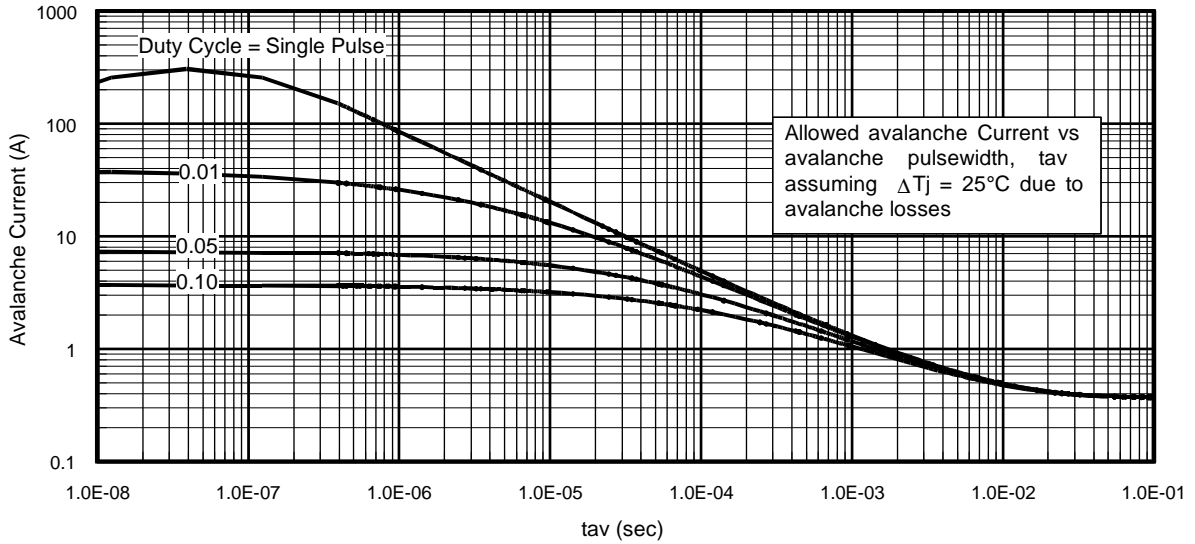


Fig 15. Typical Avalanche Current vs.Pulsewidth

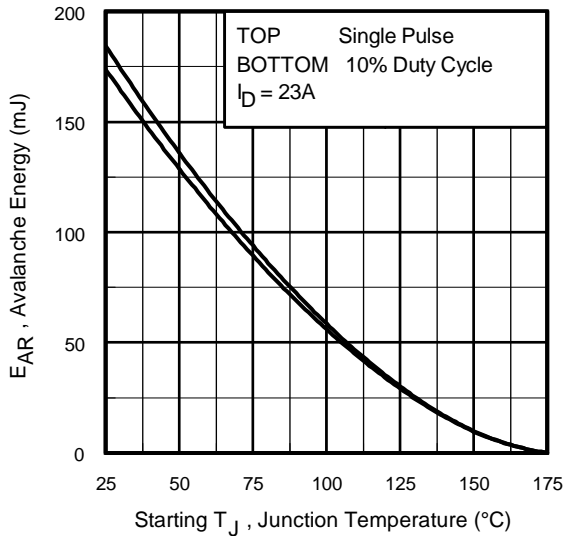


Fig 16. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

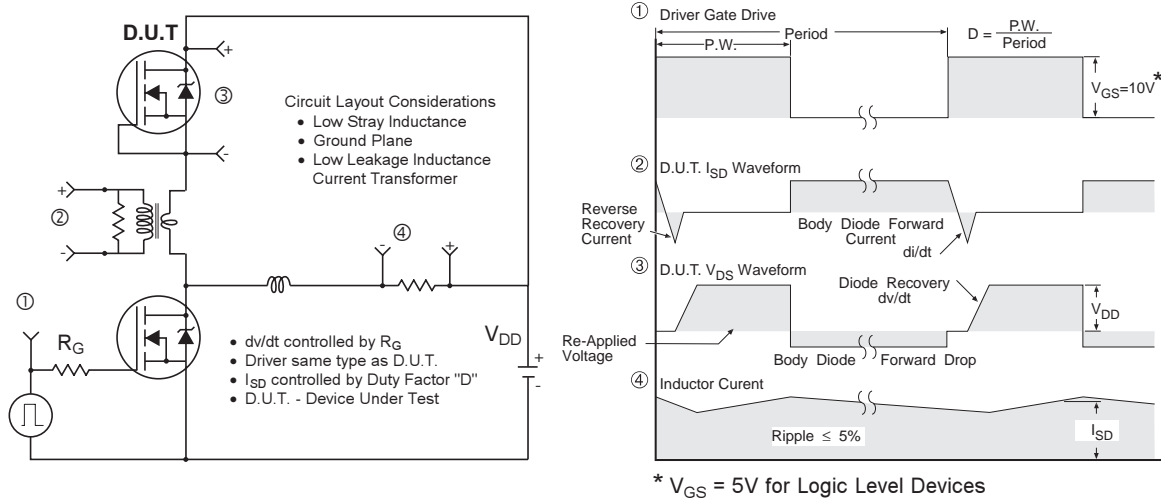


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

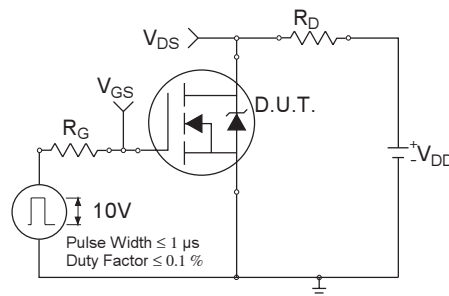


Fig 18a. Switching Time Test Circuit

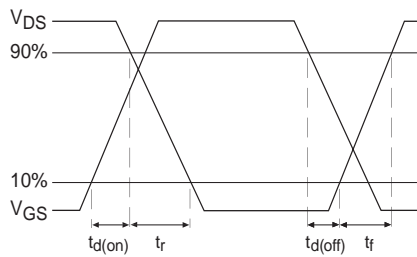
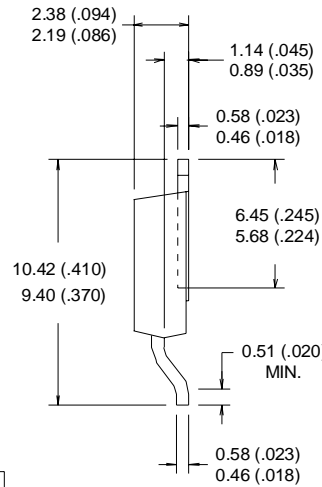
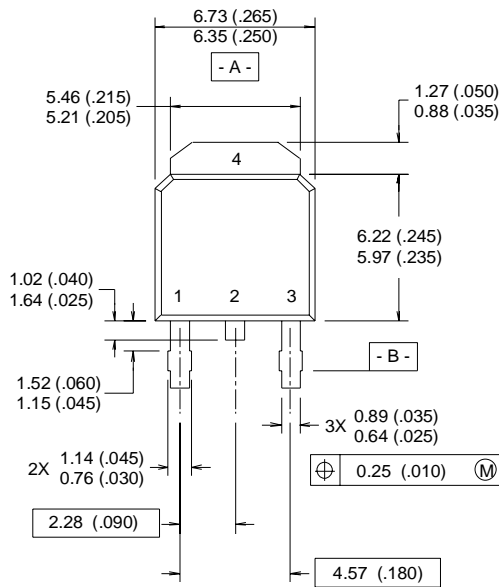


Fig 18b. Switching Time Waveforms

TO-252AA (D-Pak) Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

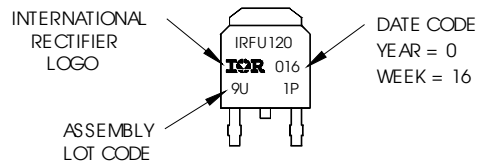
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-252AA.
- 4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

TO-252AA (D-Pak) Part Marking Information

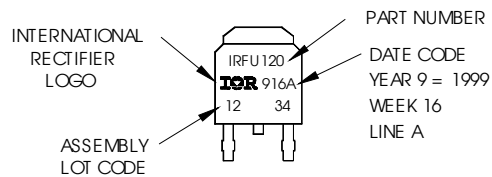
Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
 WITH ASSEMBLY
 LOT CODE 9U1P



Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
 WITH ASSEMBLY
 LOT CODE 1234
 ASSEMBLED ON WW 16, 1999
 IN THE ASSEMBLY LINE "A"

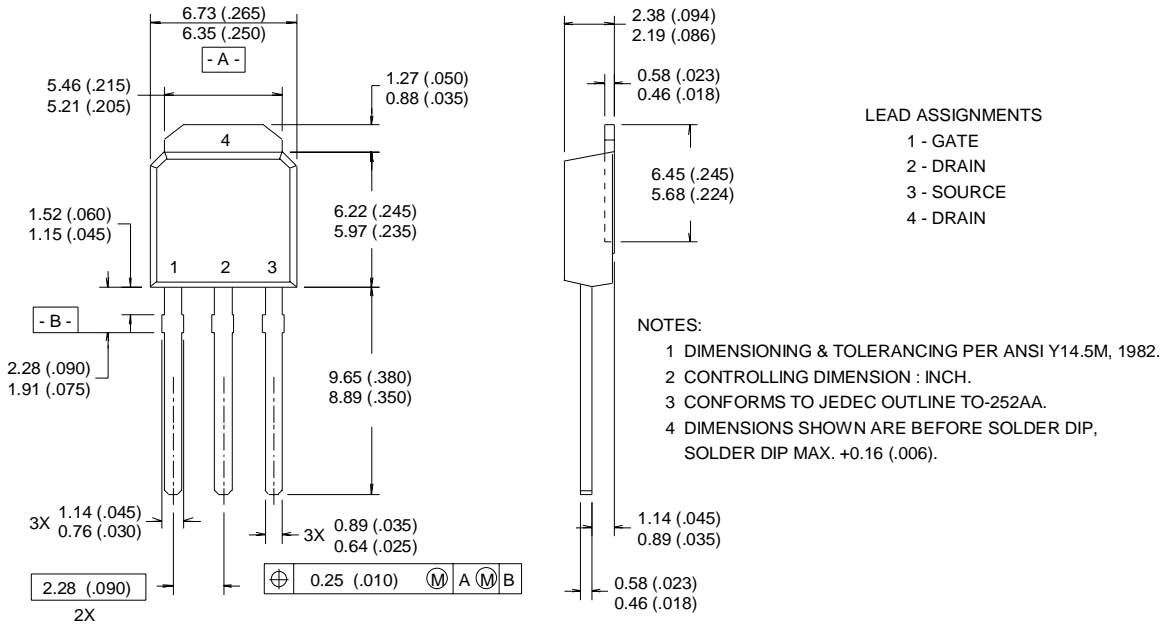


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I-Pak (TO-251AA) Package Outline

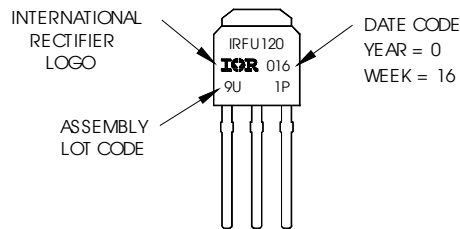
Dimensions are shown in millimeters (inches)



I-Pak (TO-251AA) Part Marking Information

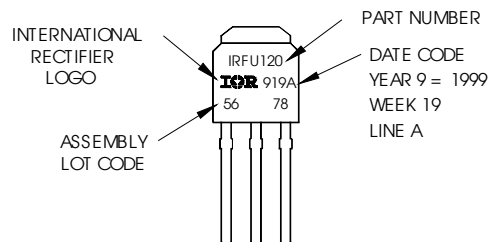
Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



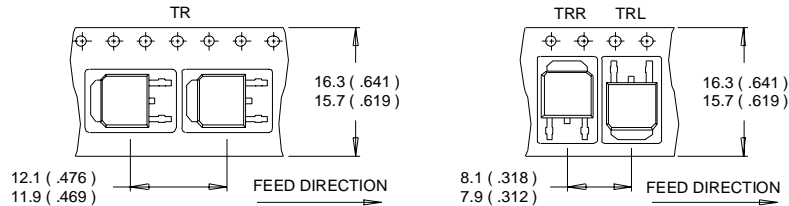
Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

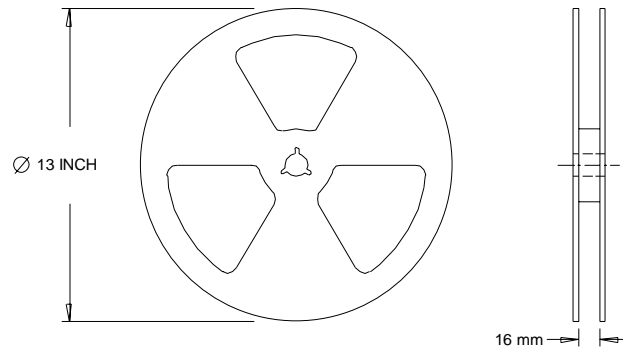


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.71\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 23\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value.
- ③ $I_{SD} \leq 23\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Automotive [Q101] market.
 Qualification Standards can be found on IR's Web site.