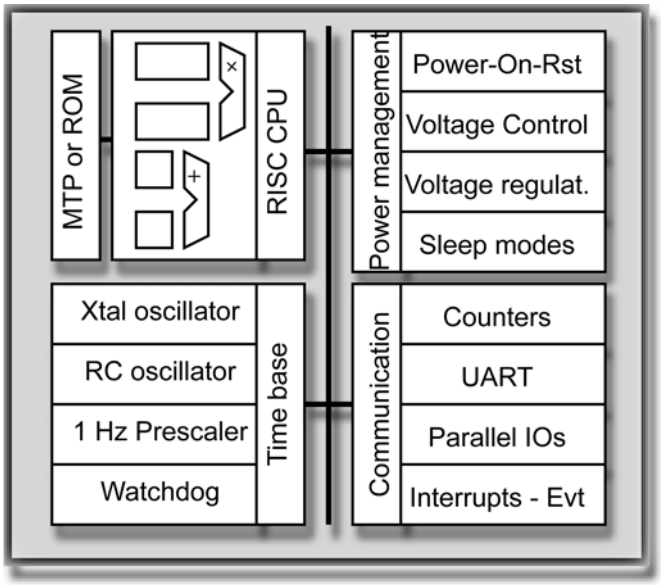

XE88LC03

Ultra Low-Power Microcontroller

General Description

- The XE88LC03 is an ultra low-power low-voltage microcontroller unit (MCU) with extremely high efficiency, allowing for 1 MIPS at 300uA at 2.4 V, and 8 x 8 bits multiplying in one clock cycle.
- XE88LC03 is available with on chip Multiple-Time-Programmable (MTP) program memory.

Applications

- Internet connected appliances
- Portable, battery operated instruments
- RF system supervisor
- Remote control
- HVAC control

Key product Features

- Ultra low-power MCU
  - 300 uA at 1 MIPS operation
  - 6 uA at 32 kHz operation
  - 1 uA time keeping
- Low-voltage operation (2.4 - 5.5 V supply voltage)
- 22 kB (8 kW) MTP, 512 + 8 B RAM
- 4 counters
- PWM, UART
- Analog matrix switching
- independant RC and crystal oscillators
- 5 reset, 17 interrupt, 8 event sources
- 100 years MTP Flash retention at 55°C

Ordering Information

Reference	Memory type	Temperature	Package
XE88LC03MI000	MTP Flash	-40°C to 85°C	die
XE88LC03MI015	MTP Flash	-40°C to 85°C	SO28
XE88LC03MI026	MTP Flash	-40°C to 85°C	TQFP32

1 Detailed Pin Description

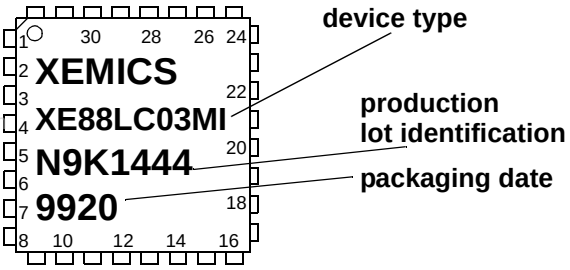

Figure 1.1: Pinout of the XE88LC03 in TQFP32 package

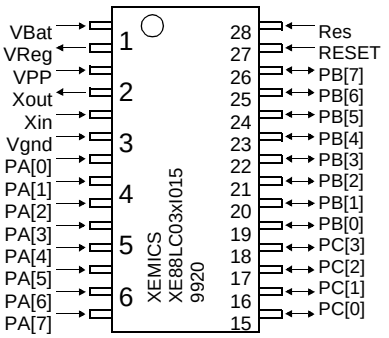

Figure 1.1: Pinout of the XE88LC03 in SOP28 package

Pin					Description
Position in SO28	Position in TQFP32	Function name	Second function name	Type	
1	13	Vbat		Power	Positive power supply
2	14	Vreg		Analog	Regulated supply
3	15	VPP	Vhigh/TEST	Special	Test mode/High voltage for MTP programing
4	16	XOut	OscOut/ptck	Analog/Input	Connection to Xtal/ Peripheral clock for test and MTP programing
5	17	XIn	OscIn/crck	Analog/Input	Connection to Xtal/ CoolRISC clock for test and MTP programing
6	18	Vss		Power	Negative power supply, connected to substrate
7	19	PA(0)	testin	Input	Input of Port A/ Data input for test and MTP programing/ Counter A input
8	20	PA(1)	testck	Input	Input of Port A/ Data clock for test and MTP programing/ Counter B input
9	21	PA(2)		Input	Input of Port A/ Counter C input/ Counter capture input
10	22	PA(3)		Input	Input of Port A/ Counter D input/ Counter capture input
11	23	PA(4)		Input	Input of Port A
12	24	PA(5)		Input	Input of Port A
13	25	PA(6)		Input	Input of Port A
14	26	PA(7)		Input	Input of Port A
15	27	PC(0)		Input/Output	Input-Output of Port C
16	28	PC(1)		Input/Output	Input-Output of Port C
17	29	PC(2)		Input/Output	Input-Output of Port C
18	30	PC(3)		Input/Output	Input-Output of Port C
	31	PC(4)		Input/Output	Input-Output of Port C
	32	PC(5)		Input/Output	Input-Output of Port C
	1	PC(6)		Input/Output	Input-Output of Port C
	2	PC(7)		Input/Output	Input-Output of Port C
19	3	PB(0)	testout	Input/Output/Analog	Input-Output-Analog of Port B/ Data output for test and MTP programing/ PWM output

Table 1.1: Pin-out of the XE88LC03 in SO28 and TQFP32
(see Table “IO pins performances” on page 15 for drive capabilities of the pins)

Pin					Description
Position in SO28	Position in TQFP32	Function name	Second function name	Type	
20	4	PB(1)		Input/Output/Analog	Input-Output-Analog of Port B/ PWM output
21	5	PB(2)		Input/Output/Analog	Input-Output-Analog of Port B
22	6	PB(3)	SOU	Input/Output/Analog	Input-Output-Analog of Port B, Output pin of USRT
23	7	PB(4)	S0/SCL	Input/Output/Analog	Input-Output-Analog of Port B/ Clock pin of USRT
24	8	PB(5)	S1/SIN	Input/Output/Analog	Input-Output-Analog of Port B/ Data input or input-output pin of USRT
25	9	PB(6)	Tx	Input/Output/Analog	Input-Output-Analog of Port B/ Emission pin of UART
26	10	PB(7)	Rx	Input/Output/Analog	Input-Output-Analog of Port B/ Reception pin of UART
27	11	RESET		Input	Reset pin (active high)
28	12	Reserved		Analog	To be connected to VSS

Table 1.1: Pin-out of the XE88LC03 in SO28 and TQFP32
(see Table “IO pins performances” on page 15 for drive capabilities of the pins)

2 Absolute maximum ratings

Stresses beyond these listed in this chapter may cause permanent damage to the device. No functional operation is implied at or beyond these conditions. Exposure to these conditions for an extended period may affect the device reliability.

Parameter	Value	Remarks
VBAT with respect to VSS	-0.3V to 6.0V	
Input voltage on any input pin	VSS-0.3V to VBAT+0.3V	
Storage temperature	-55°C to 125°C	1
Storage temperature for programmed MTP devices	-40°C to 85°C	1

Table 2.1: Absolute maximum ratings

Note: 1) For unprogrammed MTP devices. Blocking bits and software must be rewritten in MTP devices if storage temperature exceedes storage temperature for programmed devices.

These devices are ESD sensitive. Although these devices feature proprietary ESD protection structures, permanent damage may occur on devices subjected to high energy electrostatic discharges. Proper ESD precautions have to be taken to avoid performance degradation or loss of functionality.

3 Electrical Characteristics

All specification are -40°C to 85°C unless otherwise noted. ROM operates up to 125°C.

Operation conditions		min	typ	max	Unit	Remarks
Power supply	ROM version	2.4		5.5	V	
	MTP version	2.4		5.5	V	
Operating speed	2.4 V to 5.5 V	0.032		2	MHz	
Instruction cycle	any instruction		500		ns	4
Current requirement	CPU running at 1 MIPS			310	uA	1
	CPU running at 32 kHz on Xtal, RC off			10	uA	1
	CPU halt, timer on Xtal, RC off			1	uA	1
	CPU halt, timer on Xtal, RC ready			1.7	uA	1
	CPU halt, Xtal off timer on RC at 100 kHz			1.4	uA	1
	Voltage level detection			15	uA	
MTP Flash instruction memory	Prog. voltage		11.5		V	
	Erase time	0.2		1	s	5
	Write/Erase cycles	10	100			3
	Data retention	10			years	85°C, 2
		100			years	55°C, 2

Table 3.1: Specifications and current requirement of the XE88LC03

Note:
1) Power supply: 2.4 V - 5.5 V, temperature is 27°C.
2) < 10 erase cycles.
3) More cycles possible during development, with restraint retention
4) With 2 MHz clock, all instructions are using exactly 1 clock cycle
5) Longer erase time may degrade retention

4 CPU

The XE88LC03 CPU is a low power RISC core. It has 16 internal registers for efficient implementation of the C compiler. Its instruction set is made of 35 generic instructions, all coded on 22 bits, with 8 addressing modes. All instructions are executed in one clock cycle, including conditional jumps and 8x8 multiplication.

5 Memory organization

The CPU uses a Harvard architecture, so that memory is organized in two separated fields: program memory and data memory. As both memories are separated, the central processing unit can read/write data at the same time it loads an instruction. Peripherals and system control registers are mapped on data memory space.

Program memory is made in one page. Data is made of several 256 bytes pages.

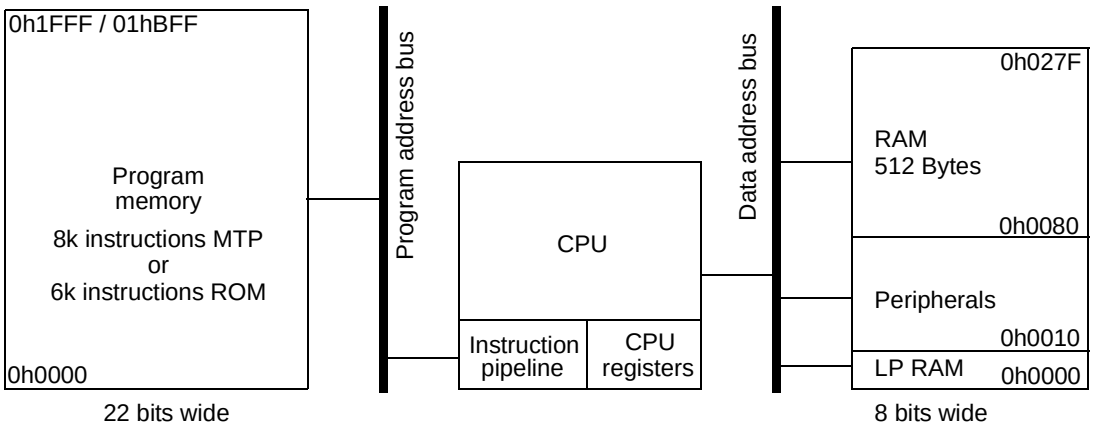

Figure 5.1: Memory organization

5.1 Program memory

The program memory is implemented as Multiple Time Programmable (MTP) Flash memory or ROM. The power consumption of MTP memory is linear with the access frequency (no significant static current).

Size of the MTP Flash memory is 8192 x 22 bits (= 22 kBytes)

block	size	address
MTP	8192 x 22	H0000 - H1FFF

Table 5.1: Program addresses for MTP memory

5.2 Data memory

The data memory is implemented as static Random-Access Memory (RAM). The RAM size is 512 x 8 bits plus 8 low power RAM bytes that require very low current when addressed. Programs using the low-power RAM instead of RAM will use even less current.

block	size	address
LP RAM	8 x 8	H0000 - H0007
RAM	512 x 8	H0080 - H027F

Table 5.2: RAM addresses

6 Registers list

Left column include register name and address.

Right columns include bit name, access (r: read, r0: always 0 when read, w: write, c: cleared by writing any value, c1: cleared by writing 1), and reset status (0 or 1) and signal. Empty bits are reserved for future use and should not be written, neither should their read value be used for any purpose as it may change without notice.

6.1 Peripherals mapping

block	size	address	Page
LP RAM	8x8	H0000-H0007	Page 0
System control	16x8	H0010-H001F	
Port A	8x8	H0020-H0027	
Port B	8x8	H0028-H002F	
Port C	4x8	H0030-H0033	
Reserved	4x8	H0034-H0037	
MTP	4x8	H0038-H003B	
Event	4x8	H003C-H003F	
Interrupts control	8x8	H0040-H0047	
reserved	8x8	H0048-H004F	
UART	8x8	H0050-H0057	
Counters	8x8	H0058-H005F	
Zooming ADC	8x8	H0060-H0067	
Reserved	12x8	H0068-H0073	
DACs	8x8	H0074-H007B	
Other (VLD)	4x8	H007C-H007F	
RAM1	128x8	H0080 - H00FF	
RAM2	256x8	H0100 - H01FF	Page 1
RAM3	128x8	H0200 - H027F	Page 2

Table 6.1: Peripherals addresses

6.2 Resets

The reset source name is simplified in the following registers description. Name mapping is in the next table.

reset source	name in this document
resetsystem	global
resetSynch	
resetPOR	cold
resetCold	
resetPad	
resetPconf	pconf
resetSleep	sleep

Table 6.2: Reset signal name mapping

6.3 Low power RAM

Low power RAM is a small additionnal RAM area with extremely low power requirement.

Name Address	7	6	5	4	3	2	1	0
h0000	rw	rw	rw	rw	rw	rw	rw	rw
h0001	rw	rw	rw	rw	rw	rw	rw	rw
h0002	rw	rw	rw	rw	rw	rw	rw	rw
h0003	rw	rw	rw	rw	rw	rw	rw	rw
h0004	rw	rw	rw	rw	rw	rw	rw	rw
h0005	rw	rw	rw	rw	rw	rw	rw	rw
h0006	rw	rw	rw	rw	rw	rw	rw	rw
h0007	rw	rw	rw	rw	rw	rw	rw	rw

Table 6.3: Low power RAM

6.4 System, oscillators, prescaler and watchdog

Name Address	7	6	5	4	3	2	1	0
RegSysCtrl h0010, type 1	SleepEn rw, 0 por	EnRes-PConf rw, 0 cold	EnBus-Error rw, 0 cold	EnResWD rw, 0 cold				
RegSysReset h0011, type 1	Sleep w, 0 cold	ResPor r, 0	ResBus-Error rc, 0 cold	ResWD rc, 0 cold	ResPortA rc, 0 cold	ResPad-Deb rc, 0 cold	ResPad rc, 0 cold	
RegSysClock h0012, type 1	CpuSel rw, 0 sleep	ExtClk r, 0 cold	EnExtClk rw, 0 cold	BiasRC rw, 1 cold	ColdXtal r, 1 sleep	ColdRC r, 1 sleep	EnableXtal rw, 0 sleep	EnableRC rw, 1 sleep
RegSysMisc h0013, type 1					RCOnPA0 rw, 0 sleep	DebFast rw, 0 sleep	Output-CkXtal rw, 0 sleep	Output-CkCPU rw, 0 sleep
RegSysWD h0014					WatchDog(3) special	WatchDog(2) special	WatchDog(1) special	WatchDog(0) special
RegSysPre0 h0015								ResPre ClearLow-Prescal (*) w, 0 cold
RegSysRCTrim1 h001B				RCFreq-Range rw, 0 cold	RCFreq-Coarse(3) rw, 0 cold	RCFreq-Coarse(2) rw, 0 cold	RCFreq-Coarse(1) rw, 0 cold	RCFreq-Coarse(0) rw, 0 cold
RegSysRCTrim2 h001C			RCFreq-Fine(5) rw, 1 cold	RCFreq-Fine(4) rw, 0 cold	RCFreq-Fine(3) rw, 0 cold	RCFreq-Fine(2) rw, 0 cold	RCFreq-Fine(1) rw, 0 cold	RCFreq-Fine(0) rw, 0 cold

Table 6.4: System control registers

6.5 PortA

Name Address	7	6	5	4	3	2	1	0
RegPAIn h0020	PAIn(7) r	RegPAIn(6) r	PAIn(5) r	PAIn(4) r	PAIn(3) r	PAIn(2) r	PAIn(1) r	PAIn(0) r
RegPADebounce h0021	PADeb(7) rw, 0 pconf	PADeb(6) rw, 0 pconf	PADeb(5) rw, 0 pconf	PADeb(4) rw, 0 pconf	PADeb(3) rw, 0 pconf	PADeb(2) rw, 0 pconf	PADeb(1) rw, 0 pconf	PADeb(0) rw, 0 pconf
RegPAEdge h0022	PAEdge(7) rw, 0 global	PAEdge(6) rw, 0 global	PAEdge(5) rw, 0 global	PAEdge(4) rw, 0 global	PAEdge(3) rw, 0 global	PAEdge(2) rw, 0 global	PAEdge(1) rw, 0 global	PAEdge(0) rw, 0 global
RegPAPullup h0023, type 1	PAPullUp(7) rw, 0 pconf	PAPullUp(6) rw, 0 pconf	PAPullUp(5) rw, 0 pconf	PAPullUp(4) rw, 0 pconf	PAPullUp(3) rw, 0 pconf	PAPullUp(2) rw, 0 pconf	PAPullUp(1) rw, 0 pconf	PAPullUp(0) rw, 0 pconf
RegPARes0 h0024	PARes0(7) rw, 0 global	PARes0(6) rw, 0 global	PARes0(5) rw, 0 global	PARes0(4) rw, 0 global	PARes0(3) rw, 0 global	PARes0(2) rw, 0 global	PARes0(1) rw, 0 global	PARes0(0) rw, 0 global
RegPARes1 h0025	PARes1(7) rw, 0 global	PARes1(6) rw, 0 global	PARes1(5) rw, 0 global	PARes1(4) rw, 0 global	PARes1(3) rw, 0 global	PARes1(2) rw, 0 global	PARes1(1) rw, 0 global	PARes1(0) rw, 0 global

Table 6.5: Port A registers

6.6 PortB

Name Address	7	6	5	4	3	2	1	0
RegPBOut h0028	PBOut(7) rw, 0 pconf	PBOut(6) rw, 0 pconf	PBOut(5) rw, 0 pconf	PBOut(4) rw, 0 pconf	PBOut(3) rw, 0 pconf	PBOut(2) rw, 0 pconf	PBOut(1) rw, 0 pconf	PBOut(0) rw, 0 pconf
RegPBIn h0029	PBIn(7) r	PBIn(6) r	PBIn(5) r	PBIn(4) r	PBIn(3) r	PBIn(2) r	PBIn(1) r	PBIn(0) r
RegPBDir h002A	PBDir(7) rw, 0 pconf	PBDir(6) rw, 0 pconf	PBDir(5) rw, 0 pconf	PBDir(4) rw, 0 pconf	PBDir(3) rw, 0 pconf	PBDir(2) rw, 0 pconf	PBDir(1) rw, 0 pconf	PBDir(0) rw, 0 pconf
RegPBOpen h002B	PBOpen(7) rw, 0 pconf	PBOpen(6) rw, 0 pconf	PBOpen(5) rw, 0 pconf	PBOpen(4) rw, 0 pconf	PBOpen(3) rw, 0 pconf	PBOpen(2) rw, 0 pconf	PBOpen(1) rw, 0 pconf	PBOpen(0) rw, 0 pconf
RegPBPullup h002C	PBPullUp(7) rw, 0 pconf	PBPullUp(6) rw, 0 pconf	PBPullUp(5) rw, 0 pconf	PBPullUp(4) rw, 0 pconf	PBPullUp(3) rw, 0 pconf	PBPullUp(2) rw, 0 pconf	PBPullUp(1) rw, 0 pconf	PBPullUp(0) rw, 0 pconf
RegPBAna h002D					PBAna(3) rw, 0 pconf	PBAna(2) rw, 0 pconf	PBAna(1) rw, 0 pconf	PBAna(0) rw, 0 pconf

Table 6.6: Port B registers

6.7 PortC

Name Address	7	6	5	4	3	2	1	0
RegPCOut h0030	PCOut(7) rw, 0 pconf	PCOut(6) rw, 0 pconf	PCOut(5) rw, 0 pconf	PCOut(4) rw, 0 pconf	PCOut(3) rw, 0 pconf	PCOut(2) rw, 0 pconf	PCOut(1) rw, 0 pconf	PCOut(0) rw, 0 pconf
RegPCIn h0031	PCIn(7) r	PCIn(6) r	PCIn(5) r	PCIn(4) r	PCIn(3) r	PCIn(2) r	PCIn(1) r	PCIn(0) r
RegPCDir h0032	PCDir(7) rw, 0 pconf	PCDir(6) rw, 0 pconf	PCDir) rw, 0 pconf	PCDir(4) rw, 0 pconf	PCDir(3) rw, 0 pconf	PCDir(2) rw, 0 pconf	PCDir(1) rw, 0 pconf	PCDir(0) rw, 0 pconf

Table 6.7: Port C registers

6.8 MTP

Name Address	7	6	5	4	3	2	1	0
RegEEP h0038	rw	rw	rw	rw	rw	rw	rw	rw
RegEEP1 h0039	rw	rw	rw	rw	rw	rw	rw	rw
RegEEP2 h003A	special	special	special	special	special	special	special	special
RegEEP3 h003B	special	special	special	special	special	special	special	special

Table 6.8: MTP control registers

6.9 Events

Name Address	7	6	5	4	3	2	1	0
RegEvn h003C	EvnCntA rc1, 0 global	EvnCntC rc1, 0 global	EvnPre1 rc1, 0 global	EvnPA(1) rc1, 0 global	EvnCntB rc1, 0 global	EvnCntD rc1, 0 global	EvnPre2 rc1, 0 global	EvnPA(0) rc1, 0 global
RegEvnEn h003D	EvnEnCntA rw, 0 global	EvnEnCntC rw, 0 global	EvnEnPre1 rw, 0 global	EvnEnPA(1) rw, 0 global	EvnEnCntB rw, 0 global	EvnEnCntD rw, 0 global	EvnEnPre2 rw, 0 global	EvnEnPA(0) rw, 0 global
RegEvnPriority h003E	EvnPriority(7) r,1 global	EvnPriority(6) r,1 global	EvnPriority(5) r,1 global	EvnPriority(4) r,1 global	EvnPriority(3) r,1 global	EvnPriority(2) r,1 global	EvnPriority(1) r,1 global	EvnPriority(0) r,1 global
RegEvnEvn h003F							EvnHigh r, 0 global	EvnLow r, 0 global

Table 6.9: Events control registers

6.10 Interrupts

Name Address	7	6	5	4	3	2	1	0
RegIrqHig h0040		IrqPre1 rc1, 0 global		IrqCntA rc1, 0 global	IrqCntC rc1, 0 global		IrqUartTx rc1, 0 global	IrqUartRx rc1, 0 global
RegIrqMid h0041			IrqPA(5) rc1, 0 global	IrqPA(4) rc1, 0 global	IrqPre2 rc1, 0 global	IrqVld rc1, 0 global	IrqPA(1) rc1, 0 global	IrqPA(0) rc1, 0 global
RegIrqLow h0042	IrqPA(7) rc1, 0 global	IrqPA(6) rc1, 0 global	IrqCntB rc1, 0 global	IrqCntD rc1, 0 global	IrqPA(3) rc1, 0 global	IrqPA(2) rc1, 0 global		
RegIrqEnHig h0043		IrqEnPre1 rw, 0 global		IrqEnCntA rw, 0 global	IrqEnCntC rw, 0 global		IrqEnUartTx rw, 0 global	IrqEnUartRx rw, 0 global
RegIrqEnMid h0044			IrqEnPA(5) rw, 0 global	IrqEnPA(4) rw, 0 global	IrqEnPre2 rw, 0 global	IrqEnVld rw, 0 global	IrqEnPA(1) rw, 0 global	IrqEnPA(0) rw, 0 global
RegIrqEnLow h0045	IrqEnPA(7) rw, 0 global	IrqEnPA(6) rw, 0 global	IrqEnCntB rw, 0 global	IrqEnCntD rw, 0 global	IrqEnPA(3) rw, 0 global	IrqEnPA(2) rw, 0 global		
RegIrqPriority h0046	IrqPriority(7) r, 1 global	IrqPriority(6) r, 1 global	IrqPriority(5) r, 1 global	IrqPriority(4) r, 1 global	IrqPriority(3) r, 1 global	IrqPriority(2) r, 1 global	IrqPriority(1) r, 1 global	IrqPriority(0) r, 1 global
RegIrqIrq h0047						IrqHig r, 0 global	IrqMid r, 0 global	IrqLow r, 0 global

Table 6.10: Interrupts control registers

6.11 USRT

Name Address	7	6	5	4	3	2	1	0
RegUsrtSin h0048								UsrtSin rw, 1 global
RegUsrtScl h0049								UsrtScl rw, 1 global
RegUsrtCtrl h004A					UsrtWaitS0 r, 0 global	UsrtEnWait-Cond1 rw, 0 global	UsrtEnWaitS0 rw, 0 global	UsrtEnable rw, 0 global
RegUsrtData h004D								UsrtData r
RegUsrtEdgeScl h004E								UsrtEdgeScl r, 0 global

Table 6.11: USRT control registers

6.12 UART

Name Address	7	6	5	4	3	2	1	0
RegUartCtrl h0050	UartEcho rw, 0 global	UartEnRx rw, 0 global	UartEnTx rw, 0 global	UartXRx rw, 0 global	UartXTx rw, 0 global	UartBR(2) rw, 1 global	UartBR(1) rw, 0 global	UartBR(0) rw, 1 global
RegUartCmd h0051	SelXtal rw, 0 global	UartWakeup rw, 0 global	UartRCSel(2) rw, 0 global	UartRCSel(1) rw, 0 global	UartRCSel(0) rw, 0 global	UartPM rw, 0 global	UartPE rw, 0 global	UartWL rw, 1 global
RegUartTx h0052	UartTx(7) rw, 0 global	UartTx(6) rw, 0 global	UartTx(5) rw, 0 global	UartTx(4) rw, 0 global	UartTx(3) rw, 0 global	UartTx(2) rw, 0 global	UartTx(1) rw, 0 global	UartTx(0) rw, 0 global
RegUartTxSta h0053							UartTxBusy r, 0 global	UartTxFull r, 0 global
RegUartRx h0054	UartRx(7) r	UartRx(6) r	UartRx(5) r	UartRx(4) r	UartRx(3) r	UartRx(2) r	UartRx(1) r	UartRx(0) r
RegUartRxSta h0055			UartRxSErr r	UartRxPErr r	UartRxFErr r	UartRxOErr c	UartRxBusy r	UartRxFull r

Table 6.12: UART control registers

6.13 Counters

Name Address	7	6	5	4	3	2	1	0
RegCntA h0058	CounterA(7) rw	CounterA(6) rw	CounterA(5) rw	CounterA(4) rw	CounterA(3) rw	CounterA(2) rw	CounterA(1) rw	CounterA(0) rw
RegCntB h0059	CounterB(7) rw	CounterB(6) rw	CounterB(5) rw	CounterB(4) rw	CounterB(3) rw	CounterB(2) rw	CounterB(1) rw	CounterB(0) rw
RegCntC h005A	CounterC(7) rw	CounterC(6) rw	CounterC(5) rw	CounterC(4) rw	CounterC(3) rw	CounterC(2) rw	CounterC(1) rw	CounterC(0) rw
RegCntD h005B	CounterD(7) rw	CounterD(6) rw	CounterD(5) rw	CounterD(4) rw	CounterD(3) rw	CounterD(2) rw	CounterD(1) rw	CounterD(0) rw
RegCntCtrlCk h005C	CntDSel(1) rw	CntDSel(0) rw	CntCSel(1) rw	CntCSel(0) rw	CntBSel(1) rw	CntBSel(0) rw	CntASel(1) rw	CntASel(0) rw
RegCntConfig1 h005D	CntDDownUp rw	CntCDownUp rw	CntBDownUp rw	CntADownUp rw	CascadeCD rw	CascadeAB rw	CntPWM1 rw, 0 global	CntPWM0 rw, 0 global
RegCntConfig2 h005E	CapSel(1) rw, 0 global	CapSel(0) rw, 0 global	CapFunc(1) rw, 0 global	CapFunc(0) rw, 0 global	PWM1Size(1) rw	PWM1Size(0) rw	PWM0Size(1) rw	PWM0Size(0) rw
RegCntOn h005F					CntDEnable rw, 0 global	CntCEnable rw, 0 global	CntBEnable rw, 0 global	CntAEnable rw, 0 global

Table 6.13: Counters control registers

6.14 Vld registers

Name Address	7	6	5	4	3	2	1	0
RegVldCtrl h007E					VldMult rw, 0 cold	VldTune(2) rw, 0 cold	VldTune(1) rw, 0 cold	VldTune(0) rw, 0 cold
RegVldStat h007F						VldIrq r, 0 global	VldValid r, 0 global	VldEn rw, 0 global

Table 6.14: Vmult and Vld control registers

7 Peripherals

The XE88LC03 includes usual microcontroller peripherals and some other blocks more specific to low-voltage or mixed-signal operation. There are 3 parallel ports, one input port (A), one IO and analog port (B) with analog switching capabilities and one general purpose IO port (C). A watchdog is available, connected to a prescaler. Four 8-bit counters, with capture, PWM and chaining capabilities are available. The UART can handle transmission speeds as high as 115kbaud.

Low-power low-voltage blocks include a voltage level detector, two oscillators (one internal 0.1-2 MHz RC oscillator and a 32 kHz crystal oscillator) and a specific regulation scheme that largely uncouples current requirement from external power supply (usual CMOS ASICs require much more current at 5.5 V than they need at 2.4 V. This is not the case for the XE88LC03).

7.1 Counters

- 4 8-bit counters
- Daisy chain on 16 bits
- PWM on 8-16 bits
- Capture - compare on 16 bits
- Events and interrupts generation

7.2 Prescaler

- Interrupt generated with 8 millisecond or 1 second period for ultra low power hibernation mode

7.3 Watchdog

- 2 seconds watchdog

7.4 UART

- full duplex operation with buffered receiver and transmitter.
- internal baud rate generator with programmable baud rate (300 - 115’000 bauds).
- 7 or 8 bits word length.
- even, odd, or no-parity bit generation and detection
- 1 stop bit
- error receive detection: Start, Parity, Frame and Overrun
- receiver echo mode
- 2 interrupts (receive full and transmit empty)
- enable receive and/or transmit
- invert pad Rx and/or Tx

7.5 Xtal clock

The Xtal Oscillator operates with an external crystal of 32’768 Hz.

symbol	description	min	typ	max	unit	comments
f_clk32k	nominal frequency		32768		Hz	
st_x32k	oscillator start-up time		1	2	s	for full precision
duty_clk32k	duty cycle on the digital output	30	50	70	%	
fstab_1	relative frequency deviation from nominal, for a crystal with CL=8.2 pF and temperature between -40° and +85°C	-100		+300	ppm	not included: crystal frequency tolerance and aging crystal frequency - temperature dependence

Table 7.1: Xtal oscillator specifications.

Note: Board layout recommendations for safer crystal oscillation and lower current consumption:
Keep lines xtal_in and xtal_out short and insert a VSS line between them.
Connect package of the crystal to VSS.
No noisy or digital lines near xtal_in and xtal_out.
Insert guards at VSS where needed.

7.6 RC oscillator

The RC Oscillator is always turned on at power-on reset and can be turned off after the optional Xtal oscillator has been started. The RC oscillator has two frequency ranges: sub-MHz (100KHz to 1MHz) and above-MHz (1MHz to max MCU frequency). Inside a range, the frequency can be tuned by software for coarse and fine adjustment.

Note: No external component is required for the RC oscillator.

The RC oscillator can be in 3 modes. In mode 1(RC on), the RC oscillator and its bias are on. In mode 2 (RC ready), the RC oscillator is off and the bias is on. In mode 3 (RC off), the RC oscillator and the bias are off. RC ready mode is a compromise between power consumption and start-up time.

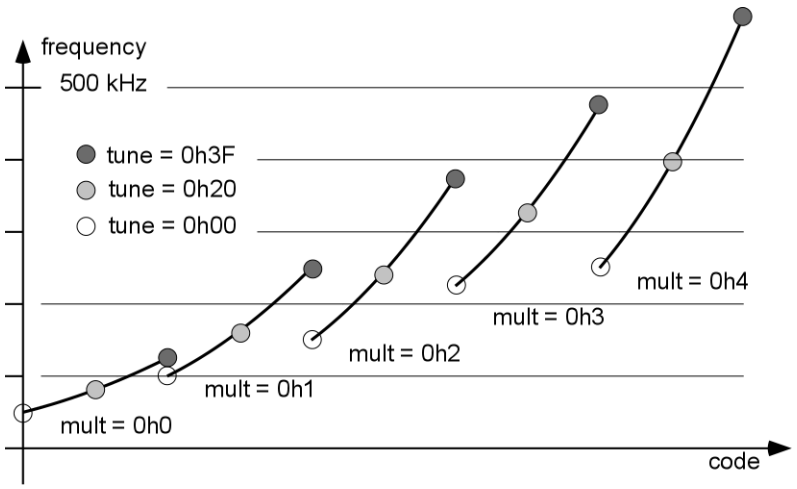

Figure 7.1: RC frequencies programming example for low range (typical values)

symbol	description	min	typ	max	unit	comments
F_{st}	frequency at start-up	40	80	120	kHz	at 27°C
range	range selection	1		10		multiplies F_{st}
mult[3:0]	coarse tuning range	1		16		4 bits, multiplies F_{st} * range
tune[5:0]	fine tuning range	0.65		1.5		6 bits, multiplies F_{st} * range * mult
	fine tuning step		1.4	2	%	
T_{st}	start-up time		30	50	ms	bias current is off (RC off)
O_{st}	overshoot at start-up			50	%	bias current is off (RC off)
T_{wu}	wakeup time		3	5	ms	bias current is on (RC ready)
O_{wu}	overshoot at wakeup			50	%	bias current is on (RC ready)
jit	jitter rms		2		$^{o}/_{oo}$	
Tdf	temperature drift		0.1		%/°C	

Table 7.2: RC specifications

7.7 Parallel IO ports

- 8 bit input port A with interrupt, reset and event generation.
- 8 bit input-output-analog port B with analog switching capabilities.
- 8 bit input-output port C.

sym	description	condition	min	typ	max	unit	Comments
	Port A: low threshold limit	Vbat = 2.4 V		1		V	0.4 Vbat
	Port A: high threshold limit			1.5		V	0.6 Vbat
	output drop when sinking 1 mA					V	
	output drop when sinking 8 mA				0.4	V	
	output drop when sourcing 1 mA					V	
	output drop when sourcing 8 mA				0.4	V	
	Port A: low threshold limit	Vbat = 5.0 V		2		V	0.4 Vbat
	Port A: high threshold limit			3		V	0.6 Vbat
	output drop when sinking 1 mA					V	
	output drop when sinking 8 mA				0.4	V	
	output drop when sourcing 1 mA					V	
	output drop when sourcing 8 mA				0.4	V	
	pull-up, pull-down resistor		50		150	kohm	

Table 7.3: IO pins performances

7.8 Voltage level detector

- Can be switched off, on or simultaneously with CPU activities
- Generates an interrupt if power supply is below a pre-determined level

The Voltage Level Detector monitors the state of the system battery. It returns a logical high value (an interrupt) in the status register if the supplied voltage drops below the user defined level.

symbol	description	min	typ	max	unit	comments	
Vth	Threshold voltage	Note 1			V	trimming values:	
						VldRange	VldTune
			3.06			1	000
			2.88			1	001
			2.72			1	010
			2.57			1	011
			2.44			1	100
			2.33			1	101
			2.22			1	110
			2.13			1	111
T_{EOM}	duration of measurement		2.0	2.5	ms	Note 2	
T_{PW}	Minimum pulse width detected		875	1350	us	Note 2	

Table 7.4: Voltage level detector operation

Note: **1)** Absolute precision of the threshold voltage is ±10%.
2) This timing is respected in case the internal RC or crystal oscillators are selected. Refer to the clock block documentation in case the external clock is used.

8 Physical description

8.1 Packages:

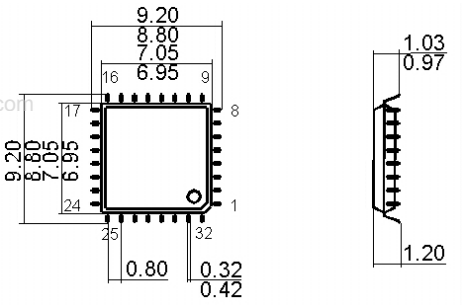

Figure 8.1: TQFP32 package, size in mm.

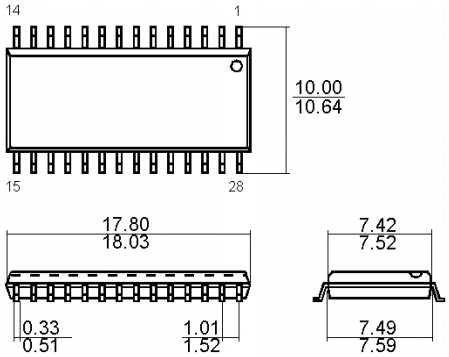

Figure 8.2: SO28 package, size in mm.

8.2 Die:

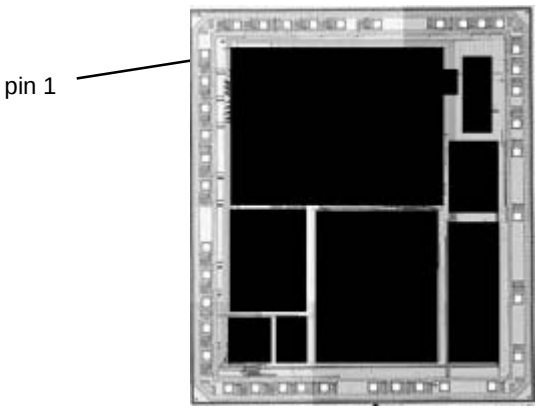

Figure 8.3: Die. Chip size is 4.0 x 3.5 mm2 for 0.3 mm thickness.
Physical chip size and exact pad positioning can change without notification.

8.2.1 Bonding pad location

Coordinates start with a point near to the bottom left border (with respect to above picture). X is horizontal, Y is vertical.

Pad size is 85 x 85 um.

Symbol	Pad	X	Y	Symbol	Pad	X	Y
		um	um			um	um
1	PC(5)	123	3493.9	21	XOut	3015.2	118
2	PC(6)	123	3221.9	22	XIn	3282.0	413.6
3	PC(7)	123	2949.8	23	Vss	3282.0	998.2
4	NC	123	2677.8	24	PA(0)	3282.0	1833.4
5	PB(0)	123	2442.6	25	PA(1)	3282.0	2484.0
6	PB(1)	123	2165.6	26	NC	3282.0	2768.6
7	PB(2)	123	1538.6	27	PA(2)	3282.0	3103.8
8	PB(3)	123	1261.6	28	PA(3)	3282.0	3313.4
9	NC	123	984.6	29	PA(4)	3282.0	3523.0
10	PB(4)	123	729.4	30	PA(5)	3114.6	3785.0
11	PB(5)	123	452.4	31	PA(6)	2930.0	3785.0
12	PB(6)	340.4	118	32	NC	2745.4	3785.0
13	PB(7)	617.4	118	33	PA(7)	2510.2	3785.0
14	RESET	894.4	118	34	PC(0)	1870.8	3785.0
15	NC	1079.0	118	35	PC(1)	1498.8	3785.0
16	VSS	1314.2	118	36	PC(2)	1226.7	3785.0
17	Vbat	1809.9	118	37	NC	954.7	3785.0
18	NC	2045.1	118	38	PC(3)	719.5	3785.0
19	Vreg	2280.3	118	39	PC(4)	447.4	3785.0
20	VPP	2532.9	118				

Table 8.1: Bonding pads location. Do not connect pads named NC. Pads 16, 23 and substrate must be connected to Vss.

9 Contacting XEMICS

You will find more information about the XE88LC03 and other XEMICS products, as well as the addresses of our representatives and distributors for your region on http://www.xemics.com.