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DSKTJ05

Silicon N-channel junction FET

For AF impedance converter

Marking Symbol : 9S, 9T

Package Code : TSSSMini3-F2-B

Absolute Maximum Ratings Ta = 25 °C

Parameter	Symbol	Rating	Unit
Drain-source voltage(Gate open)	VDSO	20	V
Drain-gate voltage(Source open)	VDGO	20	V
Drain-source current(Gate open)	IDSO	2	mA
Drain-gate current(Source open)	IDGO	2	mA
power dissipation	PD	100	mW
Operating ambient temperature	Topr	-20 to +80	°C
Storage temperature	Tstg	-55 to +150	°C

Pin name	1.	Drain
	2.	Source
	3.	Gate

Electrical Characteristics Ta = 25 °C±3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain current *1, *4	ID	VDD = 2.0 V, Rd = 2.2 kΩ ± 1%	100		320	µA
Drain-source current *4	IDSS	VDD = 2.0 V, Rd = 2.2 kΩ ± 1%, VGS = 0	110		310	µA
Mutual conductance	gm	VDS = 2.0 V, VGS = 0, f = 1 kHz	660	1 500		µS
Noise voltage *2	NV	VDD = 2.0 V, Rd = 2.2 kΩ ± 1% Co = 5 pF, A-curve			8	µV
Voltage gain	GV1	VDD = 2.0 V, Rd = 2.2 kΩ ± 1% Co = 5 pF, eG = 10 mV, f = 1 kHz	-5.0	-1.0		dB
	GV2	VDD = 1.5 V, Rd = 2.2 kΩ ± 1% Co = 5 pF, eG = 10 mV, f = 1 kHz	-7.0	-1.5		
Voltage gain difference *3	Δ | GV·f |	VDD = 2.0 V, Rd = 2.2 kΩ ± 1% Co = 5 pF, eG = 10 mV f = 1 kHz to 70 Hz		0	1.7	
Voltage gain difference	| GV1-GV2 |		0		2.0	

Note: 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. A protection diode is built-in between gate and source of transistor. However if forward current flows between gate and source transistor might be damaged. So please be careful not insert reverse.

3. *1 ID is assured for IDSS.
   *2 NV is assured for design.
   *3 Δ | GV . f | is assured for AQL 0.065. (The measurement method is used by source-grounded circuit
   *4 Rank classification

Code	S	T
Rank	S	T
ID	100 to 220	180 to 320
IDSS	110 to 210	190 to 310
Marking symbo	9S	9T

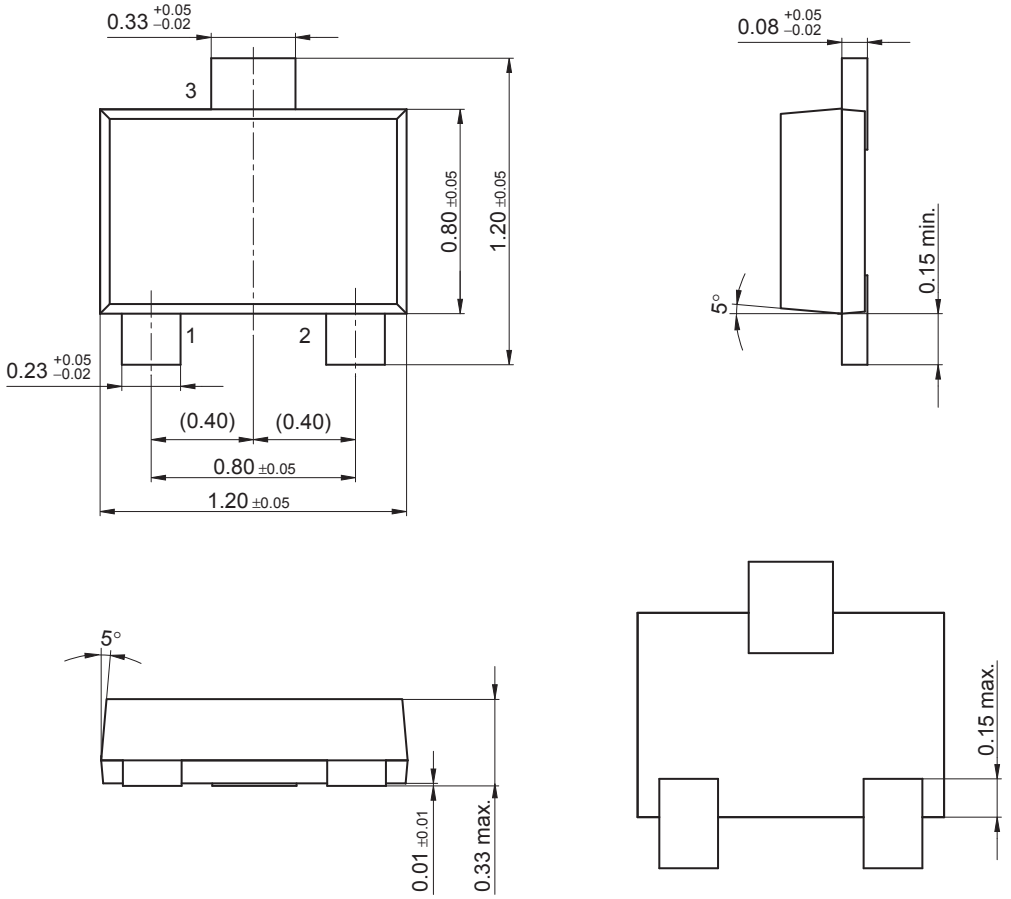
Packing

Embossed type (Thermo-compression sealing) : 10 000 pcs / reel

2010.05.31	2010.8.31	
Prepared	Revised	

TSSSMini3-F2-B

Unit: mm



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