

# DATA SHEET

## **BST70A** N-channel vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# N-channel vertical D-MOS transistor

# BST70A

### DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

### FEATURES:

- Very low  $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

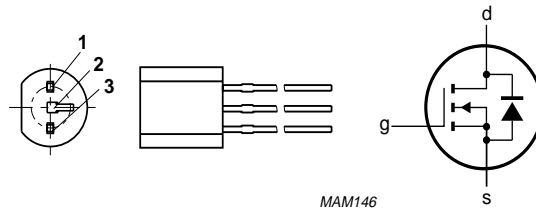
### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	80 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	0.5 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $I_D = 500\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ.	2 $\Omega$
		max.	4 $\Omega$
Transfer admittance $I_D = 500\text{ mA}; V_{DS} = 15\text{ V}$	$ Y_{fs} $	typ.	300 mS

### PINNING - TO-92 VARIANT

- 1 = source
- 2 = gate
- 3 = drain

### PIN CONFIGURATION



**Note:** Various pinout configurations available.

Fig.1 Simplified outline and symbol.

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	80 V
Gate-source voltage (open drain)	$V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	0.5 A
Drain current (peak)	$I_{DM}$	max.	1.0 A
Total power dissipation up to $T_{amb} = 25\text{ °C}$ (note 1)	$P_{tot}$	max.	1 W
Storage temperature range	$T_{stg}$		- 65 to + 150 °C
Junction temperature	$T_j$	max.	150 °C

**THERMAL RESISTANCE**

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125 K/W
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**Note**

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm × 10 mm.

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**CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$

$V_{(BR)DS}$  min. 80 V

Drain-source leakage current

$V_{DS} = 60\text{ V}; V_{GS} = 0$

$I_{DSS}$  max. 1  $\mu\text{A}$

Gate-source leakage current

$V_{GS} = 20\text{ V}; V_{DS} = 0$

$I_{GSS}$  max. 100 nA

Gate threshold voltage

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

$V_{GS(th)}$  min. 1.5 V  
max. 3.5 V

Drain-source ON-resistance (see Fig.4)

$I_D = 500\text{ mA}; V_{GS} = 10\text{ V}$

$R_{DS(on)}$  typ. 2.0  $\Omega$   
max. 4.0  $\Omega$

Transfer admittance

$I_D = 500\text{ mA}; V_{DS} = 15\text{ V}$

$|Y_{fs}|$  typ. 300 mS

Input capacitance at  $f = 1\text{ MHz}$ 

$V_{DS} = 10\text{ V}; V_{GS} = 0$

$C_{iss}$  typ. 45 pF  
max. 60 pF

Output capacitance at  $f = 1\text{ MHz}$ 

$V_{DS} = 10\text{ V}; V_{GS} = 0$

$C_{oss}$  typ. 30 pF  
max. 45 pF

Feedback capacitance at  $f = 1\text{ MHz}$ 

$V_{DS} = 10\text{ V}; V_{GS} = 0$

$C_{rss}$  typ. 8 pF  
max. 12 pF

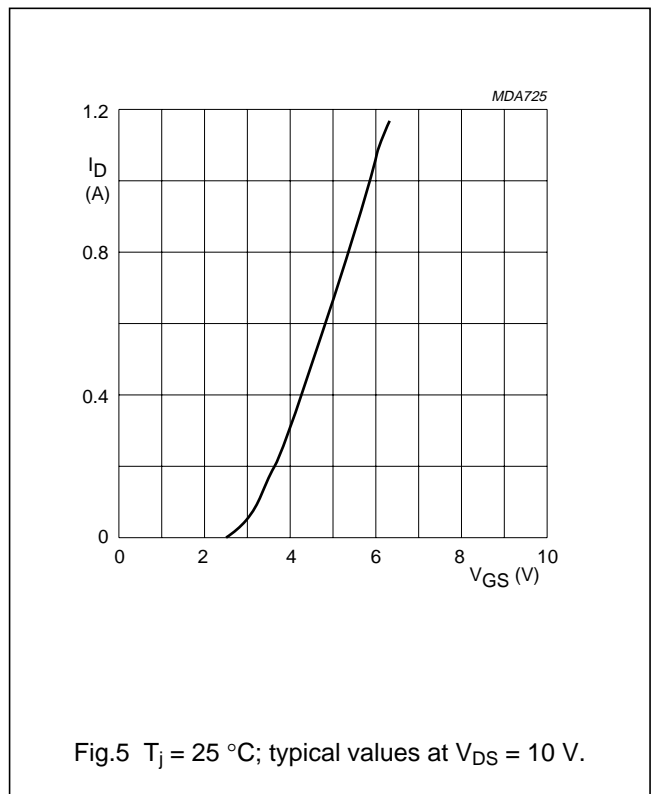
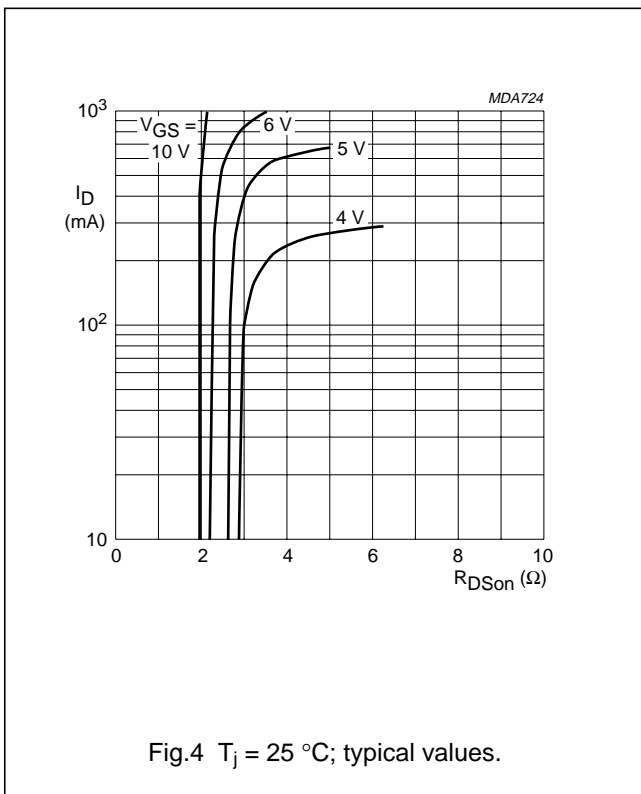
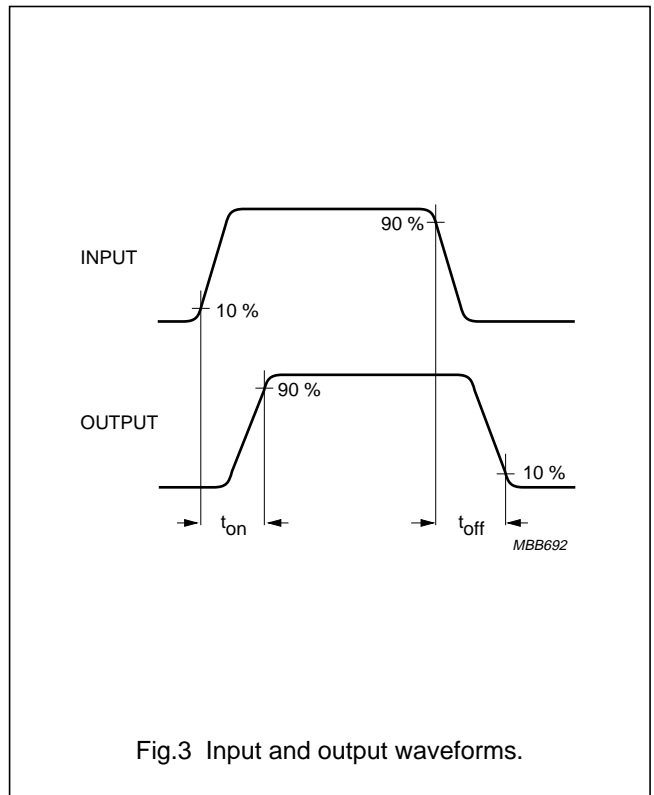
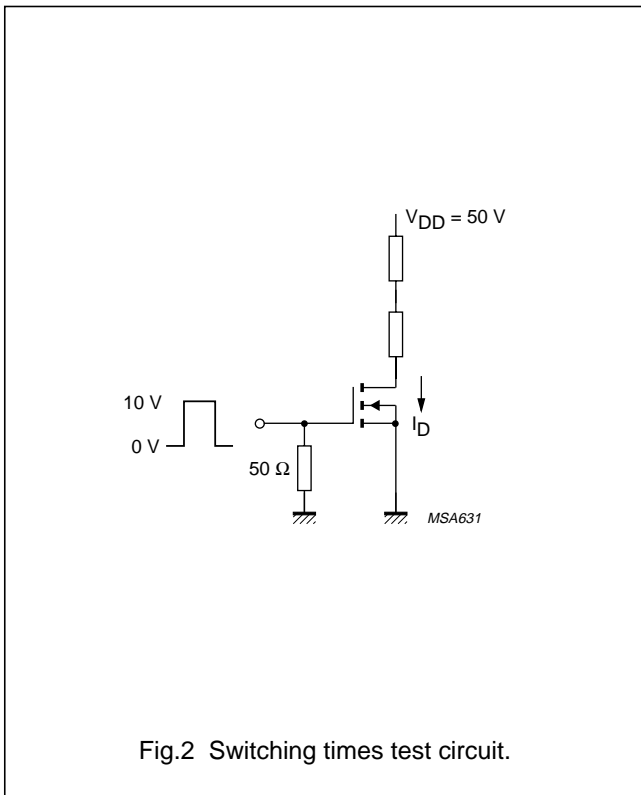
Switching times (see Figs 2 and 3)

$I_D = 500\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$

$t_{on}$  max. 10 ns  
 $t_{off}$  max. 15 ns

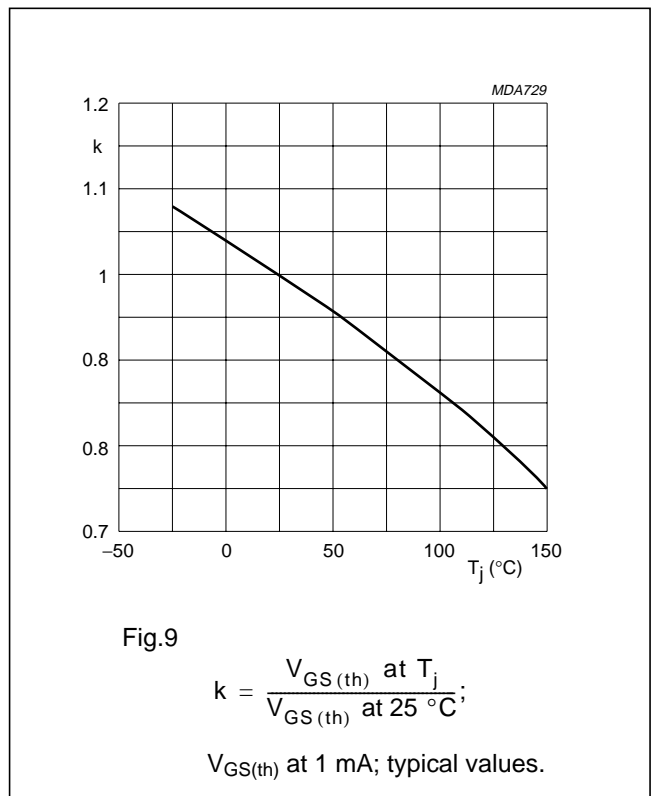
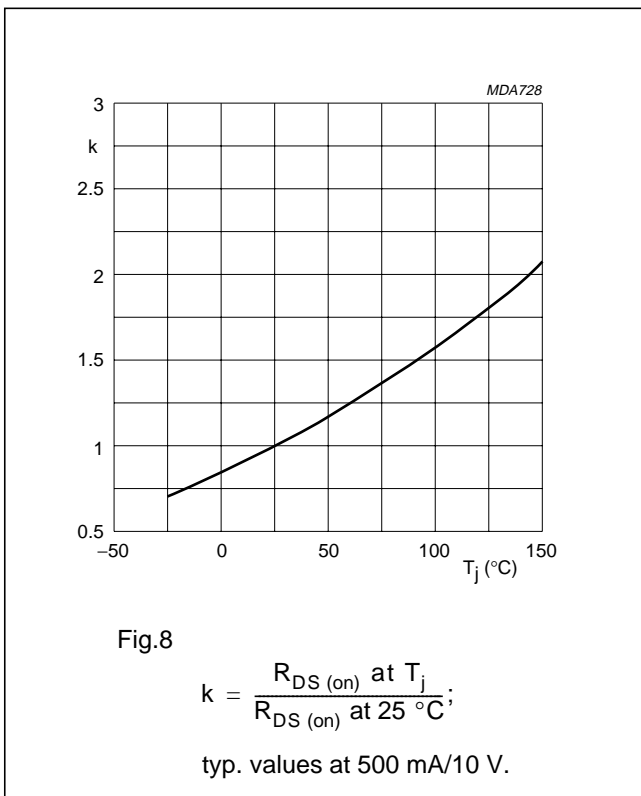
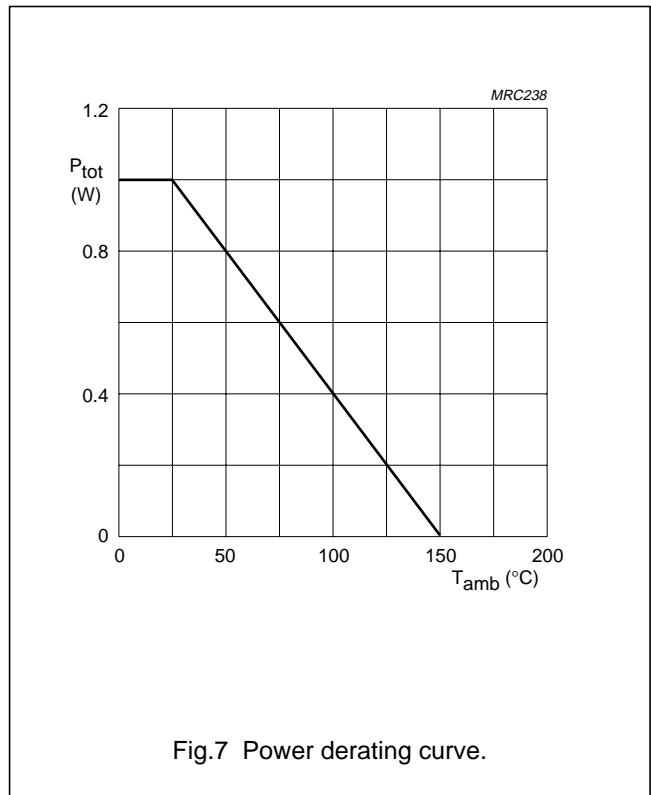
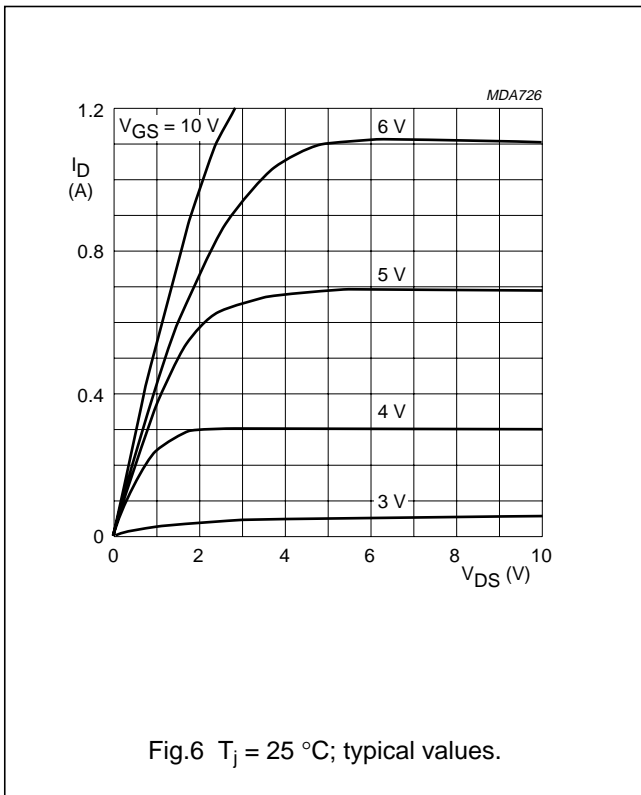
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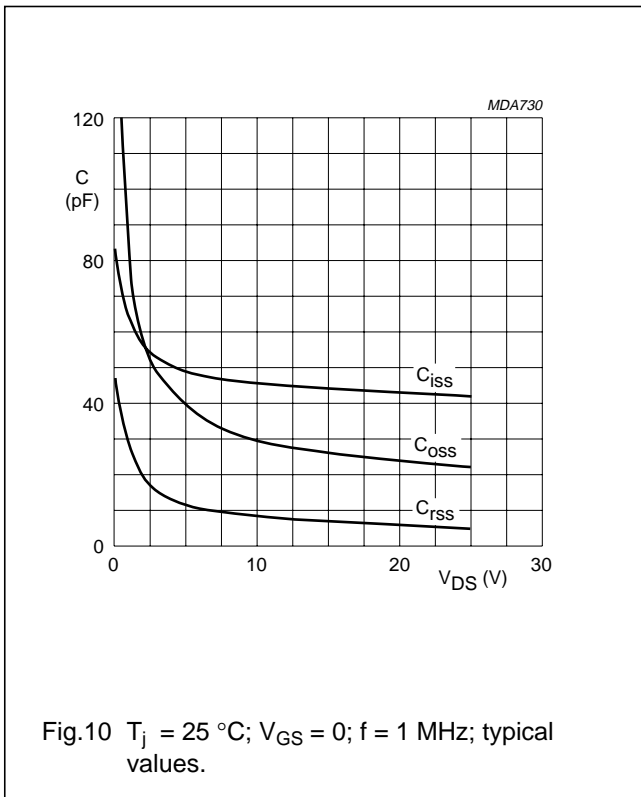
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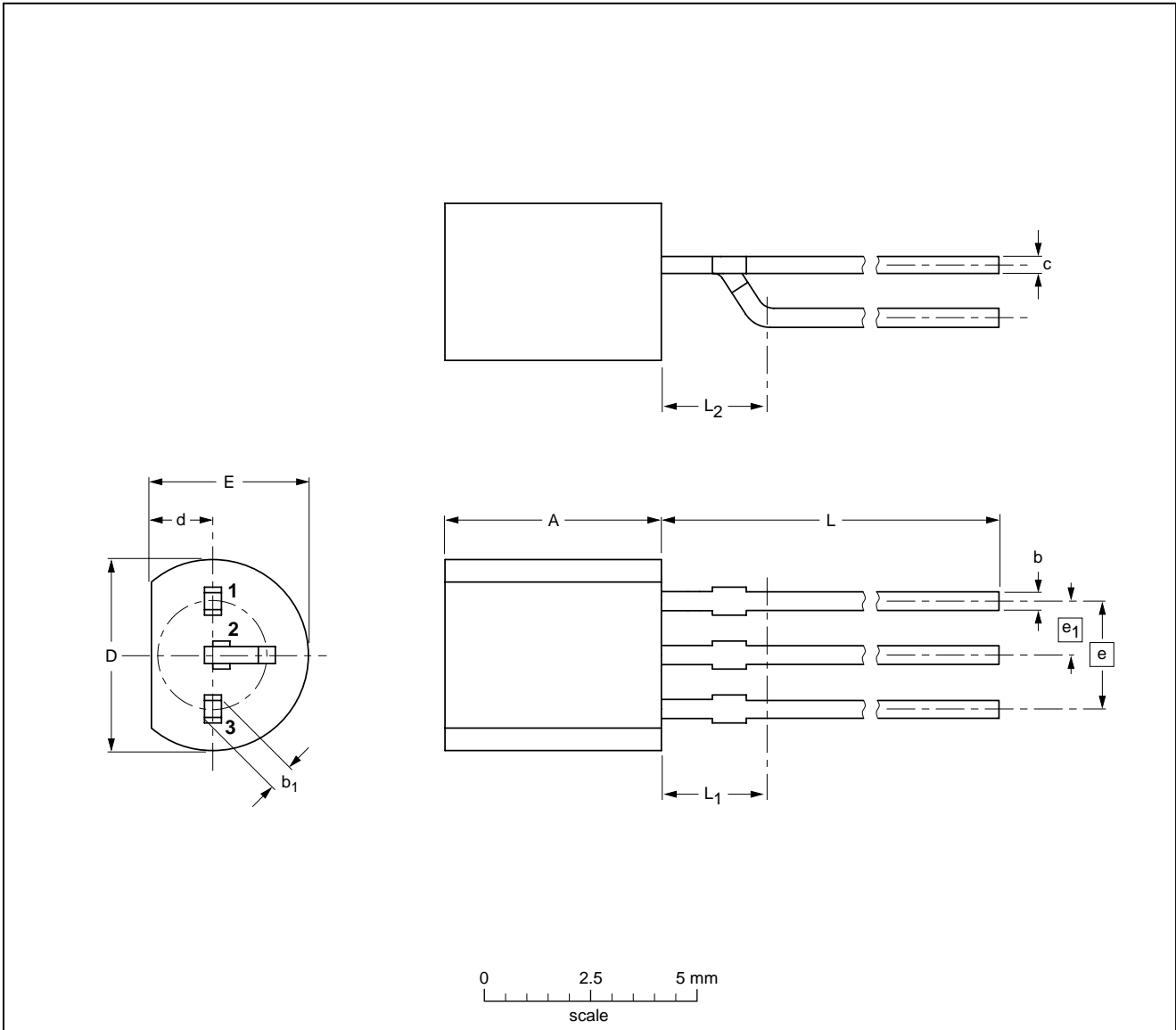
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PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max	L <sub>2</sub> max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54 variant		TO-92	SC-43		97-04-14



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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 689 211, Fax. +359 2 689 102

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Tel. +1 800 234 7381

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
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**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 0044

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580920

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

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**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 1231,  
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**Slovakia:** see Austria

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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 3 301 6312, Fax. +34 3 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
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Tel. +41 1 488 2686, Fax. +41 1 481 7730

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
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**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 625 344, Fax. +381 11 635 777

**For all other countries apply to:** Philips Semiconductors, Marketing & Sales Communications,  
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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