To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

SPECIFICATION OF INTEGRATED CIRCUIT

1. TYPE NO. M65761FP

2. FUNCTION

2.1 CIRCUIT FUNCTION QM-Coder

2.2 BLOCK DIAGRAM see the third page

3. APPLICATION FAX, PPC etc

4. OUTLINE

4.1 PACKAGE 100 Pin Plastic Molded Quad Flat Package (Fine Pitch) [100P6S-A]

4.2 OUTLINE DRAWING G465181

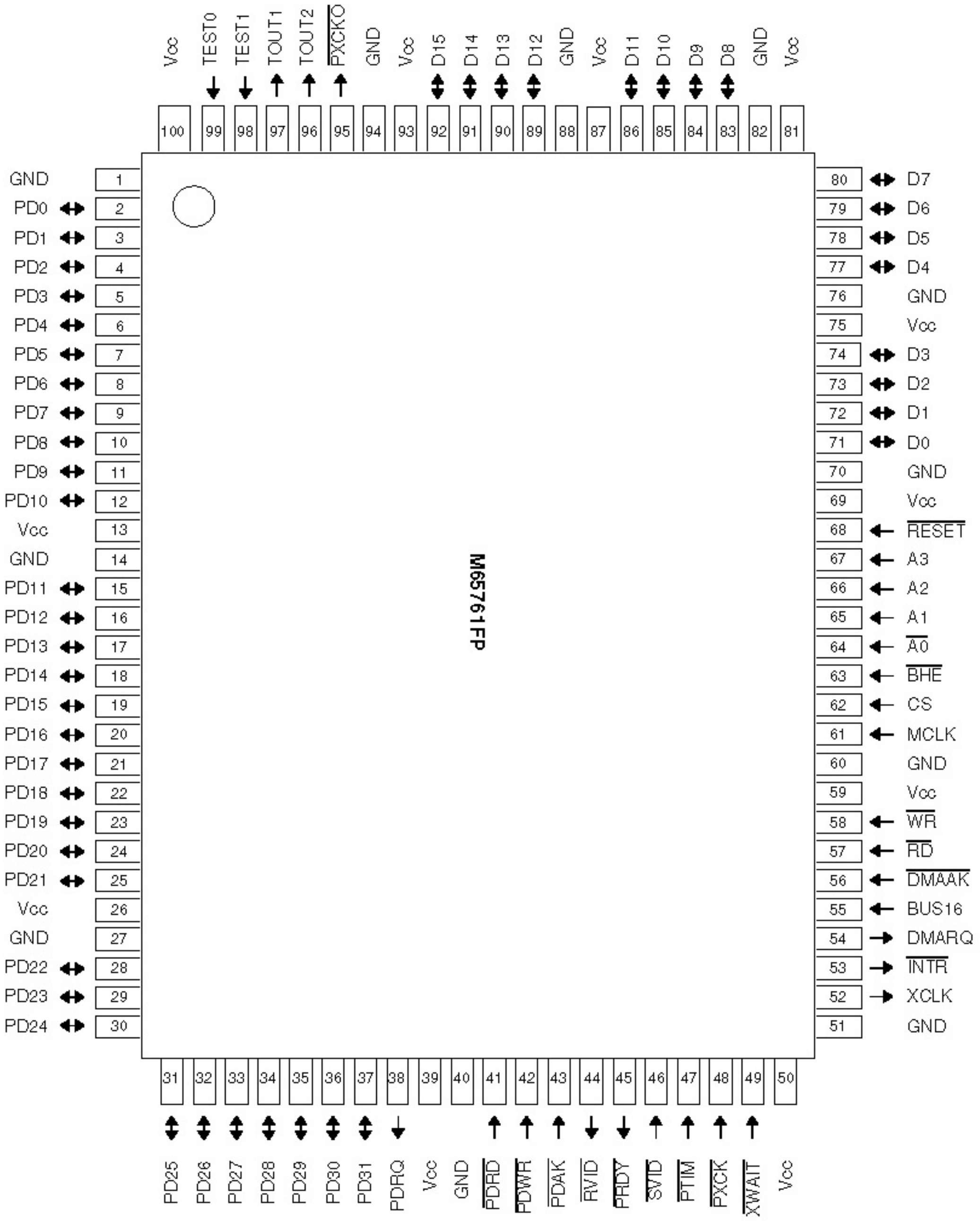
5. CIRCUIT DIAGRAM

DRAWING

6. PIN DIAGRAM see the next page (2page)

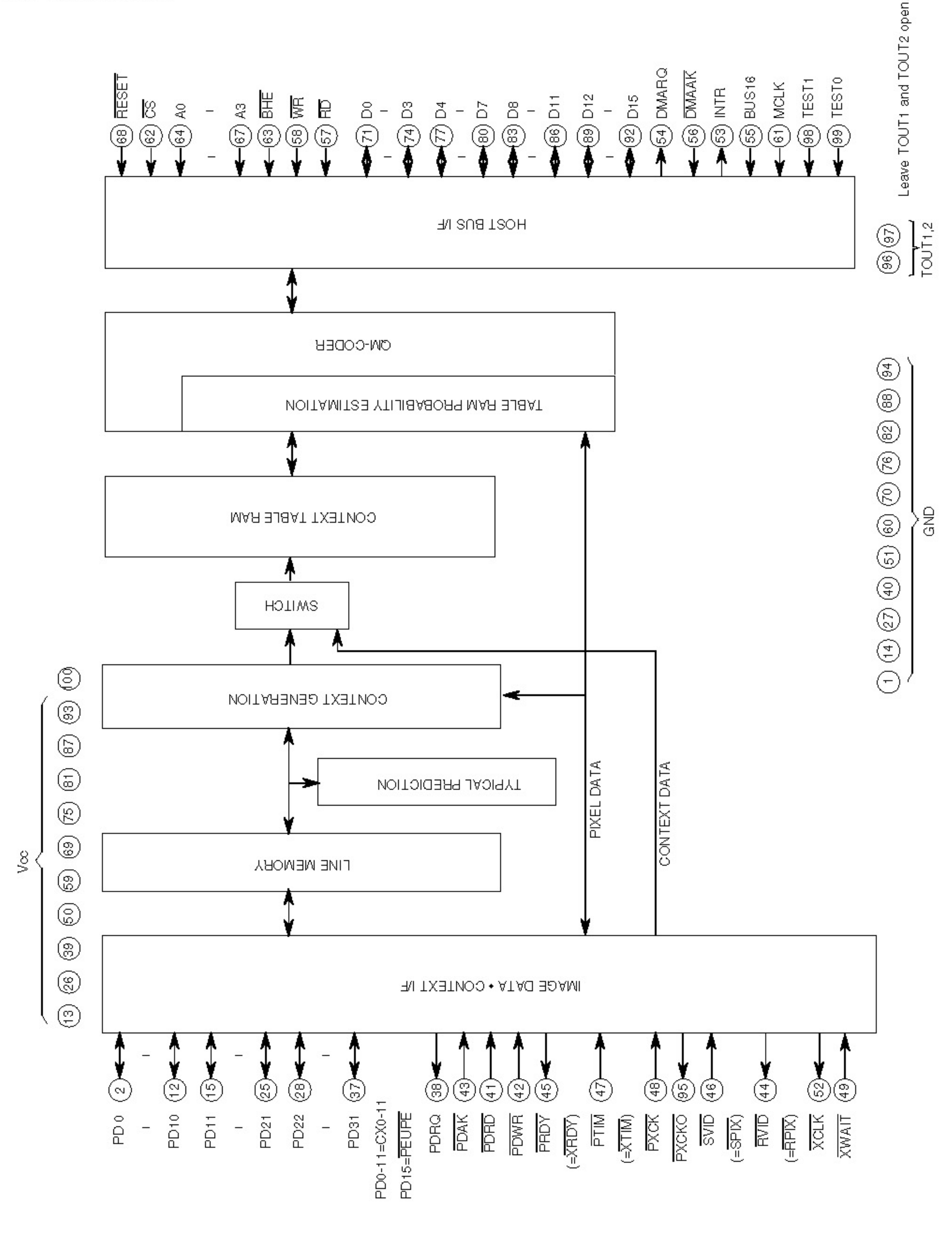
7. OTHER SPECIFICATIONS see cover page of specification

PIN CONFIGURATION (TOP VIEW)



Outline 100P6S-A

BLOCK DIAGRAM



9. CODING SPECIFICATION

(1) Coding Algorithm

- QM-Coder
  (JBIG Standard Arithmetic Coding System)

(2) Context

(i) Built-in Context Mode

a) Template Model

- 2 or 3 line 10 pixel template (See Fig9. 1)
  (This agrees with the template used with the minimum resolution of JBIG)

NOTE:The coding efficiency of the 3-line template is better than that of the 2-line template by several %.

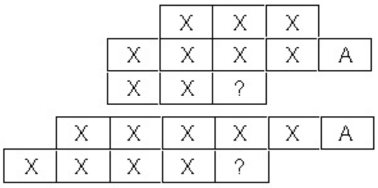


Fig. 9. 1 Template (X, A)
(Top : 3line, Bottom : 2line)

b) Adaptive Template (AT)

- It is possible to move up to 127pixcels on the coding line.
  (The position of ATgiven instruction by the MPU)

Note:It is possible to improve the coding effeciency against the dither image by the use of AT.

- It is posible to change the position of AT line by line in the middle of coding and decoding.

Note:It is not possible to change the template at the time when change the position of the AT pixels.

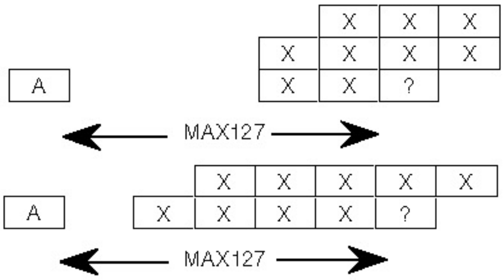


Fig. 9. 2 Adaptive template (A)

(ii) Extenal Context Mode

- It is possible to input any context up to 12 bits.
  (It is possible to interface with JBIG Progressive Coding and the Arithmatic Coding of JPEG Option Function)

(3) Typical Prediction

- Agreement with the Typical Prediction of the lowest resolution of JBIG.
  The pseudo-pixcel (SLNTP) is geneated by the symbol LNTPwhich shows whether the coding/decoding process agree with the directly before line.If they agree, the line is not coding/decoding .
  This makes it possible to shorten the time of process and rejection of the code data.
  SLNTPy =! (LNTPy $\oplus$ LNTPy-1) (y:line number, LNTPy=1; LNTPy-1=1)

(4) Deterministic Prediction

- This LSI is not equipped with the Typical Prediction.However,the DP function is realized when the DP pixels are identified and eliminated by the extenal circuits during the external context mode.

(5) Coding Data Format

- The Stripe Data Entity (SDE)
  (=Stripe coded data with byte stuffing (PSCD) + end marker (SDNORM/ SDRST)) Coding/decoding of one stripe portion os perfformed.In case of the multi-striped (construct the multi stripes) stripes are activated one at a time.

(6) Marker Code

- The SDE end marker is supported.(SDNORM=02h, SDRST=03h, ABORT=04h)
  (During coding the marker code previously set in the register is outputted.During decoding ,the marker code detected by requesting an interrupt to MPU when the marker is detected is read out od register.)

(7) Rough Estimate of Coding and Decoding Time(T1:M65761FP as a whole,T2;Processing Time of the arithmetic coding section alone)

- The total number of clocks needed for coding and decoding 1 page (stripe)is calculates roughly using the following equations.

T1≒ (p Lp) + (9/8 C) + (Lp)
- S ((1 -) p Ltp - Lp) [clock]
T2≒ (p Lp) + (9/8 C)
- S ((p Ltp) - Lp)) [clock]

p : Number of pixcels/line : about 0.3
Lp : Number of lines/page
Ltp : Number of TP line /page
C : Number of coded data bits/page
S= 1: TP exists 0: No TP : about 10

10. FUNCTIONAL DESCRIPTION OF PINS

Classification		Pin name	I/O	BUF	Function
Host Bus I/F		$\overline{\text{RESET}}$	I	S	H/W reset signal
		$\overline{\text{CS}}$	I		Chip select signal
		A0-3	I		Internal register address select signal
		$\overline{\text{BHE}}$	I		High-order(D8-15)access signal
		$\overline{\text{WR}}$	I	S	Write strobe signal
		$\overline{\text{RD}}$	I	S	Read strobe signal
		D0-15	IO	8	I/O data signal (D0-7 used on 8-bit bus)
		DMARQ	O	2	Code data DMA request signal
		$\overline{\text{DMAAK}}$	I	US	Code data DMA acknowledge signal
		INTR	O	2	Interrupt request signal
		BUS16	I	U	8-bit bus (D0-7)and 16-bit bus(D0-15)function select bus.
Image data I/F	Parallel	PD0-31	IO	U2	Parallel image I/O bus (PD0-15 used on 16-bit bus)
		PDRQ	O	2	Image data DMA request signal
		$\overline{\text{PDAK}}$	I	US	Image data DMA acknowledge signal
		$\overline{\text{PDRD}}$	I	US	Image data read strobe signal
		$\overline{\text{PDWR}}$	I	US	Image data write strobe signal
	Serial	$\overline{\text{PRDY}}$	O	2	Image data 1-line I/O start ready signal
		$\overline{\text{PTIM}}$	I	US	Image data 1-line transfer section signal
		$\overline{\text{PXCK}}$	I	US	Image data transfer clock signal
		$\overline{\text{PXCKO}}$	O	4	Image data transfer sync clock signal
		$\overline{\text{SVID}}$	I	U	Image data input signal
		$\overline{\text{RVID}}$	O	2	Image data output signal
Context I/F		CX0-11	I	U	Context input (CX0 can be fed back inside LSI) (=PD0-11)
		$\overline{\text{PEUPE}}$	I	U	PE RAM update enable (learning function ON/OFF) (=PD15)
		$\overline{\text{SPIX}}$	I	U	Coded image data input signal (=SVID)
		$\overline{\text{RPIX}}$	O	2	Decoded image data output signal (=RVID)
		$\overline{\text{XCLK}}$	O	4	Context data transfer clock signal
		$\overline{\text{XWAIT}}$	I	US	Context data transfer wait signal
		$\overline{\text{XRDY}}$	O	2	Context data 1-stripe I/O start ready signal (=PRDY)
		$\overline{\text{XTIM}}$	I	US	Context data 1-stripe transfer section signal (=PTIM)
Others		MCLK	I		Master clock input signal
		TEST0-1	I	DS	Test signal (should be connected to GND when normally used).
		Vcc/GND	–	–	Power supply (+5V)/ground

Notes:Most of the context I/F signals are used in conjunction with the image data I/F signals.
The input buffers of the input terminals (I and IO) are at TTL level.
Options are as follows.

(U:with pull-up resistors,D:with pull-down resistors,S:Schmitt trigger)
Numbers (2,4,8) of the BUF column of the output terminals (O and IO) indicate current value. (one of 2,4,or 8mA)

11. REGISTER CONFIGURATION

11. 1 List of registers

Address	Register Name	R/W	Description
0	System setting	R/W	• LSI H/W reset • Coding/decoding/image data through mode selection • Context selection(internal context/external context) • Byte swap ON/OFF of coded/image data on host bus • Bit swap ON/OFF of coded/image data on host bus • Image data I/O I/F(parallel I/F,serial I/F) • Image data bus bit width selection(32bits/16bits)
1	Parameter setting	R/W	• Template selection (2-line/3-line template) • Setting of AT pixel position (up to 127)(IF O is set,AT becomes non-existent (default position)) • Latch input/through input selection in external context input mode
2	Command	W	• Context table RAM initialization command • Coding (decoding,through) start/end command • Start/stop command for R/W of context table RAM • Selection of temporary stop and terminating end
2	Status	R	• Processing status (in process/end of processing) • Coded data read/write ready (ready/busy) • Marker code detection (SDNORM,SDRST,ABORT,others) • Interrupt request status • SC counter over flow • Processing mode (stop temporary/terminating end)
3	Interrupt enable setting	R/W	• Interrupt enable setting correspondence to each of bits positions of status register
4,5	Pixel count setting	R/W	• Setting the number of pixels on one line (in multiples of 16or32,up to 10240 pixels)
6,7	Line count setting	R/W	• Setting the number of lines to be coded/decoded(up to 65535 lines)
8,9	Processed line count	R	• Setting the number of coded/decoded lines (up to 65535 lines)
A,B	Data write buffer	W	• Buffer for writing coded data/image data/context table RAM data from MPU into LSI (DMA transferable)(RAM address is automatically incremented each time data is written.)
A,B	Data read buffer	R	• Buffer for reading coded data/image data/context table RAM data from LSI into MPU (DMA transferable)(RAM address is automatically incremented each time data is read).
C	Marker code setting	W	• Setting a terminal marker code in coding (SDNORM/SDRST)
C	Marker code read	R	• Reading a marker code in decoding (SDNORM,SDRST,ABORT,others)
D	Scaling	R/W	• Reduction in coding (1/2 reduction in horizontal and vertical directions, horizontal OR processing) • Magnification during decoding (2 lengthwise and width) • Select throwing away the leading 1byte of the coded data read when decoding • Selecting the typical prediction • Selection of prohibiting line memory initialization

Notes:When the 8bit bus is used for the data read/write buffer,use Address A only.
Incase of the 16-bit buffer,only the word access is possible.
(The byte access is not possible).

11. 2 Description of Registers

(1) System Set Up Register (W/R) (address : 0)

SYS_REG :

d7(MSB)						d0
PB	PI	BX	BS	CX	MOD	HR

d0(HR) : H/W reset (0:Active, 1:Reset state)

To make a H/W reset ,set this bit to 1 then to 0.

Reset initializes the entire LSI including the group of register and Line Memory. However, the context table RAM is not initialized.

d1-2(MOD) :This sets up the operating modes.

(d2=0,d1=0:coding, d2=1,d1=0:iage data through (lage data I/F Host I/F),

d2=0,d1=1:decoding, d2=1,d1=1:lage data through (Host I/F lage data I/F))

d3(CX) :Context select (0:internal context, 1:Image data through)

NOTE:The internal context should be selected when the image data through mode is used.

When initializing or processing R/W of the Context table RAM and coding /decoding,

This bit must be set the same.(Because RAM configration changes depending on internal/external modes.)

d4(BS) :Select data bit swap of the host bus. (0:MSB(d7)first, 1:LSB(d0)first)

d5(BX) :Select data byte swap of the host bus.(0:Lower byte(A)first, 1:Upper byte(B)first)

NOTE:BX is valid only when the host bus is 16 bits.(BUS16=HIGH)

Table 11. 2 The coed data and image data line-up on the Host bus

Bus width BUS16	Swap BX BS	Upper address(B) d15・・・・・・d8	Lower address(A) d7 ・・・・・・d0
1 16bit	0 0 0 1 1 0 1 1	b8 ・・・・・・b15 b15・・・・・・b8 b0 ・・・・・・b7 b7 ・・・・・・b0	b0 ・・・・・・b7 b7 ・・・・・・b0 b8 ・・・・・・b15 b15・・・・・・b8
0 8bit	– 0 – 1	– –	b0 ・・・・・・b7 b7 ・・・・・・b0

b0 is the first coded data on the time series/the left-hand side image data on the screen.
b15 is the last coded data on the time series/the right-hand image data on the screen.

d6(PI) :Selects the image data I/O I/F (0:Serial /F, 1:ParallelI/F)

d7(PB) :Selects the bit width of the iamge data bus (0:32bit bus (PD0-31), 1:16bit bus(PD0-15))

Table 11. 3 The image data line-up on the image data parallel bus

bit width	PD31・・・・・・PD16	PD15 ・・・・・・PD0

PB=0
PB=1
	p0 ・・・・・・p15
	–
		p16 ・・・・・・p31
		p0 ・・・・・・p15

p0 is the image data on the left-hand on the screen.
p31is the image data on the right-hand on the screen.

(2) Parameter Setup Register (W/R) (Address:1)

1) External Context Mode

PARA_REG :

d7		d4	d0
C0	LC	0	0

d6 (LC) :Condition of taking in the input from the external context are selected.

(0:through onput, 1:latch input)

When this bit is set to 1,the CX0 to CX11 of the context input is latched once using the transfer clock.("XCLK")

d7 (C0) : When this bit is set to 1,CX0 is selected.

(0:CX0 external input, 1:CX0 internal feedback)

2) Internal Context Mode

PARA_REG :

d7 d6	d5	d4 d0
AT	TM	AT

d0-4 (AT<0>-AT<4>) :ATpixel position Lower 5bits. (See Fig.9. 2)

d5 (TM) :Template select (0:3line template, 1:2line template)

d6 -7(AT<5>-AT<6>) :AT pixel position upper 2bits (the 6th and 7th bits)

Example : 3line template,AT=4 :

d7			d4				d0
0	0	0	0	0	1	0	0

2line template,AT=48 :

d7			d4				d0
0	1	1	1	0	0	0	0

NOTE) The AT pixel position at time of the internal context mode is set up by using all the AT<6:0> (0 to 127)

When the default position (when the AT pixels are not used) is used, At is set to 0.

When the 2-line templsate is used, AT should not be set to 1 to 4. In case of the 3-line template, AT=1 to 2 is not allowed.

(3) Command Register (W) (address : 2)

	d7	d3			d0
CMD_REG :	0	JP	RC	JC	IC

d0 (IC) :This command starts initialization of Context Table RAM (1:start initialization)

When this bit goes 1,the Context Rable RAM initialization starts.This bit returns to 0 automatically when the initialization is completed.

d1 (JC) :Processing (Coding/Decoding/Through) start /end command (1:start processing, 0:end processing)

When this bit goes 1,processing(coding/decoding/through)starts.

This bit returns to 0 automatically when processing of the number of set lines is finished during the selection of end of termination.

And if this JC bit is made 0 and inputting the image data is stopped during the coding porocess,the coding is stopped (flushed) even if the set lines are not filled.Mreover,if this bit made 0 during decoding and no more coded data is coming in,it is assumed that the '00'of the coded data came in and the preset lines have been processed.However,in case of the multi-striped coding ,processing should not end by making this bit "0" except in case of last stripe.

d2 (RC) :This command starts and stops R/W of Context Table RAM. (1:R/W start, 0:R/W end)

The Context Table RAM is read out or written in by making this bit to "1".

When reading/writing is finished,this bit must have "0" on it.

d3 (JP) :This selectd temporary stop and the end of termination of coding/decoding/through processing.

(1:Temporary stop selected, 0:End of processing selected)

When the process start command d1(JC)is issued by making this JP bit to 1,the processing stops temporarily when the set number of lines have been processed. Then, if the process satart command d1(JC) is issued,processing restarts.(See 11.4(3))

(4) Status Register (R) (address : 2)

	d7	d5					d0
STAT_REG :	0	PS	SC	IS	MS	DS	JS

d0 (JS) :This register indicates the status of processing in initialization,coding,decoding and through.

(0:Processing in progress(being initialized),1:End of processing)

This JS bit goes to "1"when the initialization is completed as RAM initialization command is issued.

(IC=1) This JS bit goes to "1"when all coded data has been read out during coding in case when the process start command of the processing end is issued.(JC=1,JP=0) This JS bit goes to "1" when reading all the image data has been completed during the image data through and decoding. Moreover,this JS bit stays "0" even when the set number of lines have been processed when the command to start processing the process which has been stopped temporarily has been issued (JC=1, JP=1). (However,interrupts are issued during the temporary stops.)

d1 (DS) :This is used for read and write ready of coded data.(In case of the through mode,this is used for the image data.)(1:Ready, 0:Reading no possible)

It is possible to do R/W of data by the way of the data write/read buffer when this bit is 1.

d2 (MS) :This detects the marker code during decoding.(0:not detected, 1:detected)

This bit goes to "1" if any marker is detected during decoding.

d3 (IS) :This indicates the status of the interrupt request.(0:No request, 1:Request exists)

d4(SC) :This shows the SC count over error during coding.(0:Normal, 1:There is a SC counter overflow)

NOTE:The SC counter counts the "FF" data bytes which occur duriing coding.Coding continues even when the SC counter overflows.this means correct coding data will not be outputted.(Coding error)

d5(PS) :processing modes (Stopped temporary /End of trailer)(1:Process temporaryily stopped, 0:End of processing)

This PS bit corresponds to the temporary stop and end of processing of d3 bit (JP) processing of the command register.

(5) Interrupt Enable Register (W/R) (address : 3)

	d7		d3			d0
IENB_REG :	MP	0	SE	ME	DE	JE

d0 (JE) :Temporary stop/End of trailer interrupt of initialization/coding/decoding/through .
(0:interrupt mask, 1:interrupt enable)

d1 (DE) :Coded data(Image data)read out/write in ready interrupt.
(0:interrupt mask, 1:interrupt enable)

d2 (ME) :Marker code detection interrupt during decoding. (0:interrupt mask, 1:interrupt enable)

d3 (SE) :SC count over error interrupt during coding.(0:interrupt mask, 1:interrupt enable))
This bit sets to 1 beforehand, it occurs the interruption when the SC counter is overflow during coding. Processing of coding continues, but the correct coded data is not output.
NOTE:Bits,d0-d3,are for interrupt enable of bits d0-d2 and d4 of the Status Register.
The interrupt request signal(INTR) is asserted when any one of the status bit set in the interrupt enable (D0(JE)generates interrupts even during the temporary stop),the status goes to "0" due to H/W reset or the INTR signal is negated when the interrupt mask causes factors for interrupt to be lost. Moreever, the status register will not be cleared by the generation of interrupts or the R/W of the interrupt enable register.

d7 (MP) :This specified the marker code detection time halt. (0:Continue/restart, 1:temporary halt)
Decoding will stop temporarily when the marker code is detected if this MP bit is preset to "1"during decoding. (it occures interruption when the marker code is detected, if the ME bit preset to "1".)
if decoding is not completed during the temporary halt,it is possible to reset the line number setup register. Next, if this MP bit is set to "0",decoding is restarted(Decoding continues to the line number set.)

(6) Register used to set the number of pixels (W/R)

		d7	d5	d0
(address:4)	PEL_REG_L :	PEL_L		
(address:5)	PEL_REG_H :	0	PEL_H	

d0-7 (PEL_L) :Number of pixels/line is set (Lower byte)

d0-5 (PEL_H):Number of pixels/line is set (Upper byte)

It is possible to set up 8192 pixels maximum when 3-line template is used. It is used to set up 10240 pixels maximum when 2-line template is used. The number of pixels actually coded (or decoded)should be set when reducing(or expanding).When the image bus uses 16bits(or 32bits)in parallel I/F,multiples of 16 (or 32) should be set. In case of serial I/F,multiples of 8 should be used.

(7) Line Number Setting Register (W/R)

		d7	d0
(Address:6)	LSET_REG_L :	LSET_L	
(Address:7)	LSET_REG_H :	LSET_H	

d0-7 (LSET_L):This sets the number of lines to be processed. (Lower bytes)
(1 to 65535, 0 line not used)

d0-7 (LSET_H):This sets the number of lines to be processed. (Upper bytes)

When reducing(magnification)the actual number of lines to be coded (decoded) should be set.The number of lines (relative number of lines)from the process start command to be issued from now the immediately following temporary stop/end of trailer should be set. This register should be set to the value specified before the process star command is issued. Moreover,this register can be rewritten during processing as long as the following conditions are met:

- If the maximum value, (65535), is set before the process start command is issued,it can be reset once during processing.
- If a value other than maximum value (65535) is set before the process start command is issued and if resetting becomes necessary during processing,the maximum value (65535) has to be reset once and desired value should the reset.

(8) Number of Lines to be Processed Specified (R)

		d7 d0
(address:8)	LIN_REG_L :	LINE_L
(address:9)	LIN_REG_H :	LINE_H

d0-7 (LINE_L):The number of lines actually processed is read out (Lower bytes) (0 to 65535)

d0-7 (LINE_H):The number of lines actually processed is read out (Upper bytes)

When the number of lines processed number of lines set,coding/decoding/through stops temporarily/end of processing

NOTE:The number of lines to be processed by this processing is cleared to 0 by the issuance of process start command.

(9) Data write in buffer (W) (See Note1)

		d7 d0
(address:A)	DWR_BUF_L :	DWR_L
(address:B)	DWR_BUF_H :	DWR_H

d0-7 (DWR_L):This writes in the coded data/image data/context table RAM data (Lower bytes)

d0-7 (DWR_H):This writes in the coded data/image data/context table RAM data (Upper bytes)

(10) Data read out buffer (R) (See Note1)

		d7 d0
(address:A)	DRD_BUF_L :	DRD_L
(address:B)	DRD_BUF_H :	DRD_H

d0-7 (DRD_L) :This read out the coded data/image data/context table RAM data. (Lower bytes)

d0-7 (DRD_H) :This read out the coded data/image data/context table RAM data. (Upper bytes)

NOTE1:Address A is used with 8bit bus. In case of the 16 bit bus, only the word access is possible. (Not byte access). If the number of coded data bytes is an odd number during coding, an one byte pad ("00") is attached after the end marker is issued in order to use it as a word boundary.

See Table 11.2 for the bit arrangement used during the coded data/image data. In case of the context table RAM data, only the lower byte becomes valid data regardless of the bus width of the host bus (BUS16).

Table 11. 4 Context data line-up

Host I/F Bus Width	Upper address (B)	Lower address (A)	
	d15 • • • • • • • • d8	d7	d6 • • • • • • d0
8bit	–	mps	s6 • • • • • • s0
16bit	–	mps	s6 • • • • • • s0

mps:Superior symbol MPS (expected value o/1)

s6-0:Status number ST (0 to 112)

(11) Marker code set up register (W) (address:C)

	d7 d0
MSET_REG :	MSET

d0-7 (MSET):The end marker code used during coding is set.(SDNORM=02h, SDRST=03h)

The byte set to this register is outputted as the end marker during coding.

(12) Marker code read out register (R) (address:C)

	d7 d0
MDET_REG :	MDET

d0-7 (MDET):The marker codes detected during decoding are read out.

(SDNORM=02h, SDRST=03h, ABORT=04h etc)

The marker codes detected during decoding read out as is.

(13) This register sets up various functions (W/R)

(address:D)

	d7							d0
CONV_REG :	TP	LI	OB	HO	HR	VR	HE	VE

d0 (VE):Selects expansion in lengthwise direction during decoding. (0:Equal dimension, 1: 2 expansion)

d1 (HE):Selects expansion sideways during decoding. (0:Equal dimension, 1: 2 expansion)

d0 and d1 are possible only during decoding.

d2 (VR):Selects reduction in lengthwise direction during coding. (0:Equal dimension, 1:1/2 reduction)

d3 (HR):Selects sideways reduction during coding. (0:Equal dimension, 1:1/2 reduction)

d2 and d3 are possible only during coding.

d4 (HO):Selects thinning in sideways direction during coding. (0:simple thinning, 1:OR processing)

This reduction is valid only during coding.

Note 1:This lengthwise 1/2 reduction during coding is used for the simple thinning. (Odd lines are skipped)

Note 2: The number of lines for image data to be inputs when VR=1 for coding must be twice the value set by the register which sets the number of lines.

Note 3:The number of lines for image data to be outputs when VE=1 for decoding must be twice the value set by the register which sets the number of lines.

d5(OB):This selects if the leading 1 byte is discarded during decoding. (0:Normal processing (No discarding), 1:The leading 1 byte is discarded)

If a command to start processing the first the stripe decoding is issued during decoding while OB is set to "1", the leading 1 byte of the input data is discarded. (Not used for decoding) If OB=0,the one of byte discarding process is not used. (Normal decoding used) For example, this function is used by the Host 16 bits bus when the leading 1 byte of the input data word is an invalid data.

Note :Selecting this function is valid in case of the Host 8 bits bus and the external context mode also.

d6 (LI):Line memory initialization is prohibited. (0:Initialization specified, 1:Initialization prohibited)

When a command to start processing coding/decoding of the first stripe is issued, if L1=1, the initialization of the internal line memory is prohibited. (The last image data of the immediately prior coding/decoding left in the line memory is used as the leading reference line data o the next coding/ decoding.) When LI=0, the internal line memory is initialized. (All white (0) data is used as the leading reference line data of the next coding /decoding.)In case when the previous stripe ended with SDNORM during coding/decoding of multi-stripe by setting this bit in the initialization prohibit (1).

Note :Even when LI=1is set, this LI bit is cleared (0) and the internal line memory will be initialized the same line due to the fact that the H/W reset is written into the external reset terminal or the system set up register.

d7 (TP):This selects the Typical prediction when coding and decoding. (0:Typical prediction off, 1:Typical prediction ON)

11. 3 Initialization of register

Each register is initialized as shown in the table below by writing H/W reset to the external RESET terminals or the system set up registers.

Table 11. 5 Initialization values for registers

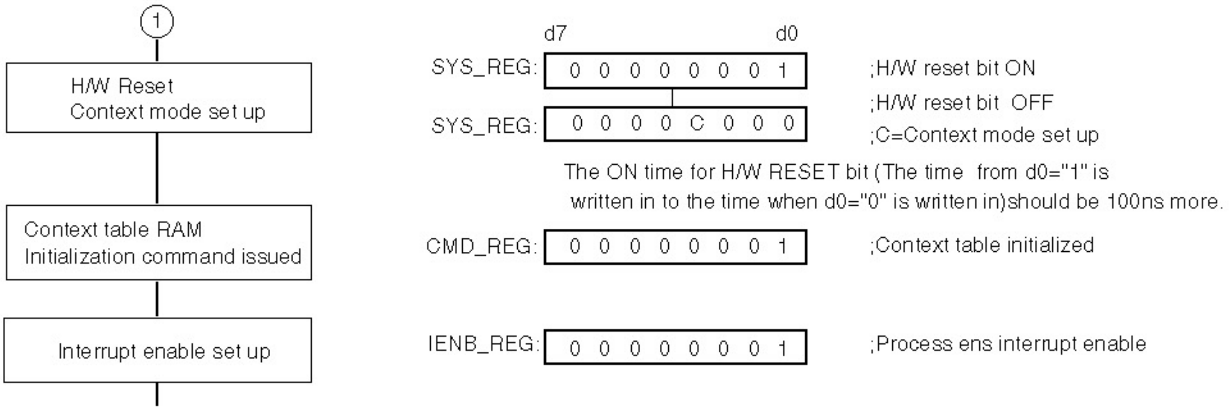
Registers	Initialization values
System set up	00h Notes
Parameter set up	00h
Command	00h
Status	00h
Interrupt enable	00h
Number of pixels set up	00h
Set up number of lines	00h
Number of lines processed	00h
Data buffer	Inderfinite
Marker code set up	00h
Marker code read out	00h
Various functions set up	00h

Note:When writing H/W RESET into the System Setup Register,the value written into is set up in the System Setup Register.

11. 4 Sequence of setting up registers

(1) Initialization sequence of the internal line memory and context table RAM

This sequence starts with the initialization set up (See Note) of internal line memory by the H/W RESET. It is followed by the initialization of the Context table RAM. (Clear)



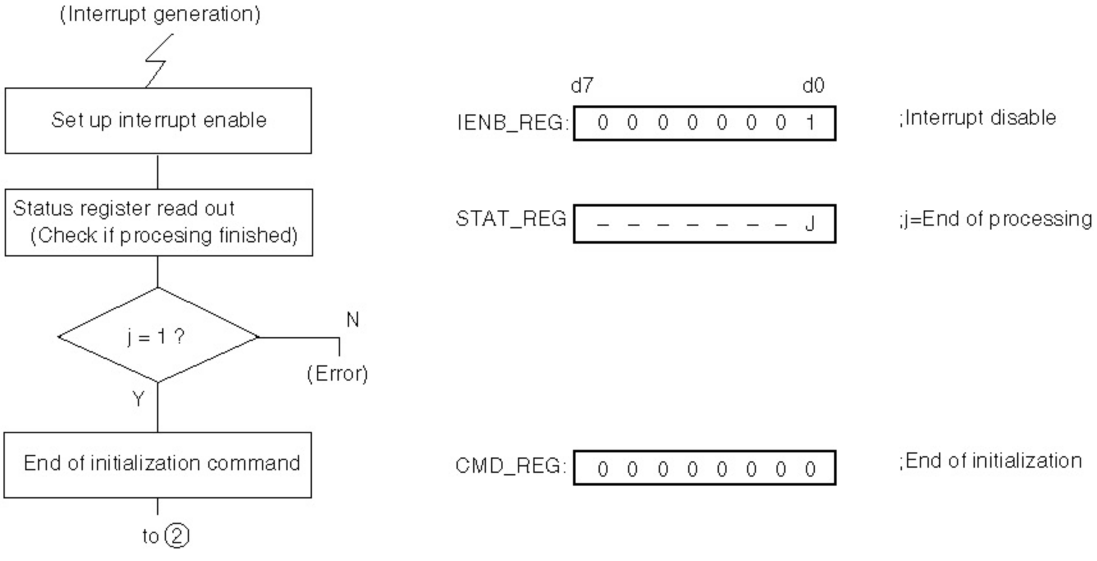
The ON time for H/W RESET bit (The time from d0="1" is written in to the time when d0="0" is written in)should be 100ns more.

[During this time,the context table RAM is initialized.]

The number of clocks needed for initialization is as follows,

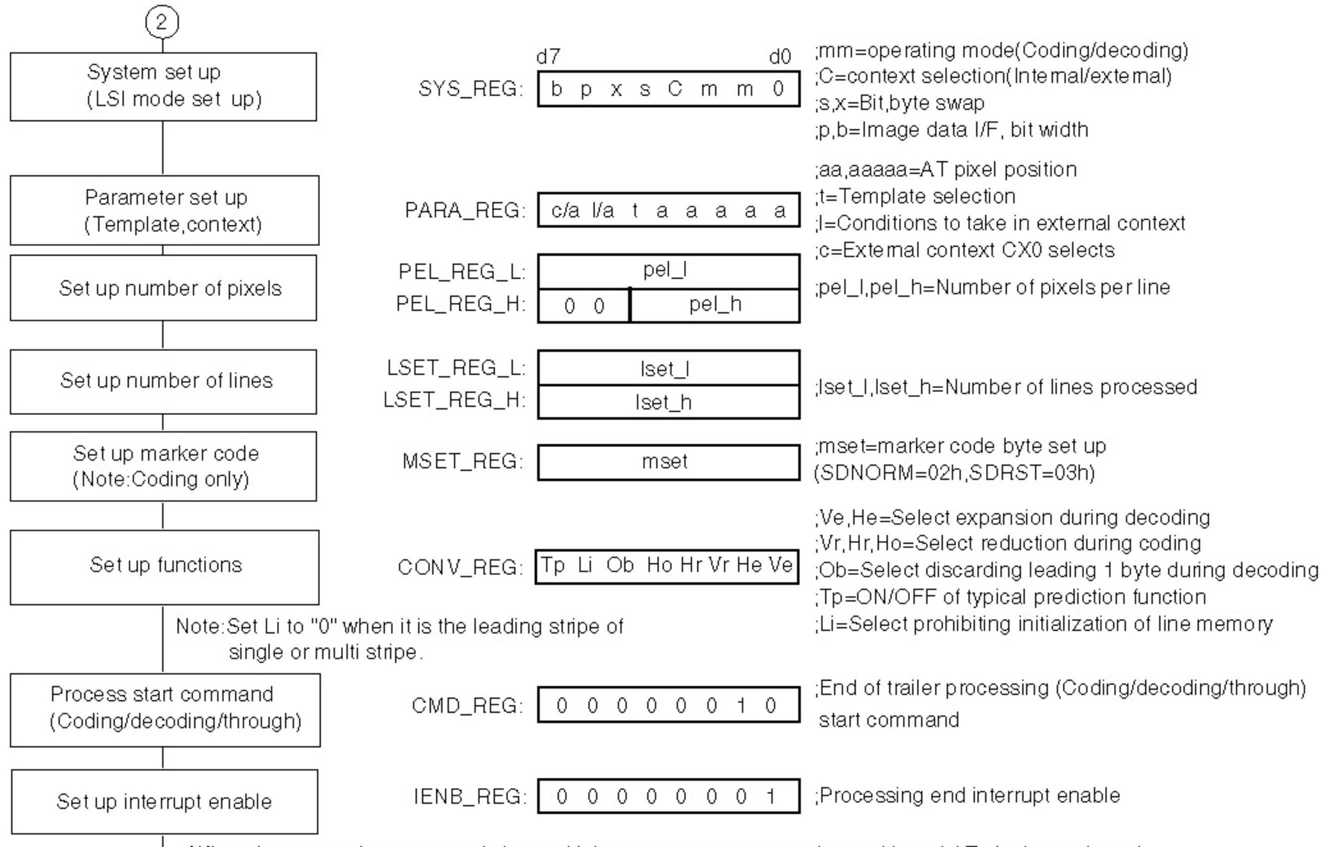
When the internal text mode is used, 1024 + [clocks]

When the external text mode is used, 4096 + [clocks]



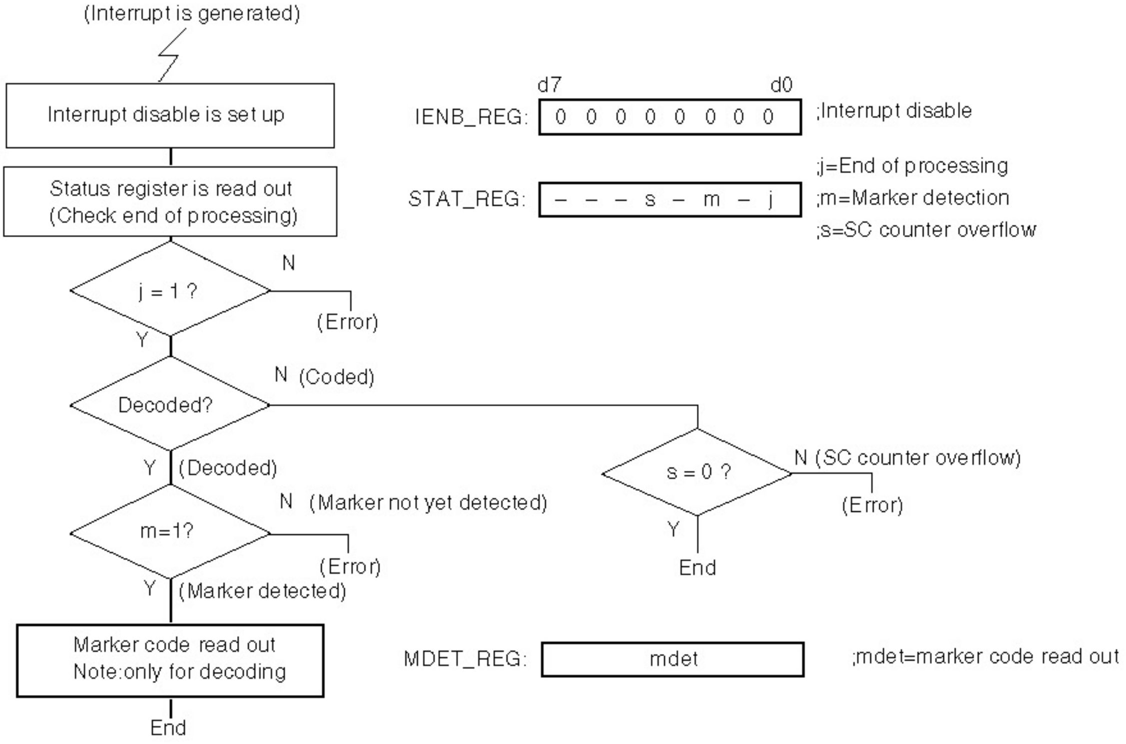
Note: Initialization of the line memory by H/W RESET is provided for for the start of coding and decoding by preparing the all white (0) data as a reference line. At the same time,it initializes the LNTP bit to LNTP=1 for the Typical Prediction .

(2) Coding/decoding of stripes (No change in the AT pixel position)/Image data through processing sequence

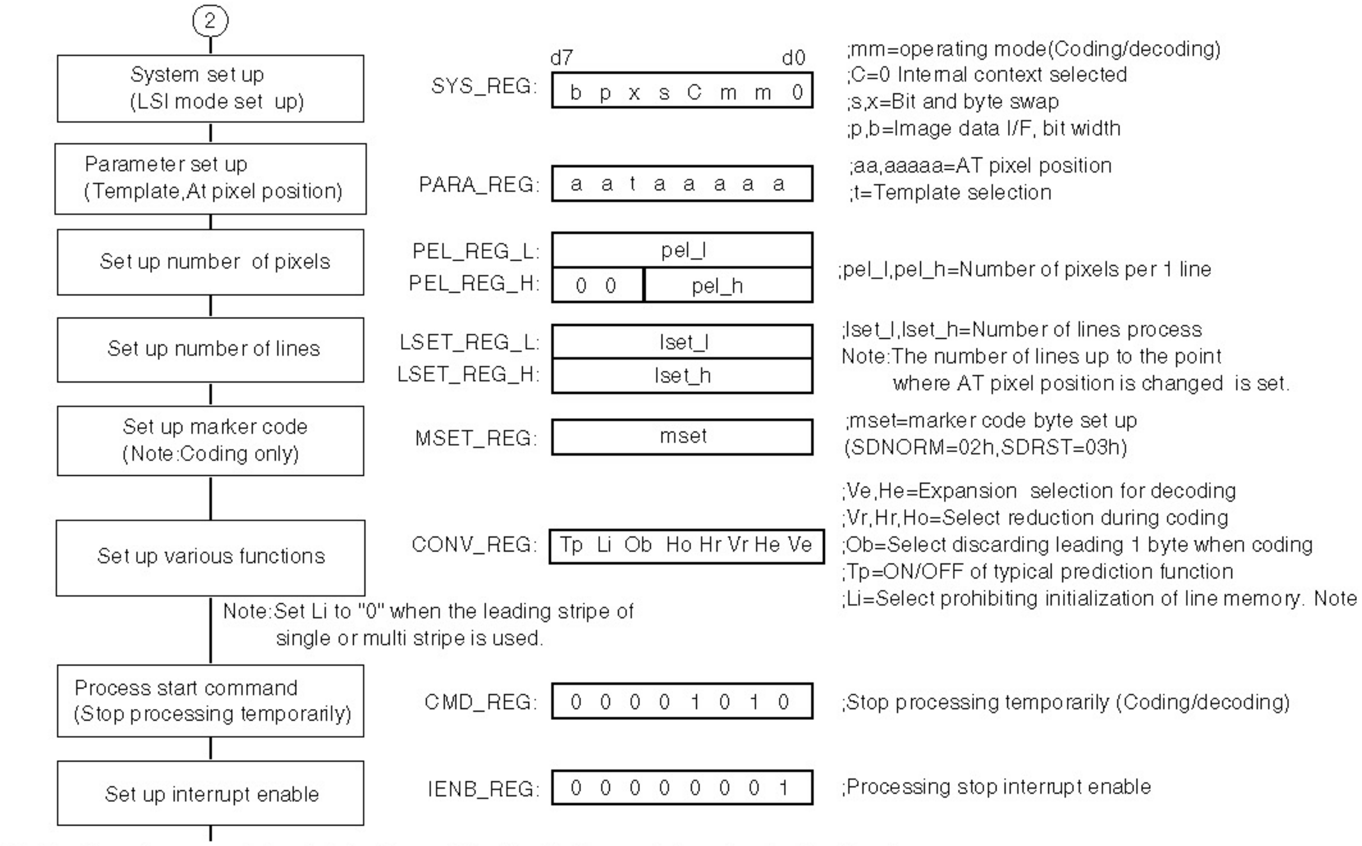

2
System set up
(LSI mode set up)
d7
d0
SYS_REG:
b p x s C m m 0
;mm=operating mode(Coding/decoding)
;C=context selection(Internal/external)
;s,x=Bit,byte swap
;p,b=Image data I/F, bit width
Parameter set up
(Template,context)
PARA_REG:
c/a l/a t a a a a a
;aa,aaaaa=AT pixel position
;t=Template selection
;l=Conditions to take in external context
;c=External context CX0 selects
Set up number of pixels
PEL_REG_L:
pel_l
PEL_REG_H:
0 0
pel_h
;pel_l,pel_h=Number of pixels per line
Set up number of lines
LSET_REG_L:
lset_l
LSET_REG_H:
lset_h
;lset_l,lset_h=Number of lines processed
Set up marker code
(Note:Coding only)
MSET_REG:
mset
;mset=marker code byte set up
(SDNORM=02h,SDRST=03h)
Set up functions
CONV_REG:
Tp Li Ob Ho Hr Vr He Ve
;Ve,He=Select expansion during decoding
;Vr,Hr,Ho=Select reduction during coding
;Ob=Select discarding leading 1 byte during decoding
;Tp=ON/OFF of typical prediction function
;Li=Select prohibiting initialization of line memory
Note:Set Li to "0" when it is the leading stripe of
single or multi stripe.
Process start command
(Coding/decoding/through)
CMD_REG:
0 0 0 0 0 0 1 0
;End of trailer processing (Coding/decoding/through)
start command
Set up interrupt enable
IENB_REG:
0 0 0 0 0 0 0 1
;Processing end interrupt enable

When the external context mode is used,it is not necessary to set the position of AT pixels,number of pixels,number of lines,and expansion,reduction/typical prediction/line memory initialization selection. (They will be invalid)

[Coding and decoding are performed during this time]– – –I/O of image data and code data is performed.
(Coding and decoding of stripe is performed.)

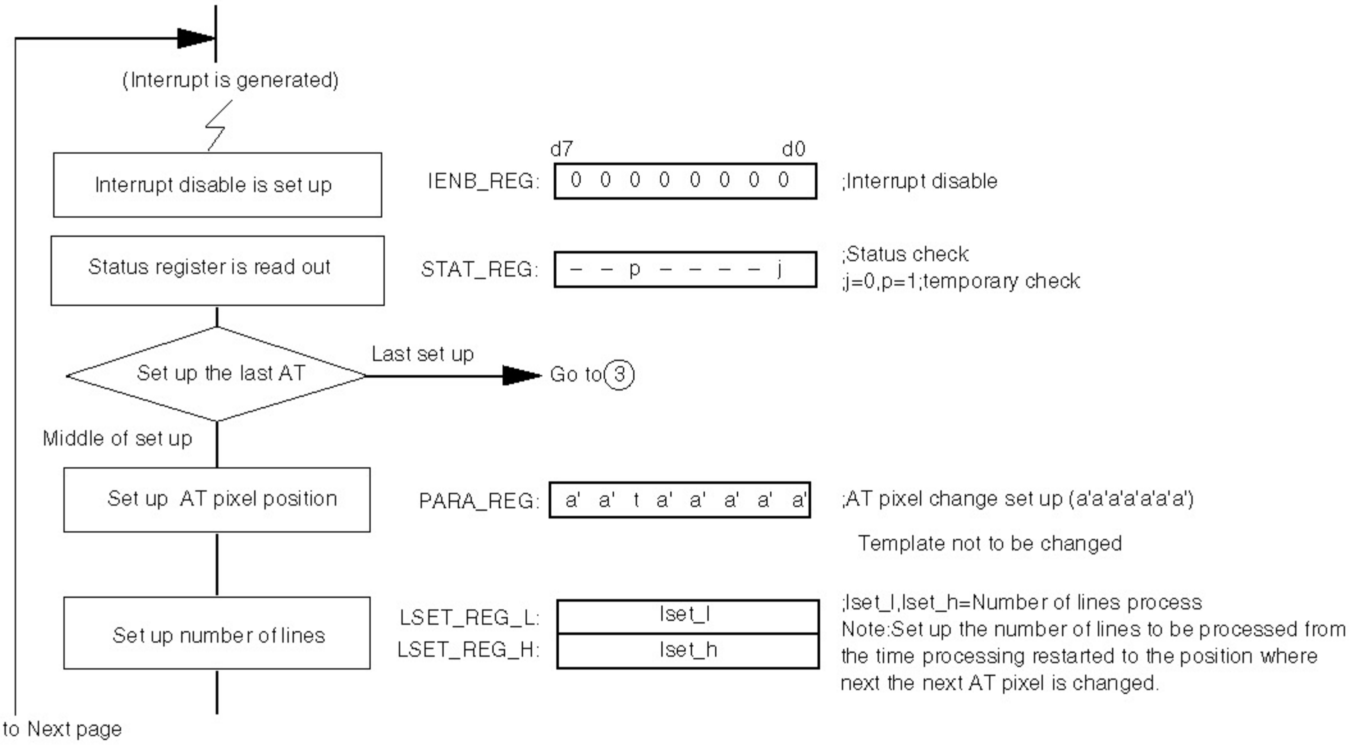


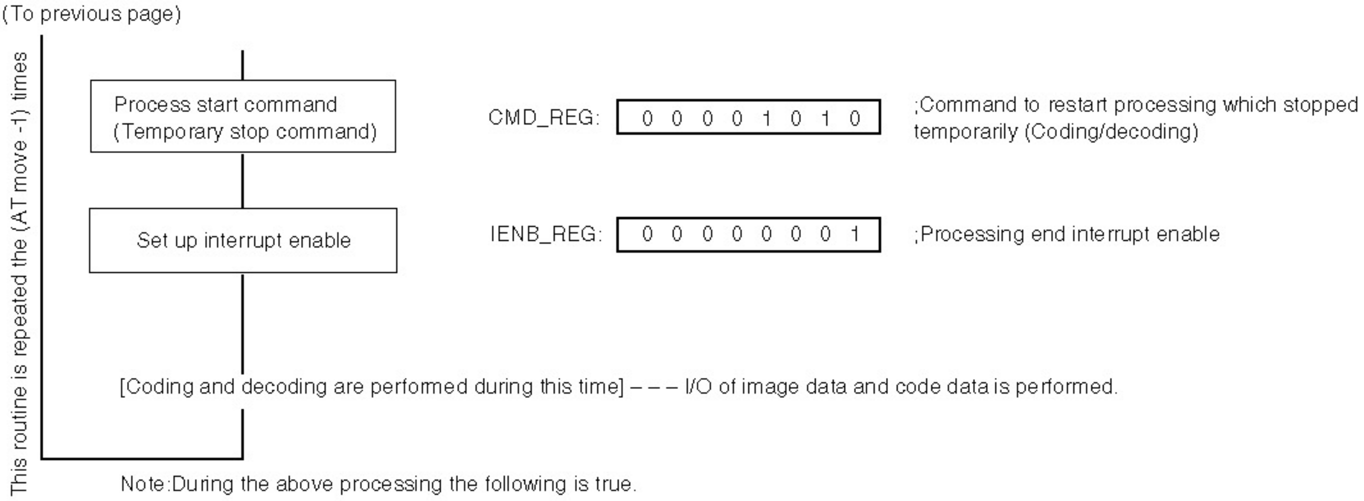
(3) Processing sequence of coding/decoding of stripes (Internal context mode and AT pixel position may change)


2
System set up
(LSI mode set up)
SYS_REG:
d7
d0
b p x s C m m 0
;mm=operating mode(Coding/decoding)
;C=0 Internal context selected
;s,x=Bit and byte swap
;p,b=Image data I/F, bit width
Parameter set up
(Template,At pixel position)
PARA_REG:
a a t a a a a a
;aa,aaaaa=AT pixel position
;t=Template selection
Set up number of pixels
PEL_REG_L:
pel_l
PEL_REG_H:
0 0 pel_h
;pel_l,pel_h=Number of pixels per 1 line
Set up number of lines
LSET_REG_L:
lset_l
LSET_REG_H:
lset_h
;lset_l,lset_h=Number of lines process
Note:The number of lines up to the point where AT pixel position is changed is set.
Set up marker code
(Note:Coding only)
MSET_REG:
mset
;mset=marker code byte set up
(SDNORM=02h,SDRST=03h)
Set up various functions
CONV_REG:
Tp Li Ob Ho Hr Vr He Ve
;Ve,He=Expansion selection for decoding
;Vr,Hr,Ho=Select reduction during coding
;Ob=Select discarding leading 1 byte when coding
;Tp=ON/OFF of typical prediction function
;Li=Select prohibiting initialization of line memory. Note
Note:Set Li to "0" when the leading stripe of single or multi stripe is used.
Process start command
(Stop processing temporarily)
CMD_REG:
0 0 0 0 1 0 1 0
;Stop processing temporarily (Coding/decoding)
Set up interrupt enable
IENB_REG:
0 0 0 0 0 0 0 1
;Processing stop interrupt enable

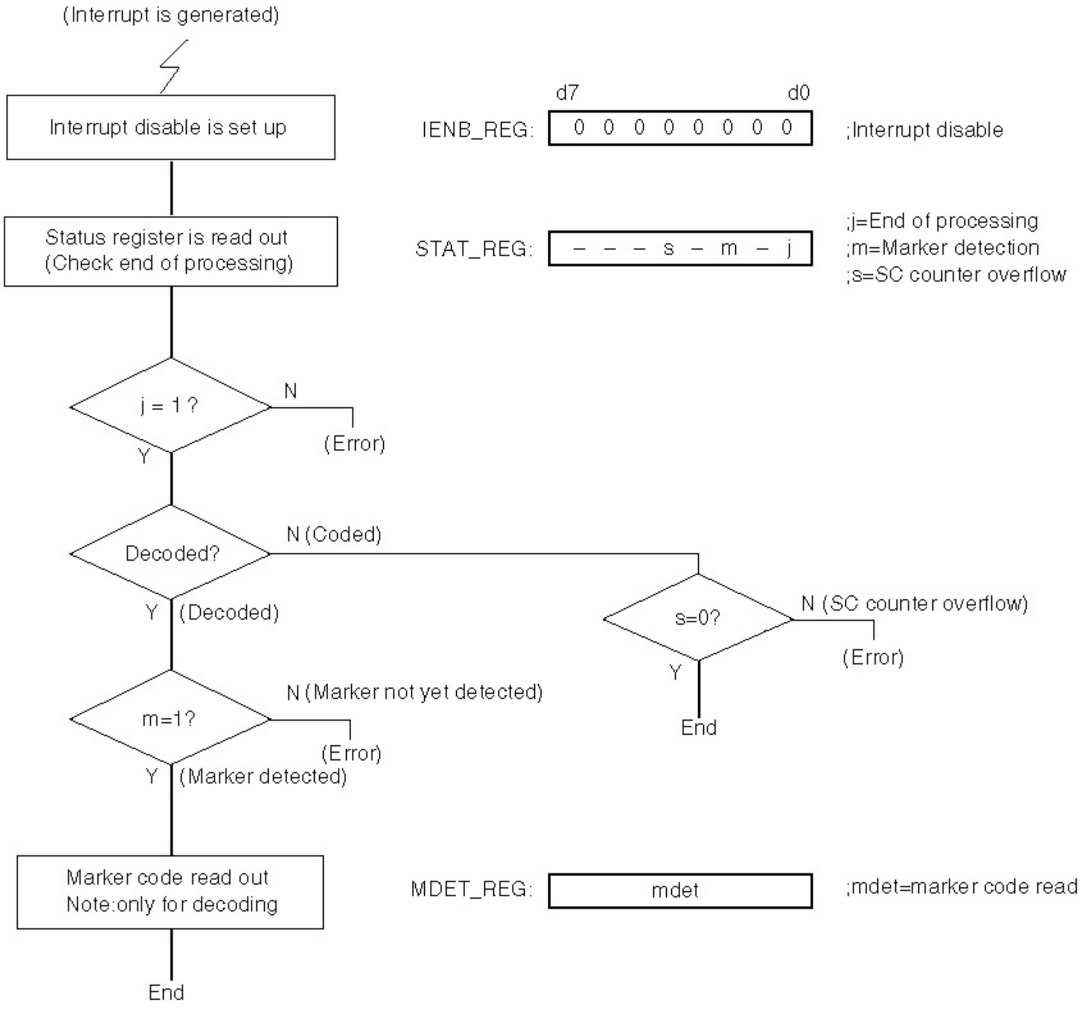
[Coding /decoding go on during this time] – – – I/O of the first image data and code data take place.

Note:During the first processing,if it is coding,(the number of lines of the input image data)=
(the value set in the register which sets the number of lines)+1
During decoding,(number of lines of the output image data)=(the value set in the register which sets the number of lines)-1



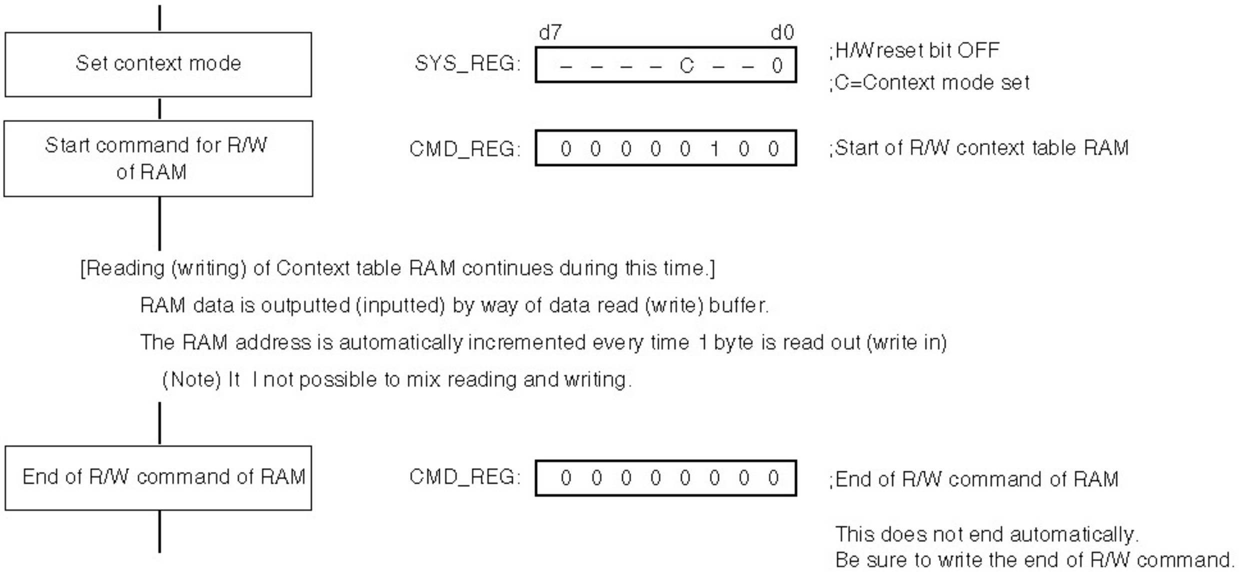

(To previous page)
This routine is repeated the (AT move -1) times
Process start command
(Temporary stop command)
CMD_REG: 0 0 0 0 1 0 1 0
;Command to restart processing which stopped temporarily (Coding/decoding)
Set up interrupt enable
IENB_REG: 0 0 0 0 0 0 0 1
;Processing end interrupt enable
[Coding and decoding are performed during this time] – – – I/O of image data and code data is performed.

Note:During the above processing the following is true.
During coding,
(The number of lines of the input image data) = (Number of lines set in the line number setting register)
During decoding,
(Number of lines of the output image data) = (Number of lines set in the line number setting register)



(4) Read out /write in sequence of context table RAM

This sequence dies R/W of context table RAM.



Set context mode

SYS_REG: d7 – – – – C – – 0 d0 ;H/Wreset bit OFF ;C=Context mode set

Start command for R/W of RAM

CMD_REG: 0 0 0 0 0 1 0 0 ;Start of R/W context table RAM

[Reading (writing) of Context table RAM continues during this time.]

RAM data is outputted (inputted) by way of data read (write) buffer.

The RAM address is automatically incremented every time 1 byte is read out (write in)

(Note) It I not possible to mix reading and writing.

End of R/W command of RAM

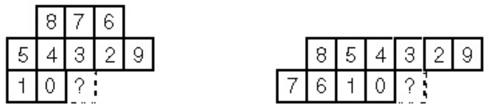
CMD_REG: 0 0 0 0 0 0 0 0 ;End of R/W command of RAM

This does not end automatically.
Be sure to write the end of R/W command.

Note:The assignment of address for context table RAM is as follows.

Internal context mode:Address 0 to 1023 of (LSB:0, MSB:9) as shown below.

External context mode:Address 0 to 4095 of (LSB:CX0, MSB:CS11)

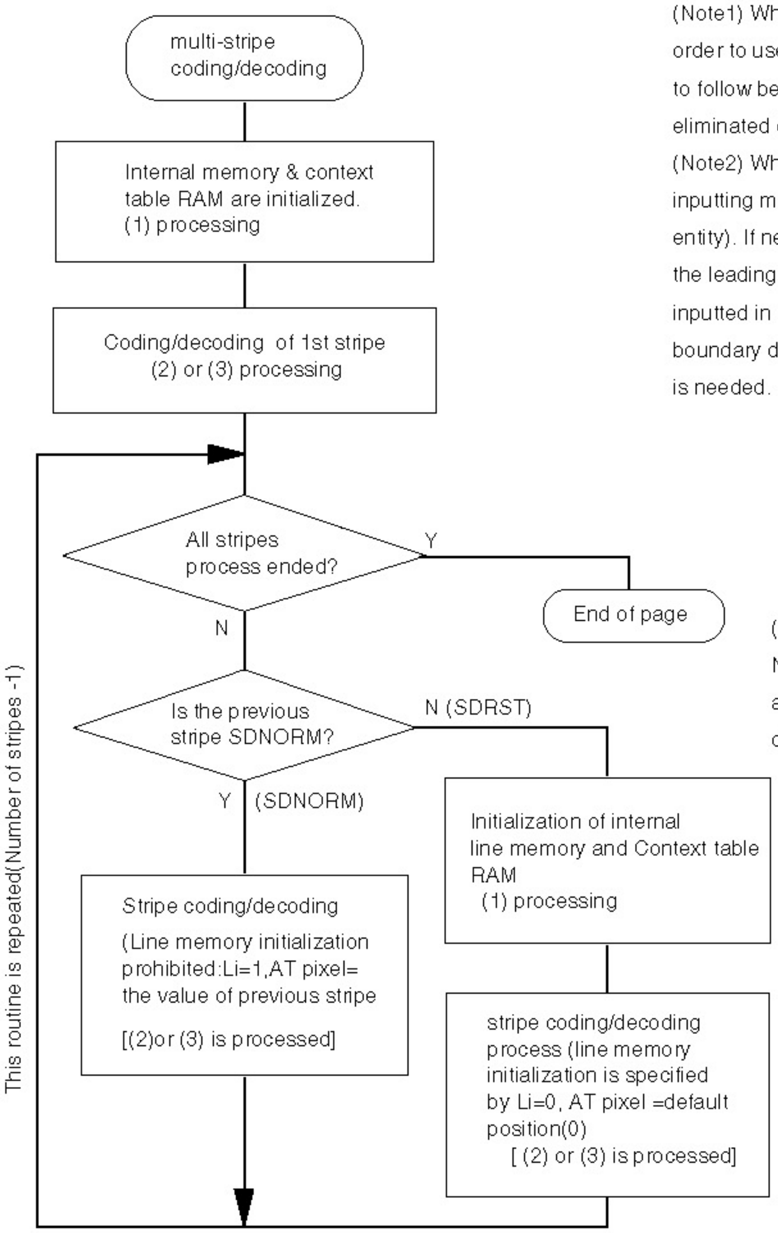


3-line template 2-line template

(AT pixel is MSB:9)

(5) Overall sequence of multi-stripe coding/decoding

The image whose 1page is composed of multiple stripes must perform (2) or (3) by stripes after the initialization of (1).


multi-stripe coding/decoding
Internal memory & context table RAM are initialized. (1) processing
Coding/decoding of 1st stripe (2) or (3) processing
All stripes process ended?
Y
End of page
N
Is the previous stripe SDNORM?
N (SDRST)
Y (SDNORM)
Initialization of internal line memory and Context table RAM (1) processing
Stripe coding/decoding (Line memory initialization prohibited:Li=1,AT pixel= the value of previous stripe [(2)or (3) is processed]
stripe coding/decoding process (line memory initialization is specified by Li=0, AT pixel =default position(0) [(2) or (3) is processed]
This routine is repeated(Number of stripes -1)

(Note1) When 16 bit bus is used for the host-bus during coding , in order to use the word boundary, he pad byte ("00") 1byte long tends to follow behind the end marker code of each stripe.This must be eliminated externally.

(Note2) When starting decoding of each stripe (during decoding), inputting must start from the leading coded data of SDE (Stripe data entity). If necessary, the leading 1 byte is discarded. (In case when the leading portion of coded data of the next stripe is already inputted in LSI (FIFO) or when it is not lined up with the lead boundary during decoding of each stripe ends,external management is needed.

(Note3) Management of marker codes (AT MOVE, NEWLEN, etc) processing (Insertion at the time of coding and detection/removing at the time of decoding) should be done externally.

(Description)

If the end marker of the stripe one before is SDNORM, do not initialize the line memory nor the Context table RAM. The AT pixel position will use the last value of the previous stripe and starts processing next stripe. In case of SDRST,initialization takes place first and then the AT pixel position is returned to the default position. Then the processing of the next stripe begins.

12. ABSOLUTE MAXIMUM RATINGS (Ta=–20 to +70 C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.3 to +7.0	V
V_I	Input voltage		-0.3 to Vcc+0.3	V
V_O	Output voltage		0 to Vcc	V
T_{stg}	Storage temperature		-65 to +150	C
P_d	Power dissipation	Ta=25 C When single IC is used	1380	mW

Note : All of the voltage is reference the GND terminal of the circuit .
Maximum value and minimum value are expression of absolute value.

13. RECOMMEND OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Vcc	Supply voltage		4.5	5.0	5.5	V
GND	GND voltage			0		V
V_I	Input voltage		0		Vcc	V
T_{opr}	Operating temperature range		-20		+70	C
C_L	Output capacitance(against IC)			50		pF

14. ELECTRICAL CHARACTERISTICS (Ta=-20 to +70 C, Vcc=5V 10% unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	"H"input voltage	PD<31:0>,A<3:0>, D<15:0>,$\overline{\text{SVID}}$, BUS16,$\overline{\text{CS}}$,$\overline{\text{BHE}}$		2.0			V
V_{IL}	"L"input voltage					0.8	V
V_{IH}	"H"input voltage	MCLK,$\overline{\text{PXCK}}$		4.5			V
V_{IL}	"L"input voltage					0.0	V
V_{T+}	Positive threshold voltage	$\overline{\text{PDRD}}$,$\overline{\text{DMAAK}}$, $\overline{\text{PDAK}}$,$\overline{\text{PTIM}}$ $\overline{\text{XWAIT}}$,$\overline{\text{PDWR}}$, TEST1,TEST0, $\overline{\text{RD}}$,$\overline{\text{WR}}$,$\overline{\text{RESET}}$				2.4	V
V_{T-}	Negative threshold voltage			0.6			V
V_H	Hysteresis width				0.2		V
V_{OH}	"H"output voltage	D<15:0>	I_{OH}=-8mA	Vcc-0.8			V
V_{OL}	"L"output voltage		I_{OH}=8mA			0.55	V
V_{OH}	"H"output voltage	$\overline{\text{XCLK}}$,$\overline{\text{PXCKO}}$	I_{OH}=-4mA	Vcc-0.8			V
V_{OL}	"L"output voltage		I_{OH}=4mA			0.55	V
V_{OH}	"H"output voltage	PD<31:0>,INTR, DMARQ,PDRQ, $\overline{\text{PRDY}}$,$\overline{\text{RVID}}$	I_{OH}=-2mA	Vcc-0.8			V
V_{OL}	"L"output voltage		I_{OH}=2mA			0.55	V
I_{IH}	"H"Input current	A<3:0>, D<15:0>,$\overline{\text{RD}}$,$\overline{\text{WR}}$, MCLK,$\overline{\text{BHE}}$, $\overline{\text{RESET}}$,$\overline{\text{CS}}$	Vcc=5.5V, V_I=5.5V			-1.0	A
I_{IL}	"L"Input current		Vcc=5.5V, V_I=0V			1.0	A
I_{OZH}	"H"output current in OFF state	D<15:0>	Vcc=5.5V, V_I=5.5V			-5.0	A
I_{OZL}	"L"output current in OFF state		Vcc=5.5V, V_I=0V			5.0	A
R_U	Pull up Resister	PD<31:0>,$\overline{\text{PDRD}}$, $\overline{\text{PDWR}}$,$\overline{\text{PDAK}}$, $\overline{\text{SVID}}$,$\overline{\text{PTIM}}$, $\overline{\text{PXCK}}$,$\overline{\text{XWAIT}}$, BUS16,$\overline{\text{DMAAK}}$	Vcc=5.5V, V_I=0V	25		100	k
R_D	Pull down Resister	TEST1,TEST0	Vcc=5.5V, V_I=5V	21		100	k
I_{CCA}	Dynamic consumption		Vcc=5.5V, V_I=Vcc, GND		100		mA

The value of register is 50k buffer's value.

15. TIMING CHARACTERISTICS (Ta=-20 to +70 C, Vcc=5V 10% unless otherwise noted)

1) Host Bus I/F

Symbol	Parameter	Test conditions	Limits			Unit	Test circuit
			Min	Typ	Max		
t_{PZL} ($\overline{RD}$-D0 to 15)	D0 to 15 output define time for $\overline{RD}$ assert	C_L=50pF	0		30	ns	1
t_{PZH} ($\overline{RD}$-D0 to 15)			0		30	ns	
t_{PLZ} ($\overline{RD}$-D0 to 15)	D0 to 15 output hold time for $\overline{RD}$ assert		0		30	ns	
t_{PHZ} ($\overline{RD}$-D0 to 15)			0		30	ns	
t_{PHL} ($\overline{DMAAK}$-DMARQ)	DMARQ negate time for $\overline{DMAAK}$ assert				20	ns	

2) Image data I/F

Symbol	Parameter	Test conditions	Limits			Unit	Test circuit
			Min	Typ	Max		
t_{PLH} ($\overline{PTIM}$-$\overline{PRDY}$)	$\overline{PRDY}$ negate time for $\overline{PTIM}$ assert	C_L=50pF			30	ns	1
t_{PHL} ($\overline{PXCK}$-$\overline{RVID}$)	$\overline{RVID}$ output define time for the fall of $\overline{PXCK}$				25	ns	
t_{PLH} ($\overline{PXCK}$-$\overline{RVID}$)					25	ns	
t_{PHL} ($\overline{PXCK}$-$\overline{PXCKO}$)	$\overline{PXCKO}$ delay time for $\overline{PXCK}$				15	ns	
t_{PLH} ($\overline{PXCK}$-$\overline{PXCKO}$)					15	ns	
t_{PHL} ($\overline{PXCKO}$-$\overline{RVID}$)	$\overline{RVID}$ output define time for the fall of $\overline{PXCKO}$				10	ns	
t_{PLH} ($\overline{PXCKO}$-$\overline{RVID}$)					10	ns	
t_{PLH} ($\overline{PTIM}$-$\overline{RVID}$)	$\overline{RVID}$ negate time for $\overline{PTIM}$ negate		0			ns	
t_{PHL} ($\overline{PDAK}$-PDRQ)	$\overline{PDRQ}$ negate time for $\overline{PDAK}$ assert				20	ns	
t_{PZL} ($\overline{PDRD}$-PD0 to 31)	PD0 to 31 output define time for $\overline{PDRD}$ assert		0		30	ns	
t_{PZH} ($\overline{PDRD}$-PD0 to 31)			0		30	ns	
t_{PLZ} ($\overline{PDRD}$-PD0 to 31)	PD0 to 31 hold time for $\overline{PDRD}$ negate		0		30	ns	
t_{PHZ} ($\overline{PDRD}$-PD0 to 31)			0		30	ns	

3) Context I/F

Symbol	Parameter	Test conditions	Limits			Unit	Test circuit
			Min	Typ	Max		
t_{PLH} ($\overline{\text{XTIM}}$-$\overline{\text{XRDY}}$)	$\overline{\text{XRDY}}$ negate time for $\overline{\text{XTIM}}$ assert time	C_L=50pF			30	ns	1
t_{PLH} ($\overline{\text{XCLK}}$-$\overline{\text{RPIX}}$)	$\overline{\text{RPIX}}$ output define time for the fall of $\overline{\text{XCLK}}$		0		30	ns	
t_{PHL} ($\overline{\text{XCLK}}$-$\overline{\text{RPIX}}$)			0		30	ns	
t_{PLH} (MCLK-$\overline{\text{XCLK}}$)	$\overline{\text{XCLK}}$ delay time for MCLK				30	ns	
t_{PHL} (MCLK-$\overline{\text{XCLK}}$)					30	ns	

16. TIMING CHARACTERISTICS (Ta=-20 to +70 C, Vcc=5V 10% unless otherwise noted)

1) Host Bus I/F

Symbol	Parameter	Test conditions	Limits			Unit	Test circuit
			Min	Typ	Max		
$t_{w}(\overline{\mathrm{RESET}})$	$\overline{\mathrm{RESET}}$ assert time	C_L=50pF	100			ns	1
$t_{su}(\overline{\mathrm{RD}}\text{-}\overline{\mathrm{CS}})$	$\overline{\mathrm{CS}}$ set up time for $\overline{\mathrm{RD}}$ assert		20			ns	
$t_{h}(\overline{\mathrm{RD}}\text{-}\overline{\mathrm{CS}})$	$\overline{\mathrm{CS}}$ hold time for $\overline{\mathrm{RD}}$ negate		20			ns	
$t_{su}(\overline{\mathrm{RD}}\text{-A0 to 3})$	$\overline{\text{A0 to 3}}$ set up time for $\overline{\mathrm{RD}}$ assert		20			ns	
$t_{su}(\overline{\mathrm{RD}}\text{-}\overline{\mathrm{BHE}})$	$\overline{\mathrm{BHE}}$ set up time for $\overline{\mathrm{RD}}$ assert		20			ns	
$t_{w}(\overline{\mathrm{RD}})$	$\overline{\mathrm{RD}}$ assert time		30			ns	
$t_{h}(\overline{\mathrm{RD}}\text{-A0 to 3})$	$\overline{\text{A0 to 3}}$ hold time for $\overline{\mathrm{RD}}$negate		20			ns	
$t_{h}(\overline{\mathrm{RD}}\text{-}\overline{\mathrm{BHE}})$	$\overline{\mathrm{BHE}}$ hold time for $\overline{\mathrm{RD}}$ negate		20			ns	
$t_{su}(\overline{\mathrm{WR}}\text{-}\overline{\mathrm{CS}})$	$\overline{\mathrm{CS}}$ set up time for $\overline{\mathrm{WR}}$ assert		20			ns	
$t_{h}(\overline{\mathrm{WR}}\text{-}\overline{\mathrm{CS}})$	$\overline{\mathrm{CS}}$ hold time for $\overline{\mathrm{WR}}$ negate		20			ns	
$t_{su}(\overline{\mathrm{WR}}\text{-A0 to 3})$	$\overline{\text{A0 to 3}}$ set up time for $\overline{\mathrm{WR}}$ assert		20			ns	
$t_{su}(\overline{\mathrm{WR}}\text{-}\overline{\mathrm{BHE}})$	$\overline{\text{A0 to 3}}$ set up time for $\overline{\mathrm{WR}}$ assert		20			ns	
$t_{w}(\overline{\mathrm{WR}})$	$\overline{\mathrm{WR}}$ assert time		30			ns	
$t_{h}(\overline{\mathrm{WR}}\text{-A0 to 3})$	$\overline{\text{A0 to 3}}$ hold time for $\overline{\mathrm{WR}}$ negate		20			ns	
$t_{h}(\overline{\mathrm{WR}}\text{-}\overline{\mathrm{BHE}})$	$\overline{\mathrm{BHE}}$ hold time for $\overline{\mathrm{WR}}$ negate		20			ns	
$t_{su}(\overline{\mathrm{WR}}\text{-D0 to 15})$	$\overline{\text{D0 to 15}}$ input set up time for $\overline{\mathrm{WR}}$ negate		20			ns	
$t_{h}(\overline{\mathrm{WR}}\text{-D0 to 15})$	$\overline{\text{D0 to 15}}$ input hold time for $\overline{\mathrm{WR}}$ negate		20			ns	
$t_{su}(\overline{\mathrm{RD}}\text{-}\overline{\mathrm{DMAAK}})$	$\overline{\mathrm{DMAAK}}$ set up time for $\overline{\mathrm{RD}}$ assert		20			ns	
$t_{h}(\overline{\mathrm{RD}}\text{-}\overline{\mathrm{DMAAK}})$	$\overline{\mathrm{DMAAK}}$ hold time for $\overline{\mathrm{RD}}$ negate		20			ns	
$t_{su}(\overline{\mathrm{WR}}\text{-}\overline{\mathrm{DMAAK}})$	$\overline{\mathrm{DMAAK}}$ set up time for $\overline{\mathrm{WR}}$ assert		20			ns	
$t_{h}(\overline{\mathrm{WR}}\text{-}\overline{\mathrm{DMAAK}})$	$\overline{\mathrm{DMAAK}}$ hold time for $\overline{\mathrm{WR}}$ negate		20			ns	

2) Image Data I/F

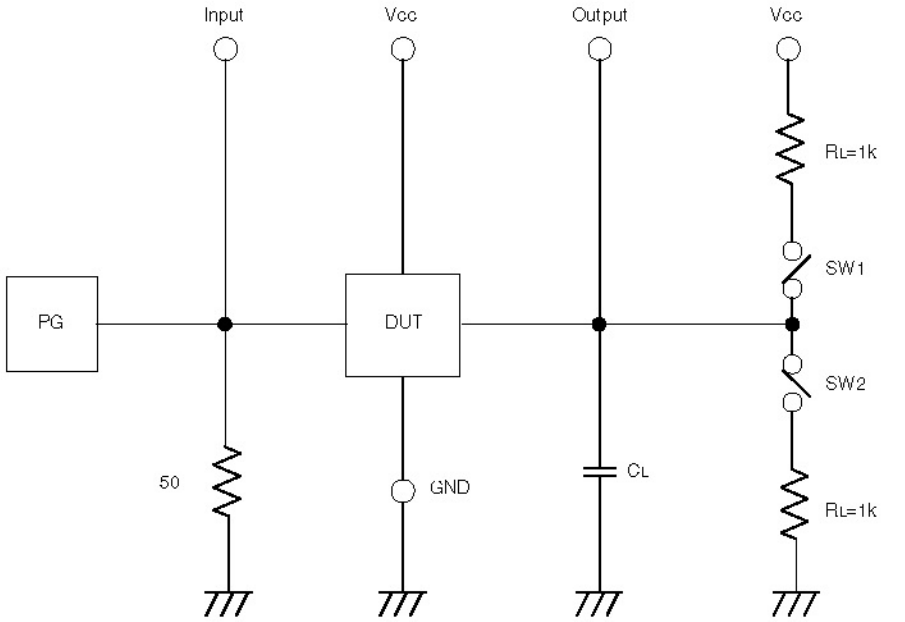
Symbol	Parameter	Test conditions	Limits			Unit	Test circuit
			Min	Typ	Max		
t_{ci}(MCLK)	MCLK period(Mx) when used image data I/F	C_L=50pF	50			ns	1
t_{wi+}(MCLK)	MCLK high level time(Mh) when used image data I/F		20			ns	
t_{wi-}(MCLK)	MCLK low level time(Ml) when used image data I/F		20			ns	
t_{ri}(MCLK)	MCLK rising time when used image data I/F				20	ns	
t_{fi}(MCLK)	MCLK falling time when used image data I/F				20	ns	
$t_{su}(\overline{\text{PXCK}}\text{-}\overline{\text{PTIM}})$	$\overline{\text{PTIM}}$ set up time for the fall of $\overline{\text{PXCK}}$		20			ns	
$t_{h}(\overline{\text{PXCK}}\text{-}\overline{\text{PTIM}})$	$\overline{\text{PTIM}}$ hold time for the rise of $\overline{\text{PXCK}}$		20			ns	
$t_{w+}(\overline{\text{PXCK}})$	$\overline{\text{PXCK}}$ high time		20			ns	
$t_{w-}(\overline{\text{PXCK}})$	$\overline{\text{PXCK}}$ low time		20			ns	
$t_{c}(\overline{\text{PXCK}})$	$\overline{\text{PXCK}}$ period		50			ns	
$t_{su}(\overline{\text{PXCK}}\text{-}\overline{\text{SVID}})$	$\overline{\text{SVID}}$ set up time for the fall of $\overline{\text{PXCK}}$		10			ns	
$t_{h}(\overline{\text{PXCK}}\text{-}\overline{\text{SVID}})$	$\overline{\text{SVID}}$ set up time for the fall of $\overline{\text{PXCK}}$		10			ns	
$t_{su}(\overline{\text{PDRD}}\text{-}\overline{\text{PDAK}})$	$\overline{\text{PDAK}}$ set up time for $\overline{\text{PDRD}}$ assert		20			ns	
$t_{h}(\overline{\text{PDRD}}\text{-}\overline{\text{PDAK}})$	$\overline{\text{PDAK}}$ hold time for $\overline{\text{PDRD}}$ negate		20			ns	
$t_{w}(\overline{\text{PDRD}})$	$\overline{\text{PDRD}}$ assert time		30			ns	
$t_{su}(\overline{\text{PDWR}}\text{-}\overline{\text{PDAK}})$	$\overline{\text{PDAK}}$ set up time for $\overline{\text{PDWR}}$ assert		20			ns	
$t_{h}(\overline{\text{PDWR}}\text{-}\overline{\text{PDAK}})$	$\overline{\text{PDAK}}$ hold time for $\overline{\text{PDWR}}$ negate		20			ns	
$t_{w}(\overline{\text{PDWR}})$	$\overline{\text{PDWR}}$ assert time		20			ns	
$t_{su}(\overline{\text{PDWR}}\text{-PD0 to 31})$	$\overline{\text{PD0 to 31}}$ input set up time for $\overline{\text{PDWR}}$ negate		20			ns	
$t_{h}(\overline{\text{PDWR}}\text{-PD0 to 31})$	$\overline{\text{PD0 to 31}}$ input hold time for $\overline{\text{PDWR}}$ negate		20			ns	

3) Context I/F

Symbol	Parameter	Test conditions	Limits			Unit	Test circuit
			Min	Typ	Max		
t_{cc}(MCLK)	MCLK period(Mx) when used context I/F	C_L=50pF	100			ns	1
t_{wc+}(MCLK)	MCLK high level time(Mh) when used context I/F		40			ns	
t_{wc-}(MCLK)	MCLK low level time(Ml) when used context I/F		40			ns	
t_{rc}(MCLK)	MCLK rising time when used context I/F				20	ns	
t_{fc}(MCLK)	MCLK falling time when used context I/F				20	ns	
t_{su}(MCLK-$\overline{\text{XTIM}}$)	$\overline{\text{XTIM}}$ assert time for the rise of MCLK		20			ns	
t_{h}($\overline{\text{XCLK}}$-$\overline{\text{XTIM}}$)	$\overline{\text{XTIM}}$ negate time for the rise of $\overline{\text{XCLK}}$				20	ns	
t_{w+}($\overline{\text{XCLK}}$)	$\overline{\text{XCLK}}$ high time			Mh		ns	
t_{w-}($\overline{\text{XCLK}}$)	$\overline{\text{XCLK}}$ low time			Ml		ns	
t_{c}($\overline{\text{XCLK}}$)	$\overline{\text{XCLK}}$ period			Mx		ns	
t_{h}($\overline{\text{XCLK}}$-$\overline{\text{XWAIT}}$)	$\overline{\text{XWAIT}}$ negate time for the rise of $\overline{\text{XCLK}}$		0		10	ns	
t_{sul}($\overline{\text{XCLK}}$-CX0 to 11)	$\overline{\text{CX0 to 11}}$ set up time for the rise of $\overline{\text{XCLK}}$		20			ns	
t_{sul}($\overline{\text{XCLK}}$-$\overline{\text{PEUPE}}$)	$\overline{\text{PEUPE}}$ set up time for the rise of $\overline{\text{XCLK}}$		20			ns	
t_{sul}($\overline{\text{XCLK}}$-$\overline{\text{SPIX}}$)	$\overline{\text{SPIX}}$ set up time for the rise of $\overline{\text{XCLK}}$		20			ns	
t_{hl}($\overline{\text{XCLK}}$-CX0 to 11)	$\overline{\text{CX0 to 11}}$ hold time for the rise of $\overline{\text{XCLK}}$		20			ns	
t_{hl}($\overline{\text{XCLK}}$-$\overline{\text{PEUPE}}$)	$\overline{\text{PEUPE}}$ hold time for the rise of $\overline{\text{XCLK}}$		20			ns	
t_{hl}($\overline{\text{XCLK}}$-$\overline{\text{SPIX}}$)	$\overline{\text{SPIX}}$ hold time for the rise of $\overline{\text{XCLK}}$		20			ns	
t_{sut}($\overline{\text{XCLK}}$-CX0 to 11)	$\overline{\text{CX0 to 11}}$ set up time for the rise of $\overline{\text{XCLK}}$		70			ns	
t_{sut}($\overline{\text{XCLK}}$-$\overline{\text{SPIX}}$)	$\overline{\text{SPIX}}$ set up time for the rise of $\overline{\text{XCLK}}$		70			ns	
t_{ht}($\overline{\text{XCLK}}$-CX0 to 11)	$\overline{\text{CX0 to 11}}$ hold time for the rise of $\overline{\text{XCLK}}$		20			ns	
t_{ht}($\overline{\text{XCLK}}$-$\overline{\text{SPIX}}$)	$\overline{\text{SPIX}}$ hold time for the rise of $\overline{\text{XCLK}}$		20			ns	
t_{k}($\overline{\text{XCLK}}$-$\overline{\text{PEUPE}}$)	$\overline{\text{PEUPE}}$ input define time for the rise of $\overline{\text{XCLK}}$				20	ns	

17. TEST CIRCUIT

1

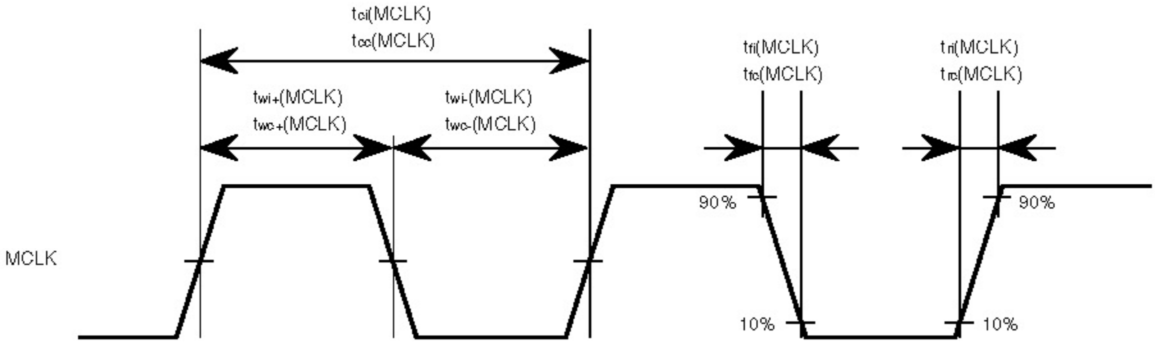


Parameter	SW1	SW2
t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Close	Open
t_{PHZ}	Open	Close
t_{PZL}	Close	Open
t_{PZH}	Open	Close

(1) characteristic of pulse generation (PG) (10% to 90%)
t_r=3ns, t_f=3ns

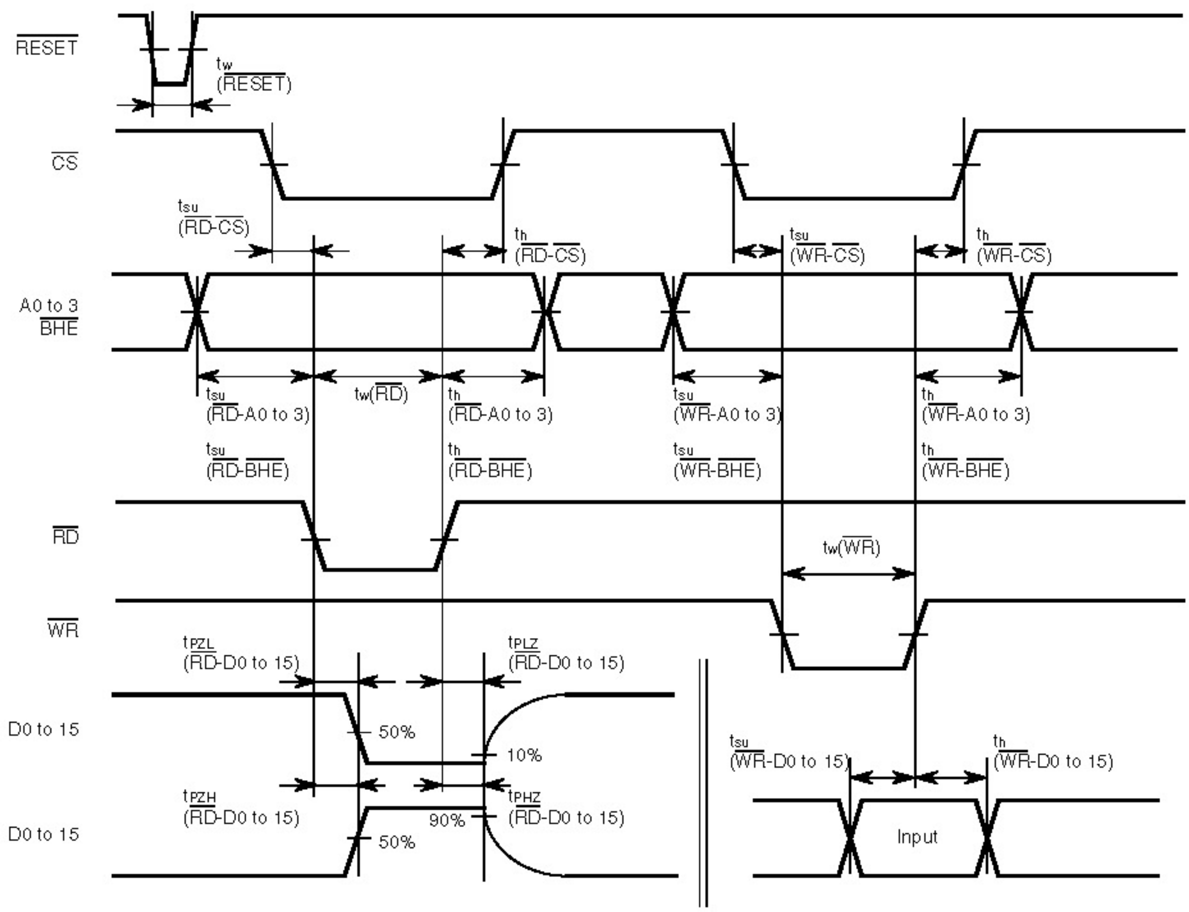
(2) Capacitance C_L includes stray wiring capacitance and probe input capacitance.

Master clock



HOST BUS I/F

(1) MPU access


$\overline{RESET}$
t_w ($\overline{RESET}$)
$\overline{CS}$
t_{su} ($\overline{RD}$-$\overline{CS}$)
t_h ($\overline{RD}$-$\overline{CS}$)
t_{su} ($\overline{WR}$-$\overline{CS}$)
t_h ($\overline{WR}$-$\overline{CS}$)
A0 to 3
$\overline{BHE}$
t_{su} ($\overline{RD}$-A0 to 3)
t_w($\overline{RD}$)
t_h ($\overline{RD}$-A0 to 3)
t_{su} ($\overline{WR}$-A0 to 3)
t_h ($\overline{WR}$-A0 to 3)
t_{su} ($\overline{RD}$-$\overline{BHE}$)
t_h ($\overline{RD}$-$\overline{BHE}$)
t_{su} ($\overline{WR}$-$\overline{BHE}$)
t_h ($\overline{WR}$-$\overline{BHE}$)
$\overline{RD}$
t_w($\overline{WR}$)
$\overline{WR}$
t_{PZL} ($\overline{RD}$-D0 to 15)
t_{PLZ} ($\overline{RD}$-D0 to 15)
D0 to 15
50%
10%
t_{su} ($\overline{WR}$-D0 to 15)
t_h ($\overline{WR}$-D0 to 15)
t_{PZH} ($\overline{RD}$-D0 to 15)
t_{PHZ} ($\overline{RD}$-D0 to 15)
90%
D0 to 15
50%
Input

(2) DMA access

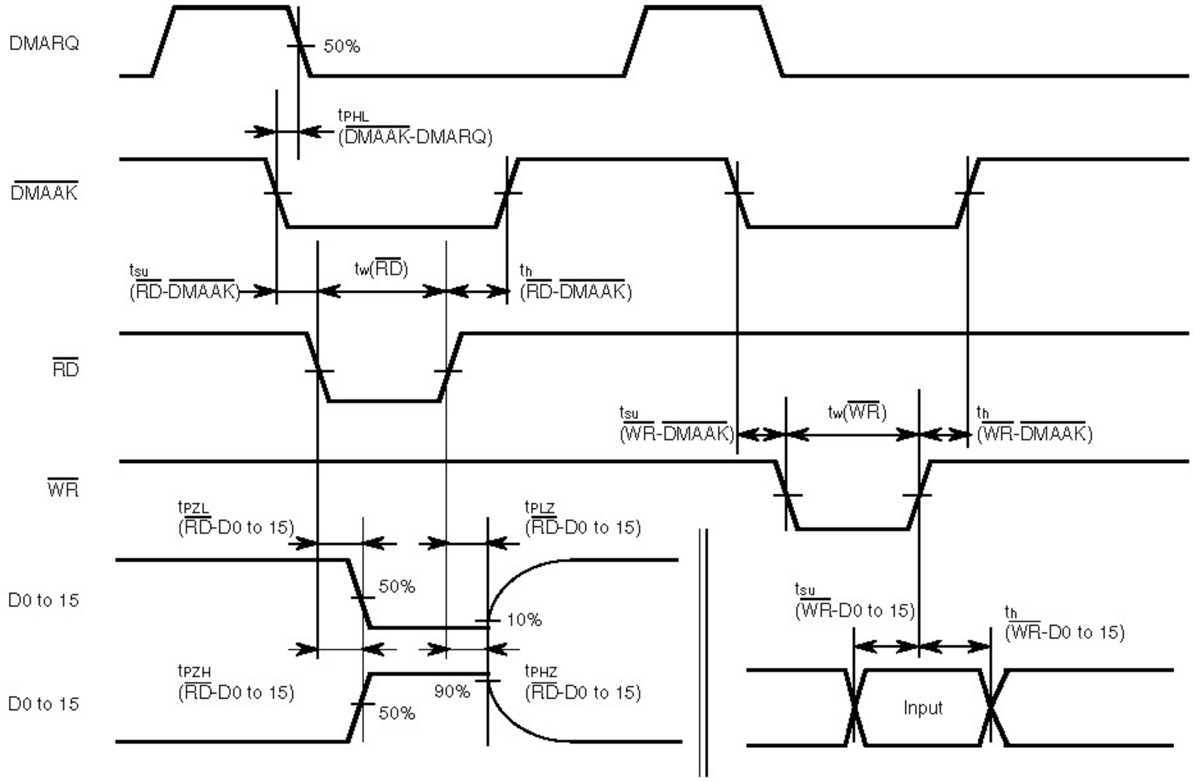
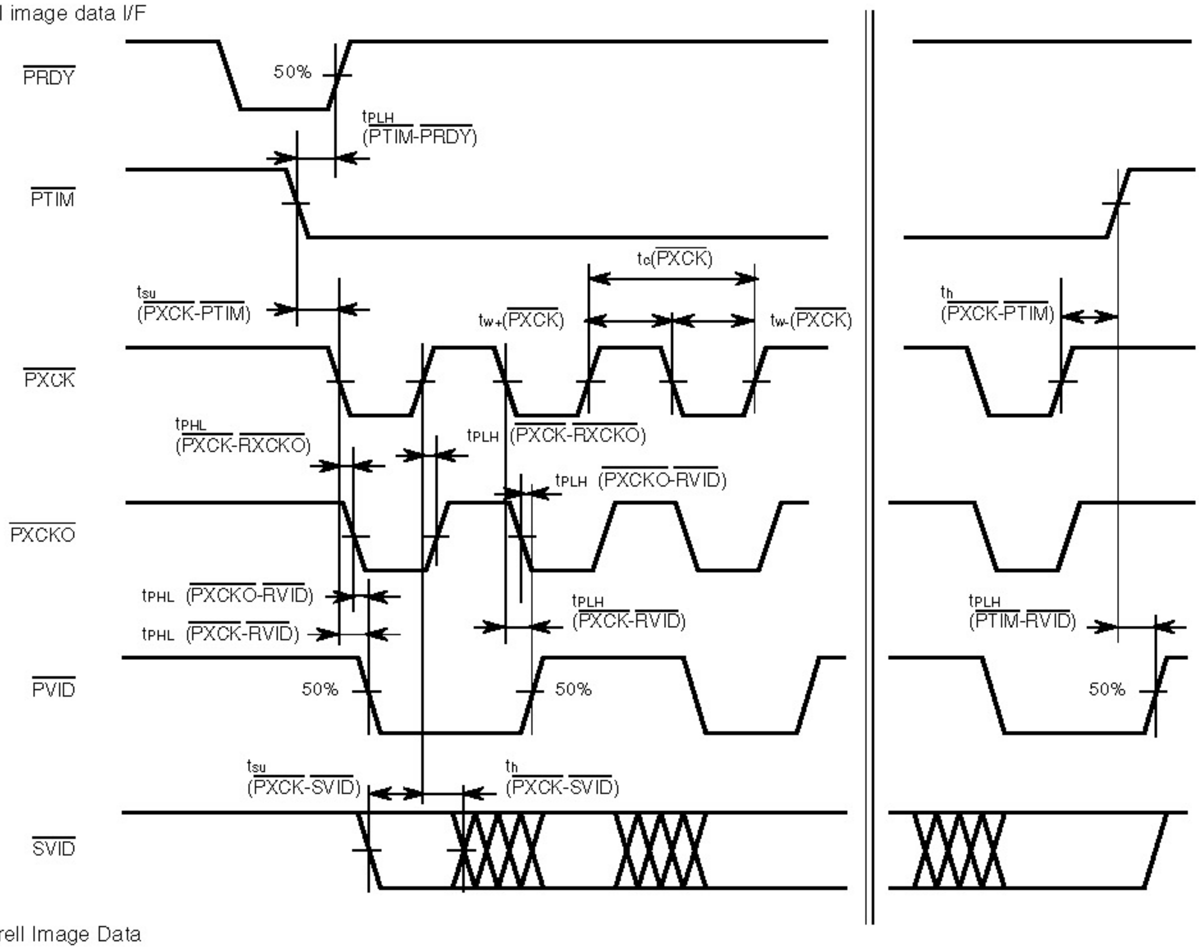
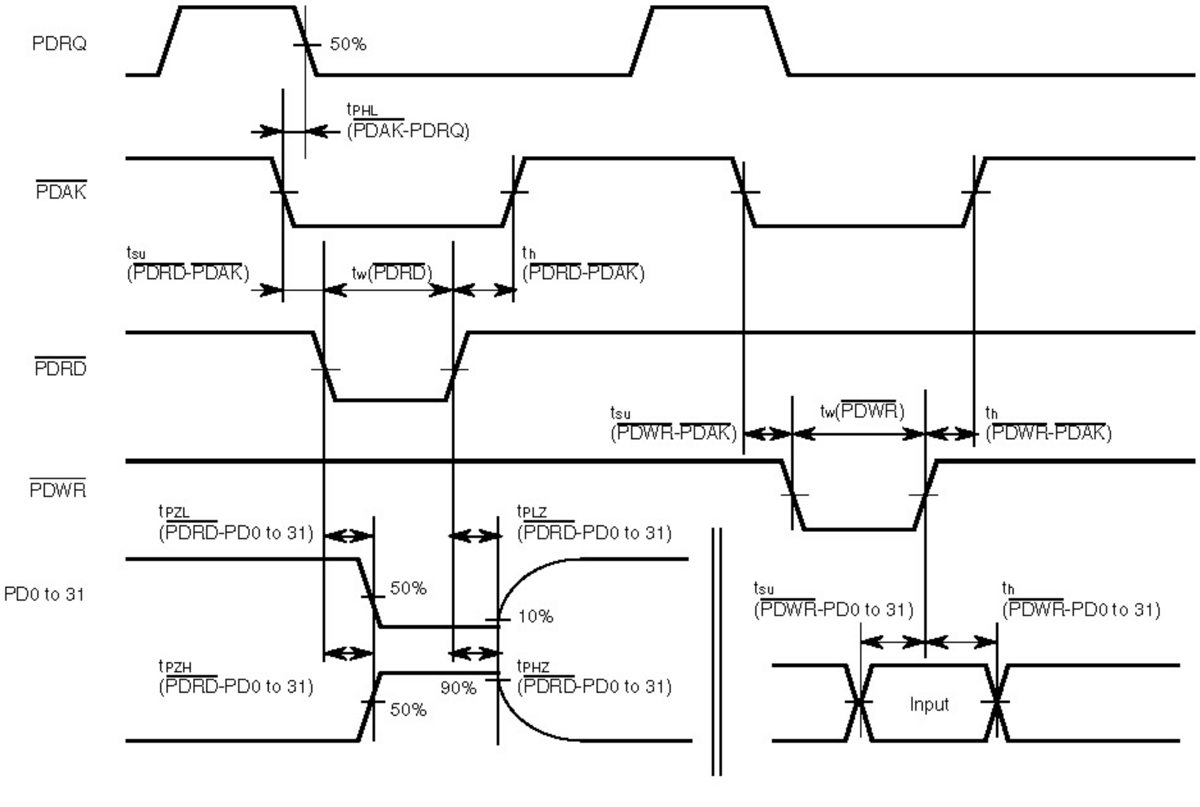

DMARQ
50%
t_{PHL} ($\overline{DMAAK}$-DMARQ)
$\overline{DMAAK}$
t_{su} ($\overline{RD}$-$\overline{DMAAK}$)
t_w($\overline{RD}$)
t_h ($\overline{RD}$-$\overline{DMAAK}$)
$\overline{RD}$
t_{su} ($\overline{WR}$-$\overline{DMAAK}$)
t_w($\overline{WR}$)
t_h ($\overline{WR}$-$\overline{DMAAK}$)
$\overline{WR}$
t_{PZL} ($\overline{RD}$-D0 to 15)
t_{PLZ} ($\overline{RD}$-D0 to 15)
D0 to 15
50%
10%
t_{su} ($\overline{WR}$-D0 to 15)
t_h ($\overline{WR}$-D0 to 15)
t_{PZH} ($\overline{RD}$-D0 to 15)
t_{PHZ} ($\overline{RD}$-D0 to 15)
90%
D0 to 15
50%
Input

IMAGE DATA I/F

(1) Serial image data I/F

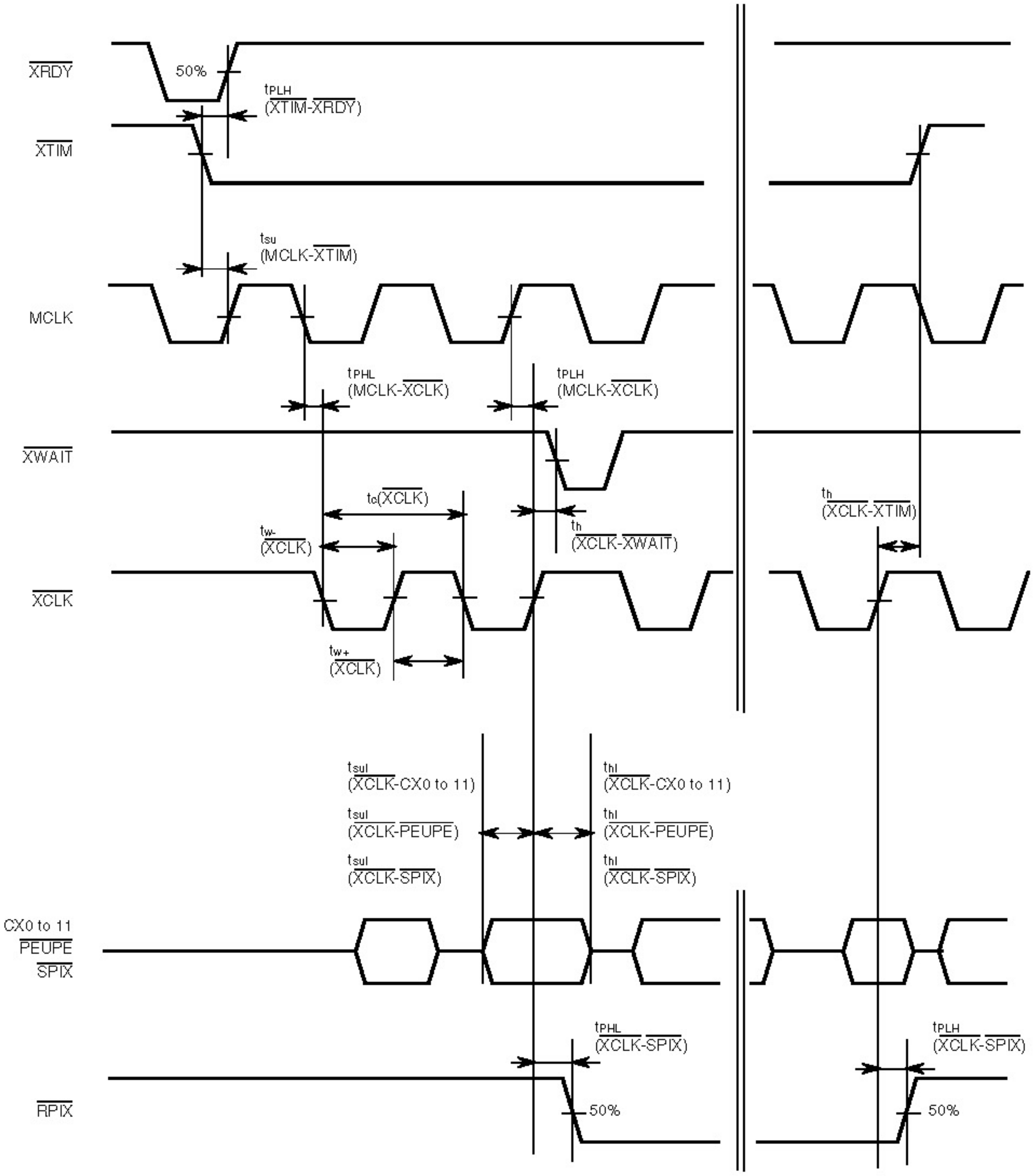


(2) Pallarell Image Data

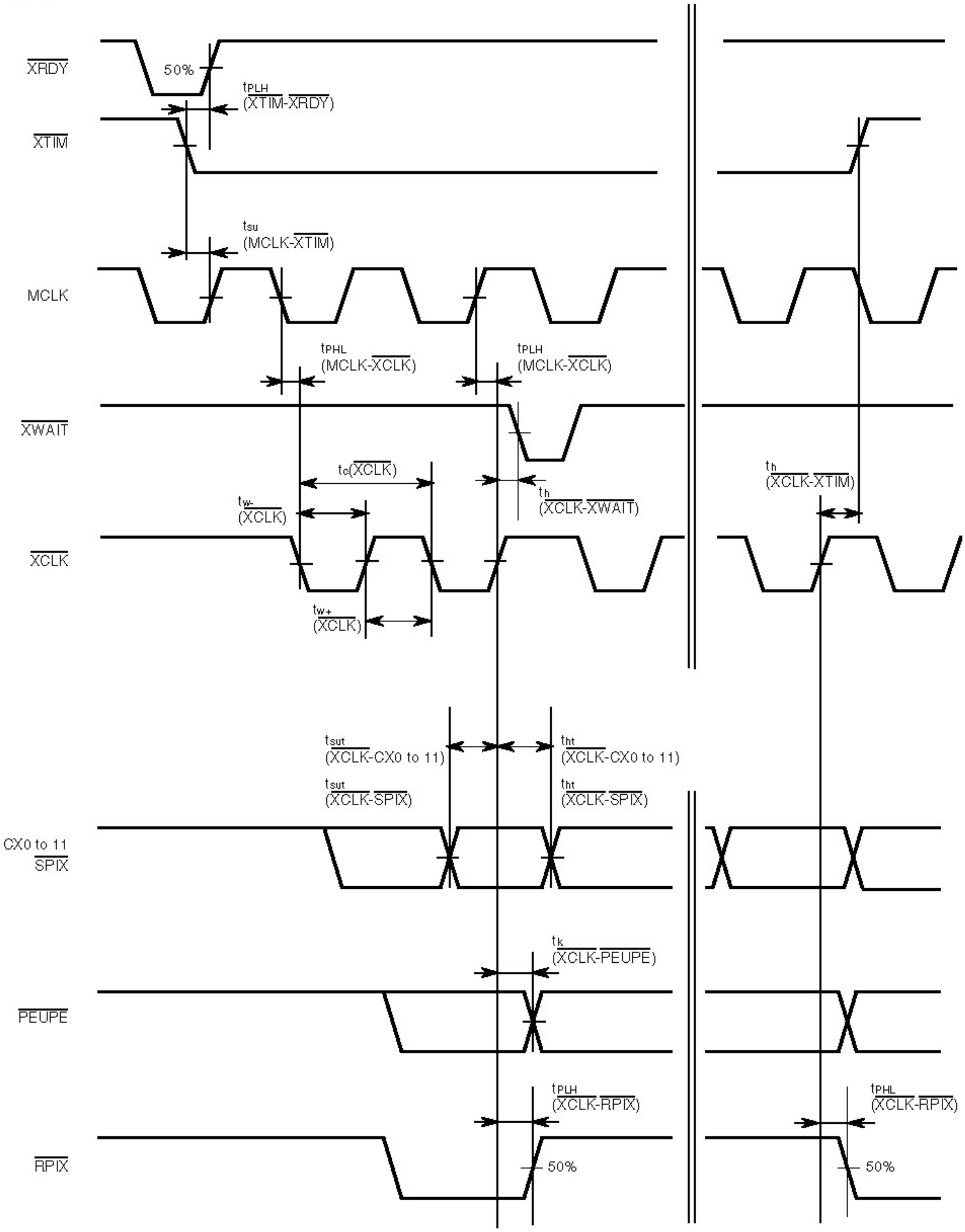


CONTEXT I/F

(1) Latch input mode



(2) Through input mode


XRDY
50%
tPLH (XTIM-XRDY)
XTIM
tsu (MCLK-XTIM)
MCLK
tPHL (MCLK-XCLK)
tPLH (MCLK-XCLK)
XWAIT
tc(XCLK)
tw- (XCLK)
th (XCLK-XWAIT)
th (XCLK-XTIM)
XCLK
tw+ (XCLK)
tsut (XCLK-CX0 to 11)
tht (XCLK-CX0 to 11)
tsut (XCLK-SPIX)
tht (XCLK-SPIX)
CX0 to 11
SPIX
tk (XCLK-PEUPE)
PEUPE
tPLH (XCLK-RPIX)
tPHL (XCLK-RPIX)
RPIX
50%
50%