USB Switch ICs

DPDT Type (Double Pole Double Throw)

BD11600NUX

No.11103EAT03

● Description

BD11600NUX is DPDT analog switches handling with USB2.0 high-speed that have both a low resistance and a low capacitance. Moreover, this is widely guaranteed from 2.5V to 5.5V as for the range of the power-supply voltage.
This has a low consumption mode by making OE "H" and the multi-selector by making the combination of OE "L" and S.
The electrostatic discharge protection circuit is built-in in all terminals.

● Features

1) VCC Operation from 2.5V to 5.5V.
2) 3Ω switches between the input to the output.
3) Low Capacity 2ch Analog SW.
4) 10-Pin SON Package. (3.0mm x 2.0mm, Height=0.6mm, 0.5mm pitch)

● Applications

Digital Still Cameras, Digital Video Camcorders, Portable Navigation Devices, TV, Portable DVD Players, Portable Game Systems, Personal computers, PDA, Mobile phones

● Line up matrix

Parameter	BD11600NUX	BD11601NUX
Supply Quiescent Current	18 μA	
Input voltage range	2.5～5.5 V	
Switch ON Resistance (VIN=0 V)	3 Ω	2.5 Ω
Switch ON Capacitance	6 pF	
Configuration	DPDT	DPST
Package	VSON010X3020	VSON008X2020

● Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Conditions
Input supply voltage	Vmax	-0.5～7.0	V	D+,D-,1D+,1D-,2D+,2D- Pins
Input supply voltage	Vmax	-0.3～7.0	V	Other Pins
Power dissipation	Pd	1.925	W	*1
Operating temperature range	Topr	-40～+85	℃	
Storage temperature range	Tstr	-55～+150	℃	

*1 When using more than at Ta=25℃, it is reduced 15.4 mW per 1℃. ROHM specification board 70mm×70mm mounting.

● Operating conditions (Ta=-40～+85℃)

Parameter	Symbol	Ratings	Unit	Conditions
Input voltage range (VCC)	VCC	2.5～5.5	V	

* This product does not especially designed to be protected from radioactivity.

●Electrical characteristics (Unless otherwise noted, Ta = 25°C, VCC=5.0V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Supply Quiescent Current 1	ICC1	-	1	3	μA	SW1, 2=OFF
Supply Quiescent Current 2	ICC2	-	18	40	μA	SW1=ON
Supply Quiescent Current 3	ICC3	-	19	40	μA	SW2=ON
Switch ON Resistance 1 (SW1, 2)	Ron1	-	3	6	Ω	VIN=0V
Switch ON Resistance 2 (SW1, 2)	Ron2	-	3.5	6	Ω	VIN=2.4V
Off-Leakage Current	Ioff	-2	0	2	μA	SW1, 2=OFF
On-Leakage Current	Ion	-2	0	2	μA	VCC>VIN, SW1, 2=ON
Switch Input Range	VIN	-0.5	-	5.5	V	SW1, 2=ON
Switch OFF Capacitance (SW1, 2)	Coff	-	4	-	pF	
Switch ON Capacitance (SW1, 2)	Con	-	6	-	pF	
Input “L” level (S, $\overline{OE}$)	VIL	-	-	0.5	V	
Input “H” level (S, $\overline{OE}$)	VIH	1.1	-	-	V	

●Electrical characteristic curves (Reference data)

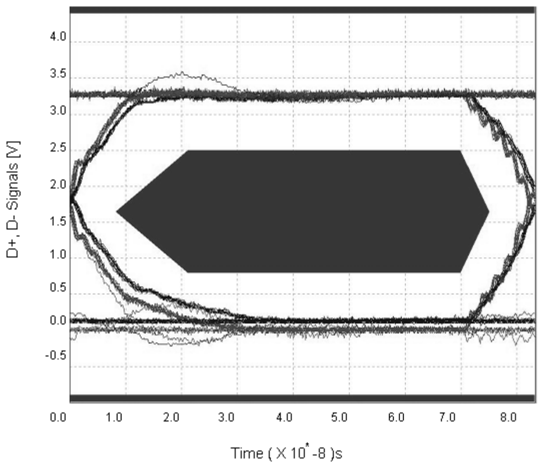


Fig.1
Eye Pattern Full Speed

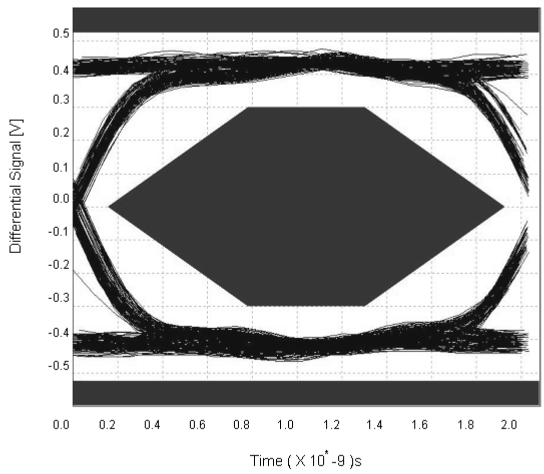


Fig.2
Eye Pattern High Speed

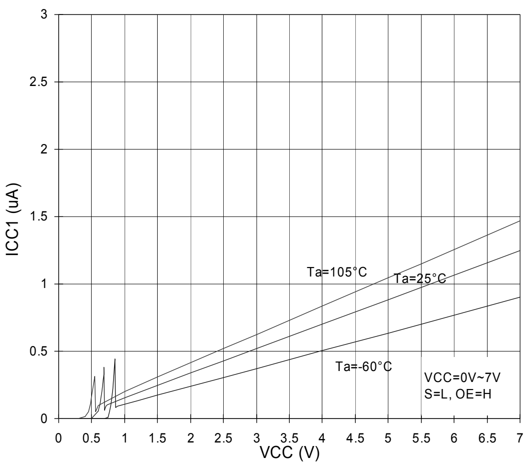


Fig.3
ICC vs Input Voltage (SW OFF)

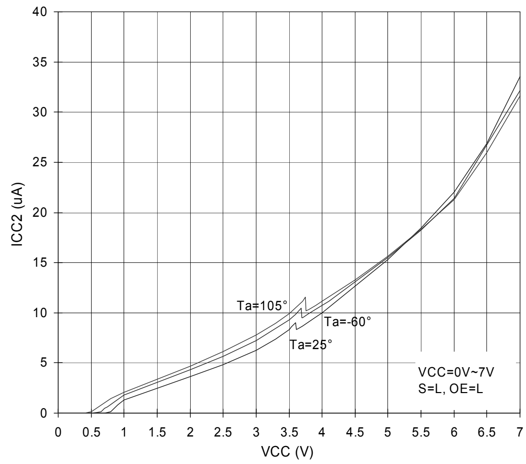


Fig.4
ICC vs Input Voltage (SW ON)

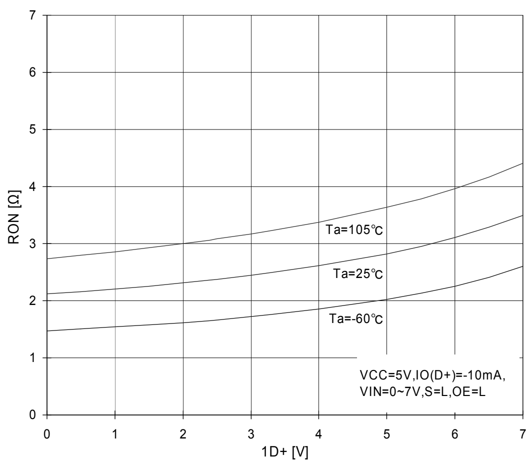


Fig.5
Ron vs Input Voltage

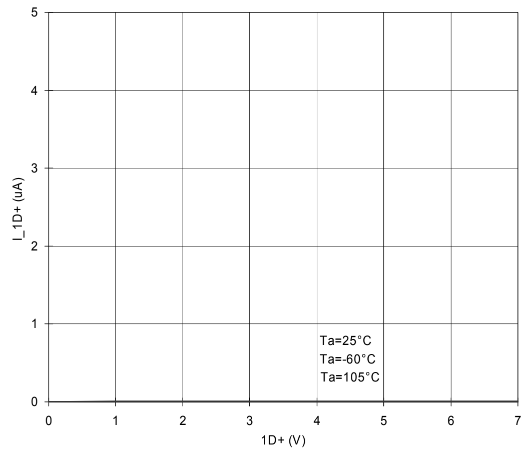


Fig.6
Leak current vs Input Voltage(SW OFF)

●Block diagram and pin configuration

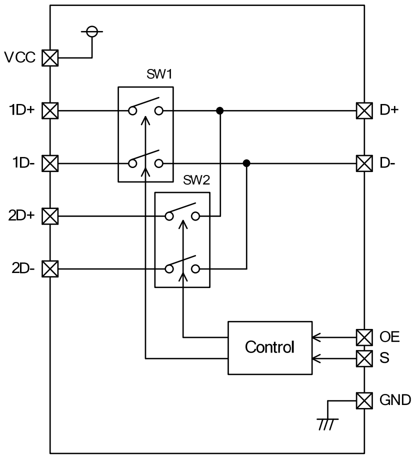


Fig.7
Block diagram

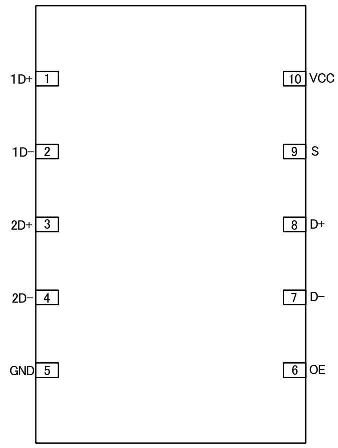


Fig.8
Pin configuration

●Package Dimensions

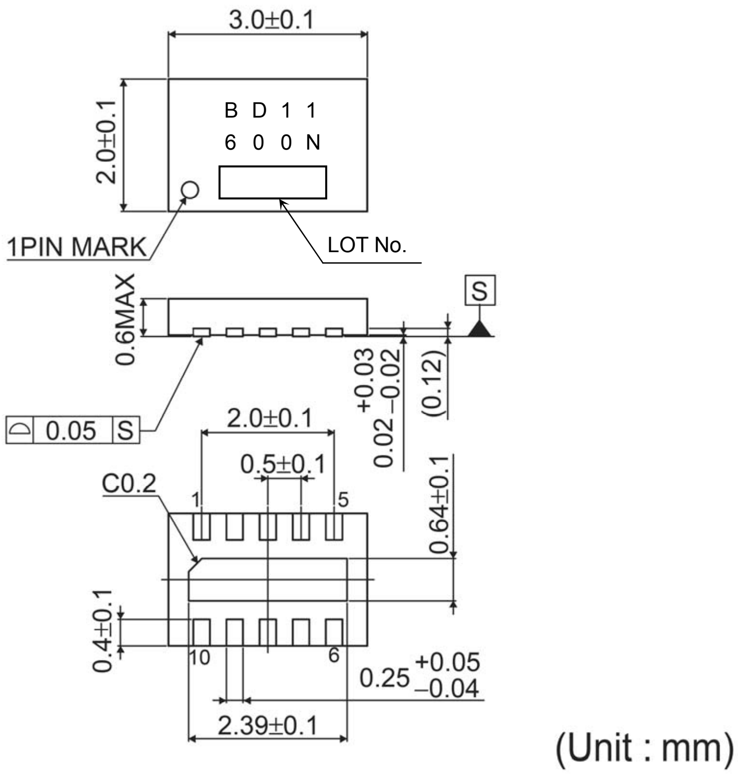


Fig.9
Package Dimensions

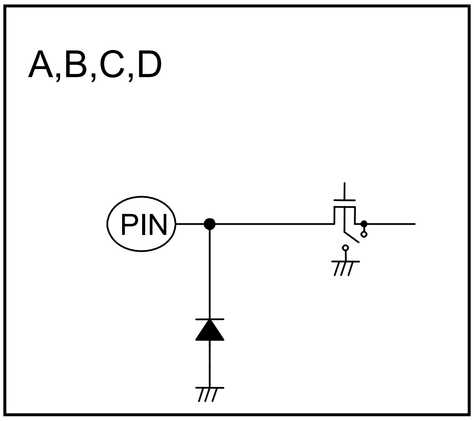
●Pin Description

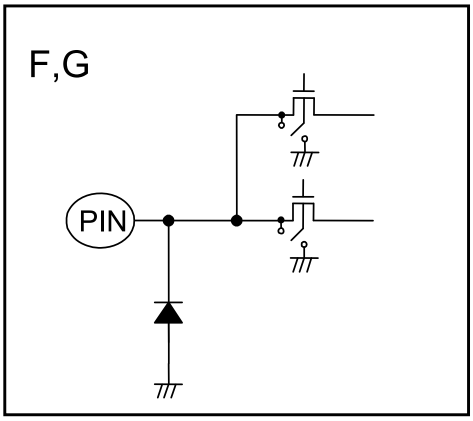
Pin NO.	Terminal circuit	Pin Name	I／O	Function
1	A	1D+	O	Analog SW terminal.
2	B	1D-	O	
3	C	2D+	O	
4	D	2D-	O	
5	-	GND	-	Ground Pin.
6	E	OE	I	Bus-Switch Analog Pin.
7	F	D-	I	Analog SW terminal.
8	G	D+	I	
9	H	S	I	Select Input Pin.
10	-	VCC	-	Power Supply.

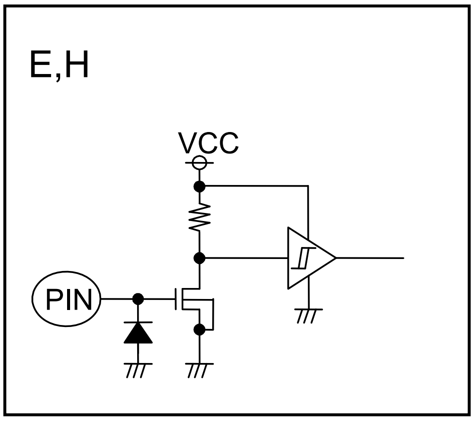
●Truth Table

$\overline{OE}$	S	SW1	SW2	Signal Pass
H	L	OFF	OFF	ALL OFF
H	H	OFF	OFF	ALL OFF
L	L	ON	OFF	1D+⇔D+, 1D-⇔D-
L	H	OFF	ON	2D+⇔D+, 2D-⇔D-

●Equivalent Circuit







●How to select parts of application

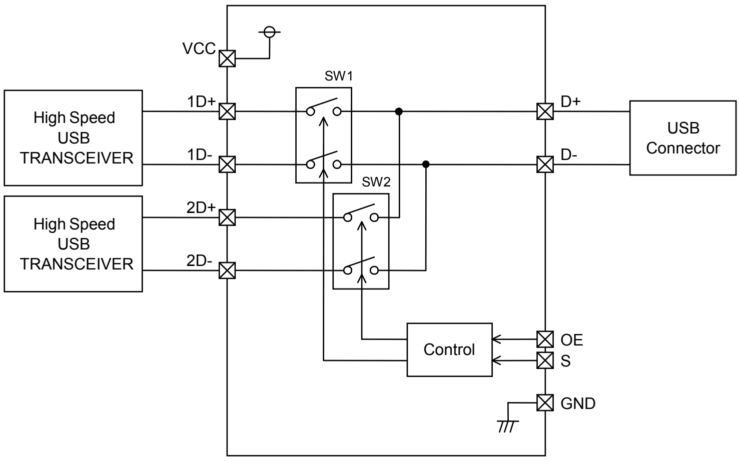


Fig.10
Application circuit of multi-USB TRANSCEIVER

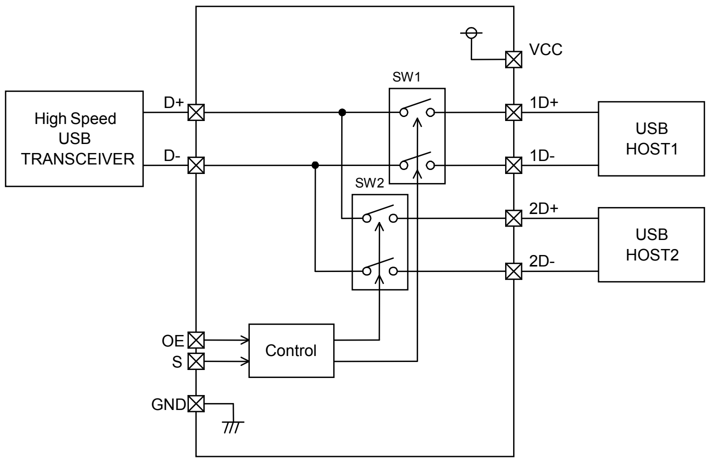


Fig.11
Application circuit of two communicating with two USB HOST

●Parameter Measurement Information

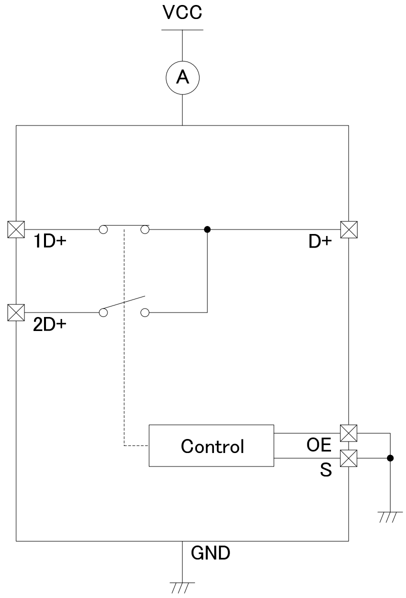


Fig.12
SW1 ON-State ICC

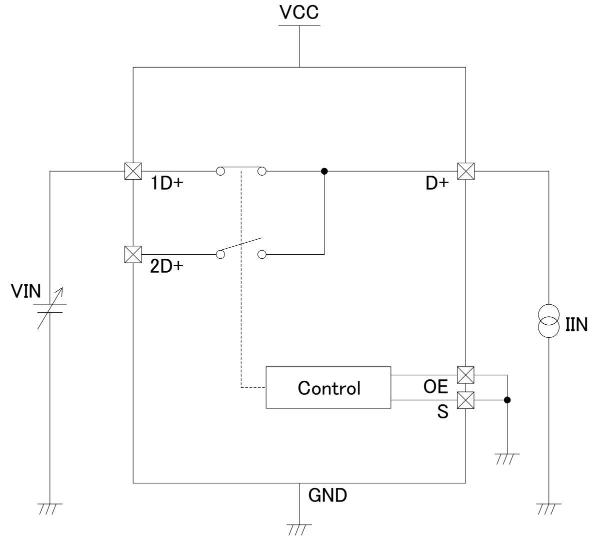


Fig.13
ON-State Resistance (Ron)

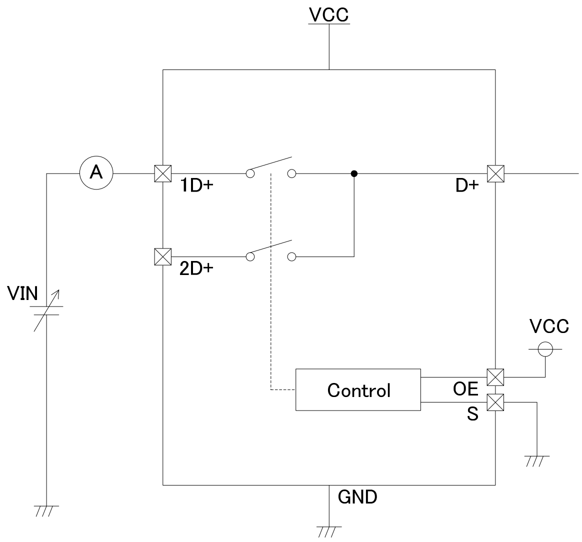


Fig.14
OFF-State Leakage current

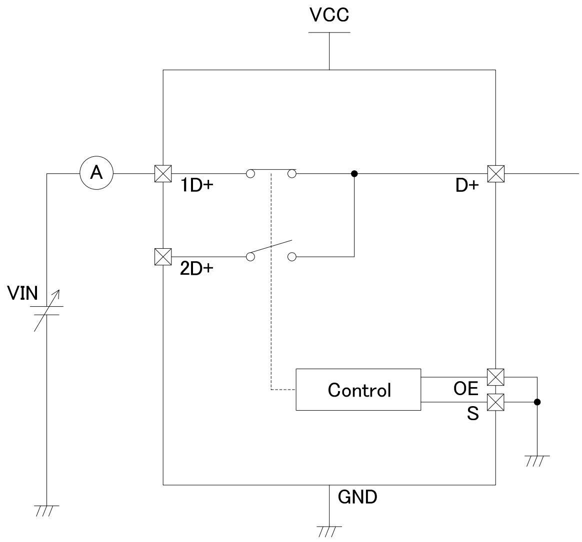


Fig.15
ON-State Leakage current

●Notes for use

(1) Absolute maximum ratings
If applied voltage (VCC), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range
This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector
There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines
In the design of the board pattern, make power supply and GND line wiring low impedance.
When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.
Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(5) GND voltage
Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation
When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(7) Operation in strong magnetic fields
Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board
When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins
Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(10) Ground wiring pattern
When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors
When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal design
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

●Power Dissipation

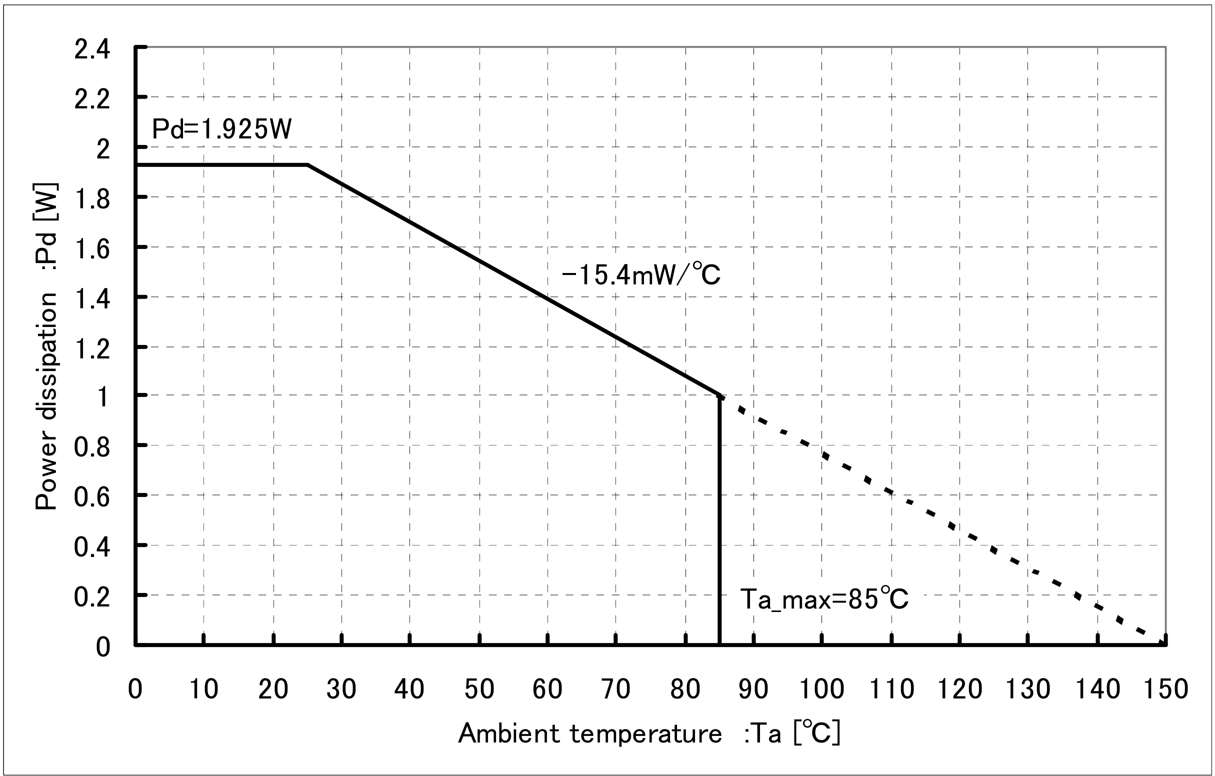


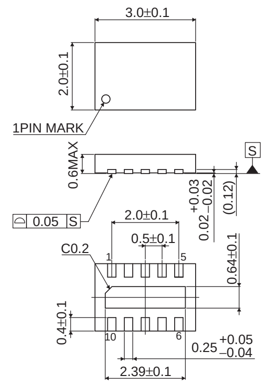
Fig.16
Power dissipation

● Ordering part number

B	D		1	1	6	0	0		N	U	X	-	E	2

- B D — Part No.
- 1 1 6 0 0 — Part No.
- N U X — Package NUX:VSON010X3020
- E 2 — Packaging and forming specification E2: Embossed tape and reel

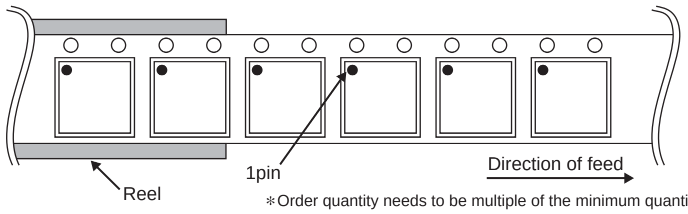
VSON010X3020



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

Notes

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