System Power Supply for TV Series

Built-in 1ch FET Synchronous Rectification Type DC/DC converters

BD8627EFV

●Description

BD8627EFV has realized the high performance and reliability required as a power supply for thin-screen TV.
With built-in FET 1ch current mode control, the DC/DC Converter series has the advantage of high-speed load response and wide phase margin.
Due to the high-speed load response, it is most suitable for TV-purpose processors with increasingly high performance, and due to the wide phase margin it leaves a good margin for board pattern & constant setting and so facilitates its application design.
As a high-reliability design, it has various built-in protection circuits (overcurrent protection, output voltage abnormal protection, thermal protection, and off-latch function at the time of abnormality etc.), therefore as an advantage it does not easily damage in every possible abnormal condition such as all-pin short circuit test etc. and hence most suitable for thin-screen TV which requires the high reliability.

●Features

1) High efficiency in all load area
2) 3.0A output current
3) Low RDS(ON) internal switches (PchMOS:85mΩ, NchMOS:65mΩ)
4) ±1% reference voltage accuracy
5) Programmable frequency : 250kHz-1MHz
6) Terminal RT OPEN/SHORT detecting function
7) Over current protection function
8) Output over voltage/low voltage protection function (over : FB > VREF +60mV , low : FB < VREF -60mV)
9) Timer off latch function in abnormal circumstances
10) Thermal shutdown function
11) Under voltage protection
12) Soft start/start delay circuit
13) Soft start time out function
14) HTSSOP-B20 package

Aug. 2008

●ABSOLUTE MAXIMUM RATING （Ta=25℃）

Parameter	Symbol	Limits	Unit
Input supply voltage	V_{IN}	7	V
Input terminal voltage	V_{INP} *1	V_{IN}	V
Output terminal voltage	V_{OUT} *2	V_{IN}	V
Output current	I_{OUT}	4	A
Power dissipation	Pd	3.2*3	W
Operating temperature	Topr	-10 ～ 85	℃
Storage temperature	Tstg	-55 ～ 150	℃

＊1 V_{INP} Application terminal： EN, SS/DELAY, TEST, FB

＊2 V_{OUT} Application terminal： SW, PDET, FC, RT, REG

＊3 (70mm×70mm, thickness 1.6mm, and four layer glass epoxy substrates)
When mounting substrate and the package back exposure part are connected with solder.
Operating at higher than Ta=25℃, 25.6mW shall be reduced per 1

Operation condition

Parameter	Symbol	MIN	TYP	MAX	Unit
Input supply voltage	V_{IN}	4.5	-	6.0	V
Output current	I_{OUT}	-	-	3.0	A

● Electrical characteristic

(Unless otherwise noted Ta=25℃, V_{IN}=5.6V)

Parameter	Symbol	Specification value			UNIT	Condition
		MIN	TYP	MAX		
VIN supply current (operating)	I_{Q_active}	-	1.3	2.0	mA	V_{FB} = 0.83V, V_{FC} = 1V
VIN supply current (standby)	I_{Q_stby}	-	350	700	μA	V_{EN} = 0V
Reference voltage (VREF)	V_{REF}	0.792	0.8	0.808	V	
Output rise detection voltage	V_{OVP}	30	60	90	mV	Monitoring FB terminal
Output decrease detection voltage	V_{LVP}	-90	-60	-30	mV	Monitoring FB terminal
Terminal PDET output current	I_{PDET}	1	-	-	mA	V_{PDET}< 0.5V
Oscillation frequency	f_{OSC}	500	550	600	kHz	R_{OSC} = 220kΩ
Pch FET ON resistance	R_{PFET}	-	85	120	mΩ	I_{SW} = 1A
Nch FET ON resistance	R_{NFET}	-	65	100	mΩ	I_{SW} = -1A
UVLO voltage	V_{UVLO}	3.8	4.0	4.2	V	
SW leak current	I_{LSW}	-	0	1	μA	V_{EN}= 0V, V_{IN} = 6V
EN terminal H threshold voltage	V_{ENH}	2.0	-	-	V	
EN terminal L threshold voltage	V_{ENL}	-	-	0.5	V	
SS/DELAY terminal source current	I_{SSSO}	2	4	6	μA	

V_{FB}:FB terminal voltage, V_{EN} :EN terminal voltage, V_{FC} :FC terminal voltage, V_{PDET}: PDET terminal voltage

Current capability should not exceed Pd.

Permissible loss

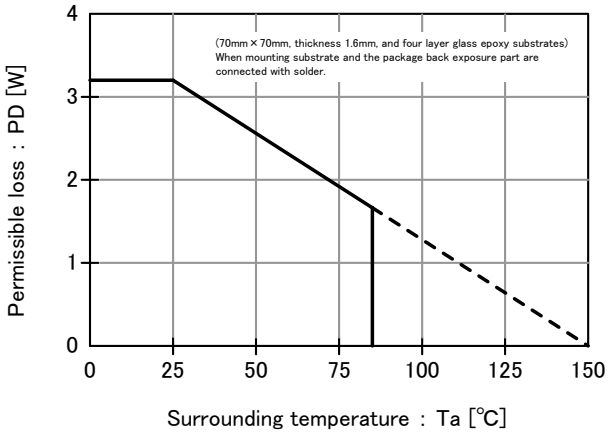


Fig. 1 heat decrease curve

● Block Diagram

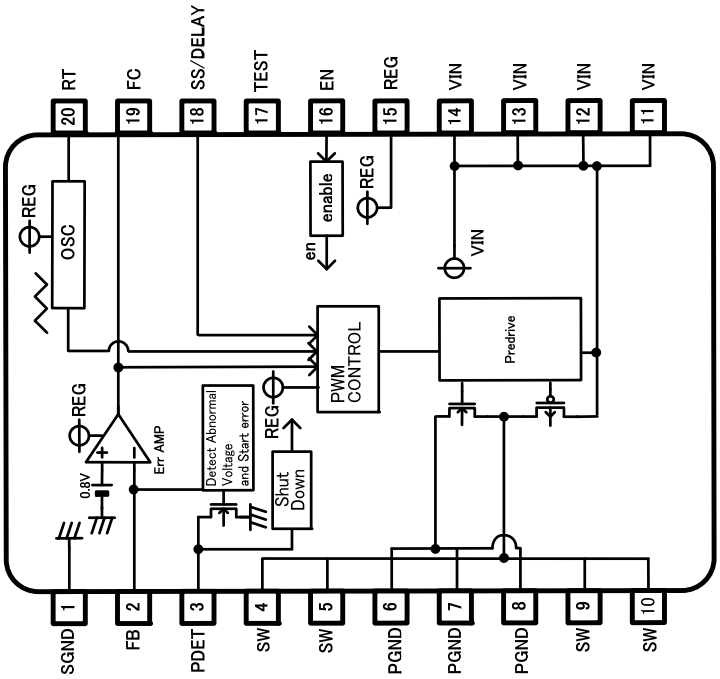
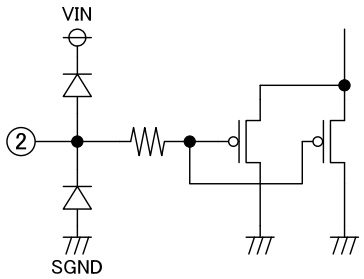
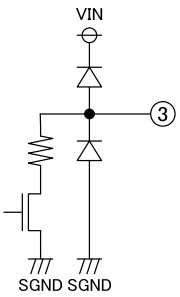
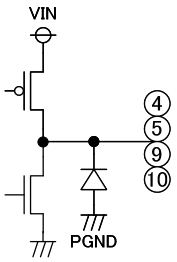


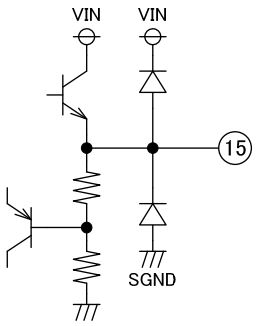
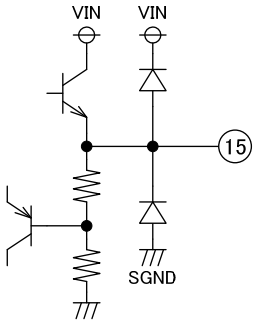
Fig.2 Block diagram

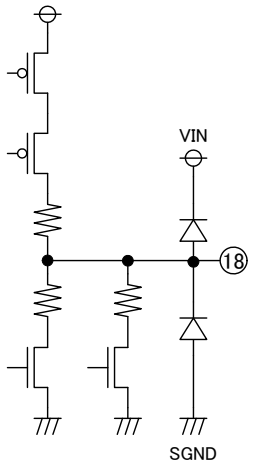
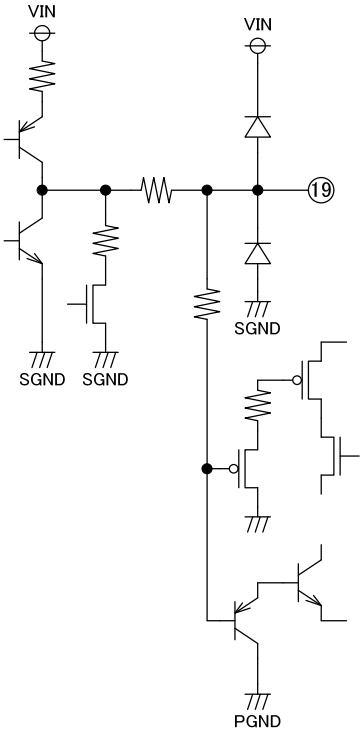
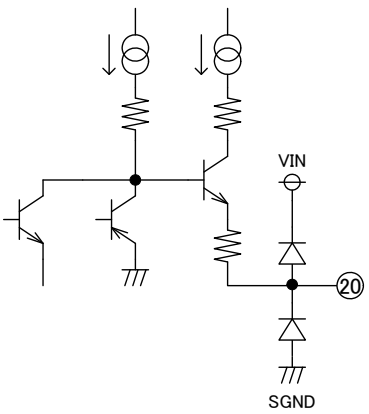
● Pin description

No.	Symbol	Description	Explanation
1	SGND	Signal GND terminal	Small signal system GND
2	FB	Feed back terminal	Output voltage detection
3	PDET	Off latch signal output	Reset output
4	SW	Output terminal	Switching output
5	SW		
6	PGND	Power GND terminal	GND for power MOSFET
7	PGND		
8	PGND		
9	SW	Output terminal	Power Mos output
10	SW		
11	VIN	Power supply input terminal	Power supply input. The decoupling is done to PGND
12	VIN		
13	VIN		
14	VIN		
15	REG	Internal regulator	Internal regulator
16	EN	Enable input	ON/OFF control for device operation
17	TEST	TEST terminal	GND short in application set
18	SS/DELAY	Soft start adjustment capacity connection terminal	The soft start time is adjusted with the connected capacitor
19	FC	Error amplifier output	Error amplifier phase compensation point
20	RT	Frequency adjustment resistance connection terminal	The switching frequency is set by the connected resistance

● Pin equivalence circuit diagram

No.	Symbol	Explanation	Terminal equivalent circuit diagram
1	SGND	GND (connected 0V)	
2	FB	Output voltage detection terminal	
3	PDET	Off latch signal output terminal	
4,5,9,10	SW	Output terminal	
6,7,8	PGND	Power GND (Same voltage as SGND)	
11,12,13,14	VIN	Power supply input terminal	

No.	Symbol	Explanation	Terminal equivalent circuit diagram
15	REG	Internal regulator output terminal	
16	EN	Enable terminal	

No.	Symbol	Explanation	Terminal equivalent circuit diagram
18	SS	Soft start time adjustment terminal	
19	FC	Error amplifier compensation terminal	
20	RT	Oscillator frequency adjustment terminal	

● Operation description

Enable control

The device can be controlled ON/OFF by EN terminal (16 pin) voltage.
An internal circuit starts when VEN reaches 0.65V.

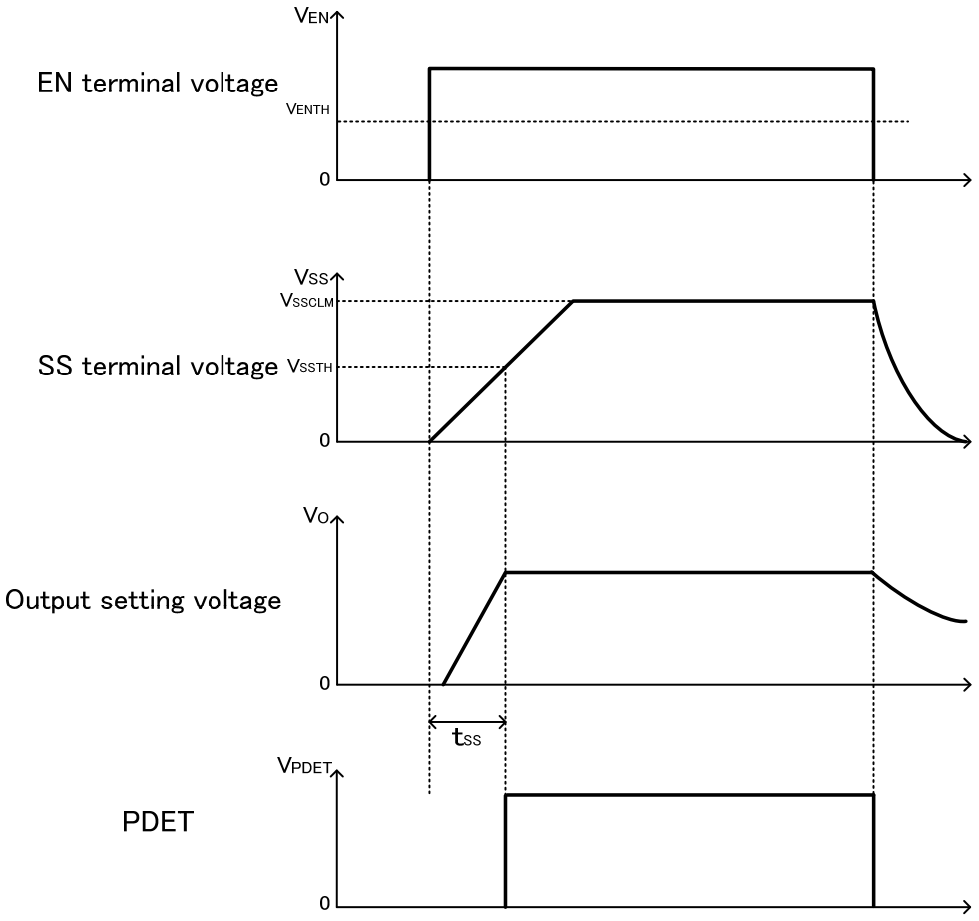


Fig. 3 ON/OFF transition wave form in EN controlling

Soft start time set function

As for BD8627EFV, output can do soft start without overshoot by charging soft start capacity (CSS) connected between SS and SGND terminal.
Also, soft start time (tss) can be set by setting soft start capacity (CSS) arbitrarily.

OSC oscillation frequency setting function

The output oscillation frequency can be set by connecting resistance between terminal RT (20 pins) and SGND (range = 250kHz - 1MHz)

The relation between RT terminal resistance and the oscillation frequency follows Fig.4.

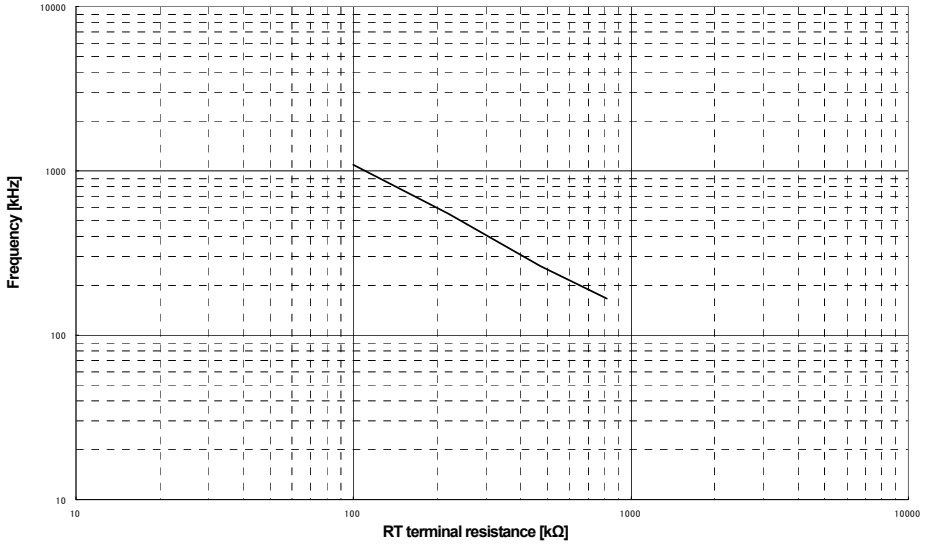


Fig. 4 RT resistance-oscillation frequency

● Protection function

Protection circuit is effective for destruction prevention due to accident so that avoid using under continuous protection operation.

Low voltage protection function (LVP)

The voltage of the terminal FB (2 pins) is compared with internal reference voltage VREF.

If FB terminal voltage falls below V_{LVP}(= VREF -60mV) and the state continues for 500us, output changes to low voltage and the state is fixed. In that case , PDET (3pin) output changes to L.

Table 4-1 output low voltage protection function

EN terminal	SS terminal	FB terminal	Low voltage protection function	Low voltage protection operation
$>V_{IHEN}$	>1.4V(typ)	$<V_{LVP}$	Effective	ON
		$>V_{LVP}$		OFF
	<1.4V(typ)	-	Invalidity	OFF
$<V_{ILEN}$	-	-	Invalidity	OFF

＊ Low voltage protection function is available when SS terminal voltage becomes more than 1.4V (typ) in the transition to ON control (during soft start).

Over voltage protection function(OVP)

The voltage of the terminal FB is compared with internal reference voltage VREF.

If FB terminal voltage is over Vovp (=VREF +60mV) and the state is continues for 500usec, output changes to low voltage and the state is fixed.

Table 4-2 output over voltage protection function

EN terminal	SS terminal	FB terminal	Over voltage protection function	Over voltage protection operation
$>V_{IHEN}$	>1.4V(typ)	$>V_{OVP}$	Effective	ON
		$<V_{OVP}$		OFF
	<1.4V(typ)	-	Invalidity	OFF
$<V_{ILEN}$	-	-	Invalidity	OFF

＊ Over voltage protection function is available when SS terminal voltage becomes more than 1.4V (typ) in the transition to ON control (during soft start).

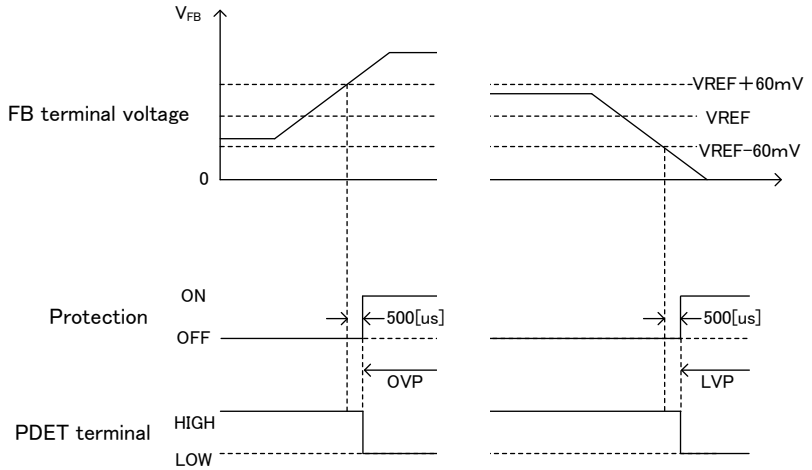


Fig. 5 Output voltage error detection range

Under voltage lock out protection (UVLO)

As for BD8627EFV, the power-supply voltage decrease detection protection circuit is built in.
It the input voltage decrease below the UVLO voltage (4.0V typ), the device state changes to the standby mode (Moreover, to prevent the chattering of the output) hysteresis width of 300mV(typ) has been installed in the UVLO cancel voltage.

RT terminal open/short protection function (RTO/RTS)

RT terminal opening/short protection function prevent the clock from abnormal oscillation.
If RT terminal open/short protection function is detected, output voltage changes to low level and is fixed.

Terminal RT opening/short protection function is always effective after the power supply start-up.
Terminal RT opening/short protection function is available if the state continue for 500usec, abnormal detection operates when the state continues about 500μsec(typ).

Soft start time-out function

If VSS doesn't exceed VSSTH within 64msec (typ) since a soft start began, BD8627EFV controls an off latch.
Vo is fixed in a low level.

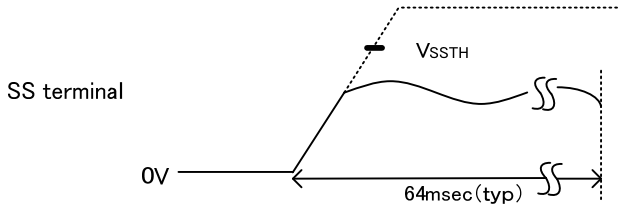


Fig. 6 Soft start time-out

Error detection (off latch) release method

BD8627EFV enters the state of an off latch when the protection function operates.
To release the off latch state, EN terminal voltage should be changed to low level once time.

Thermal shut down function

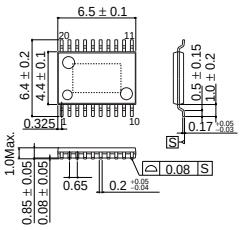
Thermal shut down circuit (TSD circuit) is built into BD8627EFV. When the temperature of the chip exceeds Tjmax=175, the DC/DC converter is fixed in a low voltage.
TSD function is aimed to shut down IC from thermal reckless driving under an abnormal state to exceed Tjmax=175. It aims at neither protection nor the guarantee of the set. Therefore, please do not use this function to protect the set.

Over current protection function

The over current protection function has been achieved by limiting the current that flows on high side MOSFET.
The current is controlled in every one cycle of the switching frequency. When an abnormal state continues for about 500μsec(typ), the output is fixed in a low level.

HTSSOP-B20

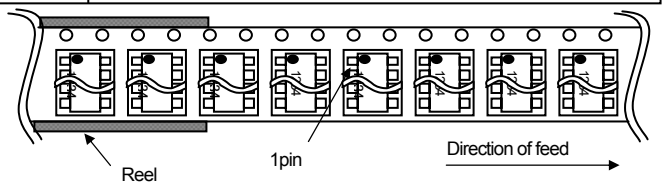
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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Published by
KTC LSI Development Headquarters
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