AK8858

PS/SD Multi Format Video Decoder

Overview

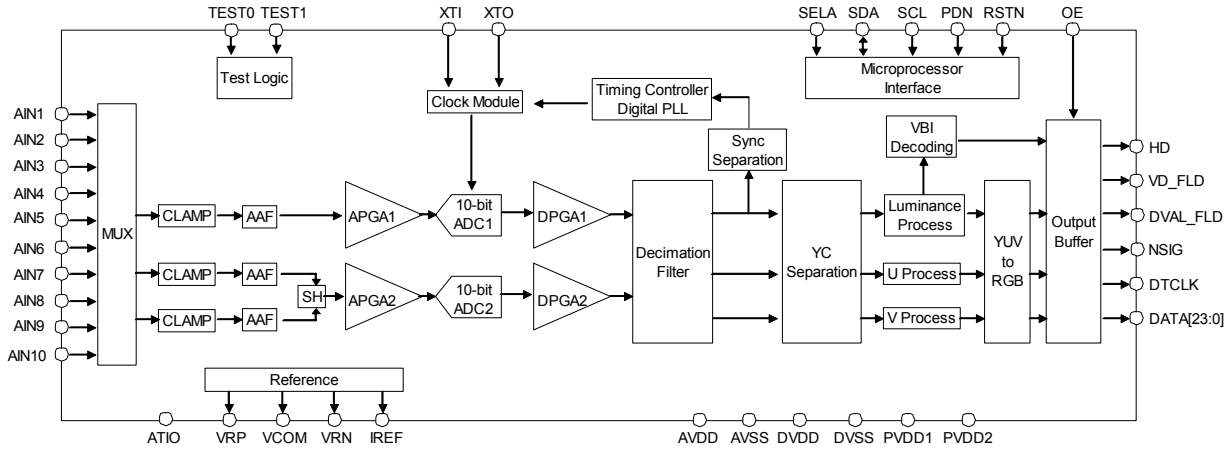
The AK8858 is a single-chip digital video decoder for composite, s-video, 525i/625i component and 525p/625p component video signals. Its output data is in YCbCr and RGB format. Its pixel clock is generated internally and synchronized with the input signal. Microprocessor access is via I2C interface.

Features

- Decodes composite and S-Video signals NTSC/ PAL-B, D, G, H, I, N, Nc, M, 60 /SECAM
- Decode 525i / 625i YPbPr component video signals
- Decode 525p / 625p YPbPr component video signals
- 10 input channel
- 10-bit 54MHz ADC 2 channel
- Internally built PLL
- Internal analog bandwidth filter
- Programmable Gain Amp (PGA) (-3.25dB～10dB)
- Adaptive automatic Gain Control (AGC)
- Auto Color Control (Composite and S-Video signals)
- Image adjustment (Contrast, Brightness, Saturation, HUE, Sharpness)
- Automatic input signal detection (NTSC/ PAL/ SECAM detect、Interlace/ Progressive detect)
- Adaptive 2-D Y/C separation
- Output data format
  YCbCr 4:2:2 or RGB 8:8:8
- Output interface
  (YCbCr)
    Interlace: ITU-R BT.656 (8bit 27MHz) and 16bit 13.5MHz with EAV/ SAV
    Progressive: 16bit 27MHz and 8bit 54MHz with EAV/ SAV
  (RGB)
    Interlace: 8bit:8bit:8bit 13.5MHz with EAV/ SAV
    Progressive: 8bit:8bit:8bit 27MHz with EAV/ SAV
  *EAV/ SAV output can be disabled via register
- HD, VD, DVALID and FIELD (VD, DVALID, FIELD can be select up to 2 output via register setting)
- Closed Caption / WSS / CGMS-A signal decoding (output via register).
- Macrovision signal detection (Rovi certification)
- I2C control
- Powerdown function
- Internal VREF
- Core supply voltage: 1.70~2.00V
- I/O power supply: 1.70~3.60V
- Operating temperature: −40°C~105°C
- 80-pin LQFP package (12.0mm x 12.0mm)

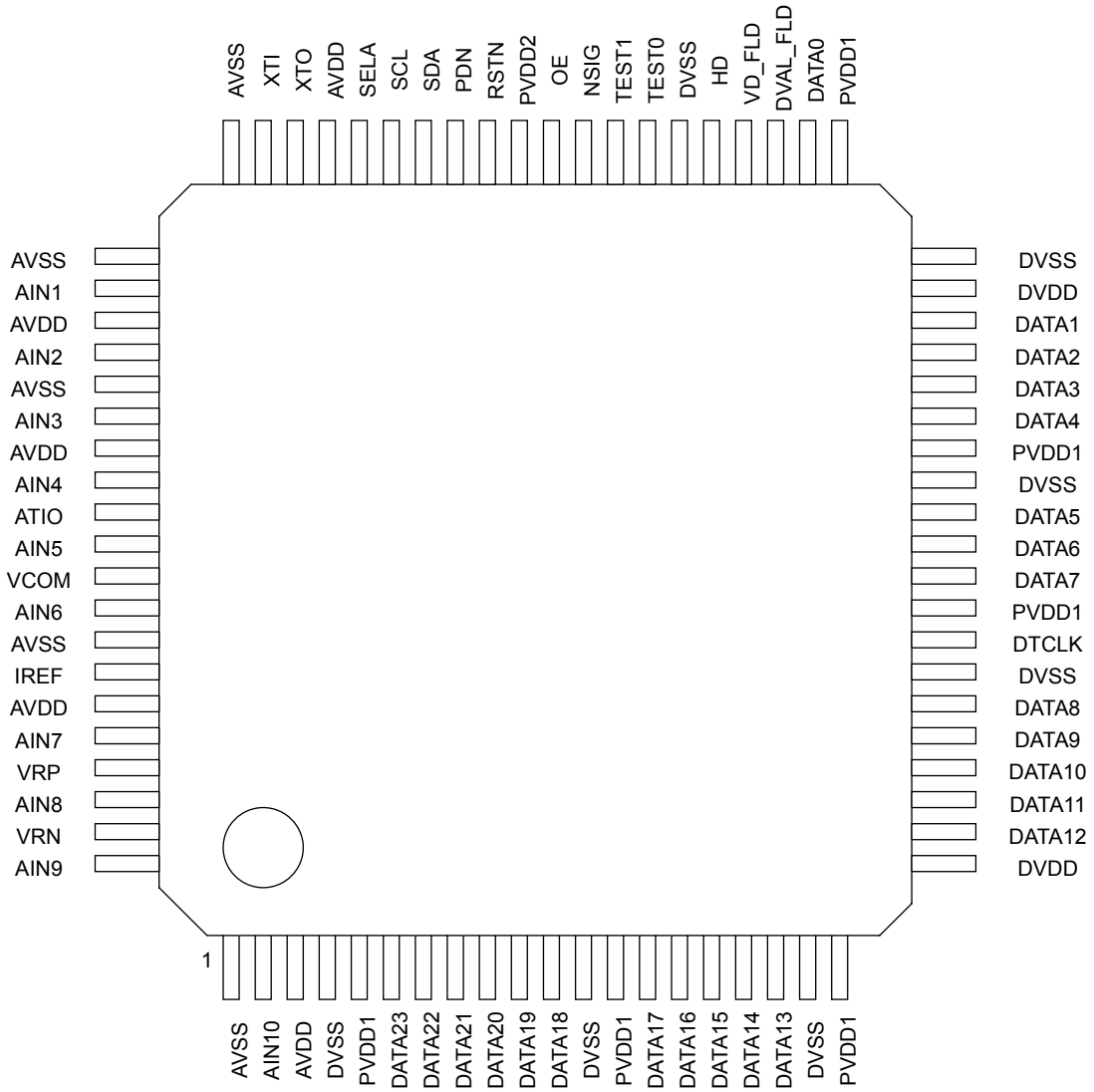
Features

[1] Functional block diagram



[2] Pin assignment

80-pin LQFP package (12.0mm x 12.0mm)



[3] Pin function description

[3.1] Pin function

Pin No.	Symbol	P/S	I/O	Functional Description
1	AVSS	A	G	Analog ground pin.
2	AIN10	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
3	AVDD	A	P	Analog power supply pin.
4	DVSS	D	G	Digital ground pin.
5	PVDD1	P1	P	I/O power supply pin.
6	DATA23	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
7	DATA22	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
8	DATA21	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
9	DATA20	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
10	DATA19	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
11	DATA18	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
12	DVSS	D	G	Digital ground pin.
13	PVDD1	P1	P	I/O power supply pin.
14	DATA17	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
15	DATA16	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
16	DATA15	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
17	DATA14	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
18	DATA13	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
19	DVSS	D	G	Digital ground pin.
20	PVDD1	P1	P	I/O power supply pin.
21	DVDD	D	P	Digital power supply pin.
22	DATA12	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
23	DATA11	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
24	DATA10	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
25	DATA9	P1	O	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1)
26	DATA8	P1	O	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1)

[Power supply] A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[Input/Output] I: intput pin, O: output pin, I/O: input/output pin, P: power supply pin, G: ground connection pin

(*1)See {[3.2] Output pin state} for relation of output to OE/PDN and RSTN pin status.

Pin No.	Symbol	P/S	I/O	Functional Description
27	DVSS	D	G	Digital ground pin.
28	DTCLK	P1	O	Data clock output pin.(*1)
29	PVDD1	P1	P	I/O power supply pin.
30	DATA7	P1	O	DATA output pin.(*1)
31	DATA6	P1	O	DATA output pin.(*1)
32	DATA5	P1	O	DATA output pin.(*1)
33	DVSS	D	G	Digital ground pin.
34	PVDD1	P1	P	I/O power supply pin.
35	DATA4	P1	O	DATA output pin.(*1)
36	DATA3	P1	O	DATA output pin.(*1)
37	DATA2	P1	O	DATA output pin.(*1)
38	DATA1	P1	O	DATA output pin.(*1)
39	DVDD	D	P	Digital power supply pin.
40	DVSS	D	G	Digital ground pin.
41	PVDD1	P1	P	I/O power supply pin.
42	DATA0	P1	O	DATA output pin.(*1)
43	DVAL_FLD	P1	O (I/O)	DVALID/ FIELD signal output pin. DVALID signal output / FIELD signal output can be selected by register setting.(*1) If test mode, it is I/O pin.
44	VD_FLD	P1	O (I/O)	VD/ FIELD signal output pin VD signal output / FIELD signal output can be selected by register setting.(*1) If test mode, it is I/O pin.
45	HD	P1	O (I/O)	HD signal output pin.(*1) If test mode, it is I/O pin.
46	DVSS	D	G	Digital ground pin.
47	TEST0	P2	I	Pin for test mode setting. Connect to DVSS.
48	TEST1	P2	I	Pin for test mode setting. Connect to DVSS.
49	NSIG	P2	O	Shows status of synchronization with input signal Low: Signal present (synchronized). High: Signal not present or not synchronized.(*1)
50	OE	P2	I	Output Enable pin. Low: Digital output pin in Hi-z output mode. High: Data output mode. Hi-z input to OE pin is prohibited.
51	PVDD2	P2	P	Microprocessor I/F power supply pin.
52	RSTN	P2	I	Reset signal input pin. Hi-z input is prohibited. Low: Reset. High: Normal operation.
53	PDN	P2	I	Power-down control pin. Hi-z input is prohibited. Low: Power-down. High: Normal operation.
54	SDA	P2	I/O	I2C data pin. Connect to PVDD2 via a pull-up register. Hi-z input possible when PDN=L.
55	SCL	P2	I	I2C clock input pin. Connect to PVDD2 via a pull-up register. Hi-z input possible when PDN=L.
56	SELA	P2	I	I2C bus address selector pin. PVDD2 connection: Slave address [0x8A] DVSS connection: Slave address [0x88]
57	AVDD	A	P	Analog power supply pin.

[Power supply] A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[Input/Output] I: intput pin, O: output pin, I/O: input/output pin, P: power supply pin, G: ground connection pin

(*1)See {[3.2] Output pin state} for relation of output to OE/PDN and RSTN pin status.

Pin No.	Symbol	P/S	I/O	Functional Description
58	XTO	A	O	Crystal connection pin. Use 24.576 MHz crystal. When PDN=L, output level is AVSS. If crystal is not used, connect to NC or AVSS.
59	XTI	A	I	Crystal connection pin. Use 24.576 MHz crystal resonator. For input from 24.576 MHz crystal oscillator, use this pin.
60	AVSS	A	G	Analog ground pin.
61	AVSS	A	G	Analog ground pin.
62	AIN1	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
63	AVDD	A	P	Analog power supply pin.
64	AIN2	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
65	AVSS	A	G	Analog ground pin.
66	AIN3	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
67	AVDD	A	P	Analog power supply pin.
68	AIN4	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
69	ATIO	A	I/O	Aanalog test pin. For normal operation, connect to AVSS.
70	AIN5	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
71	VCOM	A	O	Common internal voltage for AD converter. Connect to AVSS via 0.1uF ceramic capacitor (±10%).
72	AIN6	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
73	AVSS	A	G	Analog ground pin.
74	IREF	A	O	Analog circuit reference current setting pin. Connect to AVSS via 6.8KΩ (±1% accuracy) resistor.
75	AVDD	A	P	Analog power supply pin.
76	AIN7	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
77	VRP	A	O	Internal reference positive voltage pin for AD converter. Connect to AVSS via 0.1uF ceramic capacitor (±10%).
78	AIN8	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
79	VRN	A	O	Internal reference negative voltage pin for AD converter. Connect to AVSS via 0.1uF ceramic capacitor (±10%).
80	AIN9	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 107. If it is not used, connect to NC.

[Power supply] A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[Input/Output] I: intput pin, O: output pin, I/O: input/output pin, P: power supply pin, G: ground connection pin

(*1)See {[3.2] Output pin state} for relation of output to OE/PDN and RSTN pin status.

[3.2] Output pin state

Relation of output to OE/PDN and RSTN pin status.

OE	PDN	RSTN	DATA[23:0], DTCLK, HD, VD_FLD, DVAL_FLD	NSIG
L	x	x	Hi-Z output	L output
H	L		L output	L output
H	H	L	L output	L output
		H	DOUT	DOUT

(x: Don't care, DOUT: Data output)

State of DATA pin except for RGB 8:8:8 format output

YCbCr8bit output			YCbCr16bit output		
DATA[23:16]	DATA[15:8]	DATA[7:0]	DATA[23:16]	DATA[15:8]	DATA[7:0]
Low output	Low output	DOUT	Low output	DOUT	DOUT

(DOUT: Data output)

In the absence of AIN signal input, output will be black data (Y=0x10, Cb/Cr=0x80).
(Blueback output can be obtained by register setting). *(Sub Address: 0x0D [3:2])

[4] Electrical specifications

[4.1] Absolute maximum ratings

Parameter	Min	Max	Unit	Notes
Supply voltage DVDD, AVDD PVDD1, PVDD2	 −0.3 −0.3	 2.2 4.2	 V V	
Analog input pin voltage A (VinA)	−0.3	AVDD + 0.3 (≤ 2.2)	V	(*1)
Digital input pin voltage P1 (VioP1)	−0.3	PVDD1 + 0.3 (≤ 4.2)	V	(*2)
Digital output pin voltage P2 (VioP2)	−0.3	PVDD2 + 0.3 (≤ 4.2)	V	
Input pin current (IIn)	−10	10	mA	Power supply pin is not included
Storage temperature	−40	150	°C	

(*1) DTCLK, DATA [23:0], HD, VD_FLD, DVAL_FLD

(*2) OE, SELA, PDN, RSTN, SDA, SCL, NSIG, TEST0, TEST1

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).
All power supply grounds (AVSS, DVSS) should be at the same electric potential.
If digital output pins are connected to data bus, the data bus operating voltage should be in the same range as shown above from the digital output pin.
The setting other than above may cause the eternal destruction to the deivce.
Normal operational is not guaranteed for the above setting.

[4.2] Recommended operating conditions

Parameter	Min	Typ	Max	Unit	Condition
Analog supply voltage (AVDD) Digital supply voltage (DVDD)	1.70	1.80	2.00	V	AVDD = DVDD
MPU I/F supply voltage (PVDD1) Data output i/F supply voltage (PVDD2)	1.70	1.80	3.60	V	PVDD1 ≥ DVDD PVDD2 ≥ DVDD
Operating temperature (Ta)	−40		85	°C	

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).
All power supply grounds (AVSS, DVSS) should be at the same electric potential.

[4.3] DC characteristics

(Ta: −40°C~85°C / DVDD=AVDD=1.7V~2.0V / PVDD1=DVDD~3.6V / PVDD2=DVDD~3.6V)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Digital P2 input high voltage(*1)	VPIH	0.8PVDD2			V	PVDD2<2.7V
		0.7PVDD2			V	PVDD2≥2.7V
Digital P2 input low voltage(*1)	VPIL			0.2PVDD2	V	PVDD2<2.7V
				0.3PVDD2	V	PVDD2≥2.7V
XTI input high voltage	VXIH	0.8AVDD				
XTI input low voltage	VXIL			0.2AVDD		
Digital input leak current(*1)	IL			±10	uA	
Digital P1 output high voltage(*2)	VOH1	0.7PVDD1			V	IOH1 = −600uA
Digital P1 output low voltage(*2)	VOL1			0.3PVDD1	V	IOL1 = 1mA
Digital P1 output Hi-z leak current (*2)	HIL			±10	uA	
NSIG output high voltage	VOH2	0.7PVDD2			V	IOH2 = −600uA
NSIG output low voltage	VOL2			0.3PVDD2	V	IOL2 = 1mA
I2C(SDA)L output	VOLC			0.4 0.2 PVDD2	V	IOLC = 3mA PVDD2≥2.0V PVDD2<2.0V

(*1) Collective term for SDA, SCL, SELA, OE, PDN, RSTN, TEST0 and TEST1 pins.

(*2) Collective term for DTCLK, DATA [23:0], HD, VD_FLD and DVAL_FLD pins.

[4.4] Analog characteristics

(AVDD=1.8V, Ta=25˚C)

[4.4.1] Input Range

Parameter	Symbol	Min	Typ	Max	Units	Condition
Input range	VIMX	0		0.60	Vpp	

[4.4.2] AAF (Anti-Aliasing Filter)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Pass band ripple	Gp	−1		+1	dB	Progressive signal: ~12MHz Interlace signal: ~6MHz
Stop band blocking	Gs	20	30		dB	Progressive signal: 54MHz Interlace signal: 27MHz

[4.4.3] Analog PGA

Parameter	Symbol	Min	Typ	Max	Units
Resolution	RES		2		bit
Minimum gain	GMN		-3		dB
Maximum gain	GMX		6		dB
Gain step	GST	2.75	3	3.25	dB

[4.4.4] ADC

Parameter	Symbol	Min	Typ	Max	Units	Condition
Resolution	RES		10		bit	
Operating clock frequency	FS		54		MHz	Progressive decode : Y signal
			27			Interlace decode : Y signal Progressive decode : PbPr signal
Intergral nonlinearity	INL		±1.0	±2.0	LSB	
Differential nonlinearity	DNL		±0.5	±1.0	LSB	
S/N	SN		53		dB	Fin=1MHz*, FS=54MHz, PGA GAIN default setting
S/(N+D)	SND		52		dB	Fin=1MHz*, FS=54MHz PGA GAIN default setting
Full scale Gain matching	IFGM			5	%	
ADC internal common voltage	VCOM		0.96		V	
ADC internal positive VREF	VRP		1.26		V	
ADC internal negative VREF	VRN		0.66		V	

*Fin = AIN input signal frequency

[4.4.5] Current consumption

(AVDD = DVDD = PVDD1 = PVDD2 = 1.8V, Ta = −40~85˚C)

Parameter	Symbol	Min	Typ	Max	Units	Condition
(Active mode)						
Total	IDD		110	151	mA	ADC 3ch operational(*1)
Analog block	AIDD		68		mA	ADC 3ch operational(*1)
			60		mA	YC: ADC 2ch operational(*2)
			35		mA	CVBS: ADC 1ch operational(*2)
Digital block	DIDD		28		mA	(*1) With crystal connected Load condition: CL=15pF
I/O block	PIDD		14		mA	
(Power down mode)						PDN=L(DVSS)(*3)
Total	SIDD		≤1	100	uA	
Analog block	ASIDD		≤1		uA	
Digital block	DSIDD		≤1		uA	
I/O block	PSIDD		≤1		uA	

(*1) Progressive YPbPr signal decode

(*2) Reference value

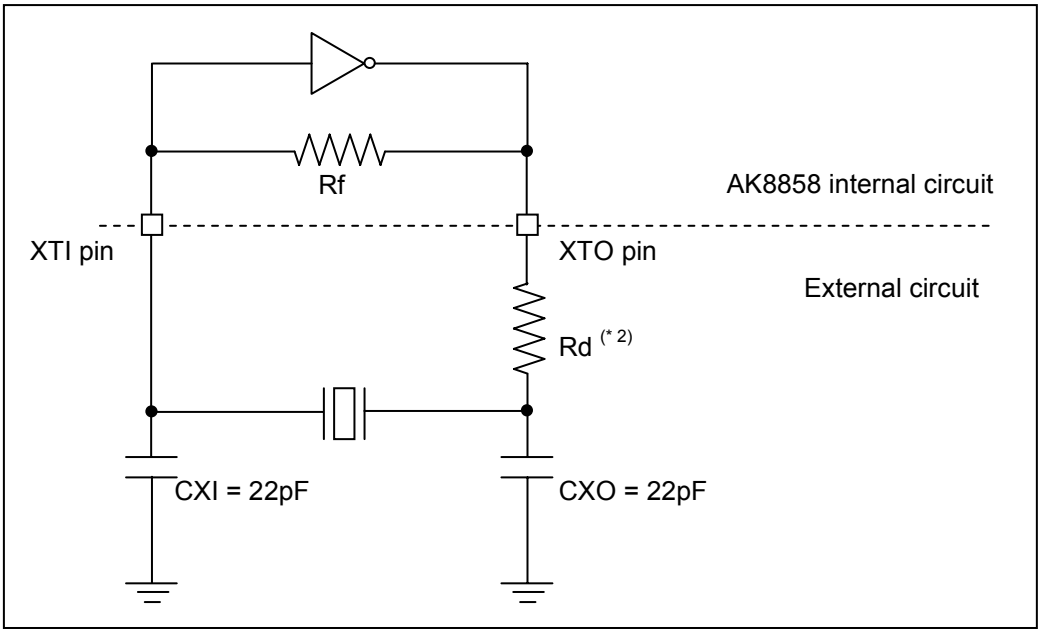
(*3) OE pin and RSTN pin must always be brought to the voltage polarity to be used or to ground level

[4.4.6] Crystal circuit block

Parameter	Symbol	Min	Typ	Max	Units	Notes
Frequency	f0		24.576		MHz	
Frequency tolerance	Δf / f			±100	ppm	
Load capacitance	CL		15		pF	
Effective equivalent resistance	Re			100	Ω	(*1)
Crystal parallel capacitance	CO		0.9		pF	
XTI terminal external connection load capacitance	CXI		22		pF	CL=15pF
XTO terminal external connection load capacitance	CXO		22		pF	CL=15pF

(*1) Effective equivalent resistance generally may be taken as Re = {R1 x (1+CO/CL)2}. (R1 is the crystal series equivalent resistance)

Example connection

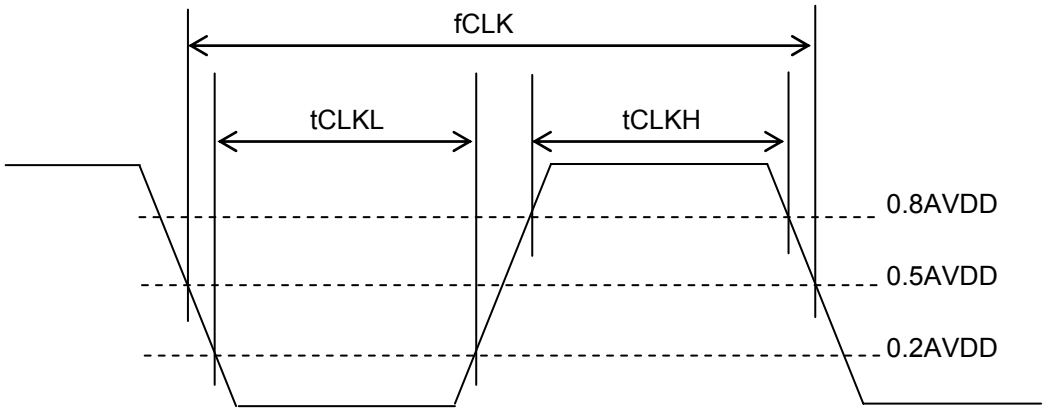


(*2) Determine need for and appropriate value of limiting resistance (Rd) in accordance with the crystal specifications.

[5] AC Timing

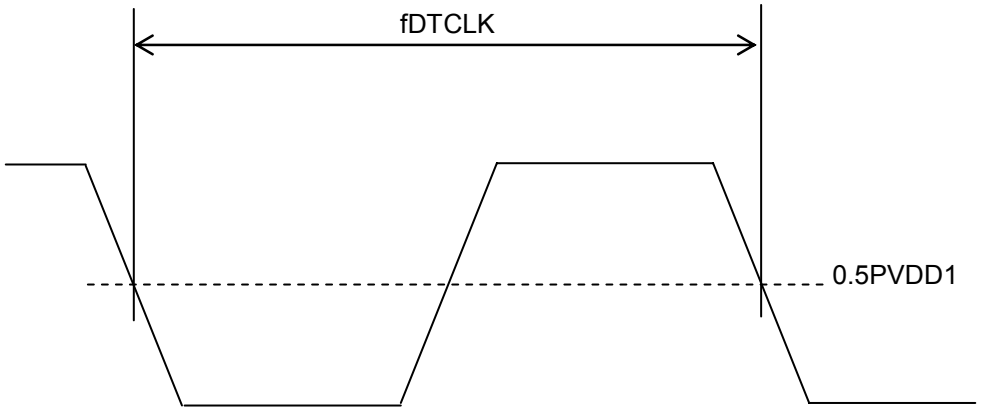
(1.70≤DVDD≤2.00, DVDD≤PVDD1≤3.60, DVDD≤PVDD2≤3.60)
(Ta = −40~85˚C, Load condition: CL=15pF)

[5.1] Clock input



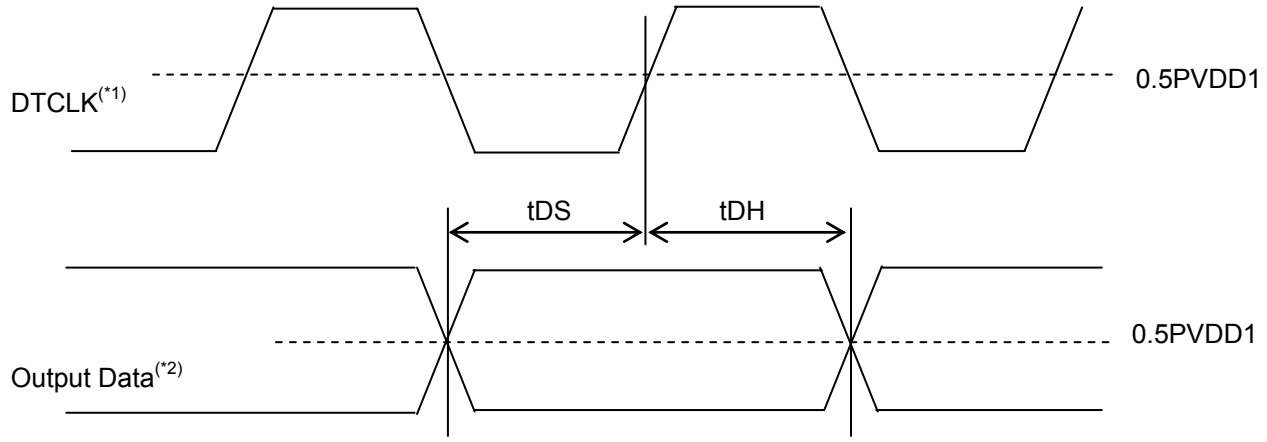
Parameter	Symbol	Min	Typ	Max	Units
Input CLK	fCLK		24.576		MHz
CLK pulse width H	tCLKH	16			nsec
CLK pulse widthL	tCLKL	16			
Frequency tolerance				±100	ppm

[5.2] Clock output (DTCLK output)



Parameter	Symbol	Min	Typ	Max	Units	Condition
DTCLK	fDTCLK		13.5		MHz	(Interlace) 16bit YCbCr output (Interlace) RGB output
			27			(Interlace) 8bit YCbCr output (Progressive) 16bit YCbCr output (Progressive) RGB output
			54			(Progressive) 8bit YCbCr output

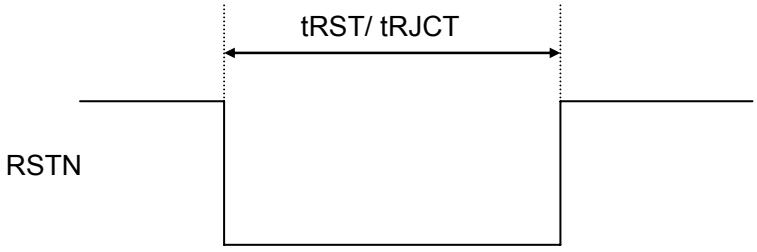
[5.3] Output data timing



Parameter	Symbol	Min	Typ	Max	Units	Condition
Output Data Setup Time	tDS	20			nsec	(Interlace) 16bit YCbCr output (Interlace) RGB output
		10				(Interlace) 8bit YCbCr output (Progressive) 16bit YCbCr output (Progressive) RGB output
		5				(Progressive) 8bit YCbCr output
Output Data Hold Time	tDH	20			nsec	(Interlace) 16bit YCbCr output (Interlace) RGB output
		10				(Interlace) 8bit YCbCr output (Progressive) 16bit YCbCr output (Progressive) RGB output
		5				(Progressive) 8bit YCbCr output

(*1) It is possible to invert the polarity of DTCLK by setting register. (Sub Address: 0x07[7]).
(*2)Output Data is general term of DATA [23:0], HD, VD_FLD and DVAL_FLD.

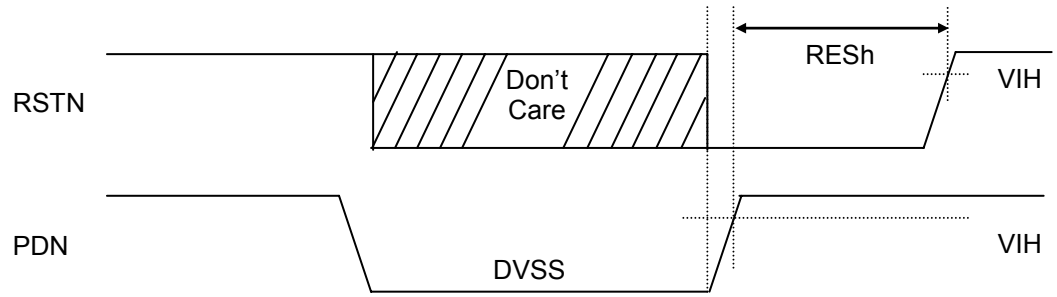
[5.4] Reset pulse



Parameter	Symbol	Min	Typ	Max	Units
RSTN pulse width	tRST	500			nsec
RSTN pulse eject	tRJCT			50	

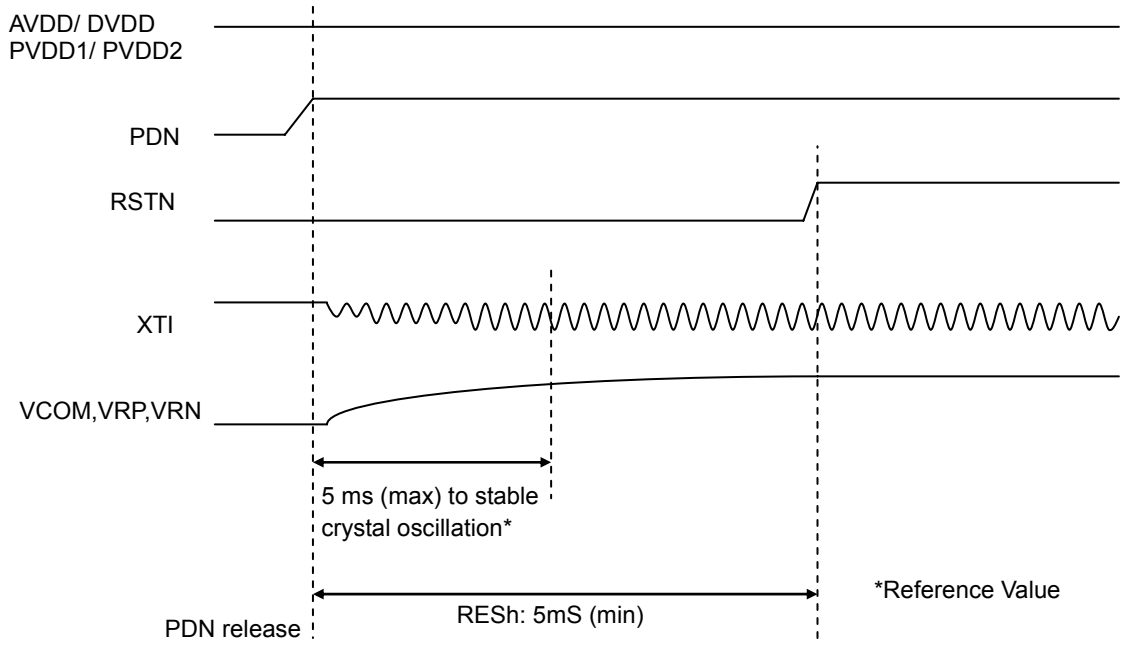
[5.5] Power-down release sequence

Reset must be applied after PDN release (PDN=Hi).

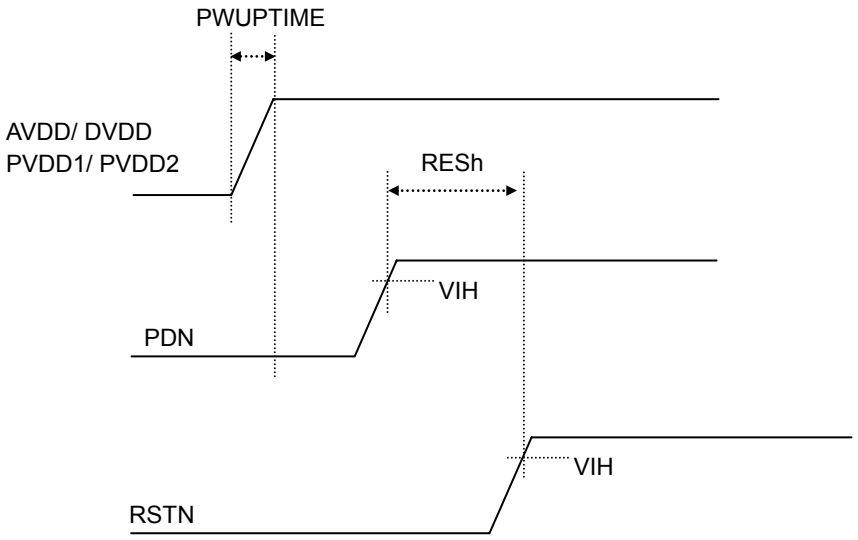


Parameter	Symbol	Min	Typ	Max	Units
Reset width after PDN release	RESh	5			ms

To perform power-down, all control signals must always be brought to the voltage polarity to be used or to ground level.



[5.6] Power-on sequence

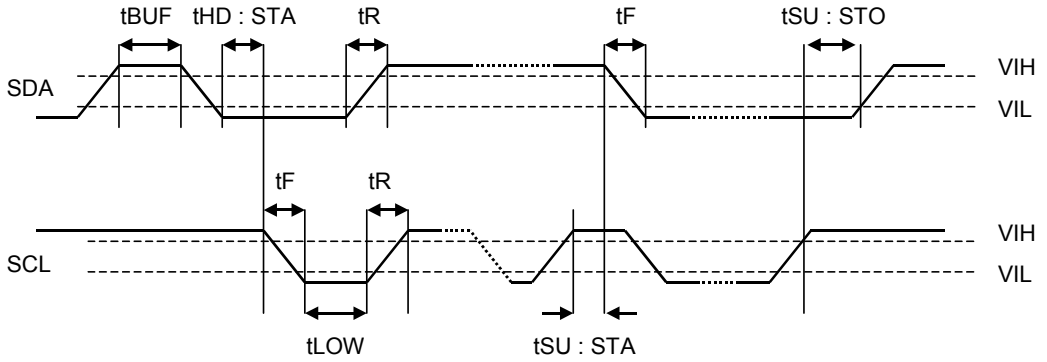


Parameter	Symbol	Min	Typ	Max	Units
POWERUP TIME	PWUPTIME			100	msec
Reset width after PDN release	RESh	5			

At power-on, PDN must be set to ground level (PDN=Low).
AVDD/DVDD/PVDD1/PVDD2 should be raised at power-on less than 100msec.
After PDN release, RSTN must stay on Low level more than 5msec.

[5.7] I2C bus input timing

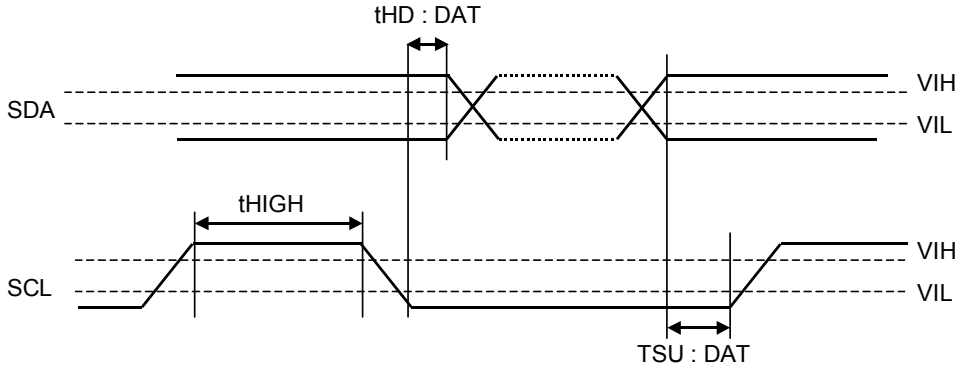
[5.7.1] Timing 1



Parameter	Symbol	Min	Max	Units
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

*The timing relating to the I2C bus is as stipulated by the I2C bus specification, and not determined by the device itself. For details, see I2C bus specification.

[5.7.2] Timing 2



Parameter	Symbol	Min	Max	Units
Data Setup Time	tSU:DAT	100(*1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9(*2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

(*1) If I2C is used in standard mode, tSU:DAT≥250ns is required.

(*2) This condition must be met if the AK8858 is used with a bus that does not extend tLOW (to use tLOW at minimum specification).

[6] Functional overview

The following key functions are characteristic of the AK8858 and its operational performance.

(1) It accepts composite video signal (CVBS), S-video and component YPbPr input with 10 input pins available for this purpose.The decode signal is selected via register setting.

(2) It contains an internal analog band limiting filter (anti-aliasing) in front of the AD converter input.

(3) Its analog circuit clamps the input signal to the sync tip (analog sync tip clamp). Its digital circuit clamps the digitized input data to the pedestal level (digital pedestal clamp).

(4) It has auto detection mode via register setting which automatically recognizes the input signal category.

(5) Its adaptive AGC function enables measurement of the input signal size and determination of the input signal level.

(6) Its ACC function enables measurement of the input signal color burst size and determination of the appropriate color burst level.

(7) It performs adaptive two-dimensional Y/C separation, in which its phase detector selects the best correlation from among vertical, horizontal, and diagonal samples and optimum Y/C separation mode.

(8) Its digital pixel spacing adjustor can align vertical positions by vertical pixel positioning.

(9) Its operated in line-locked, frame-locked, or fixed clock mode with automatic transition and optimum mode selection by automatic scanning.

(10) In PAL-B, D, G, H, I and N decoding, it can perform phase-difference correction for each line.

(11) Its output interface is ITU-R BT.656 (EAV/SAV) compliant. For connection of devices having no ITU-R BT.656 interface, it shows the active video region by HD/ VD/ DVALID/ FIELD signal output.

(12) Its output data format is in YCbCr format and RGB (8:8:8) format.

(13) It judges the chroma signal quality from the color burst of the input signal, and can apply color kill if the signal quality is judged insufficient. It can also apply color kill if the color decode PLL clock control.

(14) Its image quality adjustment function includes contrast, brightness, hue, color saturation, and sharpness adjustment.

(15) Its luminance and color signal band limiting filter are adjustable via register setting.

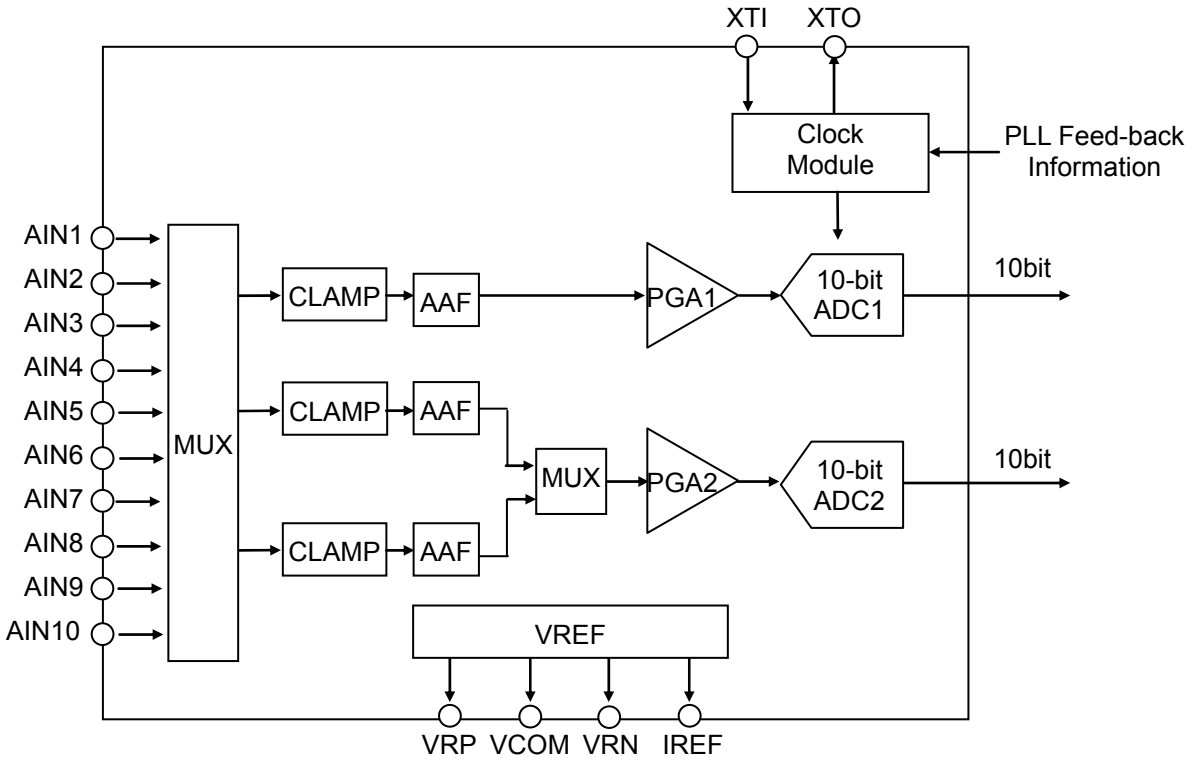
(16) It can decode conflated closed caption data, WSS signals, VBID(CGMS-A) and write them separately to the storage register.

(17) Its enables Macrovision signal type notification, in cases where the Macrovision signal is included in the decoded data.

[7] Functional description

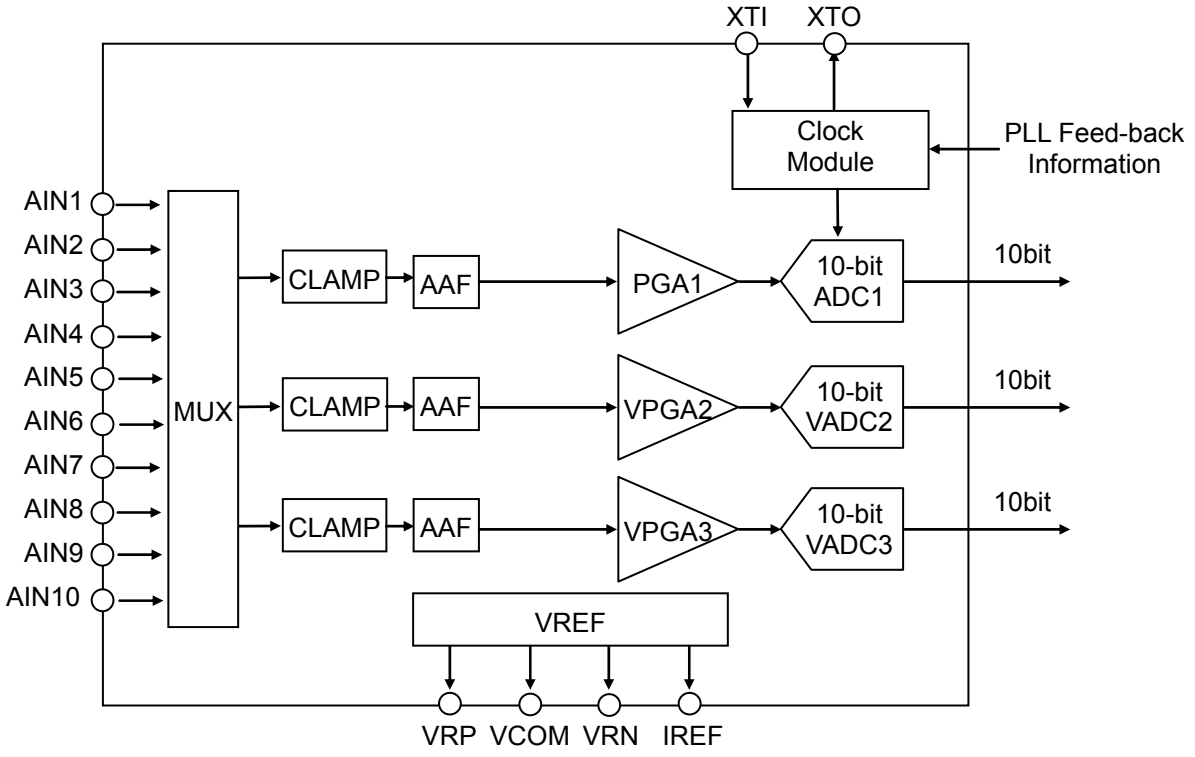
[7.1] Analog circuit description

Analog circuit block is shown below.



When decode YPbPr component video signal, Pb/Pr signal is converted to digital data by PGA2 and ADC2 after the data was sampled at sample hold circuit.

Time sharing operational status of ADC and PGA is shown below (PGA2 and ADC2 is shown as VPGA2, VADC2, VPGA3 and VADC3).



[7.1.1] CVBS signal decoding

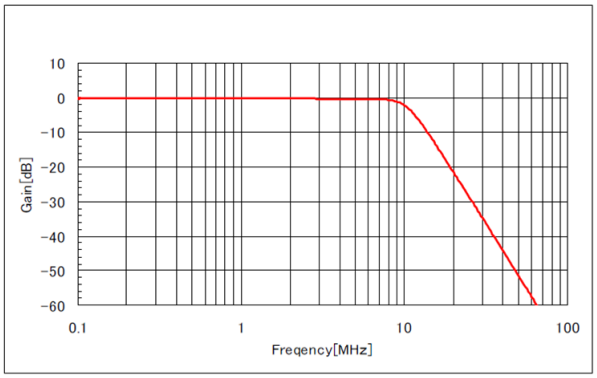
The data is converted to digital at PGA1 and ADC1. Sampling clock is 27MHz.
The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows: ±1dB (~6MHz), −30dB (27MHz)

[7.1.2] S(Y/C) video signal decoding

Y signal data is converted to digital at PGA1 and ADC1. Sampling clock is 27MHz.
C signal data is converted to digital at PGA2 and ADC2. Sampling clock is 27MHz.
The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows: ±1dB (~6MHz), −30dB (27MHz)

[7.1.3] 525i/625i YPbPr component video signal decoding

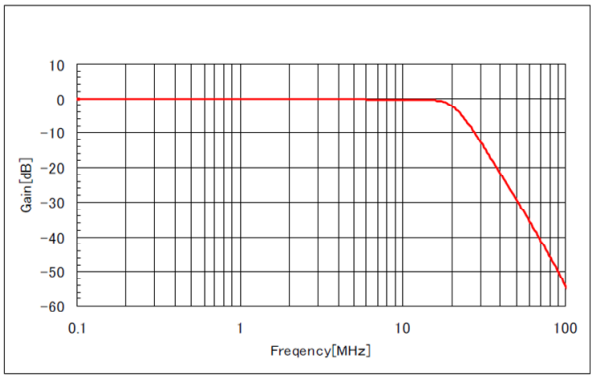
Y signal data is converted to digital at PGA1 and ADC1. Sampling clock is 27MHz.
Pb signal data is converted to digital at VPGA2 and VADC2. Sampling clock is 27MHz.
Pr signal data is converted to digital at VPGA3 and VADC3. Sampling clock is 27MHz.
The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows: ±1dB (~6MHz), −30dB (27MHz)



AAF Chracteristic (except Progressive)

[7.1.4] 525p/625p YPbPr component video signal decoding

Y signal data is converted to digital at PGA1 and ADC1. Sampling clock is 54MHz.
Pb signal data is converted to digital at VPGA2 and VADC2. Sampling clock is 27MHz.
Pr signal data is converted to digital at VPGA3 and VADC3. Sampling clock is 27MHz.
The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows: ±1dB (~12MHz), −30dB (54MHz)



AAF Chracteristic (Progressive)

[7.2] Analog Interface

The AK8858 accepts composite video signal (CVBS), S(Y/C) video signal, YPbPr component video signal (D1/D2) input with 10 input pins available for this purpose.

Sub Address:0x00 Default Value:0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMOD	SELSRC1	SELSRC0	ADC3SEL	ADC2SEL	ADC1SEL2	ADC1SEL1	ADC1SEL0
Default Value							
0	0	0	0	0	0	0	0

The connection settings are shown below.

ADC1SEL[2:0]-bit: Input selection for ADC1. (for CVBS or Y)

Setting	ADC1 Input
000	AIN1
001	AIN2
010	AIN3
011	AIN4
100	AIN5
101	AIN6

ADC2SEL-bit: Input selection for ADC2 (VADC2). (for C or Pb)

Setting	ADC2 Input
0	AIN7
1	AIN8

ADC3SEL-bit: Input selection for ADC3 (VADC2). (for Pr)

Setting	ADC3 Input
0	AIN9
1	AIN10

SELSRC[1:0]-bit: Decode signal type setting bit.

Setting	Input signal
00	Composite (CVBS) video signal
01	S-Video signal
10	Component video signal
11	Analog power-down (CLAMP, AAF, PGA, ADC is power-down)

[7.3] Input Clock mode

CLKMOD-bit: Input clock setting bit.

Setting	Input clock
0	For crystal
1	External clock input (clock generator)

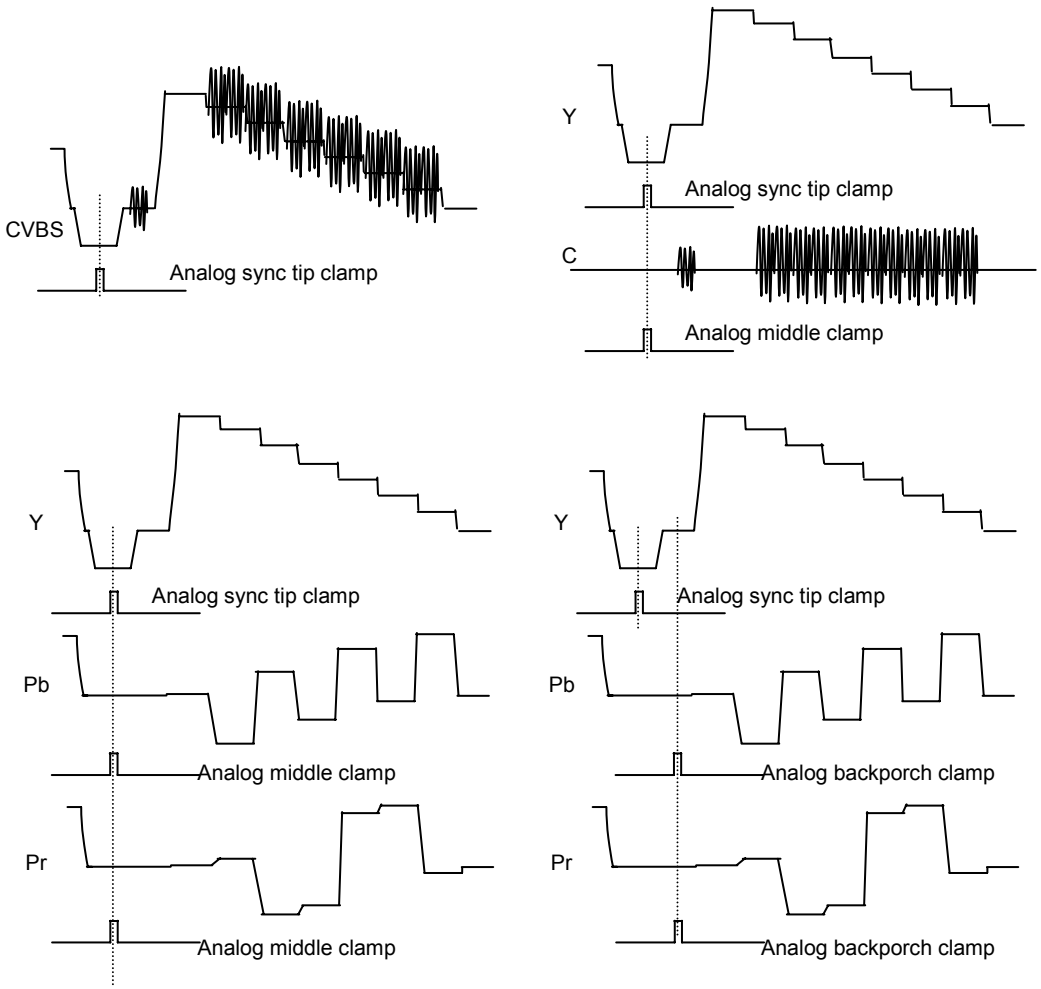
[7.4] Analog clamp circuit

The analog circuit of the AK8858 clamps the input signal to the reference level. The way to clamp the input signal is as follows.

The clamp timing pulse, with its origin at the falling edge of the internally synchronized and separated sync signal, is generated at approximately the central position of the sync signal.

Input signal		Clamp Level	Clamp pulse position
Composite (CVBS) video signal		Sync tip level	Sync tip
S(Y/C) video signal	Y signal	Sync tip level	Sync tip
	C signal	Pedestal level	Sync tip of Y
Component video signal	Y signal	Sync tip level	Sync tip
	Pb signal	Pedestal level	Clamp timing is performs by sync tip clamp or backporch clamp. If Pb and Pr signal have sync signl, set clamp timing to backporch clamp.
	Pr signal	Pedestal level	

Clamp Timing Pulse



Additionary, the AK8858 can change the position, width and current value of clamp pulse via register Clamp Control 1 Register (R/W) [Sub Address 0x01] and Clamp Control 2 Register (R/W) [Sub Address 0x02].

Sub Address: 0x01 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLP-WIDTH1	CLP-WIDTH0	CLP-STAT1	CLP-STAT0	Reserved	BCLP-STAT2	BCLP-STAT1	BCLP-STAT0
Default Value							
0	0	0	0	0	0	0	0

Sub Address: 0x02 Default Value: 0x01

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	YPBPRCP	UDG1	UDG0	CLPG1	CLPG0
Default Value							
0	0	0	0	0	0	0	1

BCLPSTAT[2:0]-bit: Set the position of analog backporch clamp pulse.

Setting	Clamp position	Notes
000	Same position with “CLPSTAT” setting	
001	(1/128)H delay from “CLPSTAT” setting	
010	(2/128)H delay from “CLPSTAT” setting	
011	(3/128)H delay from “CLPSTAT” setting	
100	(4/128)H advance from “CLPSTAT” setting	
101	(3/128)H advance from “CLPSTAT” setting	
110	(2/128)H advance from “CLPSTAT” setting	
111	(1/128)H advance from “CLPSTAT” setting	

Set only the position of analog backporch clamp pulse.

CLPSTAT[1:0]-bit: Set the position of clamp pulse.

Setting	Clamp position	Notes
00	Sync tip/ middle/ bottom clamp: Center of horizontal sync Backporch clamp: Center of backporch interval	
01	(1/128)H delay	
10	(2/128)H advance	
11	(1/128)H advance	

The positions of all clamp pulse are changed.

CLPWIDTH[1:0]-bit: Set the clamp pulse width. Pulse width is change according to sampling clock units.

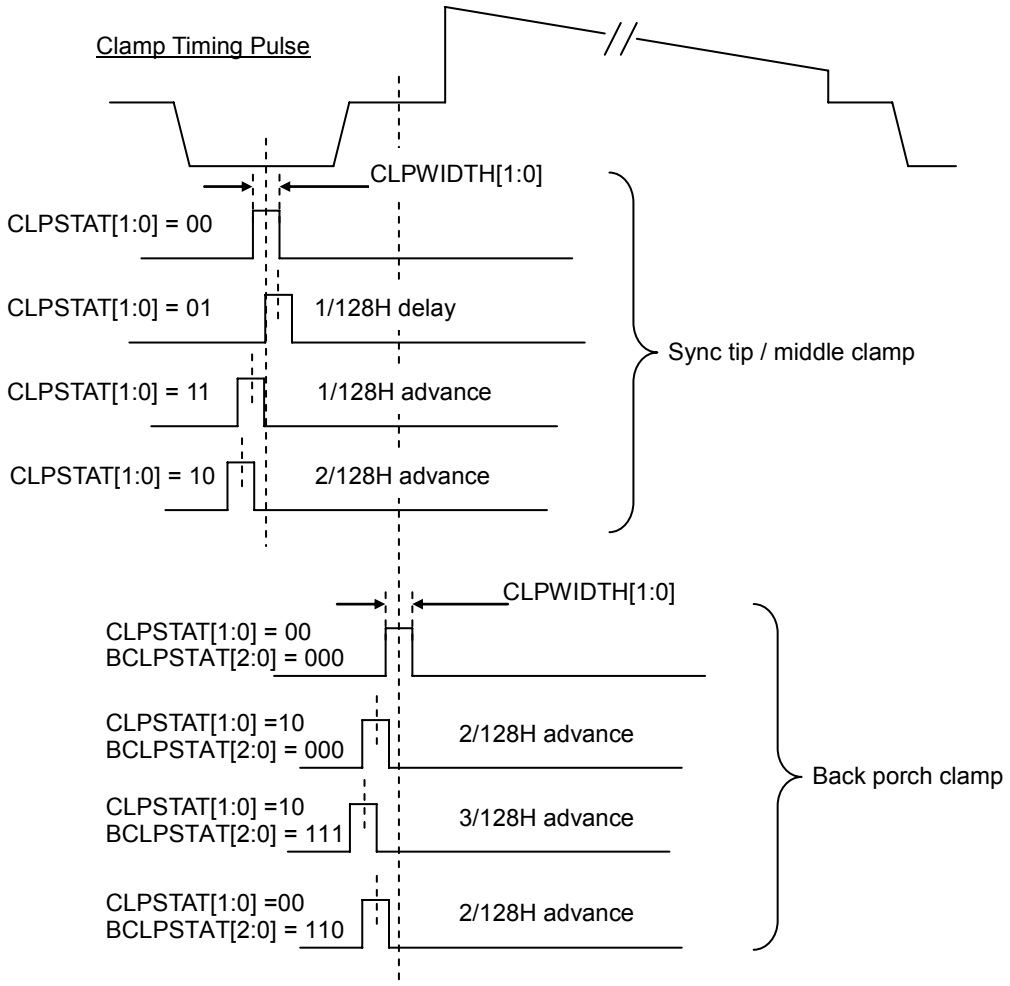
Setting	Clamp width	Notes
00	7 clock	Clock units 525i, 625i: 27MHz 525p, 625p: 54MHz
01	15 clock	
10	31 clock	
11	63 clock	

The width of all clamp pulse is changed.

YPBPRCP-bit: Set the clamp position of PbPr signal of YPbPR component video signal.

Setting	Clamp position	Notes
0	Sync tip timing	
1	Backporch timing	

The relation between CLPSTAT and BCLPSTAT is shown as follows.



Clamp current value setting

CLPG[1:0]: Set the current value of fine clamp in analog block.

Setting	Clamp current value	Notes
00	Min.	Middle 1 = (Min. x 3 times) Middle 2 = (Min. x 5 times) Max. = (Min. x 7 times)
01	Middle 1 (Default)	
10	Middle 2	
11	Max.	

UDG[1:0]: Set the current value of rough clamp in analog block.

Setting	Clamp current value	Notes
00	Min. (Default)	Middle 1 = (Min. x 2 times) Middle 2 = (Min. x 3 times) Max. = (Min. x 4 times)
01	Middle 1	
10	Middle 2	
11	Max.	

Its digital circuit clamps the digitized input data to the pedestal level (digital pedestal clamp).

[7.5] Input video signal categorization

Set the input video signal.

Composite (CVBS) video signal, S-Video signal, and Component video signal can be select via register Input Channel Select Register (R/W) [Sub Address 0x00].

When decode composite (CVBS) video signal and S-Video signal, it is necessary to set subcarrier frequency, color encode format, line frequency, and Setup ON/OFF of input signal via register Input Video Standard Register (R/W) [Sub Address 0x04].

When decode component video signal, it is necessary to set line frequency and Setup ON/OFF. It is also necessary to set sync signal and signal ratio of input video signal via register Miscellaneous Setting Register (R/W) [Sub Address 0x03].

Sub Address: 0x04 Default Value:0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AUTODET	SETUP	BW	VLF	VCEN1	VCEN0	VSCF1	VCSF0
Default Value							
0	0	0	0	0	0	0	0

Sub Address: 0x03 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	CSCL	CSSL	Reserved
Default Value							
0	0	0	0	0	0	0	0

VCSF[1:0]-bit: Setting for subcarrier frequency of input signal.

Setting	Subcarrier frequency	Formats
00	3.57954545 MHz	NTSC
01	3.57561149 MHz	PAL-M
10	3.58205625 MHz	PAN-Nc
11	4.43361875 MHz	PAL-B,D,G,H,I,N, NTSC-4.43, PAL60, SECAM*

*For SECAM input signal, set VCSF[1:0] to 11.

For component video signal input, VCSF[1:0] setting is not necessary.

VCEN[1:0]-bit: Setting for color encode format of input signal.

Setting	Color encode format	Notes
00	NTSC	
01	PAL	
10	SECAM	In case of YPbPr, SECAM is prohibited.
11	Reserved	

For component video signal input, VCEN[1:0] setting is not necessary.

VLF-bit: Setting for line frequency of each input frame.

Setting	Number of lines	Notes
0	525	NTSC-M, J, NTSC-4.43, PAL-M, PAL-60
1	625	PAL-B, D, G, H, I, N, Nc, SECAM

BW-bit: Setting for decoding of input signal as monochrome signal (monochrome mode)

Setting	Signal type	Notes
0	Not monochrome (monochrome mode OFF)	
1	Decode as monochrome signal (monochrome mode ON)	

In the monochrome mode (BW=1), the input signal is treated as a monochrome signal, and all sampling data digitized the AD converter passes through the luminance process and is processed as luminance signal, and the CbCr code is output as 0x80 regardless of the input.

SETUP-bit: Setting for presence or absence of input signal SETUP.

Setting	ON/OFF	Notes
0	Setup absent	
1	Setup present	With the Setup present setting, the luminance and color signals are processed as follows: Yout = (YIN-7.5IRE)/0.925 Uout = UIN/0.925, Vout = VIN/0.925 YOUT: Y after setup YIN: Y before setup UOUT: U after setup UIN: U before setup VOUT: V after setup VIN: V before setup

In auto detection mode, the default setting of Setup processing via register STUPATOFF-bit of Control 2 Register (R/W) [Sub Address 0x0D]-bit6 is shows as follows.

Detected signal	Register setting		Setup present/ absent
	Setup-bit	STUPATOFF-bit	
NTSC-M,J PAL-B,D,G,H,I,N PAL-Nc , 60 SECAM	0	0	Setup absent
		1	Setup absent
	1	0	Setup present
		1	Setup present
PAL-M NTSC-4.43	0	0	Setup present
		1	Setup absent
	1	0	Setup present
		1	Setup present

In case of YPbPr signal input, auto Setup processing is not performed.

AUTODET-bit: Settings for auto detection of input signal (auto detetction mode)

Setting	ON/OFF	Notes
0	OFF	Manual setting
1	ON	

CSSL-bit: Settings for sync and video signal ratio of input signal.

Setting	S/V ratio	Notes
0	300/700	EIA-770.2
1	286/714	EIA-770.1

Only available when component input signal is selected.

CSCL-bit: Settings for color level of component input signal.

Setting	Video level	Notes
0	700mV	EIA-770.2
1	714mV	EIA-770.1

Only available when component input signal is selected.

CMPSEL-bit: Interlace and Progressive setting for YPbPr component input signal.

Setting	YPbPr component video signal
0	Interlace (525i/ 625i)
1	Progressive (525P/ 625P)

VERTS-bit: Select of VLOCK or Direct Lock

Setting	SYNC mechanism	Notes
0	VLOCK mechanism	
1	Direct LOCK mechanism	

[7.6] Auto detection mode of input signal

The video input signal can be automatically detected (auto detection mode) via register.

Settings for auto detection of input signal (auto detetction mode) Sub Address: 0x04 [7]

Name	Setting	ON/OFF	Notes
AUTODET	0	OFF(Manual setting)	
	1	ON	

The auto detetction recognizes the following parameters (AUTODET-bit=1).

Number of lines per frame:

525/626

Subcarrier frequency:

3.57954545 (MHz)
3.57561149 (MHz)
3.58205625 (MHz)
4.43361875 (MHz)

Color encoding formats:

NTSC/PAL/SECAM

Progressive setting:

Interlace / Progressive

Monochrome signal*:

Not monochrome/monochrome.

*Note: Automatic monochrome detection is active if the color kill setting is ON.

The detected result of auto detetction mode is reflected to Input Video Status Register. The input signal status can be recognized by reading this register.

Sub Address: 0x25

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FIXED	UNDEF	ST_BW	ST_VLF	ST_VCEN1	ST_VCEN0	ST_VSCF1	ST_VCSF0

In addition, auto detetction function of the input signal is recognized by the changing of internal status.
If FIXED-bit changed from 0 to 1, the detetction is completed. During FIXED-bit is 0, the AK8858 may attempt to recognize the input signal and the output code during this period cannot be trusted. If the AK8858 cannot recognize the input signal, UNDEF-bit is changed from 0 to 1 to indicate the status of the input signal.

[7.7] Auto detection restriction of input signal

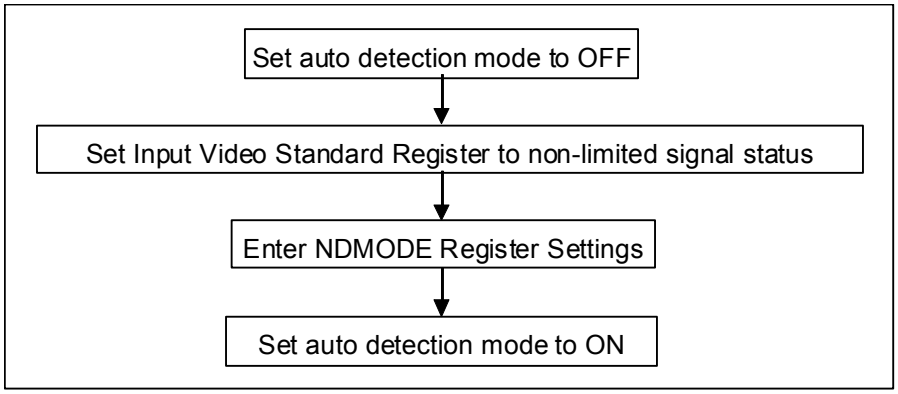
In auto detection mode, the candidates for detection can be limited via register NDMODE Register.

Sub Address:0x06 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ND625L	ND525L	NDPAL60	NDNTSC443	Reserved	NDSECAM	NDPALNC	NDPALM
Default Value							
0	0	0	0	0	0	0	0

In making the above register settings, the following restrictions apply.

1. Setting both NDNTSC443-bit and NDPAL60-bit to 1 is prohibited.
2. Setting both ND525L-bit and ND625L-bit to 1 is prohibited.
3. To limit candidate formats, it is necessary to have the auto detetction mode OFF while first setting the register to non-limited signal status and next the NDMODE settings, and then setting the auto detetction mode to ON.



[7.8] Output data blanking interval

Setting vertical blanking intervals. Sub Address: 0x05[2:0]

VBIL[2:0]-bit	525/625	Vertical blanking interval	Notes
001	525i	Line1~Line20 and Line263.5~Line283.5	+1Line
	625i	Line623.5~Line24.5 and Line311~Line336	
	525p	Line1~Line43	
	625p	Line 621~Line625 and Line1~Line45	
010	525i	Line1~Line21 and Line263.5~Line284.5	+2Lines
	625i	Line623.5~Line25.5 and Line311~Line337	
	525p	Line1~Line44	
	625p	Line 621~Line625 and Line1~Line46	
011	525i	Line1~Line22 and Line263.5~Line285.5	+3Lines
	625i	Line623.5~Line26.5 and Line311~Line338	
	525p	Line1~Line45	
	625p	Line 621~Line625 and Line1~Line47	
000	525i	Line1~Line19 and Line263.5~Line282.5	Default
	625i	Line623.5~Line23.5 and Line311~Line335	
	525p	Line1~Line42	
	625p	Line 621~Line625 and Line1~Line44	
101	525i	Line1~Line16 and Line263.5~Line279.5	-3Lines
	625i	Line623.5~Line20.5 and Line311~Line332	
	525p	Line1~Line39	
	625p	Line 621~Line625 and Line1~Line41	
110	525i	Line1~Line17 and Line263.5~Line280.5	-2Lines
	625i	Line623.5~Line21.5 and Line311~Line333	
	525p	Line1~Line40	
	625p	Line 621~Line625 and Line1~Line42	
111	525i	Line1~Line18 and Line263.5~Line281.5	-1Line
	625i	Line623.5~Line22.5 and Line311~Line334	
	525p	Line1~Line41	
	625p	Line 621~Line625 and Line1~Line43	
100	Reserved	Reserved	

As indicated in this table, the default values are:

(525i) Line1~Line19 and Line263.5~Line282.5

(625i) Line623.5~Line23.5 and Line311~Line335

(525P) Line1~Line42

(625P) Line 621~Line625 and Line1~Line44

The other specific values are set by entering the difference from these default values.

[7.9] Output data code Min/Max setting

LIMIT601-bit: Setting for output data code Min/Max Sub Address: 0x05[3]

LIMIT601-bit	Output data code Min~Max	EAVSAV-bit	Notes
0	Y: 1~254 Cb, Cr: 1~254 R, G, B: 1~254	0	(*1)
	Y: 0~255 Cb, Cr: 0~255 R, G, B: 0~255	1	
1	Y: 16~235 Cb, Cr: 16~240 R, G, B: 16~235	X	(*2)

All internal calculating operations are made with Min = 1, Max = 254.

(*1)In case of LIMIT601-bit =0, the output code Min and Max values is set according to EAVSAV-bit status.

(*2)In case of LIMIT601-bit =1, codes 1~15 and 236~254 are respectively clipped to 16,235(Cb, Cr is 240).

[7.10] Output Pin state

DATA[23:0], HD, VD_FLD, DVAL_FLD and NSIG pins can be Low output by register.

Sub Address: 0x17 [4:0]

Name	Setting	Definition	備考
DL	[0]	Normal output	Default: Normal output
	[1]	[D23: D0] pin output fixed at low	
VDFL	[0]	Normal output	Default: Normal output
	[1]	VDFL pin output fixed at low	
DVALFL	[0]	Normal output	Default: Normal output
	[1]	DVALFL pin output fixed at low	
NL	[0]	Normal output	Default: Normal output
	[1]	NL pin output fixed at low	
HL	[0]	Normal output	Default: Normal output
	[1]	HL pin output fixed at low	

OE, PDN and RSTN pins are prior to these register.

[7.11] Slice function

The results of VBI slicing by the AK8858 slicing function are output as ITU-R BT.601 digital data. The VBI interval is set via VBIL[2:0]-bits. VBI slicing is performed in the luminance in the luminance signal processing path, so that the Cb/Cr value of the effective line 601 output code is output at the same level as the corresponding luminance signal.

Setting for slice level Sub Address: 0x05 [5]

Name	Definition
SLLVL	[0]: 25IRE [1]: 50IRE

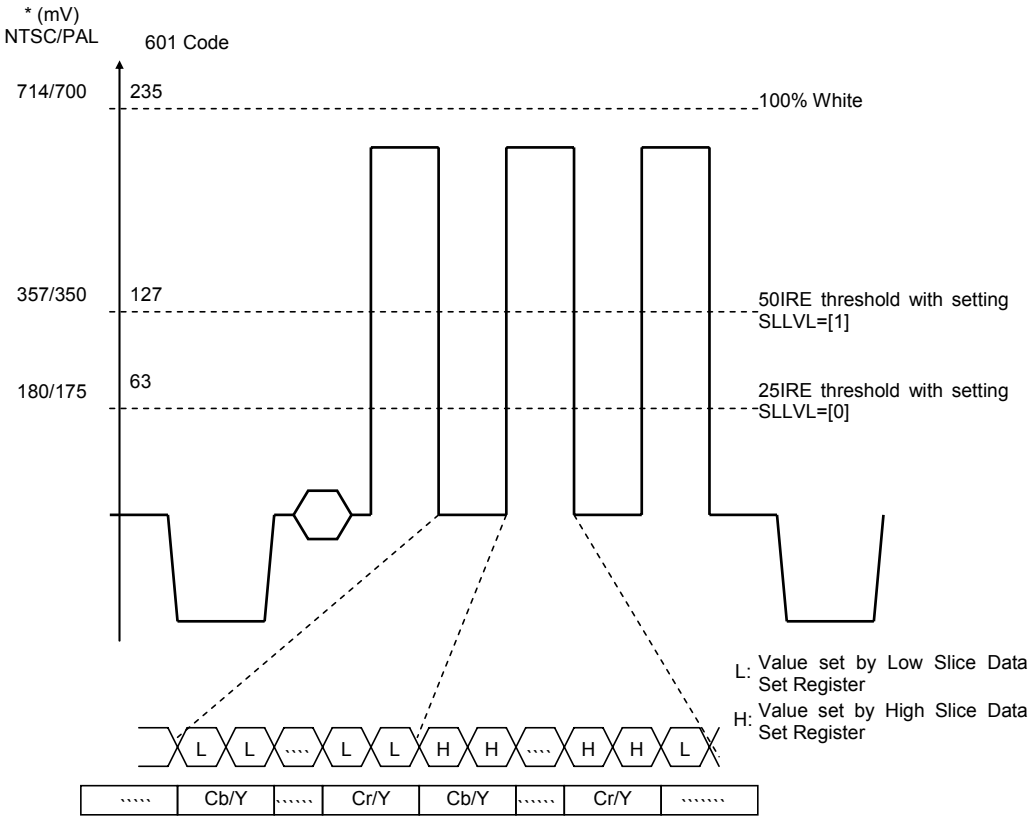
Hi/Low Slice Data Set Register of output data, as follows.

Setting for higher of two values resulting from slicing Sub Address: 0x18

Name	Definition
H0 ~ H7	Default: 0xEB(235) Note that a setting of 0x00 or 0xFF corresponds to a special 601 code.

Setting for lower of two values resulting from slicing Sub Address: 0x19

Name	Definition
L0 ~ L7	Default: 0x10(16) Note that a setting of 0x00 or 0xFF corresponds to a special 601 code.



*Threshold values (mV) are approximate

High/Low conversion is performed for either the Cb/Y or the Cr/Y combination. The above figure is an example of the conversion points for Cb/Y.

[7.12] VBI period decode data

The AK8858 decode data during VBI period can be selected via register.

Settings for decode data in the VBI period Sub Address: 0x05 [7:6]

Name	Setting value	Decode data	Notes
VBIDEC0 ~ VBIDEC1	[00]	Black level output	Y = 0x10 Cb/Cr = 0x80
	[01]	Monochrome mode	Y = data converted to 601 level Cb/Cr = 0x80
	[10]	Sliced data output	Y/Cb/Cr = value corresponding to slice level (Value set at Hi/Low Slice Data Set Register)
	[11]	Reserved	Reserved

Note: (525i) Lne1~Line9 and Line263.5~Line272.5
(625i) Line623.5~Line6.5 and Line311~Line388
(525p) Line1~Line18
(625p) Line621~Line10

During the above period, these values are unaffected by the VBIDEC[1:0]-bits setting.
The output code during this period is black level code (Y=0x10, Cb/Cr=0x80).

[7.13] VLOCK mechanism

The AK8858 synchronizes internal operation with the input signal frame structure. If, for example, the frame structure of the input signal comprises 524 lines, the internal operation will have structure of 524 lines per frame. This mechanism is termed the VLOCK mechanism. If an input signal changes from a structure of 525 lines per frame to one of 524 lines per frame, internal operation will change accordingly, and the VLOCK mechanism will go to UnLock via a pull-in process. In such case, the UnLock status can be confirmed via the control register [VLOCK-bit*]. Note that the time required for locking of the VLOCK mechanism upon channel or other input signal switching will be about 4 frames (*Sub-address:0x22-“bit1”)

Furthermore, the AK8858 synchronizes internal operation with the vertical SYNC of the input signal. This mechanism is termed the direct LOCK mechanism.

Setting for Vertical SYNC mechanism Sub Address: 0x03 [7]

Name	Definition
VERTS	Vertical SYNC mechanism [0]: VLOCK mechanism [1]: Direct LOCK mechanism

[7.14] Adjustment of Y and C timing

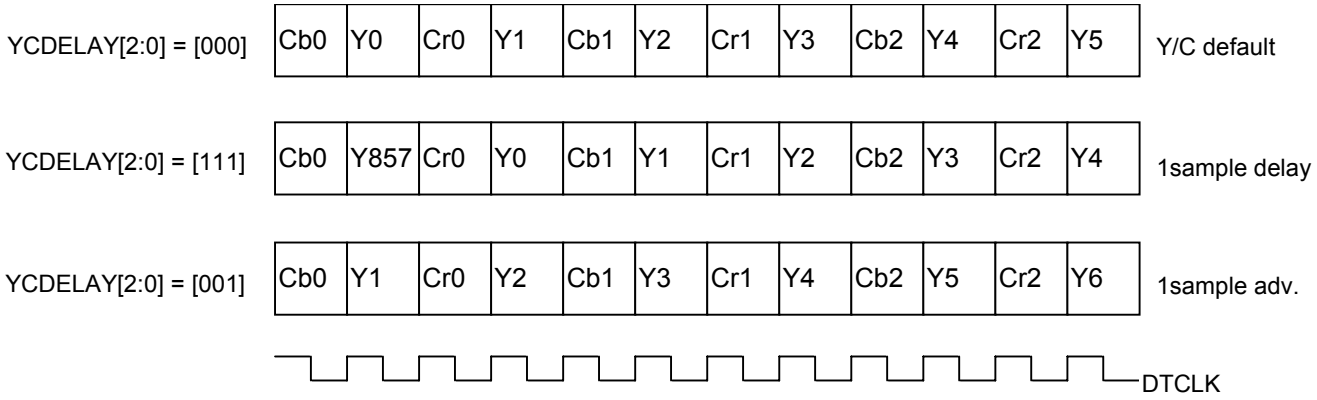
Adjustment of the position between Y and C signal

Sub Address: 0x08 [2:0]

YCDELAY[2:0]-bit	Y and C timing	Notes
001	Y advance 1 sample toward Cb, Cr.	
010	Y advance 2 sample toward Cb, Cr.	
011	Y advance 3 sample toward Cb, Cr.	
000	No delay and advance.	Default
101	Y delay 3 sample toward Cb, Cr.	
110	Y delay 2 sample toward Cb, Cr.	
111	Y delay 1 sample toward Cb, Cr.	
100	Reserved	

Note: 1sample of Interlace output is about 74ns / 1 sample of progressive output is about 37ns.

Relation between Y and C timing regardless the above setting is shown as follows.



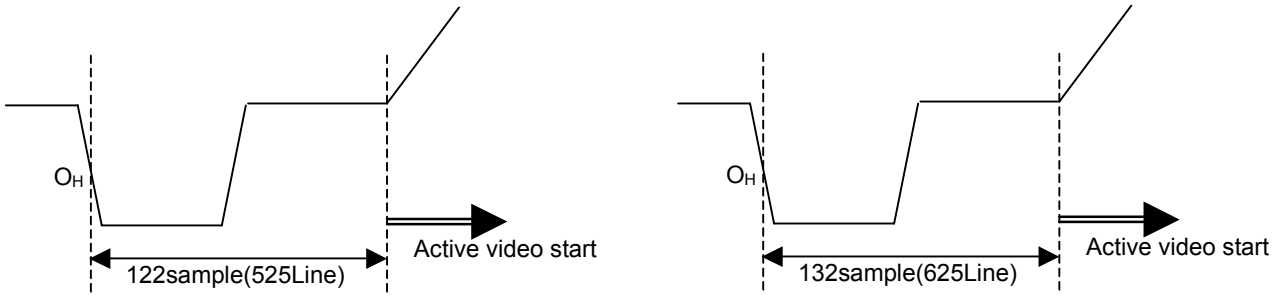
[7.15] Adjustment of active video start position

Adjustment of the active video start position

Sub Address: 0x08 [6:4]

ACTSTA[2:0]-bit	Line and active video start		Notes
001	525 Line	124th sample	D1 decode: 74ns delay D2 decode: 37ns delay
	625 Line	134th sample	
010	525 Line	125th sample	D1 decode: 148ns delay D2 decode: 74ns delay
	625 Line	135th sample	
011	525 Line	126th sample	D1 decode: 222ns delay D2 decode: 111ns delay
	625 Line	136th sample	
000	525 Line	123th sample	Default（Normal position）
	625 Line	133th sample	
101	525 Line	120th sample	D1 decode: 222ns advance D2 decode: 111ns advance
	625 Line	130th sample	
110	525 Line	121th sample	D1 decode: 148ns advance D2 decode: 74ns advance
	625 Line	131th sample	
111	525 Line	122th sample	D1 decode: 74ns advance D2 decode: 37ns advance
	625 Line	132th sample	
100	Reserved	Reserved	

With the default value, the start position is as follows (with ITU-R BT.601 format compliance).



[7.16] PGA

The AK8858 analog PGA and digital PGA are built internally.
The analog PGA value can be set in range of -3dB to 6dB, and the gain step is 3dB/step.
The digital PGA value can be set in range -0.25dB to 4dB, and the gain step is not log scale.

Digital PGA gain equation:

$$\text{Gain(dB)} = 20LOG\left(\frac{(5\times PGA)+497}{512}\right)$$

*PGA: PGA1 or PGA2 register value (Decimal)

Default gain setting is 0x54(HEX)=1.3dB. (Analog:0dB + Digital:1.3dB)
At the default setting, when the composite video signal input with 0.5Vpp is input to the AIN pin, the decode gain setting is set to appropriate range.

PGA1 is used for CVBS and Y signals gain processing.
Setting for PGA1 value Sub Address: 0x0E [7:0]

Name	Definition
DPGA1_0 ~ DPGA1_5	Digital PGA1 gain setting. PGA gain is set by above equation.
APGA1_0 ~ APGA1_1	Analog PGA1 gain setting. [00]: −3dB [01]: 0dB [10]: +3dB [11]: +6dB

PGA2 is used for C, Pb, and Pr signals gain processing.
Setting for PGA2 value Sub Address: 0x0F [7:0]

Name	Definition
DPGA2_0 ~ DPGA2_5	Digital PGA2 gain setting. PGA gain is set by above equation.
APGA2_0 ~ APGA2_1	Analog PGA2 gain setting. [00]: −3dB [01]: 0dB [10]: +3dB [11]: +6dB

This register also can be used to read the current setting of the AGC setting.
If AGC is enable, the Gain1/2 Control Register[7:0]-bit setting value has no effect.
If AGC is disable, the Gain1/2 Control Register setting can be manually entered.

[7.17] AGC (Auto Gain Control)

The AGC function amplifies the input signal to the appropriate size and enables input to the AD converter. The AGC function in the AK8858 is adaptive, and thus includes peak AGC as well as sync AGC.

The AGC of the AK8858 measures the size of the input signal (i.e. the difference between the sync tip and pedestal levels), and adjusts the PGA value to bring the sync signal level to 286mV/300mV (525/625).

Peak AGC is effective for input signals in which the sync signal level is appropriate and only the active video signal is large.

In case of component video signal and S-Video signal inputs, AGC are adjust by Y sync level.

When AGC function is enables, the setting values of AGC can be read via register Gain Control Register.

Settings for AGC time constant Sub Address: 0x0A [1:0]

AGCT[1:0]-bit	Time constant	Notes
00	Disable	AGC OFF, PGA register enabled.
01	Fast	T= 1Field
10	Middle	T= 7Fields
11	Slow	T= 29Fields

T is the time constant.

Settings for AGC non-sensing range Sub Address: 0x0A [3:2]

AGCC[1:0]-bit	Non-sensing range	Notes
00	±2LSB	
01	±3LSB	
10	±4LSB	
11	None	

Settings for freezing AGC function Sub Address: 0x0A [4]

AGCFRZ-bit	AGC status	Notes
0	Non-frozen	
1	Frozen	

Settings for selection of quick or slow transition between peak and sync AGC Sub Address: 0x0B [0]

AGCTL-bit	AGC transition	Notes
0	Quick	
1	Slow	

[7.18] ACC (Auto Color Control)

The ACC of the AK8858 measures the level of the input signal color burst and adjusts to the appropriate level. The ACC is not applicable to SECAM, and YPbPr input signals.

The ACC and Color saturation functions operate independently. If ACC is enabled, the color saturation adjustment is applied to the signal that has been adjusted to the appropriate level by the ACC.

Settings for ACC time constant Sub Address: 0x0A [6:5]

ACCT[1:0]-bit	Time constant	Notes
00	Disable	ACC OFF
01	Fast	T= 2Fields
10	Middle	T= 8Fields
11	Slow	T= 30Fields

Settings for freezing ACC function Sub Address: 0x0A [7]

ACCFRZ-bit	ACC status	Notes
0	Non-frozen	
1	Frozen	

[7.19] Y/C separation

The adaptive two-dimensional Y/C separation of the AK8858 utilizes a co-relation detector to select the best-correlated direction from among vertical, horizontal, and diagonal samples, and selects the optimum Y/C separation mode.

For NTSC-4.43, PAL-60, and SECAM inputs, the Y/C separation is one-dimensional only, regardless of the setting.

Setting for Y/C separation Sub Address: 0x0C [1:0]

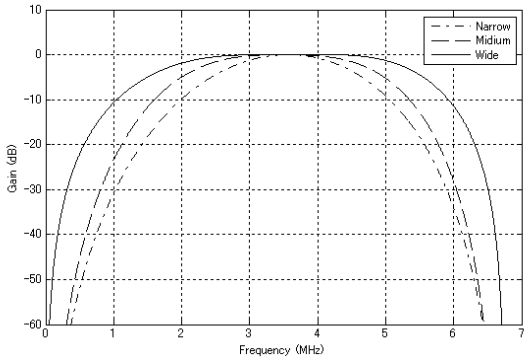
Name	Setting Value	YC separation mode	Notes
YCSEP0 ~ YCSEP1	[00]	Adaptive	
	[01]	1-D	1-D (BPF)
	[10]	2-D	(NTSC-M,J, PAL-M): 3 Line 2-D (PAL-B,D,G,H,I,N,Nc): 5 Line 2-D
	[11]	Reserved	

[7.20] C Filter

The bandwidth of the C filter can be set via register, as follows.

Settings for C filter bandwidth, for input signal with 3.58 MHz subcarrier wave. Sub Address: 0x0B [2:1]

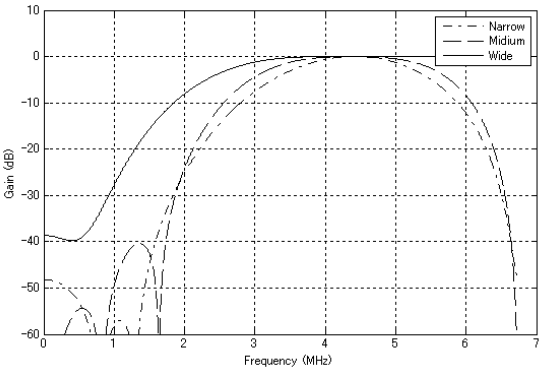
C358FIL[1:0] -bit	C filter bandwidth	Notes
00	Narrow	NTSC-M,J , PAL-M , PAL-Nc
01	Medium	
10	Wide	
11	Reserved	



Settings for C filter bandwidth, for input signal with 4.43 MHz subcarrier wave. Sub Address: 0x0B [4:3]

C443FIL[1:0] -bit	C filter bandwidth	Notes
00	Narrow	PAL-B,D,G,H,I,N , NTSC-4.43 , PAL-60
01	Medium	
10	Wide	
11	Reserved	

*Note: No bandwidth selection is possible for SECAM input.



[7.21] Clock generation

The AK8858 operates in the following three clock modes:

1. Line-locked clock mode.
2. Frame-locked clock mode
3. Fixed clock mode

The clock mode can be set via register.

[7.21.1] Line-locked clock mode

The “line-locked clock” is generated by PLL using horizontal sync signal within the input signal. If no input signal is present, the AK8858 will switch from this mode to fixed-clock mode.

[7.21.2] Frame-locked mode

The “frame-locked clock” is generated by PLL using vertical sync signal within the input signal. If no signal is present, the AK8858 will switch from this mode to fixed-clock mode.

[7.21.3] Fixed-clock mode

No PLL control is applied in this mode, which is enabled only when either it is set via the register or no input signal is present. The sampling clock in this mode is 27MHz or 54MHz. In this mode, data capture cannot be performed in EAV (end of active video), and must be performed in SAV (start of active video) format. The number of pixels per line is not guarantee in this mode, but data guarantee is performed in the interval from SAV to EAV.

In the line-locked and frame-locked clock modes, the clock is synchronized with the input signal and the output is ITU-R BT.656 compliant. It should be noted that ITU-R BT.656 compliant output may not be possible with low-quality input signals.
It should be noted that in the fixed-clock mode the sample number will be insufficient for ITU-R BT.656 compliance, due to non-synchronization of the input data.

[7.21.4] Auto transition mode

The AK8858 transition function automatically switches among the above modes and selects the optimum one, and when no input signal is present, it switches to the fixed-clock mode.

Settings for selection of clock generation mode. Sub Address 0x0C [7:6]

CLKMODE[1:0]-bit	Clock generation mode	Notes
00	Automatic	
01	Line-locked	
10	Frame-locked	
11	Fixed-clock	

[7.22] Digital Pixel Interpolar

The digital pixel interpolar of the AK8858 aligns vertical pixel positions in both frame-lock and fixed-clock operating modes. The pixel interpolar can be set to ON or OFF via register. With a register setting of AUTO, the pixel interpolar is OFF or ON depending on the clock mode, as follows.

Line-locked clock mode	OFF
Frame-locked clock mode	ON
Fixed-clock mode	ON

Settings for pixel interpolar operation Sub Address: 0x0C [5:4]

INTPOL[1:0]-bit	Interpolar operation	Notes
00	Auto	Dependent on clock mode
01	ON	
10	OFF	
11	Reserved	

[7.23] Phase correction

In PAL-B, D, G, H, I, N, Nc, 60, and M decoding, the AK8858 performs phase correction for each line. With this function ON, color averaging is performed for each line. In the adaptive phase correction mode, interline phase correlation is sampled and color averaging is performed for correlated samples.
Interline color averaging is also performed in NTSC-M and J decoding.
No phase correction or color averaging is performed in SECAM decoding.

Settings for phase correction Sub Address: 0x0D [1:0]

DPAL[1:0]-bit	Status	Notes
00	Adaptive phase correction mode	
01	Phase correction ON	
10	Phase correction OFF	
11	Reserved	

[7.24] No-signal output

If no input signal is found (as shown by control bit NOSIG-bit), the output signal is black-level, blue-level (blueback), or input-state (sandstorm), depending on the register setting.

Settings for output signals for no input signal Sub Address: 0x07 [3:2]

NSIGMD [1:0]-bit	Output	Notes
00	Black-level	
01	Blue-level (blueback)	
10	Input-state (sandstorm)	
11	Reserved	

[7.25] Output data format

AK8858 output YCbCr or RGB data.

Output format	bit
YCbCr	8bit
	16bit
RGB	24bit

Settings for YCbCr output data width Sub Address: 0x09 [0]

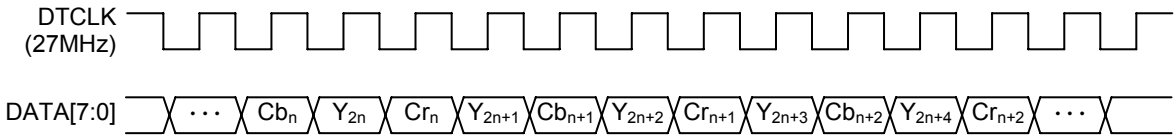
Name	Definition	Notes
ODFMT	[0]: 8bit	If RGBCNV = [1], output data is 24bit.
	[1]: 16bit	

Settings for RGB output Sub Address: 0x09 [2]

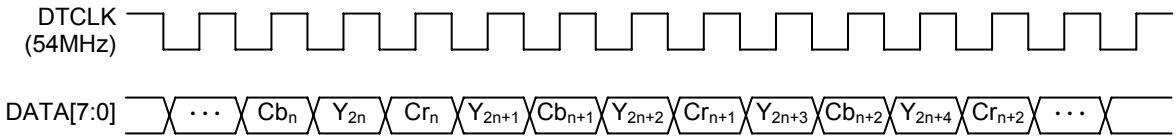
Name	Definition	Notes
RGBCNV	[0]: YCbCr [1]: RGB	If RGBCNV = [1], output data is 24bit.

[7.25.1] YCbCr 8bit output format

Interlace



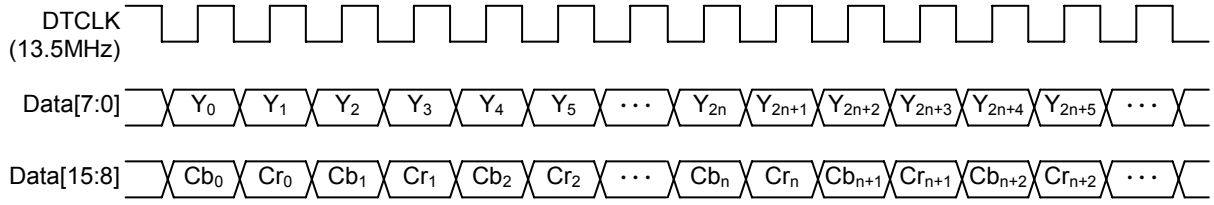
Progressive



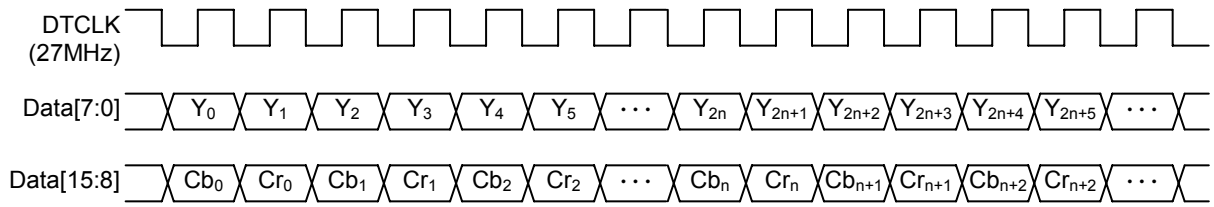
DATA[23:8] is low output.

[7.25.2] YCbCr 16bit output format

Interlace



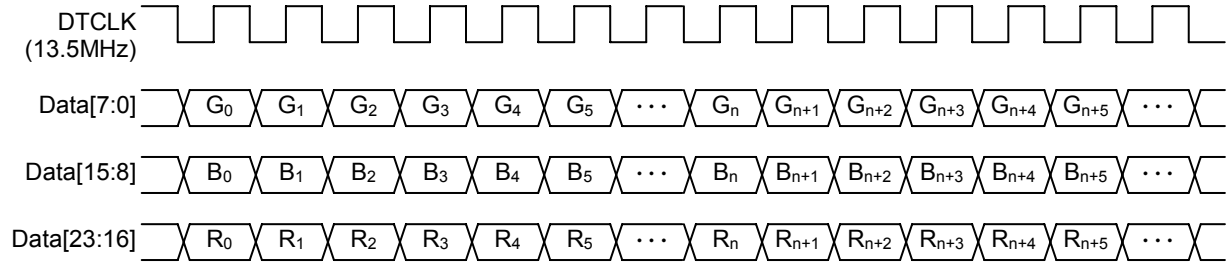
Progressive



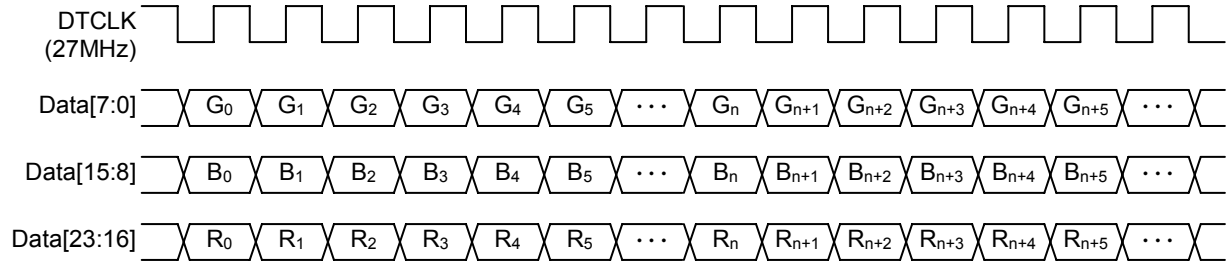
DATA[23:16] is low output.

[7.25.3] RGB 24bit output format

Interlace



Progressive



[7.26] Output Interface

[7.26.1] Interface with EAV/SAV

SYNC code is output with the output data.

[7.26.1.1] EAV/ SAV code

Those code succeeding 0xFF – 0x00 – 0x00 which are fed as input data become EAV/SAV codes.

EAV/SAV codes have following meanings, started with MSB.

Bit Number		MSB							LSB
WORD	VALUE	7	6	5	4	3	2	1	0
0	0xFF	1	1	1	1	1	1	1	1
1	0x00	0	0	0	0	0	0	0	0
2	0x00	0	0	0	0	0	0	0	0
3	0xXX (EAV/ SAV)	1	F	V	H	P3	P2	P1	P0

F=0: Field1
F=1: Field2
*In case of Progressive (525P/ 625P) output, F-bit output is always 0.

V=0: Exept for Field Blanking
V=1: Field Blanking

H=0: SAV
H=1: EAV

P3, P2, P1, P0: Protection bit

Following is a relation between protection bit and F/V/H-bit.

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0

Reference standards

Input format	Reference
525i	ITU-R.BT656
625i	ITU-R.BT656
525p	SMPTE 293M
625p	ITU-R. BT1358

[7.26.1.2] EAV/SAV code position

YCbCr 8bit 525Line

Cb 359	Y 718	Cr 359	Y 719	Cb 360	Y 720	Cr 360	Y 721	…	Cb 428	Y 856	Cr 428	Y 857	Cb 0	Y 0	Cr 0	Y 1
				0xFF	0x00	0x00	EAV		0xFF	0x00	0x00	SAV				

YCbCr 8bit 625Line

Cb 359	Y 718	Cr 359	Y 719	Cb 360	Y 720	Cr 360	Y 721	…	Cb 431	Y 862	Cr 431	Y 863	Cb 0	Y 0	Cr 0	Y 1
				0xFF	0x00	0x00	EAV		0xFF	0x00	0x00	SAV				

YCbCr 16bit 525Line

Y 718	Y 719	Y 720	Y 721	Y 722	Y 723	…	Y 854	Y 855	Y 856	Y 857	Y 0	Y 1
		0xFF	0x00	0x00	EAV		0xFF	0x00	0x00	SAV		

Only Y signal with EAV/SAV

YCbCr 16bit 625Line

Y 718	Y 719	Y 720	Y 721	Y 722	Y 723	…	Y 860	Y 861	Y 862	Y 863	Y 0	Y 1
		0xFF	0x00	0x00	EAV		0xFF	0x00	0x00	SAV		

Only Y signal with EAV/SAV

RGB 24bit 525Line

RGB 718	RGB 719	RGB 720	RGB 721	RGB 722	RGB 723	…	RGB 854	RGB 855	RGB 856	RGB 857	RGB 0	RGB 1
		0xFF	0x00	0x00	EAV		0xFF	0x00	0x00	SAV		

All of RGB signal with EAV/SAV

RGB 24bit 625Line

RGB 718	RGB 719	RGB 720	RGB 721	RGB 722	RGB 723	…	RGB 860	RGB 861	RGB 862	RGB 863	RGB 0	RGB 1
		0xFF	0x00	0x00	EAV		0xFF	0x00	0x00	SAV		

All of RGB signal with EAV/SAV

[7.26.1.3] F-bit, V-bit

Code relation between F-bit in EAV/SAV and line number.

F-bit	525i	625i	525P/625P
0	Line4~Line265	Line1~Line312	F-bit = 0
1	Line266~Line525 Line1~Line3	Line313~Line625	

Code relation between V-bit in EAV/SAV and line number.

Interlace Sub Address: 0x05 [4]

Name	Setting	525i		625i	
		V-bit=0	V-bit=1	V-bit=0	V-bit=1
TRSVSEL	[0] BT. 656-3	Line10~Line263 Line273~Line525	Line1~Line9 Line264~Line272	Line23~Line310 Line336~Line623	Line1~Line22 Line311~Line335 Line624~Line625
	[1] BT. 656-4 or SMPTE125M	Line20~Line263 Line283~Line525	Line1~Line19 Line264~Line282		

Not affected by VBIL[2:0]-bit

Progressive Sub Address: 0x05 [4]

Name	Setting	525p		625p	
		V-bit=0	V-bit=1	V-bit=0	V-bit=1
TRSVSEL	[0] SMPTE293M or EIA-770.2-A	Line43~Line525	Line1~Line42	Line45~Line620	Line1~Line44 Line621~Line625
	[1] EIA-770.2-C	Line46~Line525	Line1~Line45		

Not affected by VBIL[2:0]-bit

[7.26.1.4] exclude EAV/SAV flag

Sub Address: 0x09 [3]

Name	Definition
EAVSAV	[0]: Output data with EAV/SAV flag. [1]: Output data without EAV/SAV flag.

If LIMIT601*= [0], output code range are 0~255 (*Sub Address: 0x05 [3])

[7.26.1.5] Operating used EAV/SAV

[7.26.1.5.1] Line-locked and frame-locked clock modes

In both of these modes, the output data are compliant with ITU-R BT.656 (525i/625i), SMPTE293M (525p), and ITU-R. BT1358 (625p), which is requires the following samples and line numbers.

- Number of samples for 1 line:
  858 samples (525i/525) / 864 samples (625i/625p)
- Number of lines for 1 frame:
  525 lines / 625 lines

It may not be possible, however to meet these requirement if the input signal quality is poor.

[Line drop/repeat processing]

A line drop or a line repeat will result in output signal with 524/624 or 526/626 lines per frame respectively. Line drop/repeat processing may be performed at any line in the frame.

[Pixel drop/repeat processing]

A pixel drop or a pixel repeat will result in output signals less or more than the required 858/864 samples in the last line of the frame or field respectively.

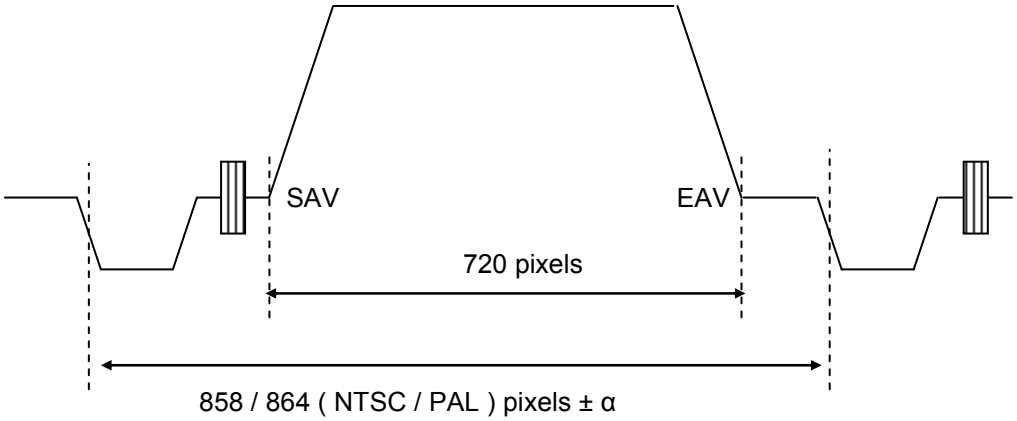
Note: In the event of output-stage buffer failure, line drop/repeat processing will be performed even if the register is for pixel drop/ repeat processing.

Line or pixel drop/repeat Sub Address: 0x0D [5:4]

ERRHND-bit	Processing mode	Notes
00	Line Drop / Line Repeat	Default
01	Pixel Drop / Pixel Repeat by Field	
10	Pixel Drop / Pixel Repeat by Frame	
11	Reserved	

[7.26.1.5.2] Fixed clock mode

In fixed-clock mode, operation is at an internally generated 27 MHz clock, from a 24.576 MHz input clock. The output signal is therefore not synchronized with the input signal, and thus not ITU-R BT.656 compliant. Data is output in SAV format. As shown in the following figure, EAV is guaranteed for 720 pixels from SAV, but the number of pixels from EAV to SAV is not.



[7.26.2] Interface used timing signal

For connection with devices having no ITU-R BT.656 interface, the AK8858 DVALID signal output identifies the active video interval by remaining low throughout that period, as shown in the following figure.
In RGB output mode, it is suggest to use this interface when output the valid data

[7.26.2.1] HD pin output

AK8858 output HD signal for horizontal synchronization.

Pin name	Interlace / Progressive	525-Line	625-Line
HD	Interlace	Low for 4.7us at 15.734 kHz interval.	Low for 4.7us at 15.625 kHz interval.
	Progressive	Low for 2.35us at 31.468 kHz interval.	Low for 2.35us at 31.250 kHz interval.

[7.26.2.2] VD_FLD or DVAL_FLD pin output

AK8858 output VD, FIELD and DVALID signal.

Pin name	Interlace / Progressive	Output	525-Line	625-Line
VD_FLD	Interlace	VD	Low output at Line4~Line6 or Line266.5~Line269.5	Low output at Line1~Line3.5 or Line313.5~Line315
		FIELD	ODD-Field: Low, EVEN-Field: High	
	Progressive	VD	Low output at Line7~Line12	Low output at Line1~Line5
		FIELD	Toggle by each flame	
DVAL_FLD	Interlace	DVALID	Low during active video interval	
		FIELD	ODD-Field: Low, EVEN-Field: High	
	Progressive	DVALID	Low during active video interval	
		FIELD	Toggle by each flame	

Select output from VD_FLD pin Sub Address: 0x07 [5]

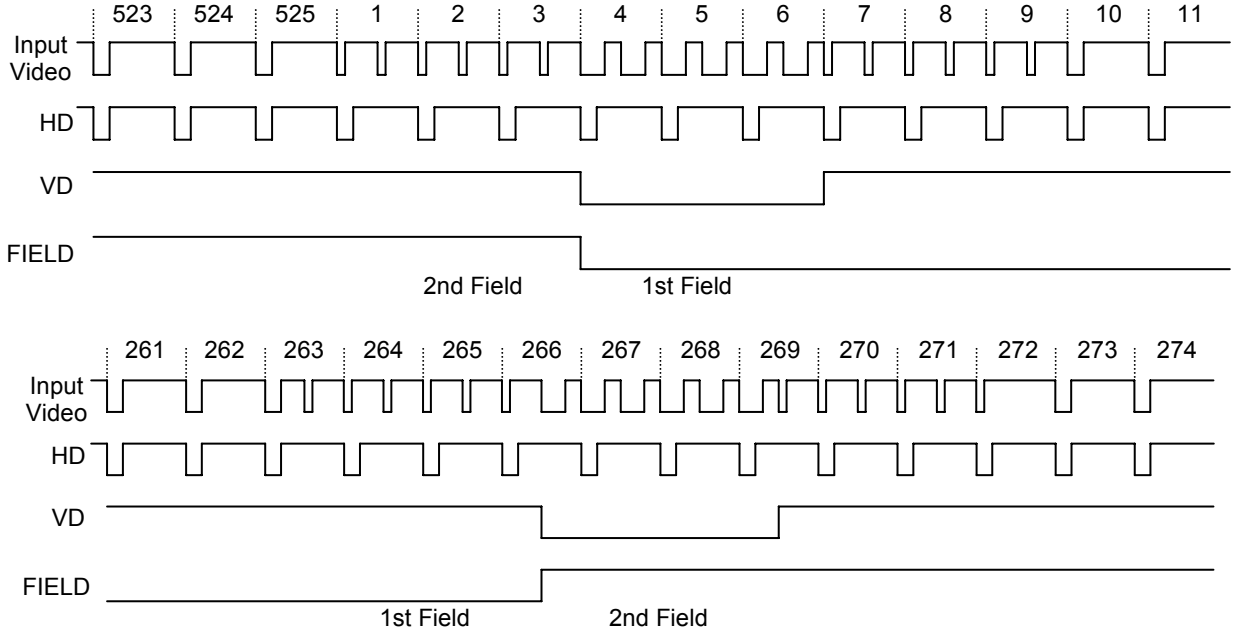
Name	Definition	Notes
VDFSEL	[0]: VD [1]: FIELD	

Select output from DVAL_FLD pin Sub Address: 0x07 [6]

Name	Definition	Notes
DVALFSEL	[0]: DVALID [1]: FIELD	

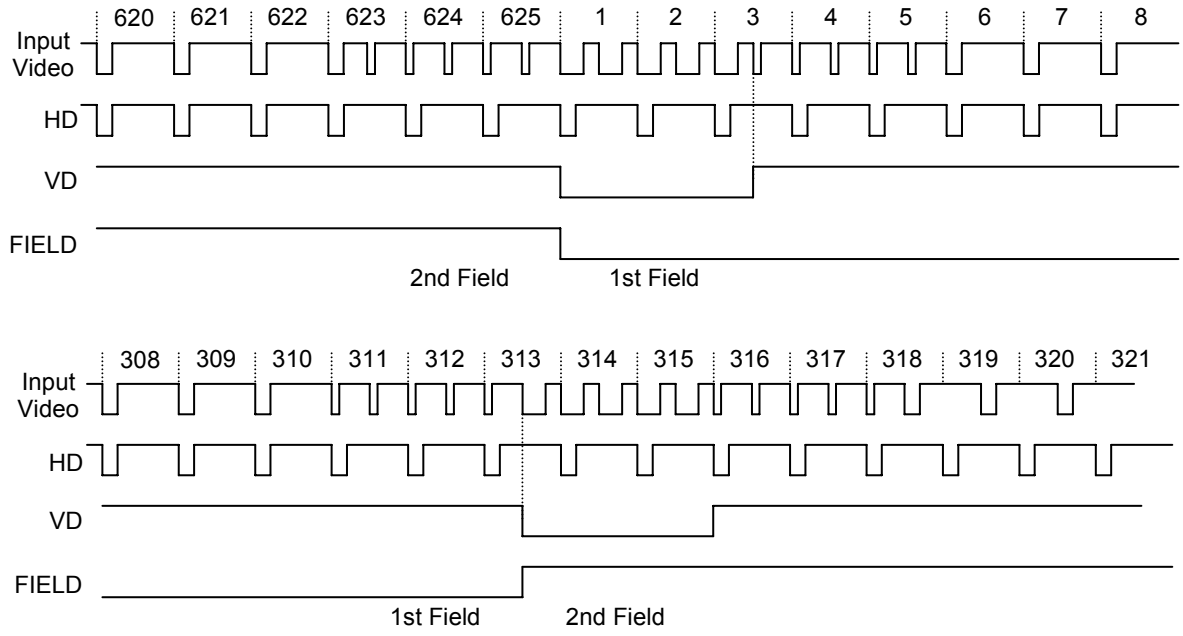
[7.26.2.3] Position of HD, VD and FIELD

[7.26.2.3.1] 525Line Interlace



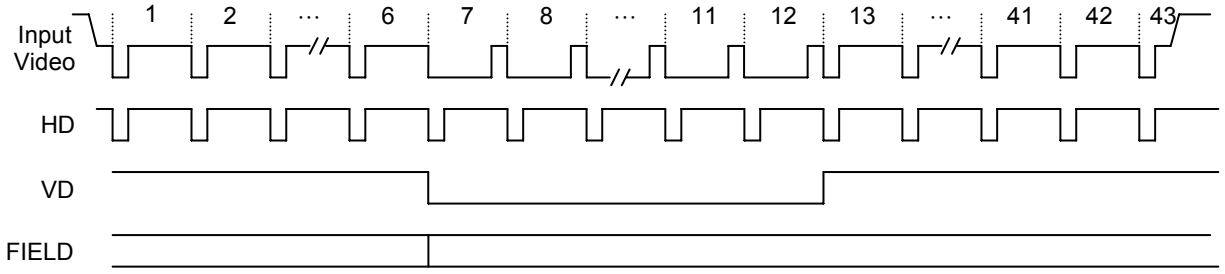
If 262 or 263 line signal input, FIELD signali is toggled.

[7.26.2.3.2] 625Line Interlace



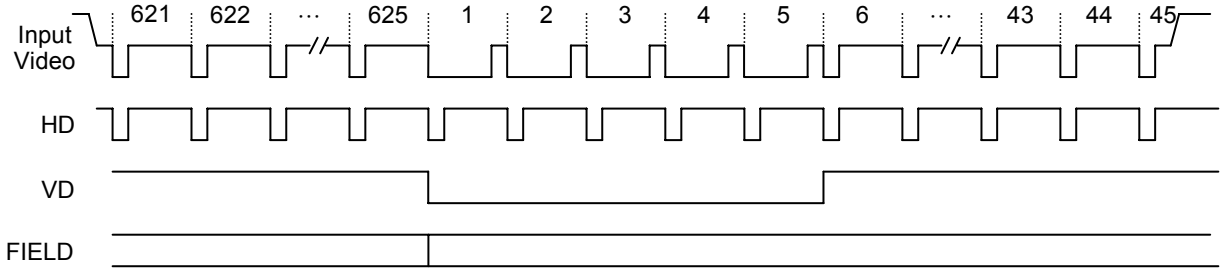
If 312 or 313 line signal input, FIELD signali is toggled.

[7.26.2.3.3] 525Line Progressive



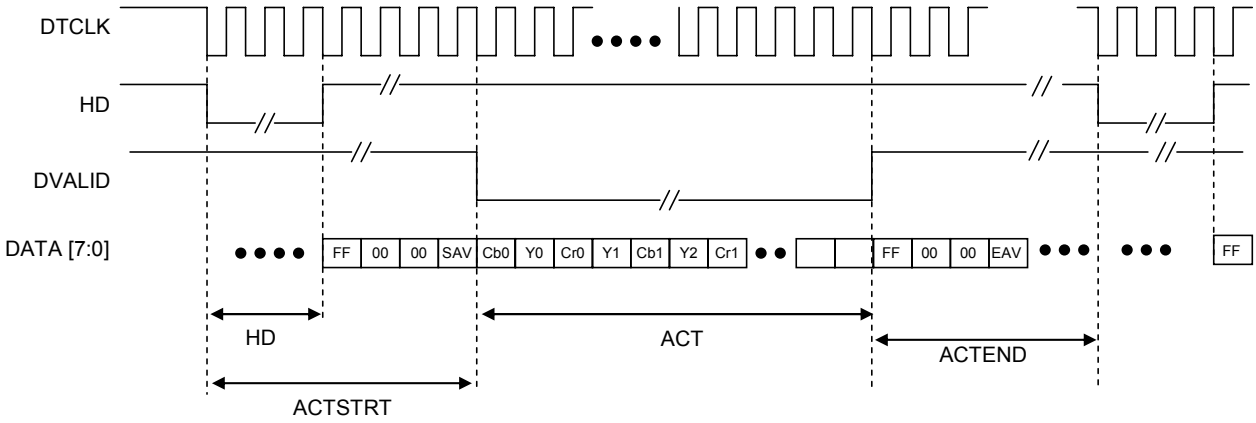
FIELD signal is toggled.

[7.26.2.3.4] 625Line Progressive



FIELD signal is toggled.

[7.26.2.4] Position of HD, DVALID and EAV/SAV code



Input signal	bit	HD (CLK)	ACTSTRT (CLK)	ACT (CLK)	ACTEND (CLK)	Notes
525Line	YCbCr 8bit	128	244	1440	32	1CLK = DTCLK rate
	YCbCr 16bit	64	122	720	16	
	RGB 24bit	64	122	720	16	
625Line	YCbCr 8bit	128	264	1440	24	
	YCbCr 16bit	64	132	720	12	
	RGB 24bit	64	132	720	12	

[7.26.2.5] Pin polarity

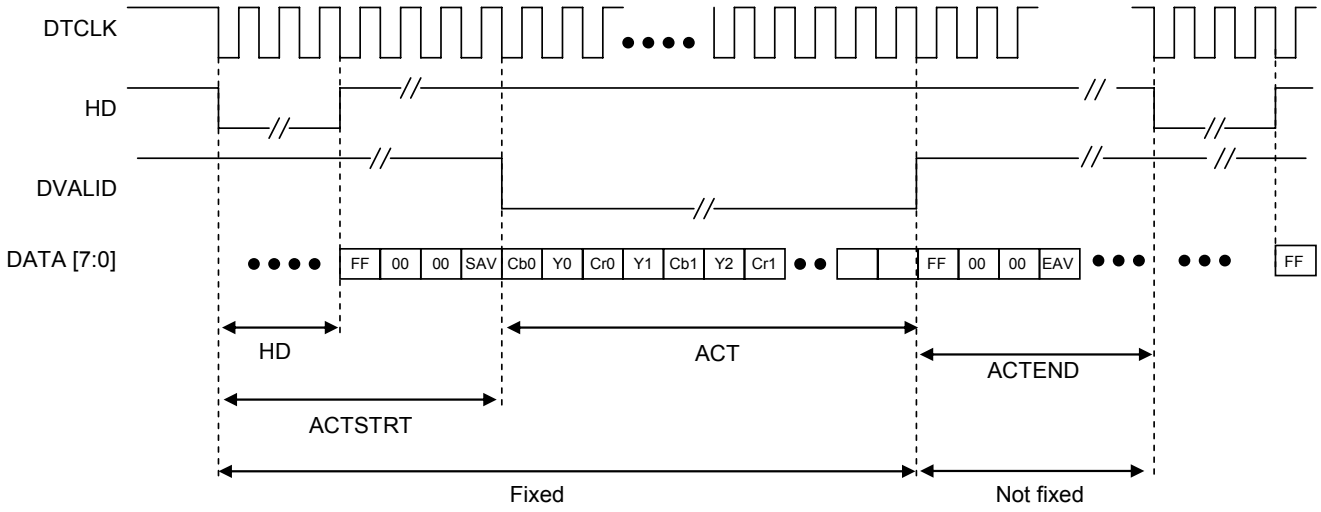
Sub Address: 0x0B [7:5]

Register Name	Pin name	Signal	Setting	
			[0]	[1]
HDP	HD	HD	Active Low	Active High
VD_FP	VD_FLD	VD	Active Low	Active High
		Field	Low: Odd-Field High: Even-Field	Low: Even-Field High: Odd-Field
DVAL_FP	DVAL_FLD	DVALID	Active Low	Active High
		Field	Low: Odd-Field High: Even-Field	Low: Even-Field High: Odd-Field

DTCLK polarity Sub Address: 0x07 [7]

Name	Definition
CLKINV	[0]: Normal output (rise edge to data) [1]: Inverted(fall edge to data)

[7.26.2.6] Timing signal on fixed clock mode



[7.27] Sync separation, sync detection, black-level detection and digital pedestal clamp

The AK8858 performs sync separation and sync detection on the digitized input signal, uses the detected sync signal as the timing reference for the decoding process, and calculates the phase error from the separated sync signal and applies it to control of the sampling clock.

The digitally converted input signal is clamped in the digital signal processing block. The internal clamp position depends on the input signal type (either 286 mV sync or 300 mV sync), but pedestal position is output as code 16 (8-Bit, ITU-R BT.601) for both types. The digital pedestal clamp function can adjust the time constant and set the coring level.

Black-level tuning can be performed in the sync separation block. The black-level fine-tuning band, which is 10 bits wide before REC 601 conversion, can be adjusted -8~+7 LSB in 1-LSB steps, with one step resulting in a change of about 0.4 LSB in the output code

Settings for digital pedestal clamp time constant Sub Address: 0x10 [5:4]

DPCT[1:0]-bit	Transition time constant	Notes
00	Fast	
01	Middle	
10	Slow	
11	Disable	Digital pedestal clamp OFF

Settings for digital clamp pedestal coring level Sub Address: 0x10 [7:6]

DPCC[1:0]-bit	Transition time constant (bit)	Notes
00	±1bit	
01	±2bit	
10	±3bit	
11	Non-coring	

Settings for black-level fine tuning Sub Address: 0x10 [3:0]

BKLVL[3:0]-bit	Code adjustment of black level	Approx. change in 601 level (LSB)
0001	+1	+0.4LSB
0010	+2	+0.8LSB
0011	+3	+1.2LSB
0100	+4	+1.6LSB
0101	+5	+2.0LSB
0110	+6	+2.4LSB
0111	+7	+2.8LSB
0000	Default	None
1000	-8	-3.2LSB
1001	-7	-2.8LSB
1010	-6	-2.4LSB
1011	-5	-2.0LSB
1100	-4	-1.6LSB
1101	-3	-1.2LSB
1110	-2	-0.8LSB
1111	-1	-0.4LSB

The black level is adjusted upward or downward by the value of the setting, which must be in 2's-complement form. Black-level adjustment is also enabled during the vertical blanking interval.

[7.28] Color killer

In CVBS or S-video input, the chroma signal quality of the input signal is determined by comparison of its color burst level against the threshold setting in the color killer control register. If the level is below the threshold, the color killer is activated, resulting in processing of the input as a monochrome signal and thus with CbCr data fixed at 0x80. Depending on the register setting, the color killer may also be activated by failure of the color decode PLL lock.

Settings for color killer ON and OFF Sub Address: 0x11 [7]

COLKILL-bit		Notes
0	Enable	
1	Disable	

Settings for color killer activation Sub Address: 0x11 [6]

CKILSEL-bit	Condition for activation	Notes
0	Burst level below threshold setting in CKLVL[3:0]-bits	
1	Burst level below threshold setting in CKLVL[3:0]-bits, or Failure of color decode PLL lock	

For threshold setting Sub Address: 0x11 [3:0]

Name	Definition
CKLVL0 ~ CKLVL3	[CKLVL3 : CKLVL0] [0000]: −29.7dB [0001]: −28.4dB [0010]: −27.2dB [0011]: −26.2dB [0100]: −25.3dB [0101]: −24.5dB [0110]: −23.7dB [0111]: −23.0dB [1000]: −22.4dB (Default) [1001]: −21.8dB [1010]: −21.2dB [1011]: −20.7dB [1100]: −20.2dB [1101]: −19.7dB [1110]: −19.3dB [1111]: −18.9dB

Used for threshold setting with SECAM input. Sub Address: 0x11 [5:4]

Name	Definition
CKSCM0 ~ CKSCM1	[CKSCM1 : CKSCM0] [00]: {CKLVL[3:0]} [01]: {0, CKLVL[3:1]} (1bit shift) [10]: {0, 0, CKLVL[3:2]} (2bit shift) [11]: Reserved

[7.29] Image quality adjustment

Image quality adjustments consist of contrast, brightness, color saturation, and hue adjustment.

[7.29.1] Contrast adjustment

Setting for contrast adjustment inclination Sub Address: 0x12 [7:0]

Register	Definition
CONT0 ~ CONT7	[CONTSEL-bit =[0]*] YOUT = (CONT / 128) x (YIN - 128) +128 [CONTSEL-bit =[1]*] YOUT = (CONT / 128) X YIN YOUT: Contrast obtained by the calculation YIN: Contrast before the calculation CONT: Contrast gain factor (register setting value) The gain factor can be set in the range {0~ (255 / 128)} in 1/128 step. Default setting value is 0x80.

As the register setting shown in the above table, contrast adjustment inclination can be selected between 50% and 0%.

Setting for contrast adjustment inclination Sub Address: 0x0D [7]

Register	Definition
CONTSEL	[0]: 50% [1]: 0%

[7.29.2] Brightness adjustment

Setting for brightness adjustment Sub Address: 0x13 [7:0]

Name	Definition
BR0 ~ BR7	YOUT = YIN + BR YOUT: Brightness obtained by the calculation YIN: Brightness before the calculation BR: Brightness gain factor (register setting value) The gain factor can be set in the range {-128 ~ 126} in 1 step. The setting is in 2's complement.

Settings for brightness and contrast adjustment status (ON/OFF) during VBI Sub Address: 0x14 [7]

Register	Status during VBI
VBIIMGCTL	[0]: Disable [1]: Enable

[7.29.3] Color saturation adjustment

In composite (CVBS) or S-Video signals mode, saturation adjustment involves multiplication of the color signal by the gain factor setting in this register. The calculated result is U/V demodulated.
In YPbPr mode, U and V value can be adjusted indivisually.

Sub Address: 0x15 [7:0]

Name		Definition
SAT0 ~ SAT7	UTONE0 ~ UTONE7	[composite (CVBS) or S-Video signals] COUT = (SAT / 128) X CIN COUT: C signal after calculation CIN: C signal before calculation SAT: Satulation factor (register setting value) [Component video signal] UOUT = (UTONE / 128) X UIN UOUT: U signal after calculation UIN: U signal before calculation UTONE: Satulation factor (register setting value) The gain factor can be set in the range 0 to 255/128, in steps of 1/128. The default value is 0x80.

Sub Address: 0x16 [7:0]

Name	Definition
VTONE0 ~ VTONE7	[Component video signal] VOUT = (VTONE / 128) X VIN VOUT: V signal after calculation VIN: V signal before calculation VTONE: Satulation factor (register setting value) The gain factor can be set in the range 0 to 255/128, in steps of 1/128. The default value is 0x80.

(Notice)
If component mode, UTONE and VTONE default value should be changed to following parameter.

UTONE [7:0] =0x70
VTONE [7:0] =0x9D

[7.29.4] HUE adjustment

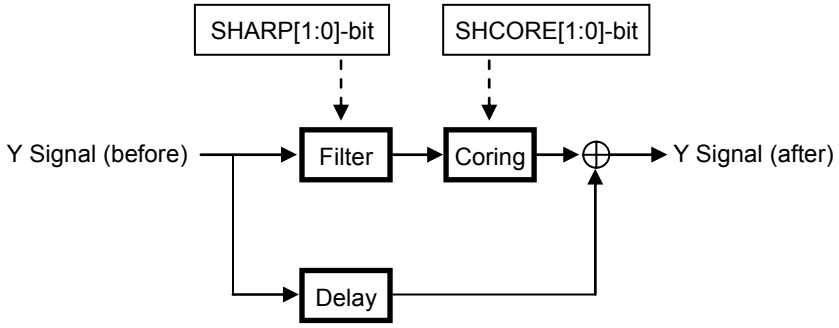
Setting for HUE adjustment Sub Address: 0x17 [7:0]

Name	Definition
HUE0 ~ HUE 7	The phase rotation can be set in the range of ±45° in 1/256step (about 0.35step). The setting is in 2's complement.

HUE adjustment only valid for composite (CVBS) and S-Video signals input.

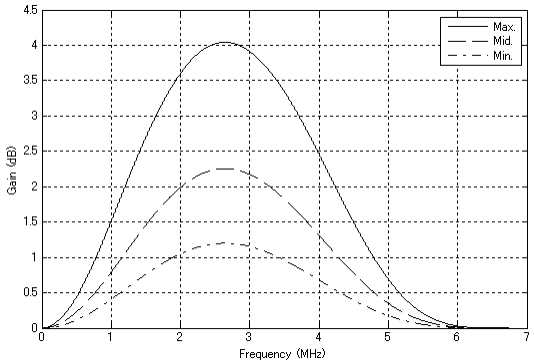
[7.29.5] Sharpness adjustment

Sharpness adjustment is performed on the luminance signal. The filter characteristic is shown in the following diagram. A sharp image can be obtained by selection of the filter with the appropriate characteristics.



Settings for filter characteristics selection Sub Address: 0x14 [1:0]

SHARP[1:0]-bit	Filter characteristics	Notes
00	No filtering	Filter disabled
01	Min	
10	Middle	
11	Max	



Settings for coring level after sharpness filtering Sub Address: 0x14 [3:2]

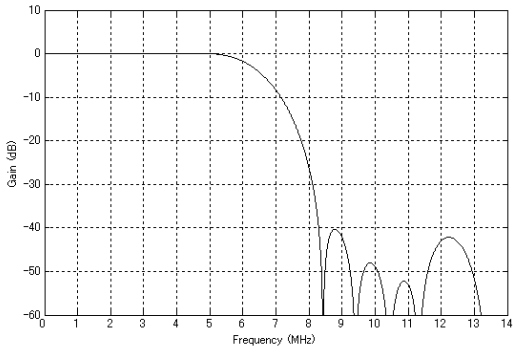
SHCORE[1:0]-bit	Coring level (LSB)	Notes
[00]	No coring	Settings apply only to filtered signal.
[01]	±1LSB	
[10]	±2LSB	
[11]	±3LSB	

[7.29.6] Luminance bandwidth adjustment

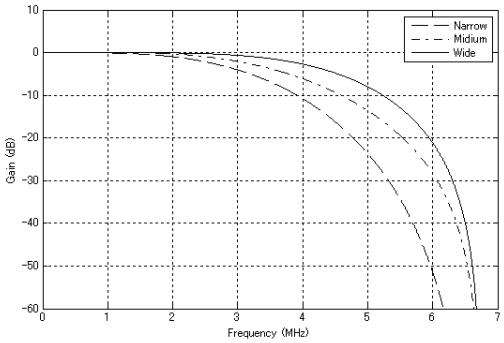
Luminance bandwidth adjustment can be performed for MPEG compression etc. The band-limiting filters for pre-compression limiting can be selected by the following register settings. Without these filters, the frequency response of the luminance signal is determined by the decimation filter.

Settings for luminance bandwidth filter Sub Address: 0x14 [5:4]

LUMFIL [1:0]-bit	Filter characteristic	Notes
00	No filter No bandwidth limit	Decimation filter characteristic -3dB at 6.29MHz
01	Narrow	-3dB at 2.94MHz
10	Mid	-3dB at 3.30MHz
11	Wide	-3dB at 4.00MHz



Luminance signal decimation filter



Luminance bandwidth filter

For 525/626p input signal, the bandwidth for each filter characteristic is expands about 2 times.

[7.29.7] Sepia output

Sepia-colored output of the decoded signal can be obtained by the following register setting.

Settings for sepia output of decoded signal Sub Address: 0x14 [6]

SEPIA –bit	Output	Notes
[0]	Normal output	
[1]	Sepia output	

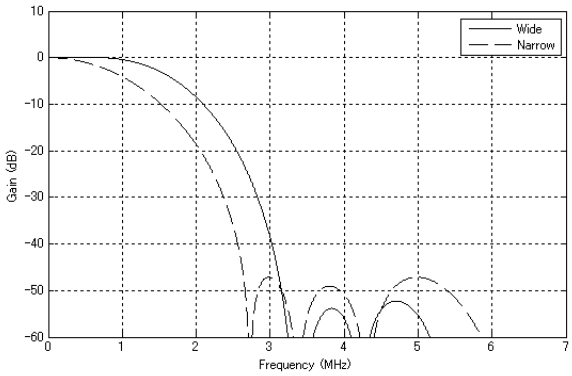
[7.29.8] U/ V Filter

U/V signal bandwidth can be set via register

[Composite (CVBS) and S-Video signal input]

Setting for U/ V filter characteristic Sub Address: 0x0C [2]

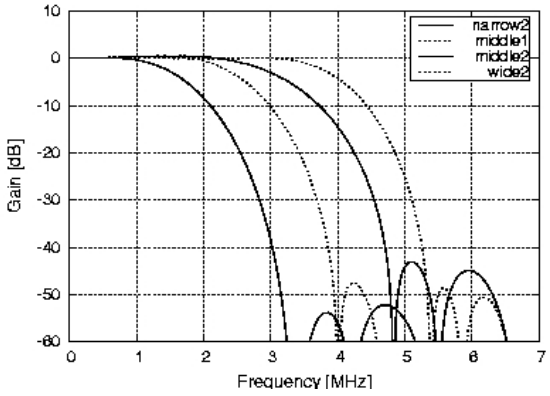
UVFILSEL0–bit	U/V filter bandwidth	Notes
0	Wide	
1	Narrow	



[YPbPr signal input]

Setting for U/ V filter characteristic Sub Address: 0x0C [3:2]

UVFILSEL[1:0] -bit	U/V filter bandwidth	Range
00	Middle 1	Narrow 2 < Middle 1 < Middle 2 < Wide 2
01	Middle 2	
10	Wide 2	
11	Narrow 2	



For 525/626p input signal, the bandwidth for each filter characteristic is expands about 2 times.

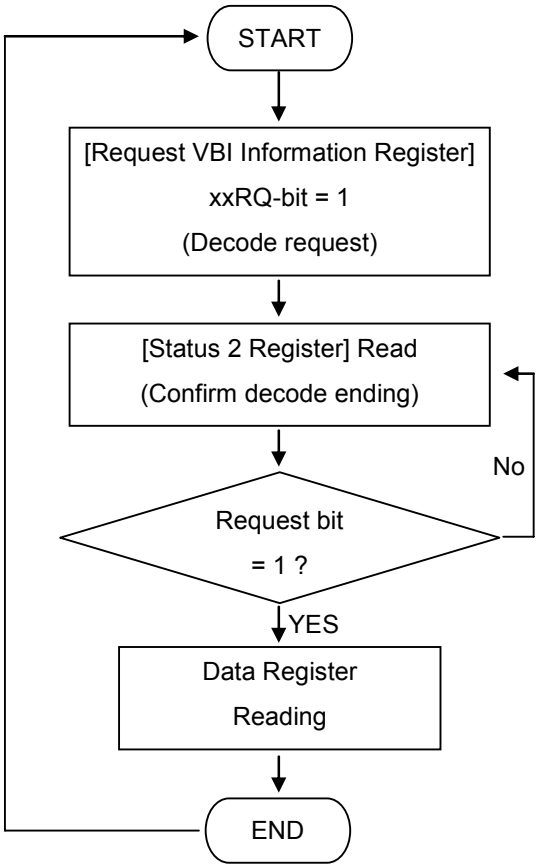
[7.30] VBI information decoding

The AK8858 decodes closed-caption, closed-caption-extended, VBID(CGMS), and WSS signals on the vertical blanking signal, and writes the decoded data into a storage register. The AK8858 reads each data bit in Request VBI Information register (Sub Address 0x1A [3:0]) as a decoding request and thereupon enters a data wait state. Data detection and decoding to the storage register are then performed which indicates the presence or absence of data at STATUS 2 register (Sub Address 0x23 [3:0]) for host. The host can therefore determine the stored values by reading the respective storage registers. The value in each storage register is retained until a new value is written in by data renewal. For VBID data (CGMS-A), the CRCC code is decoded and only the arithmetic result is stored in the register.

Signal	Line Number	Notes
Closed Caption	Line21	525i
Closed Caption Extended Data	Line284	525i
VBID	Line20 / 283 Line20 / 333 Line41	525i 625i 525p
WSS	Line23 Line43	625i 625p

Following are store registers. (Sub Address: 0x26 ~ 0x2D)
Closed Caption 1 Register, Closed Caption 2 Register, WSS 1 Register, WSS 2 Register,
Extended Data 1 Register, Extended Data 2 Register, VBID 1 Register and VBID 2 Register

Reading data flow chart



[7.31] Internal status indicators Register

[7.31.1] No signal detect

Indicates presence or absence of signal Sub Address: 0x22 [0]

Name	Setting	Definition	Notes
NOSIG	[0]	Signal detected	
	[1]	No signal detected	

[7.31.2] VLOCK status

Indicates status of VLOCK Sub Address: 0x22 [1]

Name	Setting	Definition	Notes
VLOCK	[0]	Synchronized	
	[1]	Not synchronized	

[7.31.3] Interlace Status

Indicate interlace or not of input video signal Sub Address: 0x22 [2]

Name	Setting	Definition	Notes
FRMSTD	[0]	525/625 interlace	
	[1]	not 525/625 interlace	

[7.31.4] Status of color killer operation

Indicates status of color killer Sub Address: 0x22 [3]

Name	Setting	Definition	Notes
COLKILON	[0]	Not color killer operation	
	[1]	Color killer operation	

[7.31.5] Status of clock mode

Indicates status of clock modeko Sub Address: 0x22 [5:4]

Name	Setting	Definition	Notes
SCLKMODE0 ~ SCLKMODE1	[00]	Fixed clock operation	
	[01]	Line lock clocked operation	
	[10]	Frame lock clocked operation	
	[11]	Reserved	

[7.31.6] Luminance over flow

Indicates status of luminance decode result after passage through AGC block Sub Address: 0x22 [6]

Name	Setting	Definition	Notes
PKWHITE	[0]	Normal	
	[1]	Overflow	

[7.31.7] Chrominance over flow

Indicates status of color decode result after passage through ACC block Sub Address: 0x22 [7]

Name	Setting	Definition	Notes
OVCOL	[0]	Normal	
	[1]	Overflow	

[7.31.8] Field status

Indicates decoding signal field status Sub Address: 0x23 [4]

Name	Setting	Definition	Notes
REALFLD	[0]	EVEN field	
	[1]	ODD field	

[7.31.9] AGC status

Indicates status of adaptive AGC Sub Address: 0x23 [5]

Name	Setting	Definition	Notes
AGCSTS	[0]	Sync AGC operation	
	[1]	Peak AGC operation	

[7.32] Macrovision signal detection

The AK8858 can detect a decode signal contains Macrovision signal.
The detection result can be confirmed via register.

Indicate signal contains Macrovision signal Sub Address: 0x24 [2:0]

Name	Definition
AGCDET	0: No Macrovision AGC process detected 1: Macrovision AGC process detected
CSDET	0: No Color Stripe Process detected 1: Color Stripe Process detected
CSTYPE	0: Color Stripe Type 2 in input signal 1: Color Stripe Type 3 in input signal

If detect macrovision signal on progressive decoding, AGCDET-bit = [1].

[7.32.1] Macrovision Color Stripe Cancel

This function is cancellor for macrovision color stripe. Set CSCAN bit to [1].

Color stripe cancel Sub Address: 0x03 [6]

Name	Definition
CSCAN	[0]: Color stripe on screen (Cancel function is not operated) [1]: No Color stripe on screen (Cancel function is operated)

[7.33] Auto detection result of input video signal

In auto detection mode, the result can be acknowledged by reading the following register.

Indicates result and status of auto detection mode Sub Address: 0x25 [7:0]

Name	Definition
ST_VSCF0 ~ ST_VSCF1	(CVBS or S-video signal decoding) Input video signal subcarrier frequency indicator [ST_VSCF1 : ST_VSCF0] (MHz) [00]: 3.57954545 (NTSC-M,J) [01]: 3.57561149 (PAL-M) [10]: 3.58205625 (PAL-Nc) [11]: 4.43361875 (PAL-B,D,G,H,I,N,60 , NTSC-4.43, SECAM) (Component signal decoding) Interlace or Progressive indicator [00]: Interlace [01]: Progressive [10]: Reserved [11]: Reserved
ST_VCEN0 ~ ST_VCEN1	Input signal color encode format indicator [ST_VCEN1 : ST_VCEN0] [00]: NTSC [01]: PAL [10]: SECAM [11]: Reserved
ST_VLF	Input signal line number indicator [0]: 525-Line (NTSC-M,J , NTSC-4.43 , PAL-M,60) [1]: 625-Line (PAL-B,D,G,H,I,N,Nc , SECAM)
ST_BW	Input signal monochrome indicator* [0]: Not monochrome [1]: Monochrome
UNDEF	Input signal detection indicator [0]: Input signal detected [1]: Input signal not detected
FIXED	Input signal detection process status [0]: Detection process in progress [1]: Detection process completed

*Monochrome auto detection is enabled if the color killer setting is ON (COLKILL-bit = [1]).

[8] Device control interface

The AK8858 is controlled via I2C bus control interface, as described below.

[8.1] I2C bus SLAVE Address

	Slave Address						
SELA pin status	MSB						LSB
Pulldown [Low]	1	0	0	0	1	0	0	R/W
Pullup [High]	1	0	0	0	1	0	1	R/W

[8.2] I2C control sequence

[8.2.1] Write sequence

After receiving a write-mode slave address first byte, the AK8858 receives the sub-address in the second byte and data in the subsequent bytes. The write sequence may be single-byte or multi-byte.

(a) Single-byte write sequence

S	Slave Address	w	A	Sub Address	A	Data	A	Stp
	8-bit		1-bit	8-bit	1-bit	8-bit	1-bit	

(b) Multi-byte writes sequence (Sequential Write Operation)

S	Slave Address	w	A	Sub Address(n)	A	Data(n)	A	Data (n+1)	A	,,,,,,	Data (n+m)	A	stp
	8-bit		1-bit	8-bit	1-bit	8-bit	1-bit	8-bit	1-bit		8-bit	1-bit	

[8.2.2] Read sequence

After receiving a read-mode slave address as first byte, the AK8858 sends data in the second and subsequent bytes.

S	Slave Address	w	A	Sub Address(n)	A	rS	Slave Address	R	A	Data1	A	Data2	A	Data3	A	,,,,
	8-bit		1	8-bit	1		8-bit		1	8-bit	1	8-bit	1	8-bit	1	

,,,,,,,, ,, | Data n | !A | stp |
|---|---|---|
| | 8-bit | 1 | |

S : Start Condition
rS : repeated Start Condition
A : Acknowledge (SDA Low)
!A : Not Acknowledge (SDA High)
stp : Stop Condition
R/W 1 : Read 0 : Write

: Received from master device (normally microprocessor)

: Output by slave device (AK8858)

[9] Register Definitions

Sub-Address	Register	Default	R/W	Function
0x00	Input Channel Select Regsiter	0x00	R/W	Input channel setting
0x01	Clamp Control 1	0x00	R/W	Clamp pulse setting register 1
0x02	Clamp Control 2	0x01	R/W	Clamp pulse setting register 2
0x03	Miscellaneous Setting	0x00	R/W	
0x04	Input Video Standard	0x00	R/W	Input video signal setting
0x05	Output Format	0x00	R/W	Output format setting
0x06	NDMODE	0x00	R/W	Auto detection limit setting
0x07	Output Control	0x00	R/W	Output pin status setting
0x08	Output Data Start andDelay Control	0x00	R/W	Output data timing setting
0x09	Output Data Format（YUV/RGB）	0x00	R/W	Output data format setting
0x0A	AGC & ACC Control	0x00	R/W	AGC and ACC setting
0x0B	Control 0	0x00	R/W	Control register type
0x0C	Control 1	0x00	R/W	Control register type
0x0D	Control 2	0x00	R/W	Control register type
0x0E	PGA1 Control	0x54	R/W	PGA1 gain setting
0x0F	PGA2 Control	0x54	R/W	PGA2 gain setting
0x10	Pedestal Level Control	0x00	R/W	Pedestal level adjustment
0x11	Color Killer Control	0x08	R/W	Color killer setting
0x12	Contrast Control	0x80	R/W	Contrast adjustment
0x13	Brightness Control	0x00	R/W	Brightness adjustment
0x14	Image Control	0x00	R/W	Image control setting
0x15	Saturation / U Tone Control	0x80	R/W	Saturation (Y) / Color (U)control
0x16	V Tone Control	0x80	R/W	Color (V) control
0x17	HUE Control	0x00	R/W	Hue adjustment
0x18	High Slice Data Set	0xEB	R/W	VBI Slice Data High setting
0x19	Low Slice Data Set	0x10	R/W	VBI Slice Data Low setting
0x1A	Request VBI Information	0x00	R/W	VBI interval decode request setting
0x1B ~ 0x21	Reserved	0x00	—	Reserved register
0x22	Status 1 Register		R	Internal status indicator
0x23	Status 2 Register		R	Internal status indicator
0x24	Macrovision Status Register		R	Input Macrovision signal indicator
0x25	Input Video Status Register		R	Input signal detection indicator
0x26	Closed Caption 1 Register		R	Closed caption data indicator
0x27	Closed Caption 2 Register		R	Closed caption data indicator
0x28	WSS 1 Register		R	WSS data indicator
0x29	WSS 2 Register		R	WSS data indicator
0x2A	Extended Data 1 Register		R	CC-Extended data indicator
0x2B	Extended Data 2 Register		R	CC-Extended data indicator
0x2C	VBID 1 Register		R	VBID data indicator
0x2D	VBID 2 Register		R	VBID data indicator
0x2E	Device and Revision ID	0x3A	R	Device ID / Revision ID
0x2F ～ 0x3F	Reserved	0x00	—	Reserved register

For all other registers, write-in is prohibited.
For all reserved registers, write-in must be limited to the default value.

[9.1] Register setting overview

[9.1.1] Input Channel Select Register (R/W) [Sub Address 0x00]

Input signal channel selection and clock mode selection register.

Sub Address: 0x00 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMOD	SELSRC1	SELSRC0	ADC3SEL	ADC2SEL	ADC1SEL2	ADC1SEL1	ADC1SEL0
Default Value							
0	0	0	0	0	0	0	0

Input Channel Select Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	ADC1SEL0 ~ ADC1SEL2	ADC 1 Select	R/W	ADC1 input signal selection 000: AIN1 001: AIN2 010: AIN3 011: AIN4 100: AIN5 101: AIN6
bit 3	ADC2SEL	ADC 2 Select	R/W	Virtual ADC2 input signal selection 0: AIN7 1: AIN8
bit 4	ADC3SEL	ADC 3 Select	R/W	Virtual ADC3 input signal selection 0: AIN9 1: AIN10
bit 5 ~ bit 6	SELSRC0 ~ SELSRC1	Select Source	R/C	Decode signal selection 00: Composite (CVBS) 01: S-Video 10: Component (YPbPr) 11: No input signal (Analog block is powerdown)
bit 7	CLKMOD	Clock Mode	R/W	Clock mode selection 0: For crystal 1: External clock input (clock generator etc.)

[9.1.2] Clamp Control 1 Register (R/W) [Sub Address 0x01]

Clamp pulse setting.

Sub Address: 0x01 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLP-WIDTH1	CLP-WIDTH0	CLP-STAT1	CLP-STAT0	Reserved	BCLP-STAT2	BCLP-STAT1	BCLP-STAT0
Default Value							
0	0	0	0	0	0	0	0

Clamp Control 1 Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	BCLPSTAT0 ~ BCLPSTAT2	Back Porch Clamp Start	R/W	Backporch clamp start position setting. The default position is at the center of Sync signal. [BCLPSTAT2 : BCLPSTAT0] [000]: Same position as default “CLPSTAT” [001]: (1/128)H delay from “CLPSTAT” [010]: (2/128)H delay from “CLPSTAT” [011]: (3/128)H delay from “CLPSTAT” [100]: (4/128)H advance from “CLPSTAT” [101]: (3/128)H advance from “CLPSTAT” [110]: (2/128)H advance from “CLPSTAT” [111]: (1/128)H advance from “CLPSTAT”
bit 3	Reserved	Reserved	R/W	Reserved
bit 4 ~ bit 5	CLPSTAT0 ~ CLPSTAT1	Clamp Start	R/W	Clamp pulse start position setting. The default position is at the center of horizontal Sync signal. [CLPSTAT1 : CLPSTAT0] [00]: Center of horizontal sync (default position) [01]: (1/128)H delay [10]: (2/128)H advance [11]: (1/128)H advance
bit 6 ~ bit 7	CLPWIDTH0 ~ CLPWIDTH1	Clamp Pulse Width	R/W	Clamp pulse width setting. Pulse width is change according to sampling clock units. [CLPWIDTH1 : CLPWIDTH0] [00]: 7-clk [01]: 15-clk [10]: 31-clk [11]: 63-clk

[9.1.3] Clamp Control 2 Register (R/W) [Sub Address 0x02]

Clamp pulse control setting.

Sub Address: 0x02 Default Value: 0x01

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	YPBPRCP	UDG1	UDG0	CLPG1	CLPG0
Default Value							
0	0	0	0	0	0	0	1

Clamp Control 2 Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	CLPG0 ~ CLPG1	Clamp Gain	R/W	Current value of fine clamp in analog circuit setting CLPG[1:0] 00: Min 01: Middle 1 (default) 10: Middle 2 11: Max
bit 2 ~ bit 3	UDG0 ~ UDG1	Up Down Gain	R/W	Current value of rough clamp in analog circuit setting [UDG1 : UDG0] 00: Min (default) 01: Middle 1 10: Middle 2 11: Max
bit 4	YPBPRCP	YPbPr Clamp	R/W	Clamp position of PbPr signal input setting 0: YPbPr sync tip timing 1: Y sync tip timing / PbPr backporch
bit 5 ~ bit 7	Reserved	Reserved	R/W	Reserved

[9.1.4] Miscellaneous Setting Register (R/W) [Sub Address 0x03]

Sub Address: 0x03 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VERTS	CSCAN	Reserved	CMPSEL	CSCL	CSSL	Reserved	Reserved
Default Value							
0	0	0	0	0	0	0	0

Miscellaneous Setting Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	Reserved	Reserved	R/W	Reserved
bit 2	CSSL	Component Signal Sync Level	R/W	YPbPr signal sync / luminance ratio level setting 0: 300/700 1: 286/714
bit 3	CSCL	Component Signal Color Level	R/W	Color (PbPr) signal level setting 0: 700mV 1: 714mV
bit 4	CMPSEL	Component Signal Select	R/W	Component signal input, interlace / progressive setting (auto detection mode is disable). 0: Interlace (525i/625i) 1: Progressive (525p/625p)
bit 5	Reserved	Reserved	R/W	Reserved
bit 6	CSCAN	Color stripe cancel	R/W	Color stripe cancel operation* 0: not operated 1: operated
bit 7	VERTS	Vertical SYNC way	R/W	Vertical sync mechanism setting 0: VLOCK mechanism 1: Direct lock mechanism

* Set CSCAN to [1].

[9.1.5] Input Video Standard Register (R/W) [Sub Address 0x04]

Input signal setting.

Sub Address: 0x04 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AUTODET	SETUP	BW	VLF	VCEN1	VCEN0	VSCF1	VCSF0
Default Value							
0	0	0	0	0	0	0	0

Input Video Standard Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	VSCF0 ~ VSCF1	Video Sub-Carrier Frequency	R/W	Input video signal subcarrier frequency setting [VSCF1:VSCF0] 00: 3.57954545 MHz (NTSC) 01: 3.57561149 MHz (PAL-M) 10: 3.58205625 MHz (PAL-Nc) 11: 4.43361875 MHz (PAL-B,D,G,H,I,N)*
bit 2 ~ bit 3	VCEN0 ~ VCEN1	Video Color Encode	R/W	Input signal color encode format setting [VCEN1:VCEN0] 00: NTSC 01: PAL 10: SECAM 11: Reserved (prohibited)
bit 4	VLF	Video Line Frequency	R/W	Input signal line frequency setting 0: 525 1: 625
bit 5	BW	Black & White	R/W	Monochrome mode (ON/OFF) setting *2 [0] : Monochrome mode OFF [1] : Monochrome mode ON
bit 6	SETUP	Setup	R/W	Setup process setting [0] : Process as input signal with no setup [1] : Process as input signal with setup
bit 7	AUTODET	Video Standard Auto Detect	R/W	Input signal auto detection setting [0]: OFF (auto detection disabled; set manually) [1]: ON (auto detection enabled)

* For SECAM input signal,change VSCF[1:0] setting to [11]

[9.1.6] Output Format Register (R/W) [Sub Address 0x05]

Output data format setting.

Sub Address: 0x05 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIDEC1	VBIDEC0	SLLVL	TRSVSEL	601LIMIT	VBIL2	VBIL1	VBIL0
Default Value							
0	0	0	0	0	0	0	0

Output Format Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	VBIL0 ~ VBIL2	Vertical Blanking Interval Length	R/W	Vertical blanking interval length setting, entered as difference from the default settings The default settings are: (525i) Line1~Line19 and Line263.5~Line282.5 (625i) Line623.5~Line23.5 and Line311~Line335 (525p) Line1~Line42 (625p) Line 621~Line625 and Line1~Line44 Examples of lengthening and shortening: If lengthened 1 line, the interval becomes (525i) Line1~Line20 and Line263.5~Line283.5 (625i) Line623.5~Line24.5 and Line311~Line336 (525p) Line1~Line43 (625p) Line 621~Line625 and Line1~Line45 If shortened 1 line, the interval becomes (525i) Line1~Line18 and Line263.5~Line281.5 (625i) Line623.5~Line22.5 and Line311~Line334 (525p) Line1~Line41 (625p) Line 621~Line625 and Line1~Line43 [VBIL2 : VBIL0] [001]: VBI lengthened 1 line [010]: VBI lengthened 2 lines [011]: VBI lengthened 3 lines [000]: Default [101]: VBI shortened 3 lines [110]: VBI shortened 2 lines [111]: VBI shortened 1 line [100]: Reserved
bit 3	601LIMIT	601 Output Limit	R/W	Output data code limit (Min-Max) setting 0: 1-254 (Y/CbCr) 1: 16-235 (Y), 16-240 (Cb/Cr)
bit 4	TRSVSEL	Time Reference Signal V Select	R/W	Setting of lines for “Time reference signal” V-bit value change in ITU-R BT.656 format 0: ITU-R Bt.656-3 1: ITU-R Bt.656-4 and SMPTE125M
bit 5	SLLVL	Slice Level	R/W	Slice level setting 0: Slice level approx. 25 IRE 1: Slice level approx. 50 IRE
bit 6 ~ bit 7	VBIDEC0 ~ VBIDEC1	VBI Decode	R/W	Setting for type of data output during interval set in Vertical Blanking Interval register * [VBIDEC1: VBIDEC0] [00]: Black level data output [01]: Monochrome data output [10]: Slice result data output [11]: Reserved

[9.1.7] NDMODE Register (R/W) [Sub Address 0x06]

Limiting auto input video signal detection candidates register setting

Sub Address: 0x06 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ND625L	ND525L	NDPAL60	NDNTSC443	Reserved	NDSECAM	NDPALNC	NDPALM
Default Value							
0	0	0	0	0	0	0	0

NDMODE Register

BIT	Register Name		R/W	Definition
bit 0	NDPALM	No Detect PAL-M	R/W	0: PAL-M candidate 1: PAL-M non-candidate
bit 1	NOPALNC	No Detect PAL-NC	R/W	0: PAL-Nc candidate 1: PAL-Nc non-candidate
bit 2	NDSECAM	No Detect SECAM	R/W	0: SECAM candidate 1: SECAM non-candidate
bit 3	Reserved	Reserved	R/W	Reserved
bit 4	NDNTSC443	No Detect NTSC-4.43	R/W	0: NTSC-4.43 candidate 1: NTSC-4.43 non-candidate
bit 5	NDPAL60	No Detect PAL60	R/W	0: PAL-60 candidate 1: PAL-60 non-candidate
bit 6	ND525L	No Detect 525 Line	R/W	0: 525 line candidate 1: 525 line non-candidate
bit 7	ND625L	No Detect 625 Line	R/W	0: 625 line candidate 1: 625 line non-candidate

In making the above register settings, the following restrictions apply,

1. Setting both NDNTSC443(bit 4) and NDPAL60(bit 5) to [1] (High) is prohibited.
2. Setting both ND525L(bit 6) and ND625L(bit 7) to [1] (High) is prohibited.
3. To limit candidate formats, it is necessary to have the auto detection mode OFF while first setting the register to non-limited signal status and next the NDMODE settings, and then setting the auto detection mode to ON.

[9.1.8] Output Control Register (R/W) [Sub Address 0x07]

Output pin status register setting.

Sub Address: 0x07 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKINV	DVALFSEL	VDFSEL	HL	NL	DVALFL	VDFL	DL
Default Value							
0	0	0	0	0	0	0	0

Output Control Register

BIT	Register Name		R/W	Definition
bit 0	DL	Data Output Low bit	R/W	0: Normal output 1: [D17: D0] pin output fixed at Low
bit 1	VDFL	VD_FLD Output Low bit	R/W	0: Normal output 1: VD_FLD pin output fixed at Low
bit 2	DVALFL	DVAL_FLD Output Low bit	R/W	0: Normal output 1: DVAL_FLD pin output fixed at Low
bit 3	NL	NSIG Output Low bit	R/W	0: Normal output 1: NSIG pin output fixed at Low
bit 4	HL	HD Output Low bit	R/W	0: Normal output 1: HD pin output fixed at Low
bit 5	VDFSEL	VD_FLD Select bit	R/W	0: VD signal output 1: FIELD signal output
bit 6	DVALFSEL	DVAL_FLD Select bit	R/W	0: DVALID signal output 1: FIELD signal output
bit 7	CLKINV	Clock Invert Setting	R/W	0: Normal output (write in data at rising edge) 1: Data and clock reversed (write in data at falling edge)

Note: Output control via pins OE, PDN, and RSTN takes priority, regardless of the above settings.

[9.1.9] Output Data Start and Delay Control Register (R/W) [Sub Address 0x08]

Ouput data timing setting register.

Sub Address: 0x08 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	ACTSTAT2	ACTSTAT1	ACTSTAT0	Reserved	YCDELAY2	YCDELAY1	YCDELAY0
Default Value							
0	0	0	0	0	0	0	0

Output Data Start and Delay Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	YCDEALY0 ~ YCDELAY2	YC Delay Control	R/W	Adjustment of Y and C timing. In D1 decode, delay or advance 1 sample unit is about 74ns In D2 decode, delay or advance 1 sample unit is about 37ns. YCDELAY[2:0] [001]: Y advance 1-sample toward C. [010]: Y advance 2-sample toward C. [011]: Y advance 3-sample toward C. [000]: No Delay and advance. [101]: Y delay 3-sample toward C. [110]: Y delay 2-sample toward C. [111]: Y delay 1-sample toward C. [100]: Reserved
bit 3	Reserved	Reserved	R/W	Reserved
bit 4 ~ bit 6	ACTSTA0 ~ ACTSTA2	Active Video Start Control	R/W	Fine-tuning video data decode start position In D1 decode, delay or advance 1 sample unit is about 74ns In D2 decode, delay or advance 1 sample unit is about 37ns. ACTSTA[2:0] [001]: 1-sample delay [010]: 2-sample delay [011]: 3-sample delay [000]: Normal start position [101]: 3-sample advance [110]: 2-sample advance [111]: 1-sample advance [100]: Reserved
bit 7	Reserved	Reserved	R/W	Reserved

[9.1.10] Output Data Format Register (R/W) [Sub Address 0x09]

Output data format setting register.

Sub Address: 0x09 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	EAVSAV	RGBO	Reserved	ODFMT
Default Value							
0	0	0	0	0	0	0	0

Output Data Format Register

BIT	Register Name		R/W	Definition
bit 0	ODFMT	Output Data Format	R/W	YCbCr output bit-width setting 0: 8-bit output 1: 16-bit output
bit 1	Reserved	Reserved	R/W	Reserved
bit 2	RGBO	RGB Convert	R/W	RGB convert output selection: 0: YCbCr data is output 1: RGB data is output
bit 3	EAVSAV	EAVSAV Disable	R/W	EAV/SAV output (ON/OFF) setting. 0: EAV/SAV ON EAV/SAV is superimposed to Y or R/G/B data. 1: EAV/SAV OFF
bit 4 ~ bit 7	Reserved	Reserved	R/W	Reserved

[9.1.11] AGC & ACC Control Register (R/W) [Sub Address 0x0A]

AGC and ACC setting register.

Sub Address: 0x0A Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ACCFRZ	ACC1	ACC0	AGCFRZ	AGCC1	AGCC0	AGCT1	AGCT0
Default Value							
0	0	0	0	0	0	0	0

AGC & ACC Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	AGCT0 ~ AGCT1	AGC Time Constance	R/W	AGC time constant (T) setting (if disabled, PGA can be set manually). AGCT[1:0] 00: Disable 01: Fast [T = 1Filed] 10: Middle [T = 7Filed] 11: Slow [T = 28Filed]
bit 2 ~ bit 3	AGCC0 ~ AGCC1	AGC Coring Control	R/W	AGC non-sensing bandwidth (LSB) setting AGCC[1:0] 00: ±2 LSB 01: ±3 LSB 10: ±4 LSB 11: No non-sensing band
bit 4	AGCFRZ	AGC Freeze	R/W	AGC freeze function (ON/OFF) setting (AGC set values are saved during freeze) 0: Non-frozen 1: Frozen
bit 5 ~ bit 6	ACCT0 ~ ACCT1	ACC Time Constance	R/W	ACC time constant (T) setting ACCT[1: 0] 00: Disable 01: Fast [T = 2Fields] 10: Middle [T =8Fields] 11: Slow [T = 30Fields]
bit 7	ACCFRZ	ACC Freeze	R/W	ACC freeze function (ON/OFF) setting (ACC set values are saved during freeze) 0: Non-frozen 1: Frozen

[9.1.12] Control 0 Register (R/W) [Sub Address 0x0B]

Sub Address: 0x0B Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DVAL_FP	VD_FP	HDP	C443FIL1	C443FIL0	C358FIL1	C358FIL0	AGCTL
Default Value							
0	0	0	0	0	0	0	0

Control 0 Register

BIT	Register Name		R/W	Definition
bit 0	AGCTL	AGC Transition Level	R/W	Transition speed setting, between peak AGC and sync AGC 0: QUICK 1: SLOW
bit 1 ~ bit 2	C358FIL0 ~ C358FIL1	C Filter 358 Select	R/W	C-filter bandwidth setting, for 3.58 MHz subcarrier system signal C358FIL[1:0] 00: Narrow 01: Middle 10: Wide 11: Reserved
bit 3 ~ bit 4	C443FIL0 ~ C443FIL1	C Filter 443 Select	R/W	C-filter bandwidth setting, for 4.43 MHz subcarrier system signal C443FIL[1:0] 00: Narrow 01: Middle 10: Wide 11: Reserved
bit 5	HDP	HD pin Polarity	R/W	HD signal polarity setting 0: ACTIVE LOW 1: ACTIV HIGH
bit 6	VD_FP	VD_F Pin Polarity	R/W	VD_FLD pin output signal polarity setting If VD signal is output 0: ACTIVE LOW 1: ACTVIE HIGH If FIELD signal is output 0: LOW=ODD / HIGH=EVEN 1: LOW=EVEN / HIGH=ODD
bit 7	DVAL_FP	DVAL_FLD pin Polarity	R/W	DVAL_FLD pin output signal polarity setting If DVALID signal is output 0: ACTIVE LOW 1: ACTVIE HIGH If FIELD signal is output 0: LOW=ODD / HIGH=EVEN 1: LOW=EVEN / HIGH=ODD

[9.1.13] Control 1 Register (R/W) [Sub Address 0x0C]

Sub Address: 0x0C Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	INTPOL1	INTPOL0	UVFILSEL1	UVFILSEL0	YCSEP1	YCSEP0
Default Value							
0	0	0	0	0	0	0	0

Control 1 Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	YCSEP0 ~ YCSEP1	YC Separation Control	R/W	Y/C separation setting YCSEP[1:0] 00: Adaptive Y/C separation 01: 1-dimensional Y/C separation 10: 2-dimensional Y/C separation 11: Reserved
bit 2 ~ bit 3	UVFILSEL0 ~ UVFILSEL1	UV Filter Select	R/W	UV filter setting (CVBS or S-video input) UVFILSEL0 0: Wide 1 1 Narrow 1 (YPbPr input) 00: Middle 1 01: Middle 2 10: Wide 2 11: Narrow 2
bit 4 ~ bit 5	INTPOL0 ~ INTPOL1	Interpolator Mode Select	R/W	Pixel interpolator setting INTPOL[1:0] 00: Auto 01: ON 10: OFF 11: Reserved
bit 6 ~ bit 7	CLKMODE0 ~ CLKMODE1	Clock Mode Select	R/W	Clock mode setting CLKMODE[1:0] 00: Automatic transition mode 01: Line-locked clock mode 10: Frame-locked clock mode 11: Fixed-clock mode

[9.1.14] Control 2 Register (R/W) [Sub Address 0x0D]

Sub Address: 0x0D Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONTSEL	STUPATOFF	ERRHND1	ERRHND0	NSIGMD1	NSIGMD0	DPAL1	DPAL0
Default Value							
0	0	0	0	0	0	0	0

Control 2 Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	DPAL0 ~ DPAL1	Deluxe PAL	R/W	Setting for color averaging (PAL phase correction block) Also applicable to NTSC. DPAL[1:0] 00: Adaptive phase correction ON 01: Phase correction ON 10: Phase correction OFF 11: Reserved
bit 2 ~ bit 3	NSIGMD0 ~ NSIGMD1	NSIG mode select	R/W	Setting for output on no-signal detection NSIGMD[1:0] 00: Black-level output (Y=0x10/CbCr=0x80) 01: Blue-level (Blueback) output (Y=0x29/Cb=0xF0/Cr=0x6E) 10: Input status (sandstorm) output 11: Reserved
bit 4 ~ bit 5	ERRHND0 ~ ERRHDN1	656 Error Handling	R/W	Setting for processing if ITU-R Bt.656 output is not possible ERRHND[1:0] 00: Line drop or repeat 01: Pixel drop or repeat, in final line of field 10: Line drop or repeat, in final line of frame 11: Reserved
bit 6	STUPATOFF	Setup Auto Control Off	R/W	Setup auto switching setting (ON/OFF) in auto signal detection mode 0: Auto setup switching ON 1: Auto setup switching OFF
bit 7	CONTSEL	Contrast Select	R/W	Contrast selector 0: 50% 1: 0%

[9.1.15] PGA1 Control Register (R/W) [Sub Address 0x0E]

PGA1 gain control register setting.

Sub Address: 0x0E Default Value: 0x54

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
APGA1_1	APGA1_0	DPGA1_5	DPGA1_4	DPGA1_3	DPGA1_2	DPGA1_1	DPGA1_0
Default Value							
0	1	0	1	0	1	0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	DPGA1_0 ~ DPGA1_5	Digital PGA1 Control	R/W	Digital PGA1 gain setting. PGA gain is set by following equation.
bit 6 ~ bit 7	APGA1_0 ~ APGA1_1	Analog PGA1 Control	R/W	Analog PGA1 gain setting. [00]: −3dB [01]: 0dB [10]: +3dB [11]: +6dB

Digital PGA gain equation:

$$\text{Gain(dB)} = 20LOG\left(\frac{(5\times PGA)+497}{512}\right)$$

*PGA: PGA1 or PGA2 register value (Decimal)

Default gain setting is 0x54(HEX)=1.3dB. (Analog:0dB + Digital:1.3dB)

[9.1.16]PGA2 Control Register (R/W) [Sub Address 0x0F]

PGA2 gain control register setting.

Sub Address: 0x0F Default Value: 0x54

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
APGA2_1	APGA2_0	DPGA2_5	DPGA2_4	DPGA2_3	DPGA2_2	DPGA2_1	DPGA2_0
Default Value							
0	1	0	1	0	1	0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	DPGA2_0 ~ DPGA2_5	Digital PGA1 Control	R/W	Digital PGA2 gain setting. PGA gain is set by above equation.
bit 6 ~ bit 7	APGA2_0 ~ APGA2_1	Analog PGA1 Control	R/W	Analog PGA2 gain setting. [00]: −3dB [01]: 0dB [10]: +3dB [11]: +6dB

[9.1.17] Pedestal Level Control Register (R/W) [Sub Address 0x10]

Pedestal level control register setting.

Sub Address: 0x10 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DPCC1	DPCC0	DPCT1	DPCT0	BKLVL3	BKLVL2	BKLVL1	BKLVL0
Default Value							
0	0	0	0	0	0	0	0

Pedestal Level Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	BKLVL0 ~ BKLVL3	Black Level	R/W	Setting for change from current pedestal level by adding to or subtracting from black level BKLVL[3 : 0] 0001: Add 1 0010: Add 2 0011: Add 3 0100: Add 4 0101: Add 5 0110: Add 6 0111: Add 7 0000: Default 1000: Subtract 8 1001: Subtract 7 1010: Subtract 6 1011: Subtract 5 1100: Subtract 4 1101: Subtract 3 1110: Subtract 2 1111: Subtract 1
bit 4 ~ bit 5	DPCT0 ~ DPCT1	Digital Pedestal Clamp Control	R/W	Time-constant setting for digital pedestal clamp DPCT[1:0] 00: Fast 01: Middle 10: Slow 11: Disable
bit 6 ~ bit 7	DPCC0 ~ DPCC1	Digital Pedestal Clamp Coring	R/W	Non-sensing bandwidth setting for digital pedestal clamp DPCC[1: 0] 00: +/-1bit 01: +/-2bit 10: +/-3bit 11: No non-sensing band

[9.1.18] Color Killer Control Register (R/W) [Sub Address 0x11]

Color killer register.

Sub Address: 0x11 Default Value: 0x08

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
COLKIL	CKILSEL	CKSCM1	CKSCM0	CKLVL3	CKLVL2	CKLVL1	CKLVL0
Default Value							
0	0	0	0	1	0	0	0

Color Killer Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	CKLVL0 ~ CKLVL3	Color Killer Level	R/W	Burst level setting for color killer activation Default value, approx. −23 dB.
bit 4 ~ bit 5	CKSCM0 ~ CKSCM1	Color Killer Lever for SECAM	R/W	Burst level setting for color killer activation in SECAM mode Adds 2 bits to CKLVL[3:0]
bit 6	CKILSEL	Color Killer Select	R/W	Color killer operational mode setting 0: Activation when burst color level is below than CKLVL[3:0]-bit threshold setting. 1: Activation when burst color level is below than CKLVL[3:0]-bit threshold setting or color decode PLL lock fails.
bit 7	COLKIL	Color Killer Set	R/W	Color killer ON/OFF setting 0: Enable 1: Disable

[9.1.19] Contrast Control Register (R/W) [Sub Address 0x12]

Contrast adjustment setting register.

Sub Address: 0x12 Default Value: 0x80

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
1	0	0	0	0	0	0	0

Contrast Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	CONT0 ~ CONT7	Contrast Control	R/W	Register for contrast adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80

[9.1.20]Brightness Control Register (R/W) [Sub Address 0x13]

Brightness adjustment setting register

Sub Address: 0x13 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

Brightness Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	BR0 ~ BR7	Brightness Control	R/W	Register for brightness adjustment in steps of 1 by 8-bit code setting in 2's complement

[9.1.21] Image Control Register (R/W) [Sub Address 0x14]

Sharpness control, Luminance bandwidth filter control, Sepia color output setting and VBI interval setting register.

Sub Address: 0x14 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIIMGCTL	SEPIA	LUMFIL1	LUMFIL0	SCCORE1	SHCORE0	SHARP1	SHARP0
Default Value							
0	0	0	0	0	0	0	0

Image Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	SHARP0 ~ SHARP1	Sharpness Control	R/W	Sharpness control (filter effect) setting SHARP[1: 0] 00: No filtering 01: Min effect 10: Middle effect 11: Max effect
bit 2 ~ bit 3	SHCORE0 ~ SHCORE1	Sharpness Coring	R/W	Setting for level of coring after passage through sharpness filter SHCORE[1:0] 00: No coring 01: ±1LSB 10: ±2LSB 11: ±3LSB
bit 4 ~ bit 5	LUMFIL0 ~ LUMFIL1	Luminance Filter	R/W	Setting for luminance band limit filter LUMFIL[1:0] 00: No filtering 01: Narrow 10: Mid 11: WIDE
bit 6	SEPIA	Sepia Output	R/W	Setting (ON/OFF) for sepia coloring of decode results 0: Normal output 1: Sepia output
bit 7	VBIIMGCTL	VBI Image Control	R/W	Setting (ON/OFF) for image adjustment during brightness and contrast adjustment VBI 0: Image adjustment inactive during VBI 1: Image adjustment active during VBI

[9.1.22] Saturation / U Tone Control Register (R/W) [Sub Address 0x15]

Saturation adjustment registers setting.

If YPbPr signal input, U tone level adjustment register setting.

Sub Address: 0x15 Default Value: 0x80

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
UTONE7	UTONE6	UTONE5	UTONE4	UTONE3	UTONE2	UTONE1	UTONE0
Default Value							
1	0	0	0	0	0	0	0

Saturation / U TONE Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SAT0 ~ SAT7	Saturation Control	R/W	Register for saturation level adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80 (CVBS or S-video input)
bit 0 ~ bit 7	UTONE0 ~ UTONE7	U Tone Control	R/W	Register for U tone level adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80 (YPbPr input)

If component mode, UTONE default value should be changed to following parameter.

UTONE [7:0] =0x70

[9.1.23] V Tone Control Register (R/W) [Sub Address 0x16]

YPbPr signal input, V tone level adjustment register setting.

Sub Address: 0x16 Default Value: 0x80

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VTONE7	VTONE6	VTONE5	VTONE4	VTONE3	VTONE2	VTONE1	VTONE0
Default Value							
1	0	0	0	0	0	0	0

V TONE Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	VTONE0 ~ VTONE7	V Tone Control	R/W	Register for V tone level adjustment in steps of 1/128 in range 1~255/128 from default value of 0x80 (YPbPr or RGB input)

If component mode, VTONE default value should be changed to following parameter.

VTONE [7:0] =0x9D

[9.1.24] HUE Control Register (R/W) [Sub Address 0x17]

HUE adjustment register setting.

Sub Address: 0x17 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Default Value							
0	0	0	0	0	0	0	0

HUE Control Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	HUE0 ~ HUE7	HUE Control	R/W	Register for hue adjustment in steps of 1/256 in range ±45° in 2's complement

[9.1.25] High Slice Data Set Register (R/W) [Sub Address 0x18]

Sub Address: 0x18 Default Value: 0xEB

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
H7	H6	H5	H4	H3	H2	H1	H0
Default Value							
1	1	1	0	1	0	1	1

High Slice Data Set Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	H0 ~ H7	High Data 0~7 Set	R/W	Register for setting sliced data from VBI slicer to High value. Important: Corresponds to 601 special code if set to 0x00 or 0xFF

[9.1.26] Low Slice Data Set Register (R/W) [Sub Address 0x19]

Sub Address: 0x19 Default Value: 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
L7	L6	L5	L4	L3	L2	L1	L0
Default Value							
0	0	0	1	0	0	0	0

Low Slice Data Set Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	L0 ~ L7	Low Data 0~7 Set	R/W	Register for setting sliced data from VBI slicer to Low value. Important: Corresponds to 601 special code if set to 0x00 or 0xFF

[9.1.27] Request VBI Information Register (R/W) [Sub Address 0x1A]

Request decode data during VBI interval setting register.

Sub Address: 0x1A Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	WSSRQ	VBIDRQ	EXTRQ	CCRQ
Default Value							
0	0	0	0	0	0	0	0

Request VBI Information Register

BIT	Register Name		R/W	Definition
bit 0	CCRQ	Closed Caption Decode Request	R/W	Setting (ON/OFF) for closed caption decode request 0: No request (OFF) 1: Request (ON)
bit 1	EXTRQ	Extended Data Decode Request	R/W	Setting (ON/OFF) for Extended Data decode request 0: No request (OFF) 1: Request (ON)
bit 2	VBIDRQ	VBID Decode Request	R/W	Setting (ON/OFF) for VBID decode request 0: No request (OFF) 1: Request (ON)
bit 3	WSSRQ	WSS Decode Request	R/W	Setting (ON/OFF) for WSS decode request 0: No request (OFF) 1: Request (ON)
bit 4 ~ bit 7	Reserved	Reserved	R/W	Reserved

[9.1.28] Sub Address 0x1B~0x21 "Reserved Register (R/W)"

Reserved register.

[9.1.29] Status 1 Register (R) [Sub Address 0x22]

The AK8858 internal status register.

Sub Address: 0x22

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OVCOL	PKWHITE	SCLKMOD1	SCLKMOD0	COLKLON	FRMSTD	VLOCK	NOSIG

Status 1 Register

BIT	Register Name		R/W	Definition
bit 0	NOSIG	No Signal	R	Input signal indicator 0: Input signal present 1: Input signal absent
bit 1	VLOCK	VLOCK	R	Input signal VLOCK synchronization status indicator 0: Input signal synchronized 1: Input signal non-synchronized
bit 2	FRMSTD	Frame Standard	R	Input signal interlace status indicator 0: Input signal 525/625 interlaced 1: Input signal not 525/625 interlaced
bit 3	COLKILON	Color Killer ON	R	Color killer status indicator 0: Color killer not operation 1: Color killer operation In component decode mode, this bit is always 0.
bit 4 ~ bit 5	SCLKMOD0 ~ SCLKMOD1	Clock Mode	R	Clock mode indicator SCLKMOD[1:0] 00: Fixed-clock mode 01: Line-locked clock mode 10: Frame-locked clock mode 11: Reserved
bit 6	PKWHITE	Peak White Detection	R	Luminance decode result flow status indicator, after passage through AGC block 0: Normal 1: Overflow
bit 7	OVCOL	Over Color Level	R	Color decode result flow status indicator, after passage through ACC block 0: Normal 1: Overflow (excessive color signal input)

[9.1.30] Status 2 Register (R) [Sub Address 0x23]

The AK8858 internal status register.

Sub Address: 0x23

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	AGSTS	REALFLD	WSSDET	VBIDDET	EXTDET	CCDET

Status 2 Register

BIT	Register Name		R/W	Definition
bit 0	CCDET	Closed Caption Detect	R	Indicator for presence of decoded data in Closed Caption 1/2 Register 0: No closed caption data present 1: Closed caption Data present
bit 1	EXTDET	Extended Data Detect	R	Indicator for presence of decoded data in Extended Data 1/2 Register 0: No extended data present 1: Extended data present
bit 2	VBIDDET	VBID Data Detect	R	Indicator for presence of decoded data in VBID 1/2 Register 0: No VBID data present 1: VBID data present
bit 3	WSSDET	WSS Data Detect	R	Indicator for presence of decoded data in WSS 1/2 Register 0: No WSS data present 1: WSS data present
bit 4	REALFLD	Real Filed	R	Input signal field status (even/odd) indicator 0: EVEN field 1: ODD field
bit 5	AGCSTS	AGC Status bit	R	AGC status indicator 0: Sync AGC active 1: Peak AGC active
bit 6 ~ bit 7	Reserved	Reserved	R	Reserved

[9.1.31] Macrovision Status Register (R) [Sub Address 0x24]

Macrovision signal status register.

Sub Address: 0x24

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	CSTYPE	CSDET	AGCDET

Macrovision Status Register

BIT	Register Name		R/W	Definition
bit 0	AGCDET	AGC Process Detect	R	Indicator for presence of Macrovision AGC in input signal 0: No Macrovision AGC present 1: Macrovision AGC present
bit 1	CSDET	Color Stripe Detect	R	Indicator for presence of Macrovision Color Stripe in input signal 0: No Color Stripe present 1: Color Stripe present
bit 2	CSTYPE	Color Stripe Type	R	Indicator for type of Color Stripe included in input signal 0: Color Stripe Type 2 1: Color Stripe Type 3
bit 3 ~ bit 7	Reserved	Reserved	R	Reserved

[9.1.32] Input Video Status Register (R) [Sub Address 0x25]

Input video status register for auto detection mode.

Sub Address: 0x25

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FIXED	UNDEF	ST_BW	ST_VLF	ST_VCEN1	ST_VCEN0	ST_VSCF1	ST_VCSF0

Input Video Status Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	ST_VSCF0 ~ ST_VSCF1	Status of Video Sub-Carrier Frequency	R	Input video signal subcarrier frequency indicator For CVBS and S (Y/C) signal decode results shows as follows: ST_VSCF[1:0] 00: 3.57954545 MHz 01: 3.57561149 MHz 10: 3.58205625 MHz 11: 4.43361475 MHz (SECAM detected result) For D1/D2 signal decode results shows as follows (this result also apply if auto detection mode is OFF) 00: D1 01: D2 10/11: Reserved
bit 2 ~ bit 3	ST_VCEN0 ~ ST_VCEN1	Status of Video Color Encode	R	Input signal color encode format indicator ST_VCEN[1:0] 00: NTSC 01: PAL 10: SECAM 11: Reserved
bit 4	ST_VLF	Status of Video Line Frequency	R	Input signal line number indicator 0: 525 line 1: 625 line
bit 5	ST_BW	Status of B/W	R	Input signal monochrome indicator 0: Not monochrome 1: Monochrome
bit 6	UNDEF	Un-Define	R	Input signal detection indicator 0: Input signal detected 1: Input signal not detected
bit 7	FIXED	Input Video Standard Fixed	R	Input signal detection process status 0: Detection process in progress 1: Detection process completed

[9.1.33] Closed Caption1 Register (R) [Sub Address 0x26]

Closed Caption data storage register

Sub Address: 0x26

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

[9.1.34] Closed Caption2 Register (R) [Sub Address 0x27]

Closed Caption data storage register

Sub Address: 0x27

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

[9.1.35] WSS 1 Register (R) [Sub Address 0x28]

WSS data storage register

Sub Address: 0x28

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WSS2-7	WSS2-6	WSS2-5	WSS2-4	WSS1-3	WSS1-2	WSS1-1	WSS1-0

[9.1.36] WSS 2 Register (R) [Sub Address 0x29]

WSS data storage register

Sub Address: 0x29

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	WSS4-13	WSS4-12	WSS4-11	WSS3-10	WSS3-9	WSS3-8

[9.1.37.] Extended Data 1 Register (R) [Sub Address 0x2A]

Closed Caption Extended data storage register

Sub Address: 0x2A

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

[9.1.38.] Extended Data 2 Register (R) [Sub Address 0x2B]

Closed Caption Extended data storage register

Sub Address: 0x2B

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

[9.1.39] VBID 1 Register (R) [Sub Address 0x2C]

VBID data storage register

Sub Address: 0x2C

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6

[9.1.40] VBID 2 Register (R) [Sub Address 0x2D]

VBID data storage register

Sub Address: 0x2D

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14

[9.1.41] Device and Revision ID Register (R) [Sub Address 0x2E]

Device ID and Revision indicator

Device ID: [0x3A]

Revision ID: Initially 0x00; revision number changes only when control software should be modified.

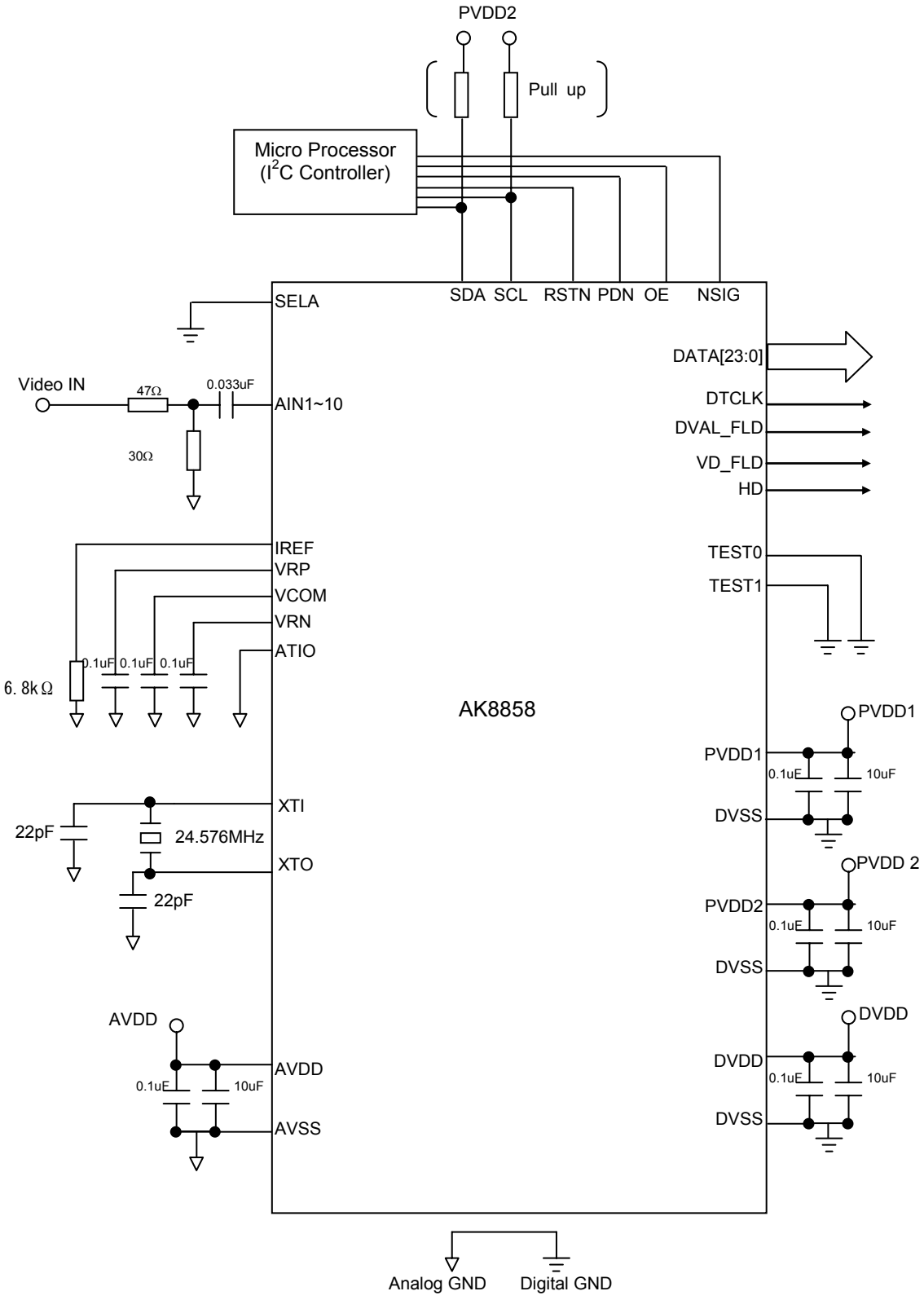
Sub Address: 0x2E

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REV1	REV0	DEVID5	DEVID4	DEVID3	DEVID2	DEVID1	DEVID0
Default Value							
0	0	1	1	1	0	1	0

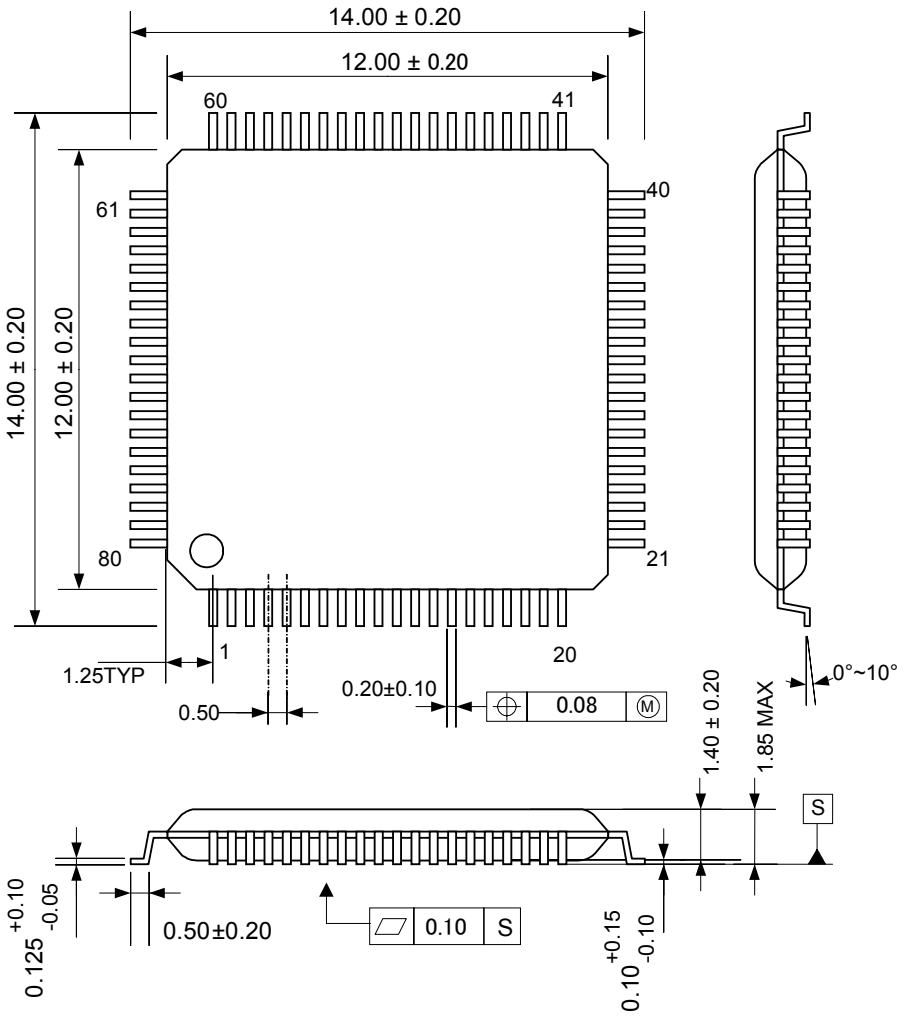
Device and Revision ID Register

BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	DEVID0 ~ DEVID1	Device ID	R	Device ID indicator (0x3A)
bit 6 ~ bit 7	REV0 ~ REV1	Revision ID	R	Revision ID indicator (initially 0x00)

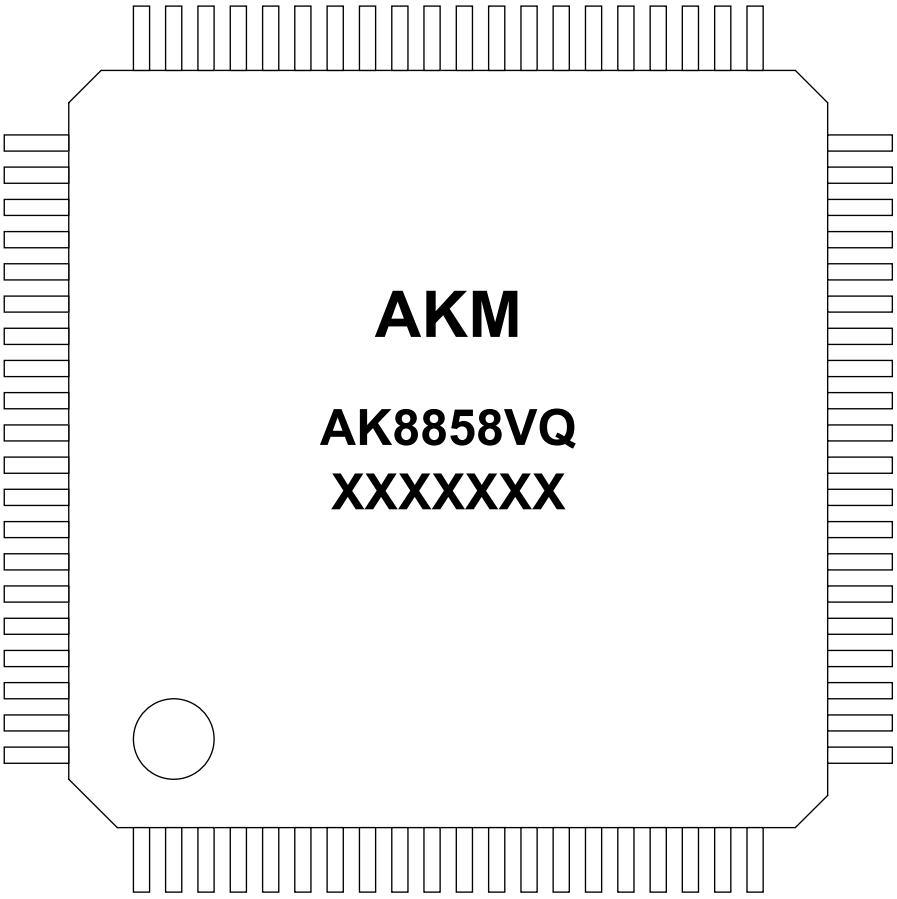
[10] System connection example



[11] Package
80-pin LQFP



[12] Marking



AKM: AKM Logo
AK8858VQ: Marketing Code
XXXXXXX (7 digits): Date Code

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