iC-LNG 16-BIT OPTO ENCODER WITH SPI AND SERIAL / PARALLEL OUTPUTS

preliminary

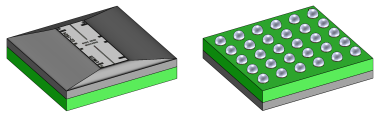
FEATURES

- Excellent matching and technical reliability thanks to system-on-chip design with integrated photodiodes
- Gray code scanning (11 digital tracks pitched at 400 µm)
- Sine/cosine analog track with electronic calibration
- Diff. sine/cosine outputs with 1024 CPR (amplitude: 500 mV)
- Position value of up to 16 bits through 6-bit interpolation
- Quadrature signals with 1024, 2048, 4096, 8192, 16384 CPR
- Index signal in phase with B low
- 14-bit parallel position data output
- Serial data readout in 1 µs cycles at 16 MHz clock frequency
- SPI interface for configuration and position data output
- 3.3 V-compatible SPI and I/O ports
- LED current control for a constant receive power (50 mA highside driver, $\sin^2+\cos^2$ or sum)
- Permanent parity monitoring of the internal RAM bits
- Alarm for configuration and illumination errors (end of life)
- Temperature range from -40°C to 110°C
- Small outline, 30-pin optoBGA package for SMT
- Illumination: iC-SN85 BLCC SN1C (850 nm encoder LED)
- Code discs:
  LNG1S 42-1024 (1024 PPR, ∅ 42 mm/18 mm),
  LNG2S 25-512 (512 PPR, ∅ 24.8 mm/2 mm)

APPLICATIONS

- Optical position sensors
- Linear scales
- Absolute, incremental, and parallel encoders
- Motor feedback systems

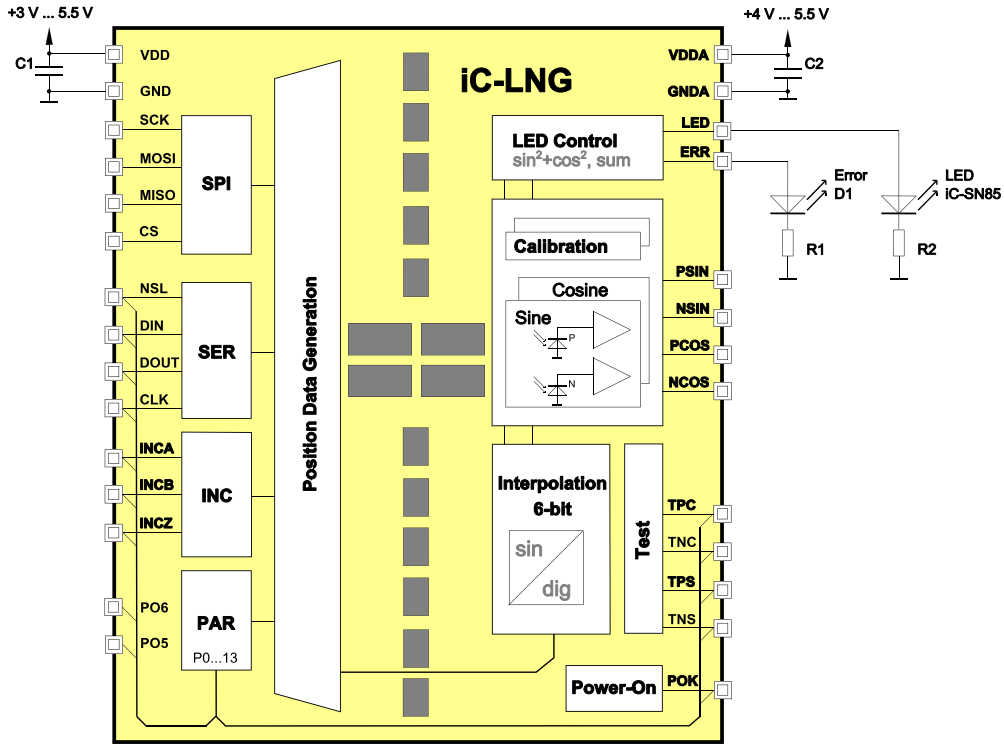
PACKAGES



30-Pin optoBGA

7.6 mm x 7.1 mm x 1.7 mm

BLOCK DIAGRAM



DESCRIPTION

iC-LNG is an optoelectronic encoder IC for absolute linear and angle measuring systems, such as glass scales and encoders. Photodiodes, amplifiers, and comparators, the entire signal conditioning unit, and interfaces for position data output have been monolithically integrated into the device.

An integrated LED current control with a driver stage allows a transmitting LED to be directly connected (e.g. iC-SN85). The optical receive power is kept constant by the control unit, regardless of temperature and aging effects. The receive power setpoint can be programmed. Should the LED current control exit its operating range, this is indicated at the error message output (end-of-life alarm at pin ERR).

The photocurrent offset and photocurrent amplitude of the analog sine/cosine signals can be calibrated. These calibrated voltage signals are lead out to pins PSIN, NSIN, PCOS, and NCOS and are used by the integrated 6-bit interpolator.

iC-LNG synchronizes the interpolator and singleturn data to form a contiguous Gray-coded position data word. A shift register or SPI interface are available for position data output. iC-LNG also outputs incremental A/B/Z signals, the resolution of which can be programmed.

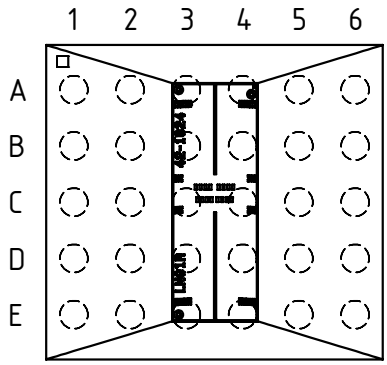
After startup iC-LNG is configured using the SPI interface. To make connection to a 3.3 V microcontroller easier, all digital I/O ports, including the SPI, can be run on 3.3 V.

Test currents can be applied to test pins TPS, TNS, TPC, and TNC to simulate photocurrents. Allocation to various tracks can be selected as required, enabling a full function test of the IC with the exception of the sensors.

CONTENTS

PACKAGES

PIN CONFIGURATION oBGA LNB2C (7.6 mm x 7.1 mm)



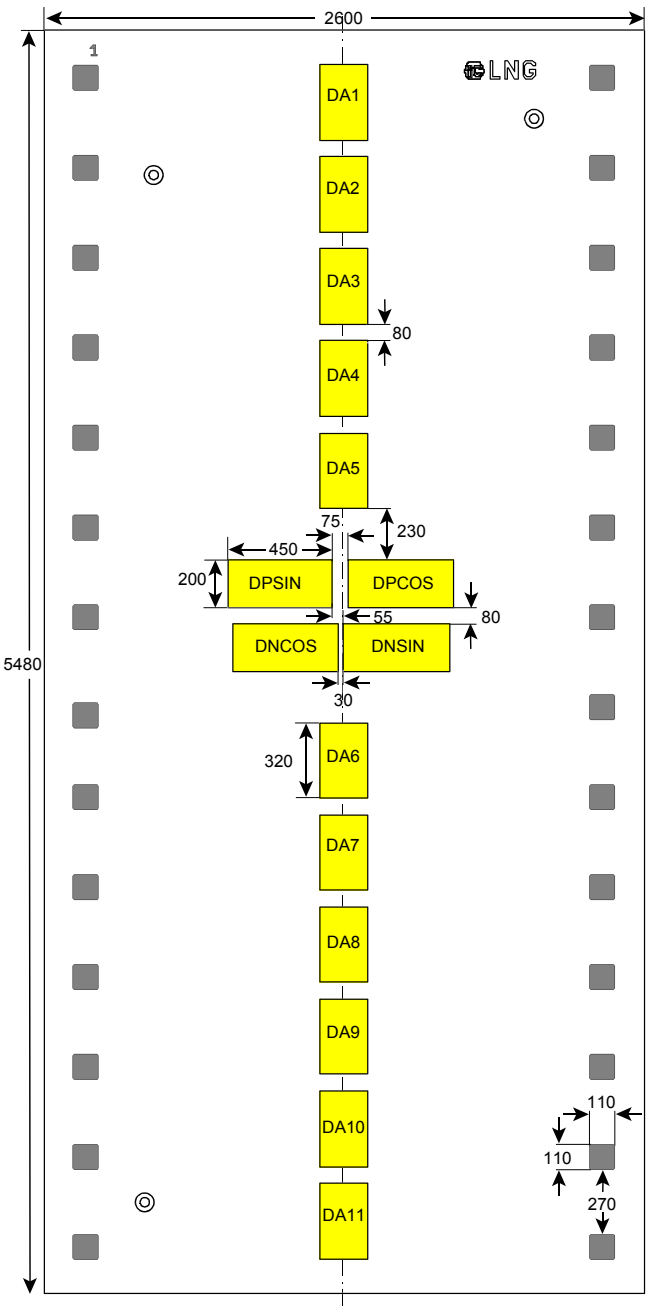
PIN FUNCTIONS

No.	Name	Function
A1	SCK	SPI Clock Input
A2	VDD	+ 3 V to + 5.5 V I/O Ports Supply Voltage
A3	GND	I/O Ports Ground
A4	LED	LED Current Control (Highside Output)
A5	VDDA	+ 4 V to + 5.5 V Supply Voltage
A6	GNDA	Ground
B1	CS	SPI Chip Select
B2	MISO	SPI Data Output
B3	MOSI	SPI Data Input
B4	PCOS	Analog Voltage Output PCOS
B5	NSIN	Analog Voltage Output NSIN
B6	PSIN	Analog Voltage Output PSIN

PIN FUNCTIONS

No.	Name	Function
C1	INCZ	Incremental Output Z / Parallel Output Bit 11
C2	TNS	Test Input NSIN / Parallel Output Bit 12
C3	TNC	Test Input NCOS / Parallel Output Bit 13
C4	TPS	Test Input PSIN / Parallel Output Bit 1
C5	TPC	Test Input PCOS / Parallel Output Bit 0
C6	NCOS	Analog Voltage Output NCOS
D1	DOUT	Shift Register Data Output / Parallel Output Bit 8
D2	DIN	Shift Register Data Input / Parallel Output Bit 9
D3	NSL	Shift Register Load / Parallel Output Bit 10
D4	INCB	Incremental Output B / Parallel Output Bit 3
D5	INCA	Incremental Output A / Parallel Output Bit 2
D6	ERR	Alarm Message Output, high active
E1	n.c.	
E2	PO6	Parallel Output Bit 6
E3	CLK	Shift Register Clock Input / Parallel Output Bit 7
E4	n.c.	
E5	PO5	Parallel Output Bit 5
E6	POK	Power Ok Indication / Parallel Output Bit 4
	n.c.	pin not connected

PAD LAYOUT



PAD FUNCTIONS

No.	Name	Function
1	GND	I/O Ports Ground
2	VDD	+ 3 V to +5.5 V I/O Ports Supply Voltage
3	SCK	SPI Clock Input
4	MOSI	SPI Data Input
5	MISO	SPI Data Output
6	CS	SPI Chip Select
7	TNC	Test Input NCOS / Parallel Output Bit 13
8	TNS	Test Input NSIN / Parallel Output Bit 12
9	INCZ	Incremental Output Z / Parallel Output Bit 11
10	NSL	Shift Register Load / Parallel Output Bit 10
11	DIN	Shift Register Data Input / Parallel Output Bit 9
12	DOUT	Shift Register Data Output / Parallel Output Bit 8
13	CLK	Shift Register Clock Input / Parallel Output Bit 7
14	PO6	Parallel Output Bit 6
15	PO5	Parallel Output Bit 5
16	POK	Power Ok Indication / Parallel Output Bit 4
17	INCB	Incremental Output B / Parallel Output Bit 3
18	INCA	Incremental Output A / Parallel Output Bit 2
19	ERR	Alarm Message Output, high active
20	TPS	Test Input PSIN / Parallel Output Bit 1
21	TPC	Test Input PCOS / Parallel Output Bit 0
22	NCOS	Analog Voltage Output NCOS
23	PCOS	Analog Voltage Output PCOS
24	NSIN	Analog Voltage Output NSIN
25	PSIN	Analog Voltage Output PSIN
26	LED	LED Current Control (Highside Output)
27	VDDA	+ 4 V to +5.5 V Supply Voltage
28	GNDA	Ground

ABSOLUTE MAXIMUM RATINGS

Maximum ratings do not constitute permissible operating conditions; functionality is not guaranteed.
Exceeding the maximum ratings can damage the device.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDDA	Voltage at VDDA		-0.3	6	V
G002	VDD	Voltage at VDD		-0.3	VDDA+0.3	V
G003	V(GND)	Voltage at GND		-0.3	0.3	V
G004	V()	Voltage at LED, PCOS, NCOS, PSIN, NSIN, TPC, TNC, TPS, TNS		-0.3	VDDA+0.3	V
G005	V()	Voltage at INCA, INCB, INCZ, ERR, CLK, DOUT, DIN, NSL, CS, MOSI, MISO, SCK, PO6, PO5, POK, TPC, TNC, TPS, TNS		-0.3	VDD+0.3	V
G006	I(VDDA)	Current in VDDA		-100	100	mA
G007	I(VDD)	Current in VDD		-50	50	mA
G008	I(GND)	Current in GND		-20	20	mA
G009	I(LED)	Current in LED		-100	20	mA
G010	I()	Current in INCA, INCB, INCZ, ERR, CLK, DOUT, DIN, NSL, CS, MOSI, MISO, SCK, PO6, PO5, POK		-60	60	mA
G011	I()	Current in PCOS, NCOS, PSIN, NSIN, TPC, TNC, TPS, TNS		-35	35	mA
G012	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G013	Tj	Chip-Temperature		-40	125	°C
G014	Ts	Storage Temperature Range	see package specification			

THERMAL DATA

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	see package specification				

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40°C to 125°C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDDA	Permissible Supply Voltage		4.0	5.0	5.5	V
002	VDD	Permissible I/O Supply Voltage	VDD ≤ VDDA	3.0		5.5	V
003	VDDA, VDD	Permissible Residual Ripple	at 150 kHz		10		mV
004	I()	Supply Current in VDDA and VDD (total sum)	without currents I(LED) and I(ERR), Tj = 27°C		15	40	mA
005	Vcz()hi	Clamp Voltage hi at VDD, GND, VDDA, GNDA, MISO, DOUT, INCA, INCB, INCZ, PO5, PO6, POK, TNS, TPS, TNC, TPC, NCOS, NSIN, PCOS, PSIN, ERR, LED	I() = 4 mA			11	V
006	Vc()hi	Clamp Voltage hi at CLK, DIN, NSL, INCA, INCB, INCZ, ERR, MISO, DOUT, POK, P05, P06, TPS, TNS, TPC, TNC	Vc()hi = V() − V(VDD), I() = 4 mA	0.3		1.2	V
007	Vc()hi	Clamp Voltage hi at CS, MOSI, SCK	Vc()hi = V() − V(VDD), I() = 4 mA	1.2		2.2	V
008	Vc()lo	Clamp Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
009	Vs()hi	Saturation Voltage hi at PO6, PO5, POK, CLK, DOUT, DIN, NSL, MISO, TPC, TNC, TPS, TNS	Vs()hi = VDD - V() VDD = 3 to 4 V, I() = 2.5 mA VDD = 4 to 5.5 V, I() = 3.5 mA			400	mV
010	Isc()hi	Short-Circuit Current hi at PO6, PO5, POK, CLK, DOUT, DIN, NSL, MISO, TPC, TNC, TPS, TNS		-100		-4	mA
011	Vs()lo	Saturation Voltage lo at PO6, PO5, POK, CLK, DOUT, DIN, NSL, MISO, TPC, TNC, TPS, TNS	VDD = 3 to 4 V, I() = 2.5 mA VDD = 4 to 5.5 V, I() = 3.5 mA			400	mV
012	Isc()lo	Short-Circuit Current lo at PO6, PO5, POK, CLK, DOUT, DIN, NSL, MISO, TPC, TNC, TPS, TNS		4		100	mA
Photodiodes							
101	Se(λ)	Spectral Application Range	Se(λ) = 0.1 x S(λ)max	400		1000	nm
102	S(λ)max	Spectral Sensitivity	λ = 690 nm		0.45		A/W
103	Asc()	Radiant Sensitive Area DPSIN, DNSIN, DPCOS, DNCOS	0.45 x 0.2 mm²		0.09		mm²
104	Ad()	Radiant Sensitive Area Digital DA1 to DA11	0.2 x 0.32 mm²		0.064		mm²
Photocurrent Amplifier							
201	Iph()	Permissible Photocurrent Range		0		200	nA
202	Z()	Equivalent Transimpedance Gain	Z() = Vout() / Iph()	1.8	3.0	4.2	MΩ
203	ΔZ()pn	Transimpedance Gain Matching of an Amplifier Pair	P-channel versus corresponding N-channel	-0.2		0.2	%
204	fhc()	Upper Cut-off Frequency (-3dB)	without LED current control	120	300	500	kHz
205	VR()	Ratio Reference Voltage Digital Tracks (Vcomp) to Sum of Analog Tracks	$VR() = \frac{Vcomp}{VPSI + VNSI + VPCI + VNCI}$		0.25		
206	Vhys()	Digital Tracks Hysteresis		15	25	40	mV
207	GR()	Coarse Gain Range	GR = 0x00 GR = 0x01 GR = 0x02 GR = 0x03		1 1.33 1.6 2		

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40°C to 125°C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
208	Vref	Reference Voltage of Photocurrent Amplifiers		0.6	0.8	1	V
209	ΔVd()sc	Analog Track Dark Signal Voltage versus Vref	ΔVd()sc = V() - Vref	-20		20	mV
210	ΔVd()dig	Digital Track Dark Signal Voltage versus Vref	ΔVd()dig = V() - Vref	-35		35	mV
Signal Conditioning							
301	GSmin, GCmin	Adjustable Gain Min	GS, GC = 0x00		1		
302	GSmax, GCmax	Adjustable Gain Max	GS, GC = 0x3F		2		
303	ΔGdiff	Differential Gain Calibration Accuracy	6 bit calibration	-0.5		0.5	LSB
304	Omin	Offset Calibration Min	OSP, OSN, OCP, OCN = 0x00	43	45	47	%VDDA
305	Omax	Offset Calibration Max	OSP, OSN, OCP, OCN = 0x7F	53	55	57	%VDDA
306	ΔOdiff	Differential Offset Calibration Accuracy	7 bit calibration	0.02	0.08	0.12	%VDDA
Analog Voltage Outputs PSIN, NSIN, PCOS, NCOS							
401	Vdc()	DC Output Voltage	Offset adjusted to VDDAH	47	50	53	%VDDA
402	Vpk()	Permissible Signal Amplitude	DC level = VDDA/2		0.5	0.6	V
403	I()mx	Permissible Output Current		-1		1	mA
404	Ri()	Output Impedance	I() = -1 to 1 mA		75	200	Ω
LED Current Control, Error Message ERR							
501	Imx()	Permissible LED Current		-100		0	mA
502	Iop()	LED Current Control Range	ERRS (internal) = 0, V(LED) > Vs(LED)	-50		-1	mA
503	Vs()	Saturation Voltage at LED	Vs() = V(VDDA) - V(LED), Tj = -40°C to 100°C, I() = -50 mA Tj = 100°C to 125°C, I() = -45 mA			1 1	V V
504	tr()	Current Rise Time LED at LED	I(LED): 0 % → 90 %		0.8	1.5	ms
505	tset()	Current Settling Time of Control Loop at LED	amplitude at PSIN, NSIN, PCOS and NCOS from 50 % to 100 % of setpoint		300		µs
506	Vs()hi	Saturation Voltage hi at ERR	Vs()hi = VDD - V(ERR) VDD = 3 V to 4 V, I() = 2.5 mA VDD = 4 V to 5.5 V, I() = 3.5 mA			400	mV
507	Isc()hi	Short-Circuit Current hi in ERR		-100		-4	mA
508	Vs()lo	Saturation Voltage lo at ERR	VDD = 3 V to 4 V, I() = 2.5 mA VDD = 4 V to 5.5 V, I() = 3.5 mA			400	mV
509	Isc()lo	Short-Circuit Current lo in ERR		4		100	mA
Interpolator							
701	AAabs	Absolute Angle Accuracy	referenced to one SIN/COS period	-5		5	DEG
702	AArel	Relative Angle Accuracy	referenced to one AB period, see Figure 1	-10		10	%
703	AAhys	Angle Hysteresis	referenced to one SIN/COS period	1		7	DEG
704	tw()hi	Duty Cycle	referenced to AB period T, see Figure 1		50		%
705	t_{AB}	Phase A versus B	see Figure 1		25		%
Incremental Outputs INCA, INCB, INCZ							
801	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V() VDD = 3 V to 4 V, I() = 2.5 mA VDD = 4 V to 5.5 V, I() = 3.5 mA			400	mV
802	Isc()hi	Short-Circuit Current hi		-100		-4	mA
803	Vs()lo	Saturation Voltage lo	VDD = 3 V to 4 V, I() = 2.5 mA VDD = 4 V to 5.5 V, I() = 3.5 mA			400	mV
804	Isc()lo	Short-Circuit Current lo		4		100	mA
805	tr()	Rise Time	CL = 30 pF, V(): 10% → 90% VDD			30	ns
806	tf()	Fall Time	CL = 30 pF, V(): 90% → 10% VDD			30	ns

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40°C to 125°C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Interface SCK, CS, MISO, MOSI							
901	fin()	Permissible Input Frequency at SCK				10	MHz
902	Vt()hi	Threshold Voltage hi at SCK, CS, MOSI				2	V
903	Vt()lo	Threshold Voltage lo at SCK, CS, MOSI		0.8			V
904	Vt()hys	Hysteresis at SCK, CS, MOSI	Vt() = Vt()hi - Vt()lo	40	100		mV
905	Ipu()	Pull-Up Current at SCK, MOSI	V() = 0 V to VDD - 1 V VDD = 3 V to 4 V VDD = 4 V to 5.5 V	 -65 -120	 -25 -60	 -5 -10	 µA µA
906	Vpu()	Pull-Up Voltage at SCK, MOSI	Vpu() = VDD - V(), VDD = 3 V to 4 V, I() = -3 µA VDD = 4 V to 5.5 V, I() = -5 µA			400	mV
907	Ipd()	Pull-Down Current at CS	V() = 1 V . . . VDD VDD = 3 V to 4 V VDD = 4 V to 5.5 V	 5 8	 25 60	 80 150	 µA µA
908	Vpd()	Pull-Down Voltage at CS	VDD = 3 V to 4 V, I() = 3 µA VDD = 4 V to 5.5 V, I() = 5 µA			400	mV
909	t_{CO}	Propagation Delay: MISO hi after Falling Edge CS	see Figure 2		30		ns
910	t_{SO}	Propagation Delay: MISO Stable after Clock Edge SCK	see Figure 2		30		ns
Shift Register CLK, NSL, DOUT, DIN							
A01	fin()	Permissible Input Frequency at CLK				16	MHz
A02	t_{NO}	Propagation Delay: DOUT after Falling Edge NSL	see Figure 3		20		ns
A03	t_{CO}	Propagation Delay: DOUT stable after Clock Edge CLK	see Figure 3		20		ns
A04	Vt()hi	Threshold Voltage hi at CLK, NSL, DIN				2	V
A05	Vt()lo	Threshold Voltage lo at CLK, NSL, DIN		0.8			V
A06	Vt()hys	Hysteresis at CLK, NSL, DIN	Vt() = Vt()hi - Vt()lo	40	100		mV
A07	Ipu()	Pull-Up-Current at CLK, NSL	V() = 0 V to VDD - 1 V VDD = 3 V to 4 V VDD = 4 V to 5.5 V	 -65 -120	 -25 -60	 -5 -10	 µA µA
A08	Vpu()	Pull-Up-Voltage at CLK, NSL	Vpu() = VDD-V(), VDD = 3 V to 4 V, I() = -3 µA VDD = 4 V to 5.5 V, I() = -5 µA			400	mV
A09	Ipd()	Pull-Down Current at DIN	V() = 1 V to VDD VDD = 3 V to 4 V VDD = 4 V 5.5 V	 5 8	 25 60	 80 150	 µA µA
A10	Vpd()	Pull-Down-Voltage at DIN	VDD = 3 V to 4 V, I() = 3 µA VDD = 4 V to 5.5 V, I() = 5 µA			400	mV
Parallel Output Bit 0 to Bit 13 (Parameter EPG = 0x1)							
B01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V() VDD = 3 V to 4 V, I() = 2.5 mA, VDD = 4 V to 5.5 V, I() = 3.5 mA			400	mV
B02	Isc()hi	Short-Circuit Current hi		-100		-4	mA
B03	Vs()lo	Saturation Voltage lo	VDD = 3 V to 4 V, I() = 2.5 mA, VDD = 4 V to 5.5 V, I() = 3.5 mA			400	mV
B04	Isc()lo	Short-Circuit Current lo		4		100	mA
B05	tr()	Rise Time	CL = 30 pF, V(): 10% → 90% VDD			30	ns
B06	tf()	Fall Time	CL = 30 pF, V(): 90% → 10% VDD			30	ns

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40°C to 125°C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power-On-Reset POK							
C01	VDDAon	Turn-on Threshold VDDA, Power-On-Reset	VDDA increasing, POK: lo → hi	3.6	3.8	4.0	V
C02	VDDAoff	Turn-off Threshold VDDA, Power-Down-Reset	VDDA decreasing, POK: hi → lo	3.3	3.5	3.7	V
C03	VDDAhys	Hysteresis VDDA	VDDAhys = VDDAon - VDDAoff	0.2	0.3		V

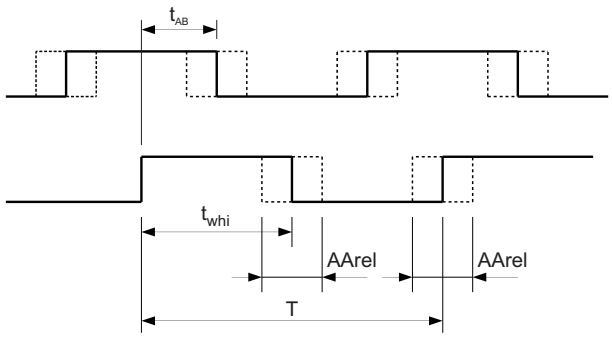


Figure 1: Definition of the relative angle accuracy

OPERATING CONDITIONS: SPI Interface

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40°C to 125°C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	T_{SCK}	Permissible Clock Period		1/fin(SCK)		
I002	t_{CS}	Setup Time: CS hi before SCK hi → lo		50		ns
I003	t_{CO}	Propagation Delay: MISO hi after CS hi → lo		(Elec. Char. No. 909)		
I004	t_{IS}	Setup Time: MOSI stable before SCK lo → hi		50		ns
I005	t_{SI}	Hold Time: MOSI stable after SCK lo → hi		50		ns
I006	t_{SO}	Propagation Delay: MOSI stable after Clock Edge SCK		(Elec. Char. No. 910)		
I007	t_{CC}	Hold Time: Between CS hi → lo and CS lo → hi		500		ns

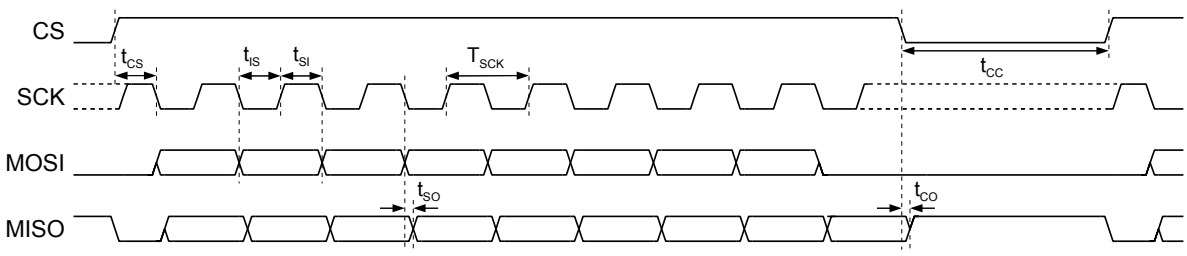


Figure 2: SPI interface timing

OPERATING CONDITIONS: Shift Register

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40°C to 125°C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	T_{CLK}	Permissible Clock Period		1/fin(CLK)		
I102	t_{NC}	Setup Time: NSL lo before CLK lo → hi		30		ns
I103	t_{NO}	Propagation Delay: DOUT stable after NSL hi → lo		(Elec. Char. No. A02)		
I104	t_{CO}	Propagation Delay: DOUT stable after Clock Edge CLK		(Elec. Char. No. A03)		
I105	t_{IC}	Setup Time: DIN stable before CLK lo → hi		30		ns
I106	t_{CI}	Hold Time: DIN stable after CLK lo → hi		30		ns
I107	t_{NN}	Wait Time: between NSL lo → hi and NSL hi → lo		60		ns

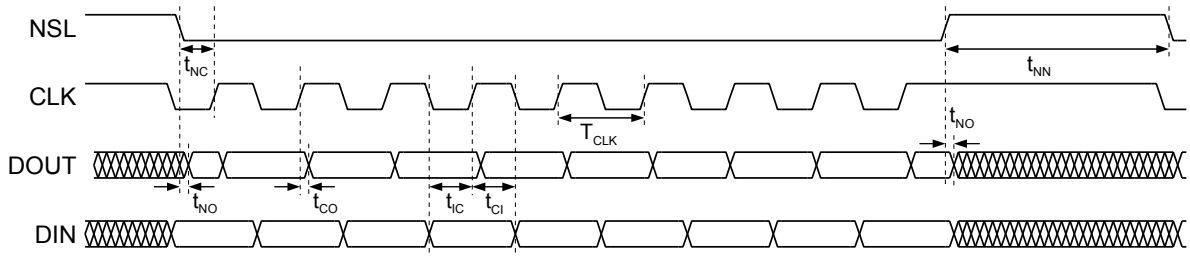


Figure 3: Shift register timing

CONFIGURATION PARAMETERS

REGISTER MAP

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Signal conditioning								
0x00	P0	–	GS(5:0)					
0x01	P1	–	GC(5:0)					
0x02	P2	OSP(6:0)						
0x03	P3	OSN(6:0)						
0x04	P4	OCP(6:0)						
0x05	P5	OCN(6:0)						
LED current control								
0x06	P6	LCSET(6:0)						
Output								
0x07	P7	NSYNC	DIR	EPG	–		GR(1:0)	
0x08	P8	INC(2:0)			STA	SRC(2:0)		
Test functions								
0x09	P9	–	TA(1:0)		TMUX(3:0)			
0x0A	PA	–						
0x0B	PB	–						
0x0C	PC	–						
0x0D	PD	–						
0x0E	PE	–						
0x0F	PF	–						

Bit 7: Parity bit (supplemented to an even number of ones)

Table 6: Register layout

The configuration registers in the internal RAM are constantly monitored by a parity check. Bit 7 of each address is the parity bit (P0-PF) and is supplemented to an even number of ones. The unused bits are also monitored. A parity error is signaled at pin ERR (high active).
Addresses in iC-LNG range from addresses 0x00 to 0x0F. As only the lower nibble of the address byte is evaluated, with addresses that are greater than 0x0F the device then returns to address range 0x00-0x0F.

After the system enable (power-on reset, pin POK lo → hi) the registers are initialized as follows:

Address	Reset value
0x00 - 0x01	0xA0
0x02 - 0x05	0xC0
0x06	0xA0
0x07	0x81
0x08	0x96
0x09 - 0x0F	0x00

Table 7: Register reset values

OPERATING MODES

iC-LNG has two operating modes. These are selected using register bit EPG.

EPG	Add. 0x07, bit 4
0	Interface mode
1	Parallel encoder mode

Table 8: Operating mode selection

In interface mode a shift register is provided for sensor data readout and an incremental interface with an index signal for the output of encoder quadrature signals at a configurable resolution. A power-on signal at pin POK indicates that the system is enabled (POK = hi).

In parallel encoder mode the sensor data is output as a 14-bit, parallel data word in Gray code. For this purpose all the relevant pins are reconfigured as outputs. Table 9 shows the pin functions for the respective operating mode (see also Parallel Encoder Mode on page 20).

The SPI interface for device configuration can also be used for position data readout and is available in both operating modes.

Pin	Pin dependent on VDD	Pin dependent on VDDA	Interface mode	Parallel encoder mode
GND	x		I/O pins ground	I/O pins ground
VDD	x		+3 V to + 5.5 V I/O pins Supply voltage	+3 V to + 5.5 V I/O pins Supply voltage
SCK	x		SPI clock	SPI clock
MOSI	x		SPI data input	SPI data input
MISO	x		SPI data output	SPI data output
CS	x		SPI chip select	SPI chip select
TNC	x		Test input NCOS	Parallel output 13
TNS	x		Test input NSIN	Parallel output 12
INCZ	x		Incremental output Z	Parallel output 11
NSL	x		Load shift register	Parallel output 10
DIN	x		Shift register data input	Parallel output 9
DOUT	x		Shift register data output	Parallel output 8
CLK	x		Shift register clock	Parallel output 7
NSL	x		Load shift register	Parallel output 6
PO5	x		Parallel output 5	Parallel output 5
POK	x		Power OK indication	Parallel output 4
INCB	x		Incremental output B	Parallel output 3
INCA	x		Incremental output A	Parallel output 2
ERR	x		Alarm message output	Alarm message output
TPS	x		Test input PSIN	Parallel output 1
TPC	x		Test input PCOS	Parallel output 0
NCOS		x	Voltage output NCOS	Voltage output NCOS
PCOS		x	Voltage output PCOS	Voltage output PCOS
NSIN		x	Voltage output NSIN	Voltage output NSIN
PSIN		x	Voltage output PSIN	Voltage output PSIN
LED		x	LED current control (highside output)	LED current control (highside output)
VDDA		x	+4 V to + 5.5 V Supply Voltage	+4 V to + 5.5 V Supply Voltage
GNDA		x	Ground	Ground

Table 9: Pin functions depending on operating mode

SPI INTERFACE

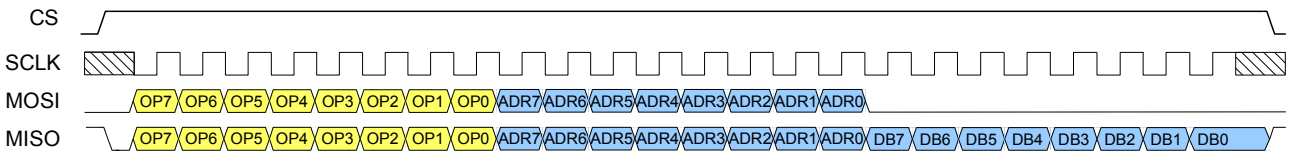


Figure 4: SPI transmission, taking the Read REGISTER opcode as an example (cont.)

General protocol description

iC-LNG's SPI interface is implemented as an SPI slave and supports SPI modes 0 and 3, meaning the idle time at SCK can be 0 or 1. Data is always accepted on a rising edge at SCK. The idle time of the MISO line is 1; on a rising edge at CS the MOSI signal is switched through to the MISO signal.
Data is sent byte by byte with the MSB (most significant bit) first. Each data transmission starts when a 1-byte opcode is sent by the SPI master (Table 10).

OPCODE	
Code	Description
0xB0	ACTIVATE
0xA6	Sensor data transmission
0xF5	Sensor data status
0x8A	Read REGISTER (cont.)
0xCF	Write to REGISTER (cont.)
0xAD	REGISTER status/data

Table 10: Instructions / opcodes

SPI data transmission for register readout takes place as follows (Figure 4):

1. The master initializes a transmission by a rising edge at CS.
2. iC-LNG transfers the level from MOSI to MISO.
3. The master transmits the OPCODE and address ADR through MOSI; iC-LNG immediately outputs OPCODE and ADR through MISO.
4. iC-LNG transmits the data requested according to the address.
5. The master ends the command by a falling edge at CS.
6. iC-LNG switches its MISO output to 1.

OPCODE description

ACTIVATE
iC-LNG's register and sensor data channels can be switched on and off using the **ACTIVATE** command. The command causes all slaves to zero their RACTIVE and PACTIVE register and to loop-in this register data between the MOSI and MISO data stream. The register and sensor or actuator data channels can be switched on and off using the following data bytes.
After a power-on iC-LNG's sensor data channel is deactivated (PACTIVE = 0) and the register communication is activated (RACTIVE = 1).

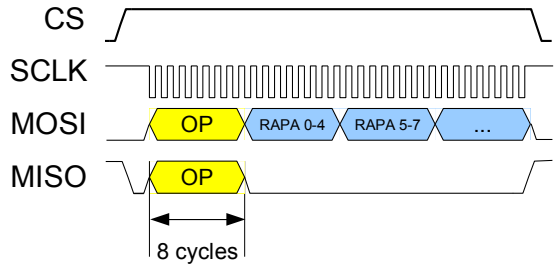


Figure 5: Setting ACTIVATE: RACTIVE/PACTIVE (several slaves)

Bytes FAIL, VALID, BUSY, and DISMISS in the STATUS byte are reset by the **ACTIVATE** command (Table 14).

RACTIVE	
Code	Description
0	Register communication deactivated
1	Register communication activated

Table 11: Register communication

If RACTIVE is not set, on commands **Read REGISTER (cont.), Write to REGISTER (cont.)** and **REGISTER status/data** the ERROR bit is set in the SPI interface STATUS byte (Table 14), indicating that the command has not been carried out. The slave immediately outputs the data at MISO which has been sent by the master through MOSI.

PACTIVE	
Code	Description
0	Sensor data channel deactivated
1	Sensor data channel activated

Table 12: Sensor data via SPI

If PACTIVE is not set, on commands **Sensor data status** or **Sensor data transmission** the ERROR bit is set in the STATUS byte (Table 14), indicating that the command has not been carried out. The slave immediately outputs the data at MISO which has been sent by the master through MOSI.

If only one slave is connected up with one register and one sensor data channel, it must be ensured that the RACTIVE and PACTIVE bits are last in the data byte (Figure 6).

NB:
If the slaves are connected in a chain (full duplex chain), with this command the master can determine the number of connected register and sensor data channels. To this end it can send a 1 after the opcode, which is repeated at MISO after the number of register and sensor data channels (Figure 6).

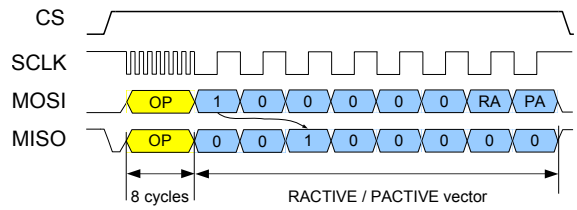


Figure 6: Setting ACTIVATE: RACTIVE/PACTIVE (one slave)

Sensor data transmission
iC-LNG samples its position data on the first rising edge at SCLK if CS is switched to 1 (REQ). The sensor data shift register is looped-in between signals MOSI and MISO for SPI communication and can then be clocked out. The size of the sensor data shift register must be set to 16 bits (cf. section on shift register output, page 21).

If invalid data is sampled in the shift register, the ERROR bit is set in the STATUS byte (Table 14) and zeroes are output as the data word.

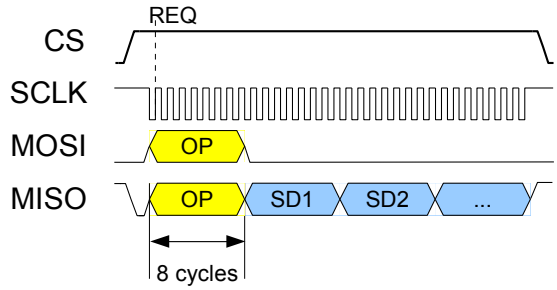


Figure 7: SDAD transmission: read SD

With command **Sensor data transmission** the master can not only read sensor data (SD) out from the slave; at the same time it can also transmit actuator data (AD) to the slave. iC-LNG ignores the transmitted actuator data.

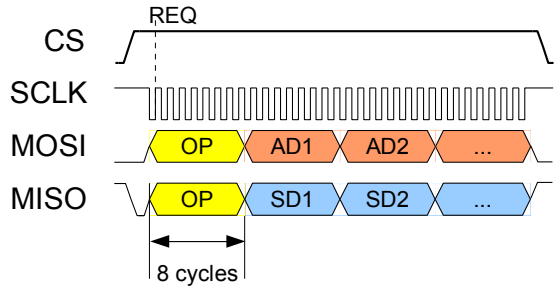


Figure 8: SDAD transmission: read SD, write AD

Sensor data status

Should the master not know the processing time, it can request sensor data using the command **Sensor data status**. iC-LNG does not need any processing time; therefore, SVALID is always valid.

The command causes

1. all slaves activated with PACTIVE to switch their SVALID register between MOSI and MISO.

2. The next request for sensor data, triggered on the first rising edge at SCLK when CS has again been set to 1, is ignored by the slave.

The end of conversion is signaled by SVALID (SV). With this command the master can poll to the end of conversion. The sensor data is readout on the command **Sensor data transmission**.

SVALID	
Code	Description
0	Sensor data invalid
1	Sensor data valid

Table 13: SVALID

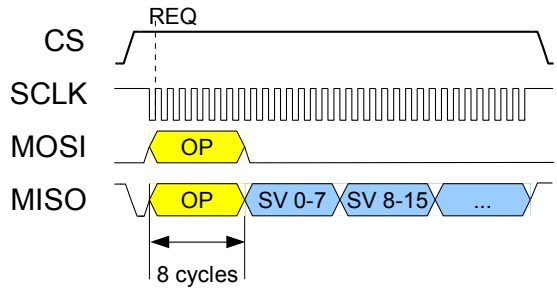


Figure 9: SDAD status

If only one slave is connected, the relevant SVALID bit is placed at bit position 7 in the SVALID byte.

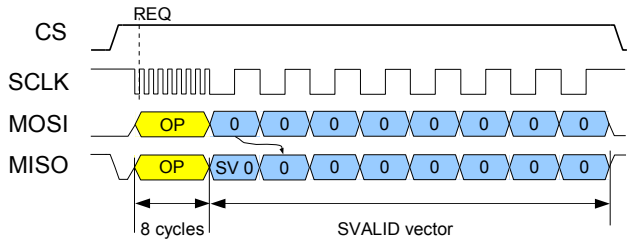


Figure 10: SDAD status (one slave)

REGISTER status/data
The status of the last REGISTER communication or the last data transmission can be queried using the **REGISTER status/data** command. The STATUS byte contains the information summarized in Table 14.

STATUS		
Bit	Name	Description of the status report
7	ERROR	Opcode invalid. Sensor data was invalid on readout
6..4	-	Reserved
3	DISMISS	Address refused
2	FAIL	Data request has failed
1	BUSY	Slave is busy with a request
0	VALID	DATA is valid
NB	Display logic: 1 = true, 0 = false	

Table 14: SPI status information

All status bits are updated with each register access. The ERROR bit is the exception to the rule; this bit signals whether an error occurred during the last communication with the SPI interface or not.

The master transmits the opcode **REGISTER status/data**. iC-LNG immediately passes the opcode on to MISO. iC-LNG then transmits the STATUS byte and a DATA byte. The DATA byte is not available in iC-LNG and is thus not defined.

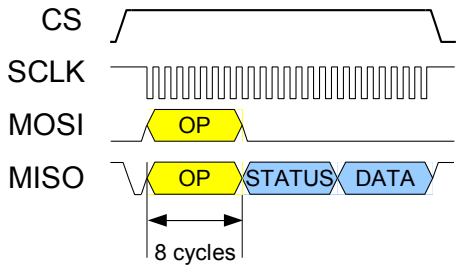


Figure 11: REGISTER status/data

Read REGISTER (cont.)
The master transmits the opcode **Read REGISTER (cont.)**. Start address ADR, from which point data is to be read, is transmitted in the 2nd byte. The slave immediately outputs the opcode and address and then transmits DATA1. The internal address counter is incremented after each data package.

If an error occurs during register readout (cont.), i.e. the address is invalid, the requested data was not valid on data byte clocking, etc., the internal address counter is incremented no further and the FAIL error bit is set in the status byte (Table 14).

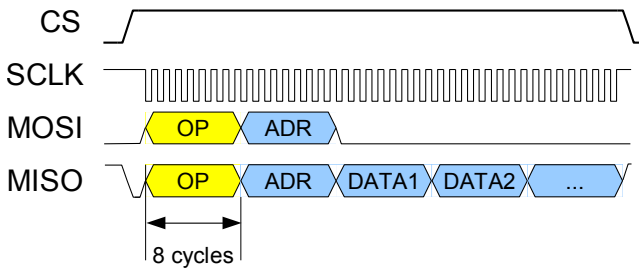


Figure 12: Read REGISTER (cont.)

Write to REGISTER (cont.)
The master transmits the opcode **Write to REGISTER (cont.)**. Start address ADR, from which point successive data DATA1-DATAn is to be written, is transmitted in the 2nd byte. The slave immediately outputs the opcode, address, and data at MISO. The slave increments its internal address counter after each DATAn data package.

If an error occurs during a write to register (cont.), i.e. the address is invalid, writing of the last address data has not finished, etc., the internal address counter is incremented no further and the FAIL error bit is set in the status byte (Table 14).

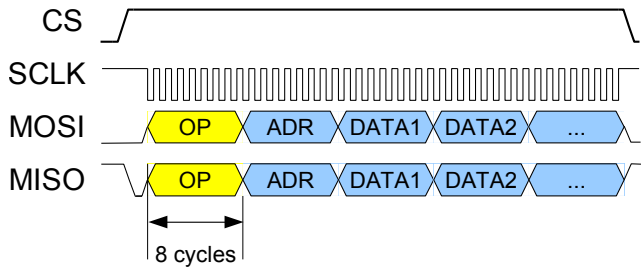


Figure 13: Write to REGISTER (cont.)

SIGNAL CONDITIONING

iC-LNG has various parameters for signal conditioning. The gain of the digital tracks and the analog track can both be set using parameter GR. A gain factor of 1.33 (GR = 0x01) can be used for most applications.

GR	Add. 0x07, bit 1:0
Code	Gain factor
0x00	1.0
0x01	1.33
0x02	1.6
0x03	2.0

Table 15: Gain range (all tracks)

The sine/cosine signals can be calibrated in amplitude and offset (Figure 14). To this end the LED current control must be programmed to sum control (LCSET(6) = 1) and the internal calibration signals switched to analog outputs PSIN, NSIN, PCOS, and NCOS (TA = 0x1).

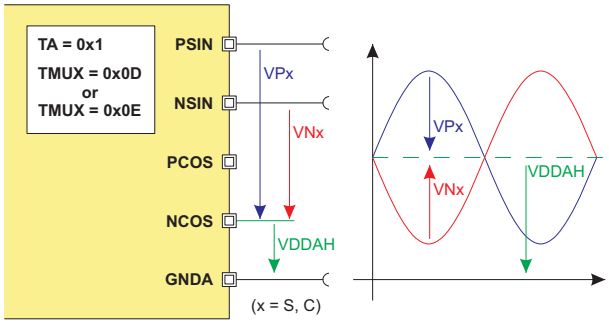


Figure 14: Sine/cosine signal calibration

To calibrate the sine signals TMUX must be programmed to 0x0D. The amplitude of signals PSIN and NSIN can then be calibrated using parameter GS. The target amplitude is 500 mVp.

GS	Add. 0x00, bit 5:0
Code	Gain factor
0x00	1.0
0x01	1.01
...	$\frac{1+GS \cdot 0.0053}{1-GS \cdot 0.0053}$
0x3F	2.0

Table 16: PSIN and NSIN gain

The offsets of PSIN and NSIN can be calibrated separately using parameters OSP and OSN. The offset of signal PSIN must be calibrated to reference signal VDDAH. This signal is available in test mode at pin NCOS. The offset of signal NSIN must then be calibrated to the calibrated offset of signal PSIN.

OSP	Add. 0x02, bit 6:0
Code	Offset value
0x00	0.45 · *VDDA*
0x01	0.4508 · *VDDA*
...	$(0.45 + \frac{OSP \cdot 0.1}{127}) \cdot VDDA$
0x7F	0.55 · *VDDA*

Table 17: PSIN offset

OSN	Add. 0x03, bit 6:0
Code	Offset value
0x00	0.45 · *VDDA*
0x01	0.4508 · *VDDA*
...	$(0.45 + \frac{OSN \cdot 0.1}{127}) \cdot VDDA$
0x7F	0.55 · *VDDA*

Table 18: NSIN offset

To calibrate the cosine signals TMUX must be programmed to 0x0E. The amplitude of signals PCOS and NCOS can then be calibrated to the same amplitude as that of the sine signals using parameter GS.

GC	Add. 0x01, bit 5:0
Code	Gain factor
0x00	1.0
0x01	1.01
...	$\frac{1+GC \cdot 0.0053}{1-GC \cdot 0.0053}$
0x3F	2.0

Table 19: PCOS and NCOS gain

The offsets of PCOS and NCOS can be calibrated separately using parameters OCP and OCN. The offset of signal PCOS must be calibrated to reference signal VDDAH. This signal is available in test mode at pin NCOS. The offset of signal NCOS must then be calibrated to the calibrated offset of signal PCOS.

OCP	Add. 0x04, bit 6:0
Code	Offset value
0x00	0.45 · *VDDA*
0x01	0.4508 · *VDDA*
...	$(0.45 + \frac{OCP \cdot 0.1}{127}) \cdot VDDA$
0x7F	0.55 · *VDDA*

Table 20: PCOS offset

OCN	Add. 0x05, bit 6:0
Code	Offset value
0x00	0.45 · *VDDA*
0x01	0.4508 · *VDDA*
...	$(0.45 + \frac{OCN \cdot 0.1}{127}) \cdot VDDA$
0x7F	0.55 · *VDDA*

Table 21: NCOS offset

The signal path of the SIN/COS tracks is shown in Figure 15 with the conditioning unit.

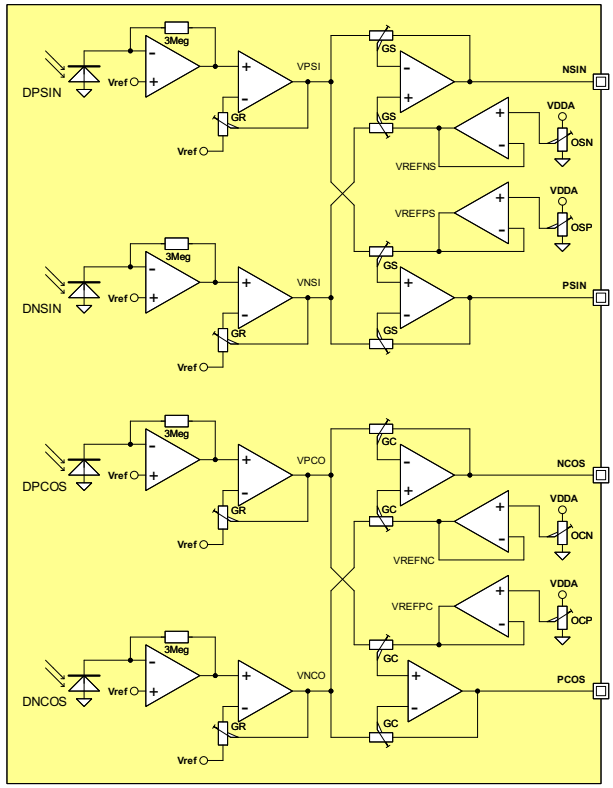


Figure 15: SIN/COS signal path

SYNCHRONIZATION

iC-LNG synchronizes the digital tracks to the interpolator.
NSYNC can be used to deactivate synchronization to check the adjustment or for code discs not in Gray code. The comparated signals of the digital tracks are then output.

NSYNC	Add. 0x07, bit 6
0	Synchronization activated
1	Synchronization deactivated

Table 22: Synchronization

PARALLEL ENCODER MODE

In parallel encoder mode an absolute position data word with a width of 14 bits is output in parallel. This position data word consists of the 11 bits of the digital tracks and of 3 bits interpolated from the analog track. The position data is output in Gray code. Parallel encoder mode is activated by parameter EPG (see also Operating Modes on page 14).

EPG	Add. 0x07, bit 4
0	Interface mode
1	Parallel encoder mode

Table 23: Selecting the operating mode

SHIFT REGISTER OUTPUT

In interface mode (EPG = 0) iC-LNG provides a shift register for the readout of position data. In order to be able to use this shift register the SPI interface sensor data channel must be deactivated by command **ACTIVATE** with **PACTIVE = 0** (Table 12).

After a power-on the shift register in iC-LNG is active. The position data is output in Gray code with the MSB first. This MSB is output in real time at the shift register output (pin DOUT) when NSL = 1. When NSL = 0 the position data is stored in the shift register and can then be output serially with rising edge CLK. The position data readout process is shown in Figure 16.

External data can be read into iC-LNG through shift register input pin DIN. This is output after the position data. For example, iC-LNG's pin ERR can be connected to pin DIN to link the alarm output to the position data.

The length of the shift register and the number of data bits used can be selected using parameter SRC, depending on the set SIN/COS resolution.

STA	Add. 0x08, bit 3
0	1024 SIN/COS cycles
1	512 SIN/COS cycles

Table 24: SIN/COS resolution

SRC	Add. 0x08, bit 2:0		
Code	Shift register length	Data bits for STA = 0	Data bits for STA = 1
0x0	16 bits	16	15
0x1	16 bits	16	15
0x2	16 bits	15	14
0x3	16 bits	14	13
0x4	16 bits	13	12
0x5	16 bits	12	11
0x6	14 bits	13	12
0x7	14 bits	12	11

Table 25: Shift register length

The MSB of the position data can be inverted by parameter DIR (code inversion).

DIR	Add. 0x07, bit 5
0	No code inversion
1	Code inversion

Table 26: Code inversion

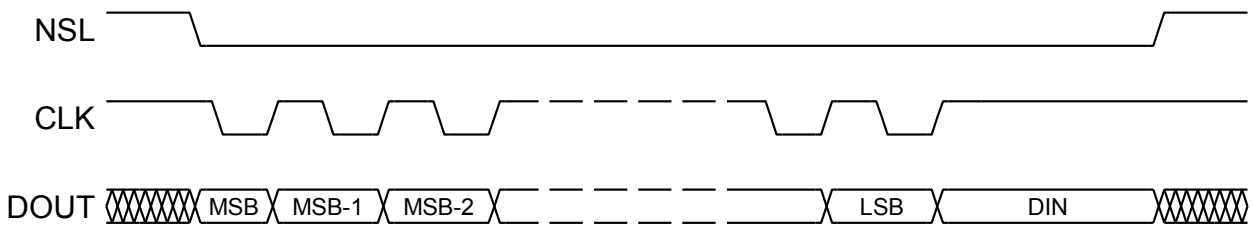


Figure 16: Shift register output (EPG = 0)

INCREMENTAL OUTPUT

At pins INCA and INCB either incremental signals with interpolation factors of 1 to 16 or internal digital signals are output. Selection is made using parameter INC.

INC	Add. 0x08, bit 6:4
0x00	Interpolation factor 1
0x01	Interpolation factor 2
0x02	Interpolation factor 4
0x03	Interpolation factor 8
0x04	Interpolation factor 16
0x05	Digital test
0x06	iC-Haus test 1
0x07	iC-Haus test 2

Table 27: Incremental output

At pin INCZ a zero pulse is output which is suitable for the selected interpolation factor. The zero pulse is symmetrical to the falling edge of the MSB signal on the digital tracks and is half an incremental cycle long gated with B low.
The phase relationship between the SIN/COS signals and the incremental signals is shown in Figure 17.

Output in digital test and iC-Haus test modes is described in the section on test functions on page 24.

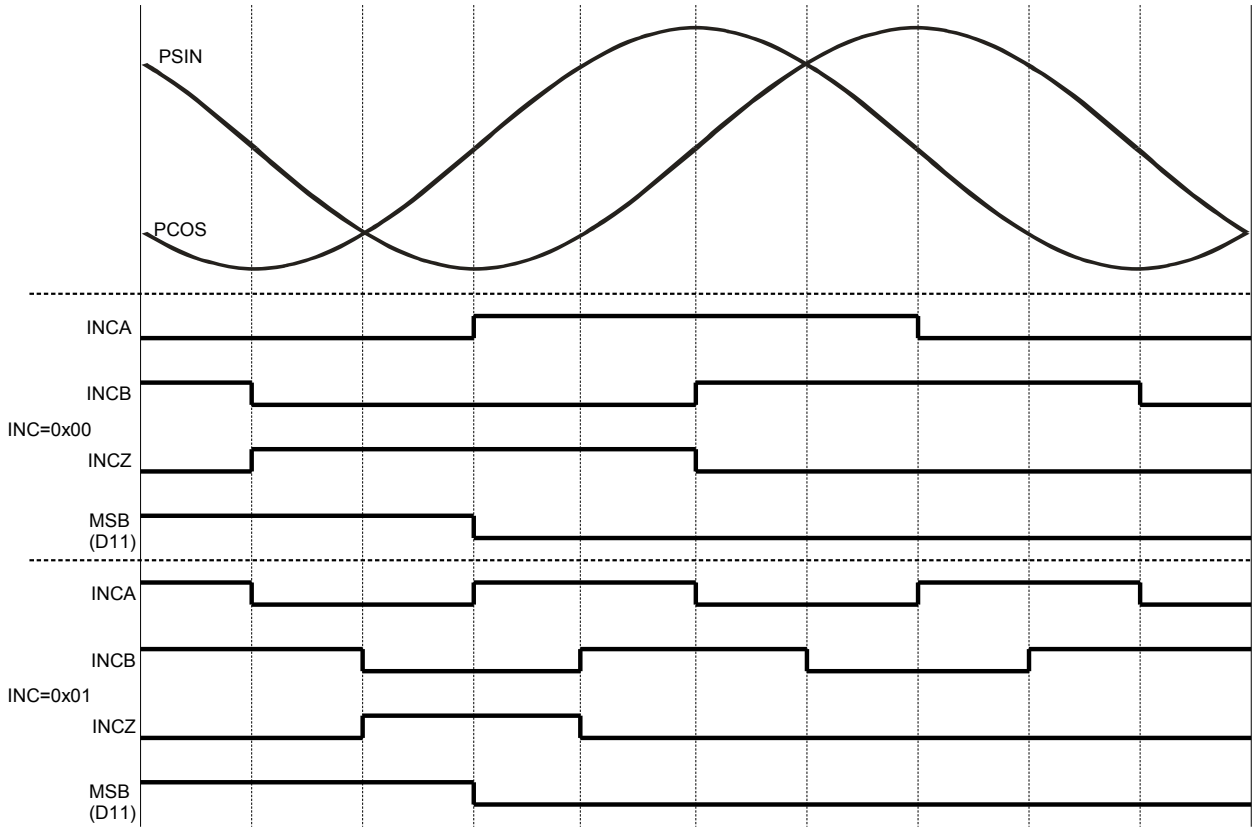


Figure 17: SIN/COS and ABZ phase relationship

LED CURRENT CONTROL

The optical receive power of the sine/cosine sensors is kept constant by the integrated LED control unit, regardless of the temperature and ageing effects of the LED. The type of control can be selected using parameter LCSET(6), the possible options being sum control or square control. So that the internal interpolator is always optimally controlled in all operating conditions, square control should be used. Sum control should be used for signal conditioning.

LCSET(6)	Add. 0x06, bit 6
0	Square control (sum of the amplitude squares)
1	Sum control (DC control prop. to VR())

Table 28: Control mode

The setpoint for the control can be configured using parameter LCSET(5:0).

LCSET(5:0)	Add. 0x06, bit 5:0	
Code	LCSET(6) = 0	LCSET(6) = 1
0x00	0.240 Vp	0.140 V
0x01	0.243 Vp	0.142 V
...	$\frac{0.24\,Vp}{1-i\cdot 0.0125}$	$\frac{0.14\,V}{1-i\cdot 0.0125}$
0x3F	1.1 Vp	0.640 V

Table 29: Control Setpoint

Error Monitoring
iC-LNG's LED current control range is monitored. Should the LED current control exit its control range, internal error ERRS is set to 1. This error signal is or-gated with iC-LNG's ERRP alarm (parity check) and output at error output ERR (cf. section on the alarm output).

ALARM OUTPUT

iC-LNG has an alarm or error output to indicate existing errors. If an error occurs, pin ERR is set to 1.

iC-LNG's LED current control range is monitored. Should the LED current control exit its control range, internal error ERRS is set to 1.

If the parity check signals an error in the RAM area, internal error ERRP is set to 1.

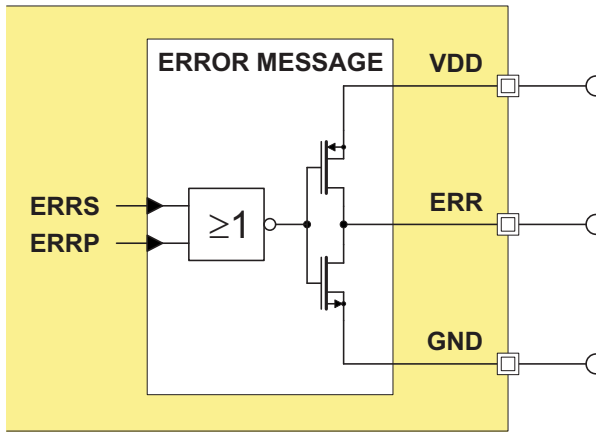


Figure 18: Alarm output

TEST FUNCTIONS

TA	Addr. 0x09; bit 5:4
Code	Output at SIN/COS
0x0	Normal operation
0x1	Test signals (cf. Table 31)
0x2	iC-Haus test
0x3	iC-Haus test

Table 30: Test modes

TMUX	Add. 0x09, bit 3:0			
Code	PSIN	NSIN	PCOS	NCOS
0x00	VPSI	VNSI	VPCI	VNCI
0x01	VPSI	VTH	A1	VREF
...	VPSI	VTH	A(TMUX)	VREF
0x0B	VPSI	VTH	A11	VREF
0x0C	VREFPS	VREFNS	VREFPC	VREFNC
0x0D	PSIN	NSIN	PCOS	VDDAH
0x0E	PCOS	NCOS	PSIN	VDDAH
0x0F	–	–	–	–

Table 31: Test signal multiplexer for analog signals

TMUX	Add. 0x09, bit 3:0	
Code	INCA	INCB
0x00	D09	D0
0x01	D1	D0
...	D(TMUX)	D0
0x0B	D11	D0
0x0C	I3	D0
0x0D	I2	D0
0x0E	I1	D0
0x0F	I0	D0

Table 32: Test signal multiplexer for digital signals

In the digital test synchronized data is output when NYSNC = 0; when NSYNC = 1 the comparator outputs of tracks 1-11 are output to D1-D11.

INC	Add. 0x08, bit 6:4	
Code	INCA	INCB
0x06	XALL	D0

Table 33: iC-Haus test 1

INC	Add. 0x08, bit 6:4	
Code	INCA	INCB
0x07	TP	NPOR

Table 34: iC-Haus test 2

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-LNG	30-Pin optoBGA, 7.6 mm x 7.1 mm, thickness 1.7 mm	Standard reticle LNG1R	iC-LNG oBGA LNB2C-1R
iC-LNG	30-Pin optoBGA, 7.6 mm x 7.1 mm, thickness 1.7 mm	Standard reticle LNG2R	iC-LNG oBGA LNB2C-2R
iC-LNG	30-Pin optoBGA, 7.6 mm x 7.1 mm, thickness 1.7 mm	Reticle on request	iC-LNG oBGA LNB2C-xR
iC-LNG	optoQFN Package	Under preparation	
		Suitable Encoder Discs:	
		1024 PPR OD / ID ⌀42.0 / 18.0 mm glass 1 mm	LNG1Sz 42-1024
		512 PPR OD / ID ⌀24.8 / 2.0 mm glass 1 mm	LNG2S 25-512

For technical support, information about prices and terms of delivery please contact:

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