

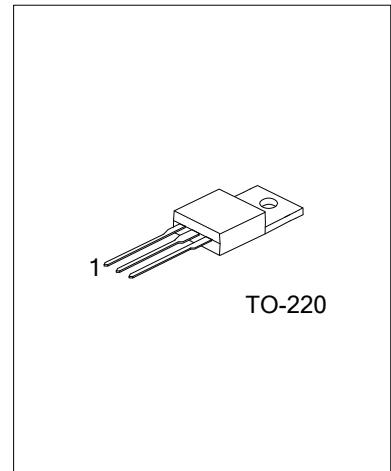


UT120N03

Preliminary

Power MOSFET

120A, 30V N-CHANNEL POWER MOSFET



DESCRIPTION

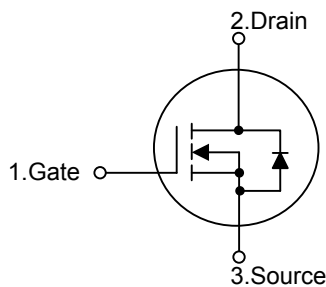
The UTC **UT120N03** is a N-channel power MOSFET using UTC's advanced trench technology to provide customers with a minimum on-state resistance and superior switching performance.

The UTC **UT120N03** is generally applied in DC to DC convertors or synchronous rectifications.

FEATURES

- * $I_D = 120A$
- * $V_{DS} = 30V$
- * $R_{DS(ON)} = 3.8m\Omega @ V_{GS} = 10V$
- * Low Gate Charge (Typical 54nC)
- * Fast Switching
- * 100% Avalanche Tested
- * High Power and Current Handling Capability

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT120N03L-TA3-T	UT120N03G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UT120N03L-TA3-T (1) Packing Type (2) Package Type (3) Lead Free	(1) T: Tube (2) TA3: TO-220 (3) G: Halogen Free, L: Lead Free
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■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	120	A
	Pulsed (Note 2)	I_{DM}	480	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	240	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	6.0	V/ns
Power Dissipation ($T_C=25^{\circ}\text{C}$)		P_D	125	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^{\circ}\text{C}$

- Note:
1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating: Pulse width limited by maximum junction temperature
 3. $L = 0.61\text{mH}$, $I_{AS} = 28\text{A}$, $V_{DD} = 27\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$
 4. $I_{SD} \leq 80\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$
 5. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 100A.

■ THERMAL CHARACTERISTICS

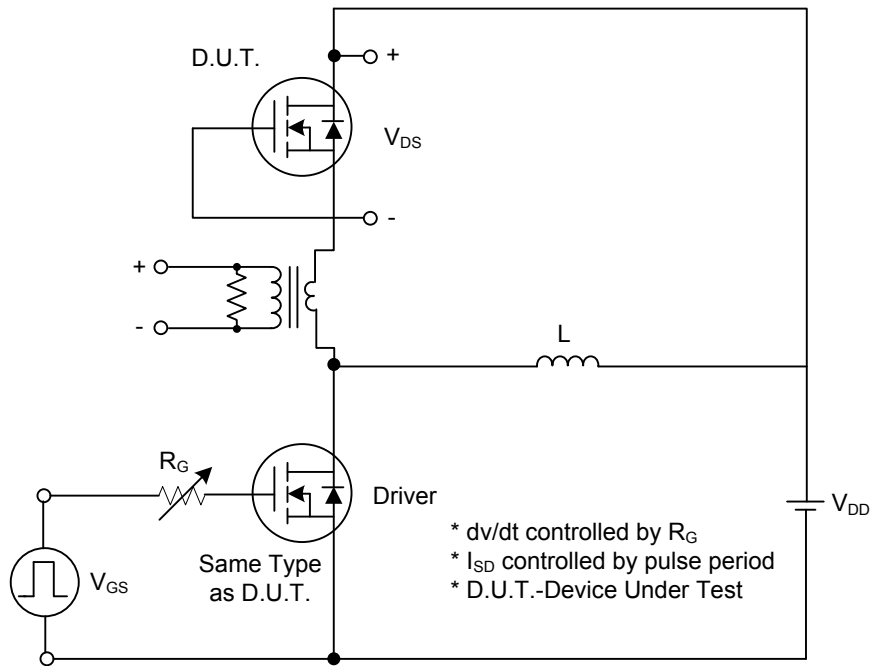
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	1	$^{\circ}\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_c=25°C, unless otherwise specified)

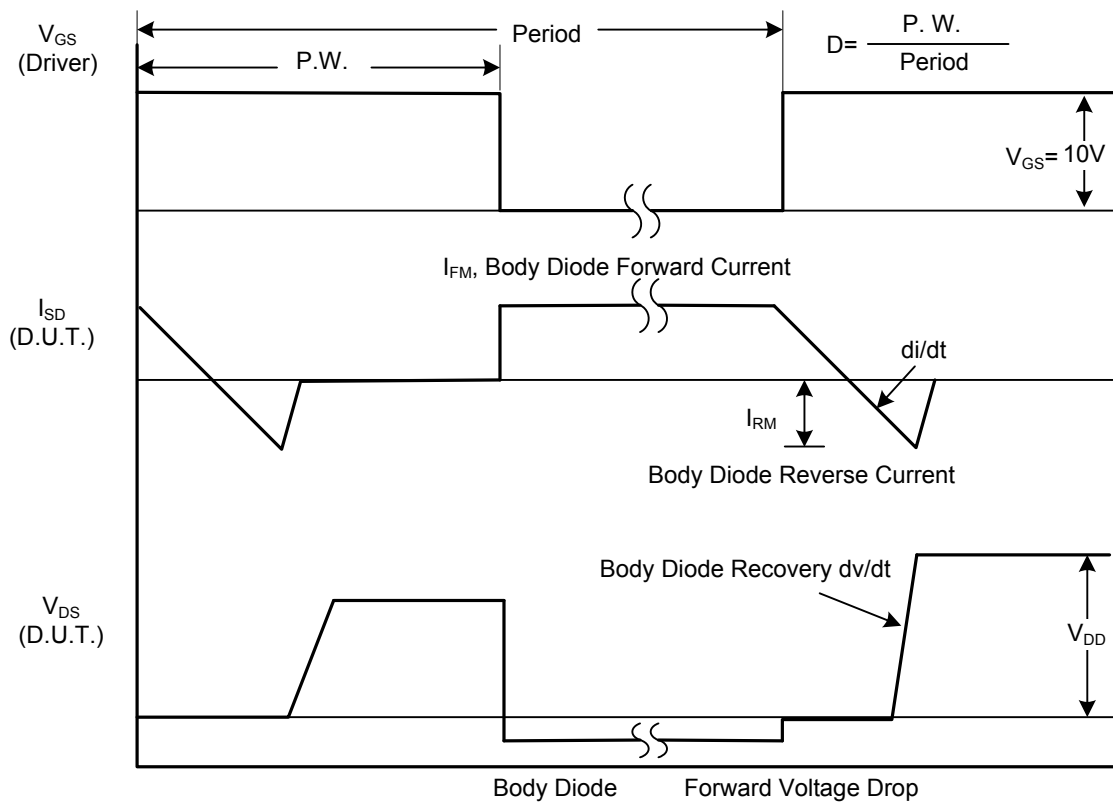
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V, T _c =25°C	30			V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =250μA				mV/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate- Source Leakage Current	Forward	V _{GS} =+20V, V _{DS} =0V		0.02	100	nA
	Reverse	V _{GS} =-20V, V _{DS} =0V		-0.02	-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =35A			3.8	mΩ
		V _{GS} =4.5V, I _D =35A			6.4	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		2990		pF
Output Capacitance	C _{OSS}			585		pF
Reverse Transfer Capacitance	C _{RSS}			340		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{GS} =5V, V _{DS} =15V, I _D =35A (Note 1, 2)		54	72	nC
Gate to Source Charge	Q _{GS}			8.0		nC
Gate to Drain Charge	Q _{GD}			10		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =15V, I _D =35A, R _G =4.7Ω, V _{GS} =5V (Note 1, 2)		9		ns
Rise Time	t _R			96		ns
Turn-OFF Delay Time	t _{D(OFF)}			47		ns
Fall-Time	t _F			37		ns
Gate Resistance	R _g			2.0		Ω
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V _{SD}	I _S =120A, V _{GS} =0V			1.25	V
Maximum Body-Diode Continuous Current	I _S				120	A
Maximum Body-Diode Pulsed Current	I _{SM}				480	A

- Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
 2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

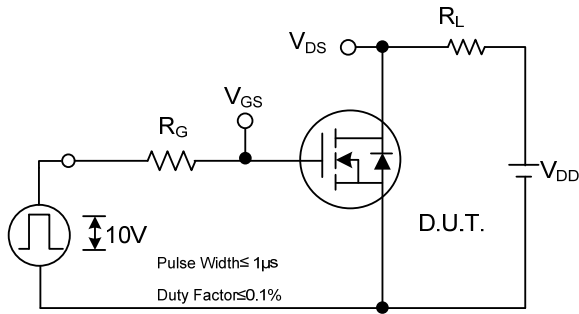


Peak Diode Recovery dv/dt Test Circuit

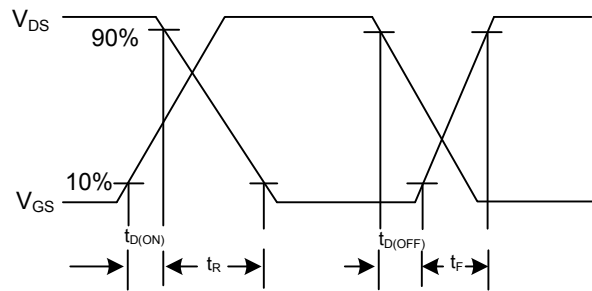


Peak Diode Recovery dv/dt Waveforms

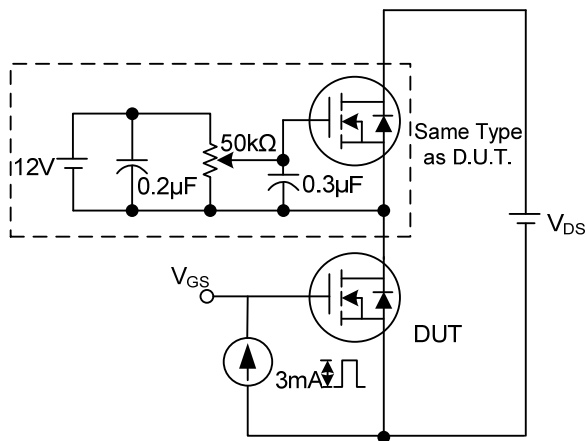
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



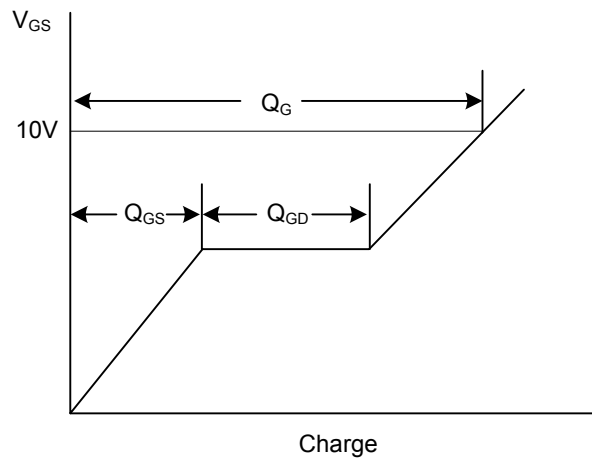
Switching Test Circuit



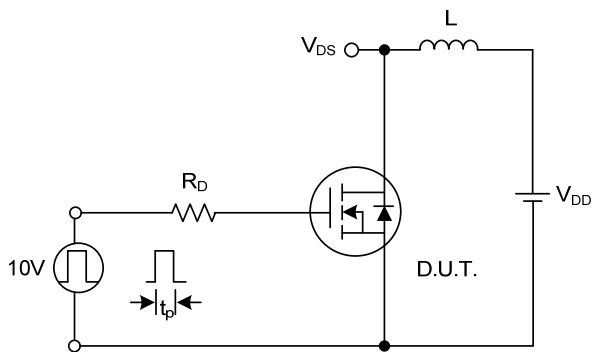
Switching Waveforms



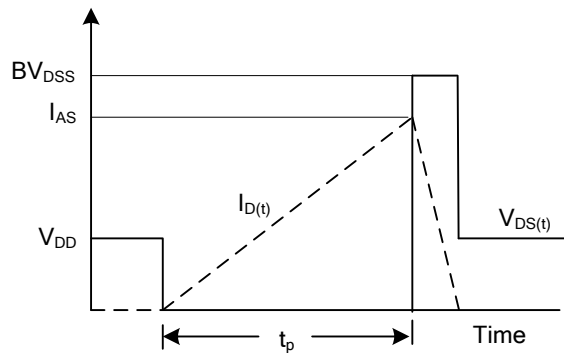
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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