# Nine-Output, 200-MHz Zero Delay Buffer

## Features

- **50-MHz to 200-MHz operating range**
- **650-ps max. Total Timing Budget™ (TTB™) window**
- **Nine low-skew outputs, grouped as 4 + 4 + 1**
  - **Output-output Skew < 200 ps**
  - **Device-device Skew < 500 ps**
- **Input-output skew < 250 ps**
- **Cycle-cycle jitter < 100 ps**
- **Three-stateable outputs**
- **< 50-μA shutdown current**
- **Spread Aware™**
- **Phase-locked loop (PLL) bypass mode (see *Table 1*)**
- **16-pin TSSOP**
- **3.3V operation**
- **Commercial/Industrial temperature**

## Description

The CY2309A is a high-performance 200-MHz zero delay buffer designed for high-speed clock distribution. The integrated PLL is designed for low jitter and optimized for noise rejection. These parameters are critical for reference clock distribution in systems using high-performance ASICs and microprocessors. The CY2309A PLL feedback is internal and is connected to CLKOUT.

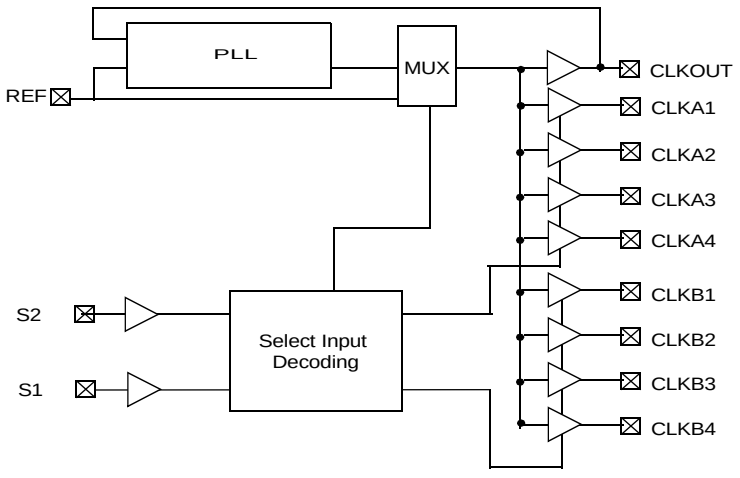
The device features a guaranteed maximum TTB window specifying all occurrences of output clocks with respect to the input reference clock across variations in output frequency, supply voltage, operating temperature, input edge rate, and process.

The CY2309A has two banks of four outputs each, which can be controlled by the select inputs as shown in *Table 1*. If all the output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes (PLL bypass mode).

The CY2309A PLL enters a power-down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 50 μA of current draw. The PLL shuts down in two additional cases, as shown in *Table 1*.

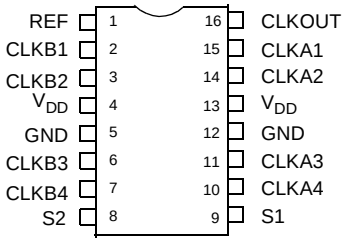
The CY2309A is available in standard (–1) or high-drive (–1H) output versions. The high-drive features faster rise and fall times.

## Block Diagram




## Pin Configuration

**TSSOP**
**Top View**



## Pin Description

| Pin | Name | Description |
|---|---|---|
| 1 | REF | Input reference frequency, 5V-tolerant input |
| 2 | CLKB1[1] | Clock output, Bank B |
| 3 | CLKB2[1] | Clock output, Bank B |
| 4 | $V_{DD}$ | 3.3V Supply |
| 5 | GND | Ground |
| 6 | CLKB3[1] | Clock output, Bank B |
| 7 | CLKB4[1] | Clock output, Bank B |
| 8 | S2[2] | Select input, 5V-tolerant input |
| 9 | S1[2] | Select input, 5V-tolerant input |
| 10 | CLKA4[1] | Clock output, Bank A |
| 11 | CLKA3[1] | Clock output, BankA |
| 12 | GND | Ground |
| 13 | $V_{DD}$ | 3.3V supply |
| 14 | CLKA2[1] | Clock output, Bank A |
| 15 | CLKA1[1] | Clock output, Bank A |
| 16 | CLKOUT[1] | Clock output, internal feedback on this pin |

**Table 1. Select Input Decoding**

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | CLKOUT[3] | Output Source | PLL Shutdown |
|---|---|---|---|---|---|---|
| 0 | 0 | Three-state | Three-state | Driven | PLL | N |
| 0 | 1 | Driven | Three-state | Driven | PLL | N |
| 1 | 0 | Driven | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |

## Zero Delay and Skew Control

Since the CLKOUT is the internal feedback to the PLL, its relative loading can adjust the input-output delay. See *Figure 1* For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay. If input-output delay adjustments are required, use the above graph to calculate loading differences between the CLKOUT and other outputs.

For zero output-output skew, be sure to load all outputs equally. For further information on using CY2309A, refer to the application note “CY2309 as PCI and SDRAM Buffers.”

**Notes:**
1. Weak pull-down.
2. Weak pull-up.
3. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

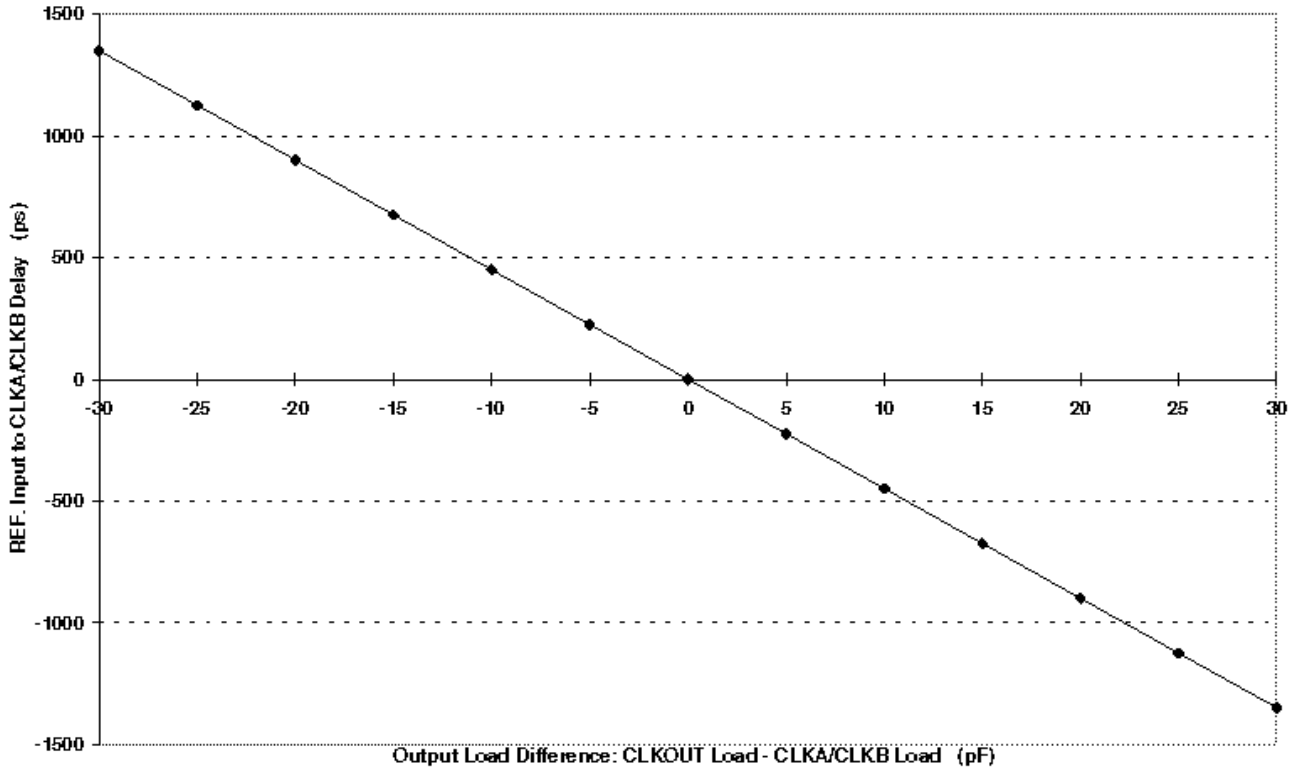



**Figure 1. REF. Input to CLKA/CLKB Delay vs. Difference in Loading between CLKOUT and CLKA/CLKB**

## Maximum Ratings

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage (Except REF, S2, S1) ..... –0.5V to $V_{DD}$ + 0.5V

DC Input Voltage (REF, S1, S2) ..... –0.5V to 7.0V

Storage Temperature ..... –65°C to +150°C

Junction Temperature ..... 125°C

Junction-to-Ambient Thermal Resistance 16-pin TSSOP ..... 115°C/W

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2000V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either $V_{SS}$ or $V_{DD}$).

**Table 2. Operating Conditions for CY2309AZC-XX Commercial Temperature Devices**

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.135 | 3.465 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| $C_{IN}$ | Input Capacitance | | 7 | pF |
| $t_{PU}$ | Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 500 | ms |

**Table 3. Electrical Characteristics for CY2309AZC-XX Commercial Temperature Devices**

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | CMOS Levels, 30% of $V_{DD}$ | | 0.25 | $V_{DD}$ |
| $V_{IH}$ | Input HIGH Voltage | CMOS Levels, 70% of $V_{DD}$ | 0.7 | | $V_{DD}$ |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0V | | 50 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{DD}$ | | 10 | µA |
| $I_{OL}$ | Output LOW Current[4], (–1) | $V_{OL}$ = 0.5V | 12 | | mA |
| | (–1H) | | 18 | | |
| $I_{OH}$ | Output HIGH Current[4], (–1) | $V_{OH}$ = $V_{DD}$ – 0.5V | | –12 | mA |
| | (–1H) | | | –18 | |
| $I_{DDS}$ | Power-down Supply Current | REF = 0V, S1 = $V_{DD}$, S2 = $V_{DD}$ | | 50 | µA |
| $I_{DD}$ | Supply Current | Unloaded outputs @ 200 MHz | | 115 | mA |
| | | Loaded outputs @ 200 MHz, $C_L$ = 10 pF | | 145 | |

**Table 4. Switching Characteristics for CY2309AZC-XX Commercial Temperature Devices[5]**

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Reference Frequency | | 50 | | 200 | MHz |
| | Reference Edge Rate | 30% to 70% of $V_{DD}$ | 0.5 | | 4 | V/ns |
| | Reference Duty Cycle | | 25 | | 75 | % |
| $t_1$ | Output Frequency | $C_L$ = 10 pF | 50 | | 200 | MHz |
| | | $C_L$ =15 pF | 50 | | 140 | MHz |
| | Duty Cycle[4] = $t_2$ / $t_1$ | Measured at $V_{DD}$/2 | 45 | 50 | 55 | % |
| $t_3$ | Rising Edge Rate[4], (–1) | 20% to 80% of $V_{DD}$, $C_L$= 15 pF | 0.8 | | 4 | V/ns |
| | Rising Edge Rate[4], (–1H) | 20% to 80% of $V_{DD}$, $C_L$= 15 pF | 1 | | 4 | V/ns |
| $t_4$ | Falling Edge Rate[4], (–1) | 80% to 20% of $V_{DD}$, $C_L$= 15 pF | 0.8 | | 4 | V/ns |
| | Falling Edge Rate[4], (–1H) | 80% to 20% of $V_{DD}$, $C_L$= 15 pF | 1 | | 4 | V/ns |

**Notes:**

4. Parameter is guaranteed by design and characterization. Not 100% tested in production.
5. All parameters specified with loaded outputs.

**Table 4. Switching Characteristics for CY2309AZC-XX Commercial Temperature Devices[5]** (continued)

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| TTB | Total Timing Budget window[6] | Outputs @ 200 MHz, Tracking Skew Not Included | | | 650 | ps |
| $t_5$ | Output to Output Skew[4] | All Outputs Equally Loaded | | | 200 | ps |
| $t_6$ | Input to Output Skew (Static Phase Error)[4] | Measured at $V_{DD}/2$, REF to CLKOUT | | | 250 | ps |
| $t_7$ | Device to Device Skew[4] | Measured at $V_{DD}/2$ | | | 500 | ps |
| $t_J$ | Cycle to Cycle Jitter[4] | Loaded Outputs | | | 200 | ps |
| | | | | | 35 | $ps_{RMS}$ |
| $t_{LOCK}$ | PLL Lock Time[4] | Stable Power Supply, Valid Clock at REF | | | 1.0 | ms |

**Table 5. Operating Conditions for CY2309AZI-XX Industrial Temperature Devices**

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.135 | 3.465 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | –40 | 85 | °C |
| $C_{IN}$ | Input Capacitance | | 7 | pF |
| $t_{PU}$ | Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 500 | ms |

**Table 6. Electrical Characteristics for CY2309AZI-XX Industrial Temperature Devices**

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | CMOS Level, 30% of $V_{DD}$ | | 0.25 | $V_{DD}$ |
| $V_{IH}$ | Input HIGH Voltage | CMOS Level, 70% of $V_{DD}$ | 0.7 | | $V_{DD}$ |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0V | | 50 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN} = V_{DD}$ | | 10 | µA |
| $I_{OL}$ | Output LOW Current[4], (–1) | $V_{OL}$ = 0.5V | 12 | | mA |
| | (–1H) | | 18 | | |
| $I_{OH}$ | Output HIGH Current[4],(–1) | $V_{OH} = V_{DD} – 0.5V$ | | –12 | mA |
| | (–1H) | | | –18 | |
| $I_{DDS}$ | Power-down Supply Current | REF = 0V S1 = $V_{DD}$, S2 = $V_{DD}$ | | 50 | µA |
| $I_{DD}$ | Supply Current | Unloaded outputs @ 133 MHz | | 80 | mA |
| | | Loaded outputs @ 133 MHz, $C_L$ = 10 pF | | 110 | |

**Table 7. Switching Characteristics for CY2309AZI–1 Industrial Temperature Devices[5]**

| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Reference Frequency | | 50 | | 133 | MHz |
| | Reference Edge Rate | 30% to 70% of $V_{DD}$ | 0.5 | | 4 | V/ns |
| | Reference Duty Cycle | | 25 | | 75 | % |
| $t_1$ | Output Frequency | $C_L$ = 15 pF | 50 | | 133 | MHz |
| | Duty Cycle[4] = $t_2 / t_1$ | Measured at VDD/2 | 40.0 | 50.0 | 60.0 | % |
| $t_3$ | Rising Edge Rate[4], (–1) | 20% to 80% of $V_{DD}$, $C_L$= 15 pF | 0.5 | | 3 | V/ns |
| | Rising Edge Rate[4], (–1H) | 20% to 80% of $V_{DD}$, $C_L$= 15 pF | 0.8 | | 4 | V/ns |
| $t_4$ | Falling Edge Rate[4], (–1) | 80% to 20% of $V_{DD}$, $C_L$= 15 pF | 0.5 | | 3 | V/ns |
| | Falling Edge Rate[4], (–1H) | 80% to 20% of $V_{DD}$, $C_L$= 15 pF | 0.8 | | 4 | V/ns |
| TTB | Total Timing Budget window[6] | Outputs @ 133 MHz, Tracking Skew Not Included | | | 650 | ps |

**Note:**

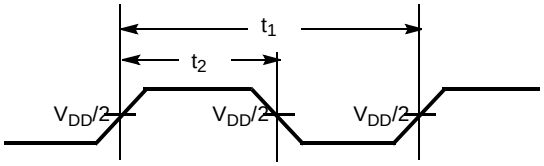
6. TTB is the window between the earliest and the latest output clocks with respect to the input reference clock across variations in output frequency, supply voltage, operating temperature, input clock edge rate, and process. The measurements are taken with the AC test load specified and include output-output skew, cycle-cycle jitter, and dynamic phase error.TTB will be equal to or smaller than the maximum specified value at a given output frequency.

**Table 7. Switching Characteristics for CY2309AZI–1 Industrial Temperature Devices[5]**

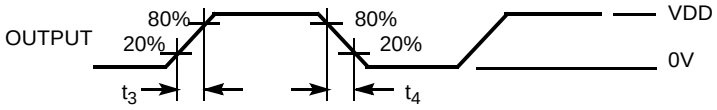
| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_5$ | Output to Output Skew[4] | All Outputs Equally Loaded | | | 200 | ps |
| $t_6$ | Input to Output Skew (Static Phase Error)[4] | Measured at $V_{DD}/2$, REF to CLKOUT | | | 250 | ps |
| $t_7$ | Device to Device Skew[4] | Measured at $V_{DD}/2$ | | | 500 | ps |
| $t_J$ | Cycle to Cycle Jitter[4] | Loaded Outputs | | | 200 | ps |
| | | | | | 35 | $ps_{RMS}$ |
| $t_{LOCK}$ | PLL Lock Time[4] | Stable Power Supply, Valid Clock at REF | | | 1.0 | ms |

## Switching Waveforms

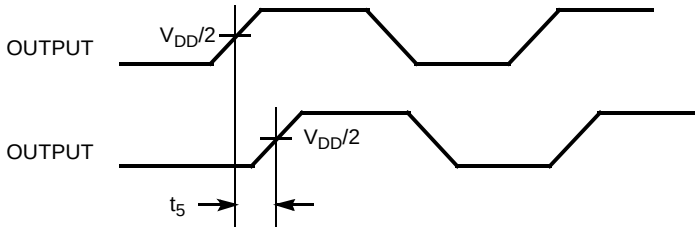
### Duty Cycle Timing



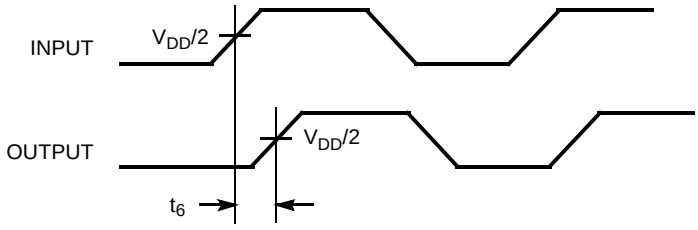

### All Outputs Rise/Fall Time




### Output-Output Skew

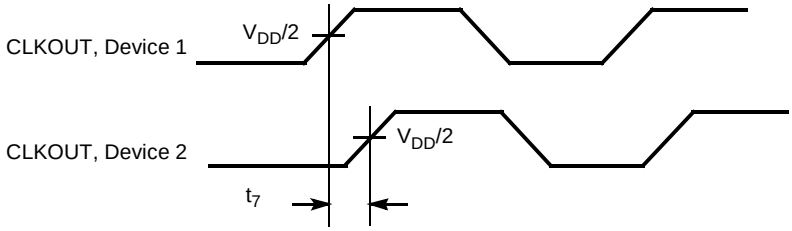



### Input-Output Propagation Delay

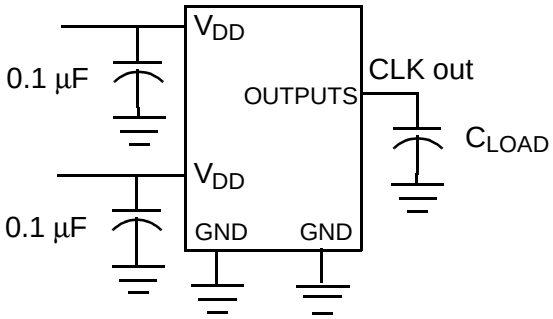


## Switching Waveforms (continued)

### Device-Device Skew




## Test Circuits

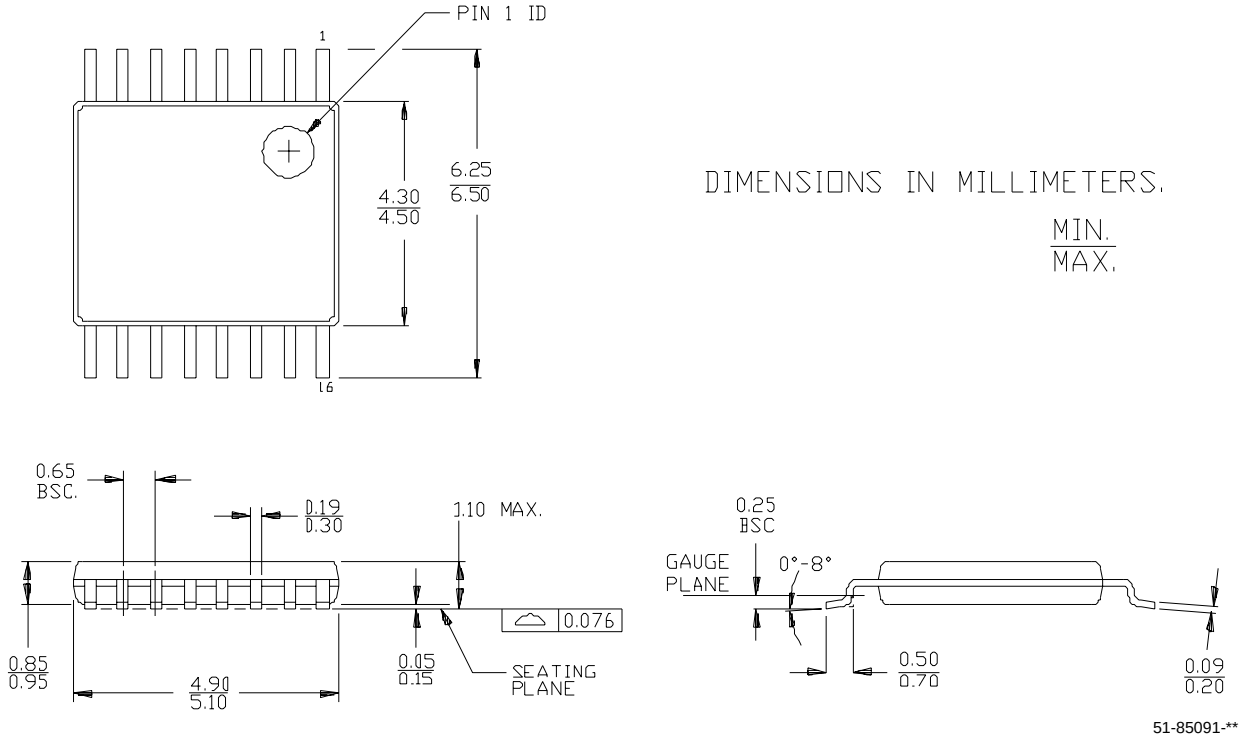



## Ordering Information

| Ordering Code | Package Type | Operating Range |
|---|---|---|
| CY2309AZC–1 | 16-pin 4.4-mm TSSOP | Commercial, 0°C to 70°C |
| CY2309AZC–1T | 16-pin 4.4-mm TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY2309AZC–1H | 16-pin 4.4-mm TSSOP | Commercial, 0°C to 70°C |
| CY2309AZC–1HT | 16-pin 4.4-mm TSSOP – Tape and Reel | Commercial, 0°C to 70°C |
| CY2309AZI–1 | 16-pin 4.4-mm TSSOP | Industrial, –40°C to 85°C |
| CY2309AZI–1T | 16-pin 4.4-mm TSSOP – Tape and Reel | Industrial, –40°C to 85°C |
| CY2309AZI–1H | 16-pin 4.4-mm TSSOP | Industrial, –40°C to 85°C |
| CY2309AZI–1HT | 16-pin 4.4-mm TSSOP – Tape and Reel | Industrial, –40°C to 85°C |

## Package Drawing and Dimensions

**16-pin Thin Shrunk Small Outline Package (4.40-MM Body) Z16**

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## Document History Page

| Document Title: CY2309A, Nine-Output, 200-MHz Zero Delay Buffer<br>Document Number: 38-07378 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 115507 | 08/19/02 | CTK | New Data Sheet |
| *A | 121893 | 12/14/02 | RBI | Power-up requirements added to Operating Conditions |
| *B | 124598 | 03/06/03 | RGL | Changed $V_{IL}$ max. value in Commercial Temp. device from 0.3V to 0.25V<br>Changed $I_{DD}$ max. values in Commercial Temp. device from 75 and 150 to 115 and 145 mA, respectively<br>Change $V_{IL}$ max. value in Industrial Temp. device from 0.3V to 0.25V<br>Changed $I_{DD}$ max.values in Industrial Temp. device from 60 and 120 mA to 80 and 110 mA<br>Removed Preliminary (final data sheet) |