405EZ

Preliminary Data Sheet

PowerPC 405EZ Embedded Processor

Features

- AMCC PowerPC® 405 32-bit RISC processor core operating at up to 416 MHz
- On-chip 32-bit peripheral bus (OPB) operating at up to 83 MHz
- On-chip 64-bit processor local bus (PLB) operating at up to 166 MHz
- 8-bit direct interface for NAND Flash devices
- 32 KB of on-chip, high-speed SRAM accessible by CPU and DMA
- Inter-chip connectivity (SPI and IIC)
- External 8-,16-, or 32-bit peripheral bus (EBC) operating at up to 83 MHz
- Boot from IIC bootstrap controller, EBC, NAND Flash, and SPI
- DMA support for all on-chip slaves and external bus, including on-chip SRAM, ADC, DAC, UARTs, and devices on the external peripheral bus
- One 10/100 Mbps Ethernet MII interface (half- and full-duplex) to external PHY
- Three USB 1.1 ports: two Host and one Device with Full-Speed on-chip PHYs
- Programmable universal interrupt controller (UIC)
- IEEE 1588 Precision Timing Protocol (PTP) controller
- Chameleon Timer™ and pulse width modulator (PWM)
- Analog-to-Digital Converter (ADC) with eight inputs and 10-bit resolution at 300 k samples/sec
- Digital-to-Analog Converter (DAC) with one input and 10-bit resolution at 30 M samples/sec
- Two CAN 2.0B protocol and ISO 11898-1 compliant channels
- Two serial ports (16750 compatible UART)
- One IIC interface operating at up to 400 kHz and supporting all standard IIC EEPROMs
- One SPI (SCP) synchronous full-duplex channel operating at up to 40 MHz
- 54 general purpose I/Os (GPIOs), each with programmable interrupts and outputs
- Supports JTAG for board-level testing
- System power management, low power dissipation and small form factor
- RoHS compliant (lead-free)

Description

With speeds up to 416 MHz, a flexible on-chip and off-chip memory architecture, a combination of an ADC, a DAC, a programmable Chameleon Timer/PWM, an IEEE 1588 PTP, and a diverse communications package that includes USB 1.1, Ethernet, and CAN, the PowerPC 405EZ embedded processor provides a low power and small footprint system-on-a-chip solution for a wide range of high performance, cost-constrained embedded applications. This includes industrial control, high-precision AC/DC and servo drive control, instrumentation, data acquisition, industrial automation, building and enclosure management, commercial and retail systems, Internet appliances, and intelligent USB peripherals. It is an easily programmable general purpose, 32-bit RISC controller that offers an upgrade path for applications in need of performance and connectivity improvements.

Technology: CU-11 CMOS, 130 nm

Package: 324-ball, 23 mm×23 mm, lead-free, plastic ball grid array (EPBGA), 1 mm ball pitch

Typical Power (Est.): 1.05W @ 166 MHz;1.48W @ 416 MHz

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Ordering, PVR, and JTAG Information

This section provides the part number nomenclature. For availability, contact your local AMCC sales office.

Product Name	Order Part Number (see **Notes:**)	Package	Rev Level	PVR Value	JTAG ID
PPC405EZ	PPC405EZ-CSAfffTx	23mm, 324-ball, EPBGA	A	0x41511460	0x0405A1E1

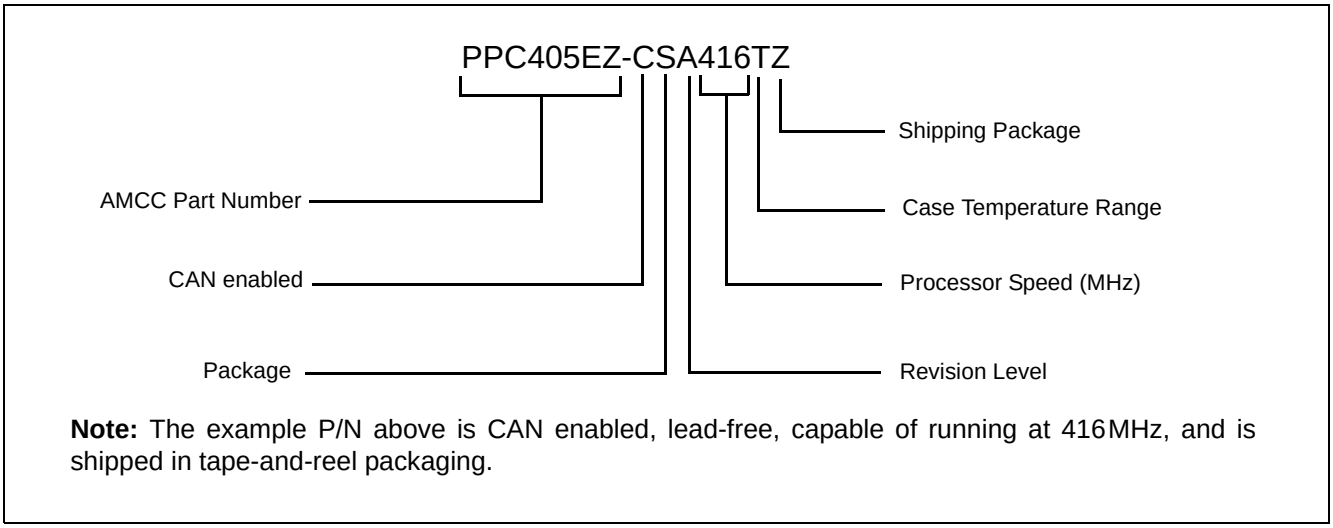
Notes:

1. C = CAN enabled
2. S = Lead-free EPBGA package (RoHS compliant)
3. A = Chip revision level A
4. fff = Processor frequency
   - 166 = 166MHz
   - 266 = 266MHz
   - 333 = 333MHz
   - 416 = 416MHz
5. T = Case temperature range, -40°C to +105°C
6. x = Shipping package type
   - Z = tape-and-reel
   - blank = tray

The part number contains a part modifier. Included in the modifier is a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only) and contain information that uniquely identifies the part. See the *PPC405EZ Embedded Processor User's Manual* for details about accessing these registers.

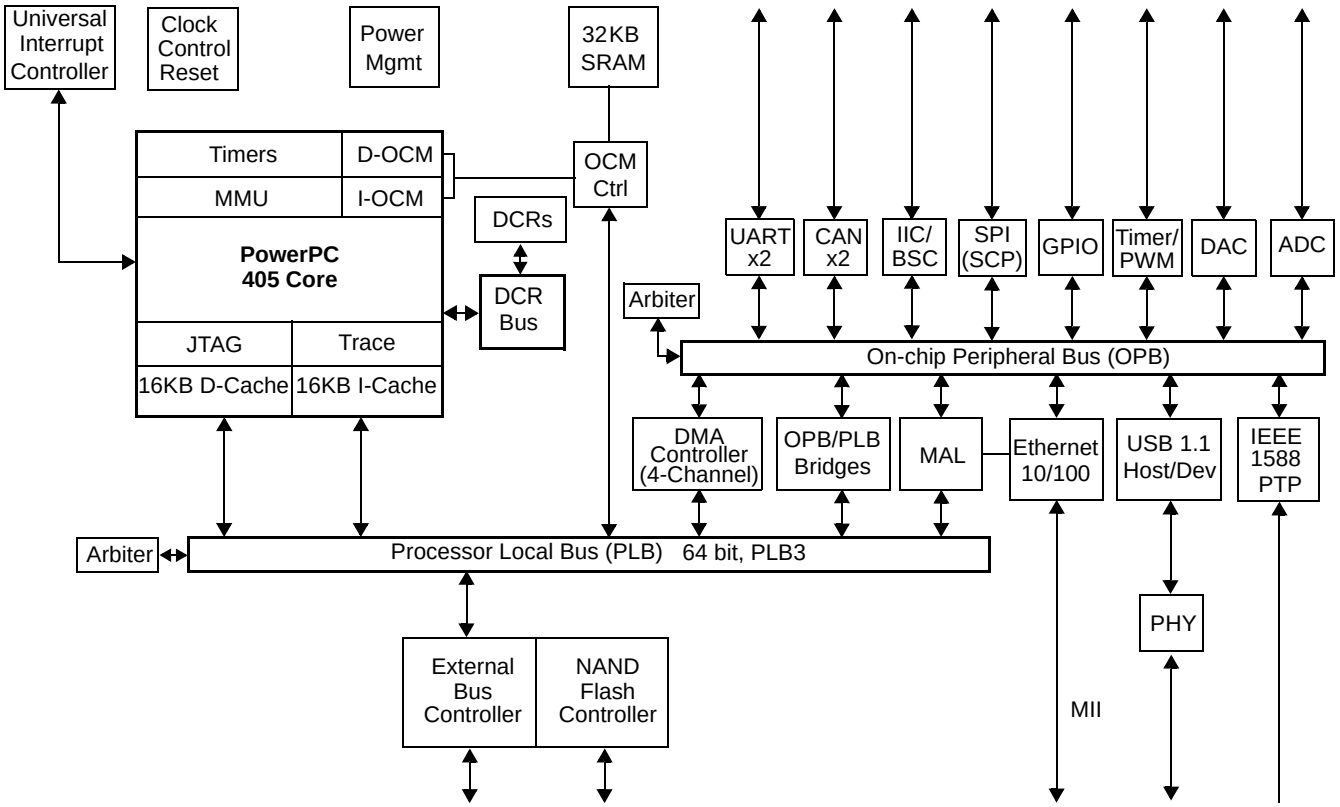
Order Part Number Key



Note: The example P/N above is CAN enabled, lead-free, capable of running at 416MHz, and is shipped in tape-and-reel packaging.

Block Diagram

Figure 1. PPC405EZ Embedded Controller Functional Block Diagram



The PPC405EZ is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an application-specific ASIC product. This approach provides a consistent way to create complex ASICs using IBM CoreConnect™ Bus Architecture.

Address Maps

The PPC405EZ incorporates two address maps. The first address map defines the possible use of addressable memory regions that the processor can access. The second address map defines Device Configuration Register (DCR) addresses (numbers). The DCRs are accessed by software running on the PPC405EZ processor through the use of **mtdcr** and **mfdcr** instructions.

Table 1. System Memory Address Map (4GB System Memory)

Function	Subfunction	Start Address	End Address	Size
General Use		0x 0000 0000	0x DFFF FFFF	3.7GB
Reserved		0x E000 0000	0x EF60 02FF	
UART 0 Registers		0x EF60 0300	0x EF60 03FF	256B
UART 1 Registers		0x EF60 0400	0x EF60 04FF	256B
IIC Registers		0x EF60 0500	0x EF60 05FF	256B
OPB Arbiter Registers		0x EF60 0600	0x EF60 06FF	256B
GPIO 0 Controller Registers		0x EF60 0700	0x EF60 07FF	256B
GPIO 1 Controller Registers		0x EF60 0800	0x EF60 08FF	256B
EMAC Registers		0x EF60 0900	0x EF60 09FF	256B
Reserved		0x EF60 0A00	0x EF60 0FFF	
CAN 0 Registers		0x EF60 1000	0x EF60 17FF	2KB
CAN 1 Registers		0x EF60 1800	0x EF60 1FFF	2KB
Chameleon Timer Registers		0x EF60 2000	0x EF60 27FF	2KB
IEEE 1588 Sync Controller Registers		0x EF60 2800	0x EF60 2FFF	2KB
USB 1.1 Host Registers		0x EF60 3000	0x EF60 31FF	512B
Reserved		0x EF60 3200	0x EF60 32FF	
DAC Registers		0x EF60 3300	0x EF60 33FF	256B
ADC Registers		0x EF60 3400	0x EF60 34FF	256B
Serial Communication Port Registers		0x EF60 3500	0x EF60 35FF	256B
Reserved		0x EF60 3600	0x EF63 FFFF	
USB 1.1 Device Registers		0x EF64 0000	0x EF67 FFFF	262KB
Reserved		0x EF68 0000	0x FFDF FFFF	
Boot Address Range		0x FFE0 0000	0x FFFF FFFF	2 MB

Notes:

1. If peripheral bus boot is selected, peripheral bank 0 is automatically configured at reset to the address range listed above.
2. After the boot process, software may reassign the boot memory regions for other uses.

Table 2. DCR Address Map

Function	Start Address	End Address	Size
Total DCR Address Space[1]	**0x000**	**0x3FF**	**1KW (4KB)[1]**
Reserved	0x000	0x00B	12B
CPR	0x00C	0x00D	2B
SDR	0x00E	0x00F	2B
Reserved	0x010	0x011	2B
EBC	0x012	0x013	2B
Reserved	0x014	0x01F	12B
OCM Controller	0x020	0x02F	16B
Reserved	0x030	0x07F	80B
PLB Arbiter	0x080	0x08F	16B
Reserved	0x090	0x09F	16B
PLB-to-OPB Bridge	0x0A0	0x0A7	8B
Reserved	0x0A8	0x0AF	8B
OPB-to-PLB Bridge	0x0B0	0x0B3	4B
Reserved	0x0B4	0x0B7	4B
CPM	0x0B8	0x0BB	4B
Reserved	0x0BC	0x0BF	4B
UIC	0x0C0	0x0CF	16B
Reserved	0x0D0	0x0DF	16B
IEEE 1588 Snapshot Source	0x0E0	0x0EF	16B
Reserved	0x0F0	0x0FF	16B
DMA	0x100	0x13F	64B
Reserved	0x140	0x2FF	578B
MAL	0x380	0x3FF	128B

Notes:

1. DCR address is 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

Power PC 405 Processor Core

The PPC405 core is a fixed-point, 32-bit RISC processor.

Features include:
- Five-stage pipeline with single-cycle execution of most instructions, including loads and stores
- Separate, configurable 16 KB D- and I-caches, both 2-way set associative
- Thirty-two 32-bit general purpose registers (GPRs)
- Unaligned load/store support
- Hardware multiply/divide
- Parity detection and reporting for the instruction cache, data cache, and translation look-aside buffer (TLB)
- Double word instruction fetch from cache
- Translation of the 4GB logical address space into physical addresses
- On-chip memory (OCM) interface
- Built-in timer and debug support
- Power management
- 32-bit DCR interface

Internal Buses

The PPC405EZ contains three internal buses: the on-chip peripheral bus (OPB), the processor local bus (PLB), and the device control register (DCR) bus. High bandwidth devices such as the processor and the DMA core utilize the PLB. Lower bandwidth I/O interfaces such as communications and timer interfaces utilize the OPB.

OPB

The OPB provides 32-bit address and data interfaces, and operates up to 83MHz. There is a bridge between the OPB and the PLB.

Features include:
- - Pipelined read support
- - Dynamic bus sizing
- - Single-cycle data transfer between masters and slaves

PLB

The Processor Local Bus (PLB) is a high-performance on-chip bus used to connect PLB-equipped master and slave devices to the PPC405 CPU. It provides a 64-bit data path with 32-bit addressing and operates at up to166MHz. There is a bridge between the PLB and the OPB.

Features include:
- Overlapping read and write transfers
- Decoupled address and data buses
- Address pipelining
- Late master request abort capability
- Hidden (overlapped) bus request/grant protocol
- Bus arbitration-locking mechanism
- Byte-enable capability allows for unaligned half word transfers and 3-B transfers
- Support for 16-, 32-, and 64-B line data transfers
- Read word address capability
- Sequential burst protocol
- Guarded and unguarded memory transfers
- DMA buffered, flyby, peripheral-to-memory, memory-to-peripheral, and DMA memory-to-memory operations

DCR Bus

The daisy-chained DCR bus provides a path for passing status and control information between the processor core and the other on-chip cores. All DCRs are 32 bits in width.

On-Chip Memory (OCM) Controller

The OCM controller connects the 405EZ processor core to two non-overlapping banks of single-port, on-chip, configurable 32KB SRAM memory. The OCM can also transfer data between the PLB and internal SRAM banks.

Features include:

- Simultaneous PLB3, instruction-Side OCM and data-Side OCM access
- PLB slave cycles support:
  - 64-bit slave attachment addressable by any PLB master
  - Single-beat read and write (1 to 8 bytes)
  - 4-, 8-, and 16-word line read and write
  - Double word and word read and write bursts
  - Slave-terminated double word and word bursts
  - Master-terminated variable length bursts
  - Data parity generation and checking
  - Read/Write protection per bank
- Instruction side interface supports:
  - One-Wait state OCM access with 1-deep write buffer
  - Data parity checking
- Data side interface supports:
  - One-wait state OCM access with 1-deep write buffer
  - Data parity generation and checking
  - Read/Write protection per bank
- Processor side data port has highest access priority (maintains predictable memory accesses to OCM)

External Bus Controller

The external bus controller (EBC) transfers data between the PLB and external memory or peripheral devices attached to the external peripheral bus. The EBC provides direct attachment of memory devices such as ROM and SRAM, DMA device paced memory devices, and DMA peripheral devices.

Features include:

- Up to 83 MHz speed
- 8-, 16-, or 32-bit data bus, 28-bit address bus
- Up to eight chip selects
- Arbitration and multi-master supported
- Flash ROM interface
- Boot from EBC (including NAND Flash interface) support
- Direct support for 8-,16-, or 32-bit SRAM and external peripherals
- CRAM/PSRAM support

NAND Flash Controller

The NAND Flash controller (NDFC) provides a simple interface between the External Bus Controller (EBC) and a variety of NAND Flash-based storage devices.

Features include:

- Attachment as internal EBC slave device (refer to the PPC405EZ Embedded Processor User’s Manual for

more details)
- Direct 8-bit interfacing to discrete NAND Flash devices
- Up to four banks of NAND Flash supported
- Device size 4MB-256MB (32Mb to 2Gb) supported
- 512B + 16B or 2kB + 64B device page sizes supported
- ECC generation - hamming code, single-bit correction, double-bit detection (SEC/DED)
- Eight-bit command write, address write, and data read/write
- Interrupt on device ready (after long page write or block erase operations)
- Boot from NAND
  - Executes up to 4 KB of boot code out of first block
  - Automatic page read accesses performed based on device configuration and read address

DMA Controller

The Direct Memory Access (DMA) controller is a Processor Local Bus (PLB) master that enables faster data transfer between memory and peripherals than is possible under program control. The 4-channel DMA controller handles data transfers between memory and peripherals and from memory-to-memory. Each channel has an independent set of registers needed for data transfer: a control register, a source address register, a destination address register, and a transfer count register.

Features include:
- Memory-to-memory transfers
- Buffered memory-to-peripheral transfers
- Buffered peripheral-to-memory transfers
- Four independent DMA channels
- Scatter/gather capability for dynamically programming multiple DMA transfers
- Programmable address increment or decrement
- Internal data buffering
- Can transfer data to/from any PLB and OPB slave, including OCM and external bus

USB Interface

The USB support provides separate Host and Device interfaces compliant with the USB1.1 Specification

Features include:
- USB1.1 Host (2 ports)
  - Compliant with *USB 1.1 Specification* and *OHCI version 1.0a Host Controller Specification*
  - Compatible with USB 2.0 Full-Speed peripherals
  - Supports Low-Speed (1.5Mbps) operation
  - All transfer types (Isochronous, Interrupt, Control, and Bulk) supported
  - Tx and Rx FIFOs: 16-entries x 32-bits each
  - Independent 32-bit OPB master and slave interfaces (master and slave can operate asynchronously)
  - Programmable OPB slave base address
  - Up to 127 connected devices supported
- USB1.1 Device (1 port)
  - Full- and Low-Speed device controller
  - 32-bit, OPB slave interface
  - Three Endpoints supported (Endpoint 0 is used for control)
    - Endpoints 1–2 can be IN, OUT, IN and OUT, IN/OUT programmable
    - Endpoints 1–2 configurable to support Interrupt/Bulk only, Isochronous only, Interrupt/Bulk or Isochronous (programmable) transfer types
    - Endpoints 1–2 configurable to support maximum packet size of 8, 16, 32, or 64 bytes
    - Endpoint 0 configurable to support maximum packet size of 8 or 16 bytes
- Full Speed (12 Mbps) USB PHY for each of the 3 USB ports
  - Tolerates shorting to 5.25V and shorting to ground if driving signal conditions meet those specified in the

Universal Serial Bus Specification

Controller Area Network (CAN)

The CAN controller module supports the concept of mailboxes. It contains 32 receive buffers, each one with its own message filter, and 32 transmit buffers with a prioritized arbitration scheme. For optimal support of Higher Level Protocols (HLP) such as DeviceNet or SDC, the message filter covers the first two data bytes.

Features include:

- CAN 2.0B protocol compliant
- ISO 11898-1 compliant
- 32 Transmit message holding registers, programmable priority arbitration
- Message abort command supported
- 32 Receive buffers (each with own message filter)
  - Message filtering: ID, IDE, Remote Transmission Request (RTR), data byte 1, and data byte 2
- Message buffers can be linked together to build bigger message arrays
- Automatic RTR response handler
- Message Abort command supported
- Maximum baud rate of 1Mbps with 8MHz system clock
- Listen-only for debugging supported
- Global masking supported
- 32-bit OPB slave interface
- Internal loopback

UART

The Universal Asynchronous Receiver/Transmitter (UART) interface provides two ports. The UART performs serial-to-parallel conversion on data received from a peripheral device or a modem, and parallel-to-serial conversion on data received from the processor.

Features include:

- Two ports (UART_0 and UART_1)
- Software modem control functions (CTS, RTS, DSR, DTR, RI, DCD) on UART_0
- Programmable auto flow (data flow controlled by RTS and CTS signals)
- 5-, 6-, 7-, or 8-bit characters
- Programmable start, stop, parity bit insertion
- 64 byte FIFOs to buffer Tx and Rx data
- LIN sub-bus specification compliant - line break generation/detection and false start bit detection
- Programmable internal/external loopback capabilities
- Low Power and Sleep mode
- Register conformance (after reset) to configuration of the NS16450 register set
- Hold and shift registers (eliminate need for precise synchronization between processor and serial data in character mode)
- Complete status reporting
- Full prioritized interrupt system controls
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generator (divides serial clock input and generates 16x clock)
- Ability to add/delete standard asynchronous communication bits such as start, stop, and parity to/from serial data
- Even, odd, or no-parity bit generation and detection
- 1-, 1.5-, or 2-stop bit generation
- Variable baud rate
- Internal diagnostic capability

- Loopback controls for isolating communications link faults
- Break, parity, overrun, framing error simulation
- OPB interface with optional DMA support

IIC Bus Interface

The Inter-Integrated Circuit (IIC) interface provides a Philips $I^2C^{®}$ compatible interface operating up to 400 kHz either as a master, a slave, or both with a bootstrap controller (BSC) included. During chip reset, the bootstrap controller can read configuration data from an IIC compatible memory device (e.g., EEPROM). This data can be used to replace the default configuration settings provided by the chip.

Features include:

- One IIC channel
- Compliant with *Philips Semiconductors I^2C Specification*, dated 1995
- 100 kHz or 400 kHz operation
- 8-bit data
- 10- or 7-bit address
- Slave Transmit and Receive
- Master Transmit and Receive
- Multiple bus masters supported
- Programmable as master, slave, or master/slave
- Boot parameters read from IIC attached memory with IIC bootstrap controller
- 32-bit OPB slave interface

Serial Peripheral Interface (SPI/SCP)

The Serial Peripheral Interface (SPI) (also known as the Serial Communications Port or SCP) is a full-duplex, synchronous, character-oriented (byte) port that allows the exchange of data with other serial devices. The SPI is a master on the serial port supporting a 3-wire interface (receive, transmit, and clock), and is a slave on the OPB.

Features include:

- One SPI/SCP channel, full duplex synchronous
- SPI/SCP master
- Up to 40 MHz
- Programmable internal loopback capabilities
- Multi-master protocol supported
- Independent masking of all interrupts (master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, receive FIFO overflow)
- Dynamic control of serial bit rate of data transfer (serial-master mode only)
- Data Item size for each data transfer under programmer control (4-to-16 bits)
- Boot from SPI supported
- 32-bit OPB slave interface

Chameleon Timer

The Chameleon Timer's Timer Service Engine (TSE) controls the local Timer RAM configured as 120 32-bit words and up to fifteen 24-bit timer channels, each with an Input Capture Register or an Output Compare Register. The Chameleon Timer interfaces to the OPB.

Features include:

- Pulse Width Modulation (PWM) and space vector PWM functions with non-overlap times
  - Programmable "deadband" intervals
  - Pulse period measurement
  - 48-bit input capture function
  - 48-bit output compare function
  - IEEE1588 time stamps
  - Automatic up, down, and up-then-down counting with modulus
- Autonomous Timer Service Engine (TSE) manages timer channels
  - CPU programs "registers" in Timer SRAM (120x32 bits)
- 15 timer channels + 1 timebase channel
- Pulse period measurements
- Configurable for seven 48-bit channels or 15 24-bit channels
- Up to two timebases available simultaneously
  - Each time base has four optional sources: three internal (Timebase A, Timebase B, and IEEE1588) and one external
- Speed/resolution: 166MHz counter, 2-clock (20ns) minimum period
- Latency: 0.49μsec worst case (based on 133MHz system clock)
- External "Fault" pin to automatically disable timer channel outputs
- Low EMC switching noise
- Unused Timer I/O pins available for GPIO use
- 32-bit OPB slave interface

General Purpose I/O (GPIO) Controller

The GPIO controller enables multiplexing of module I/O pins with multiple functions within the chip. That is, a single package pin can be assigned to multiple I/O functions. Which function the pin is assigned to is determined by register bit settings controlled by software. This significantly reduces the number of package pins needed to support multiple I/O groups.

Features include:

- Up to 54 GPIOs available
  - GPIOs are multiplexed with alternate functions
  - If not in use for dedicated functions, I/Os are available as GPIOs
- Direct control of all functions from registers programmed by means of OPB bus master accesses
- Time multiplexing of controller outputs to module outputs
- Programmable conversion of module outputs to open-drain outputs (enables sharing of active low outputs externally)
- Time multiplexing of module inputs to controller inputs

Universal Interrupt Controller (UIC)

The Universal Interrupt Controller (UIC) provides the control, status, and communications necessary between the various sources of interrupts and the PPC405 processor.

Features include:
- 32 interrupt sources supported (5 external)
- Generate interrupt on level (high or low) or edge (rising or falling)
- Programmable as synchronous (edge-capture or level-sensitive) or asynchronous (edge- or level-sensitive triggering)
- Each interrupt source/bit programmable as critical or non critical
- 32-bit DCR bus interface
- Optional interrupt handler vector generation
  - Programmable vector base address
  - Programmable vector offset size
  - Programmable interrupt priority ordering
- Programmable polarity for all interrupt types
- Interrupts of the same type do not need to be in contiguous bit positions
- Status registers provide: current state of all interrupts, current state of enabled interrupts

10/100 Ethernet

The Ethernet support provides a single 10/100 Mbps interface.

Features include:
- ANSI/IEEE Std. 802.3 and IEEE 802.3u supplement compliant
- Half-duplex and full-duplex supported
- MII interface to external PHY
- 512 byte receive FIFOs with programmable thresholds
- FCS control for transmit/receive packets
- Multiple packet handling in transmit and receive FIFOs
- Unicast, multicast, broadcast, and promiscuous address filtering
- Two 64-bit hash filters for unicast and multicast frames
- Automatic retransmission of collided frames
- Runt frame rejection
- Programmable inter-frame gap
- IEEE 802.3x compliant for frame-based flow control mechanism, including self-assembled control frame transmitting)
- Wake-on-LAN and Power-over-Internet supported
- Programmable internal/external loopback capabilities
- 32-bit OPB slave (MAC) and PLB master (MAL) interfaces
- Extensive error/status vector generation for each processed packet
- VLAN tag ID supported (according to IEEE Draft 802.3ac/D1.0 standard)
- Programmable automatic source address inclusion/replacement for transmit packets
- Programmable automatic Pad/FCS stripping for receive packets
- Programmable VLAN Tag inclusion/replacement for transmit packets

IEEE 1588 Precision Timing Protocol Controller

In a distributed control system containing multiple clocks, this feature defines messages used to exchange timing information for precision network synchronization purposes. A second UIC in the PPC405EZ is dedicated to generating snapshot triggers to the IEEE 1588 PTP controller from any interrupt source in the chip.

Analog-to-Digital Converter (ADC)

The ADC is a mixed-signal core. It uses the successive approximation (binary search) conversion technique to achieve minimal conversion time. The analog input range is 0.0V to Vref.

Features include:
- Internal 10-bit resolution SAR ADC
- Sample and hold
- Support for multiple conversion times such as
  - 3.25 μs with 4-MHz input clock
  - 52 μs with 250-kHz input clock
- Comparator
- Digital controller
- 8-channel analog input (3.3 V) with 8:1 analog multiplexer
- 10-bit parallel digital outputs
- Input trigger from Chameleon Timer supported
- OPB interface with optional DMA support

Digital-to-Analog Converter (DAC)

The DAC is a 1-channel converter, optimized for low power applications. It provides unbuffered single-ended analog current output. The single analog current output can be tied directly to an output resistor to provide twos-complementary, single-ended voltage outputs.

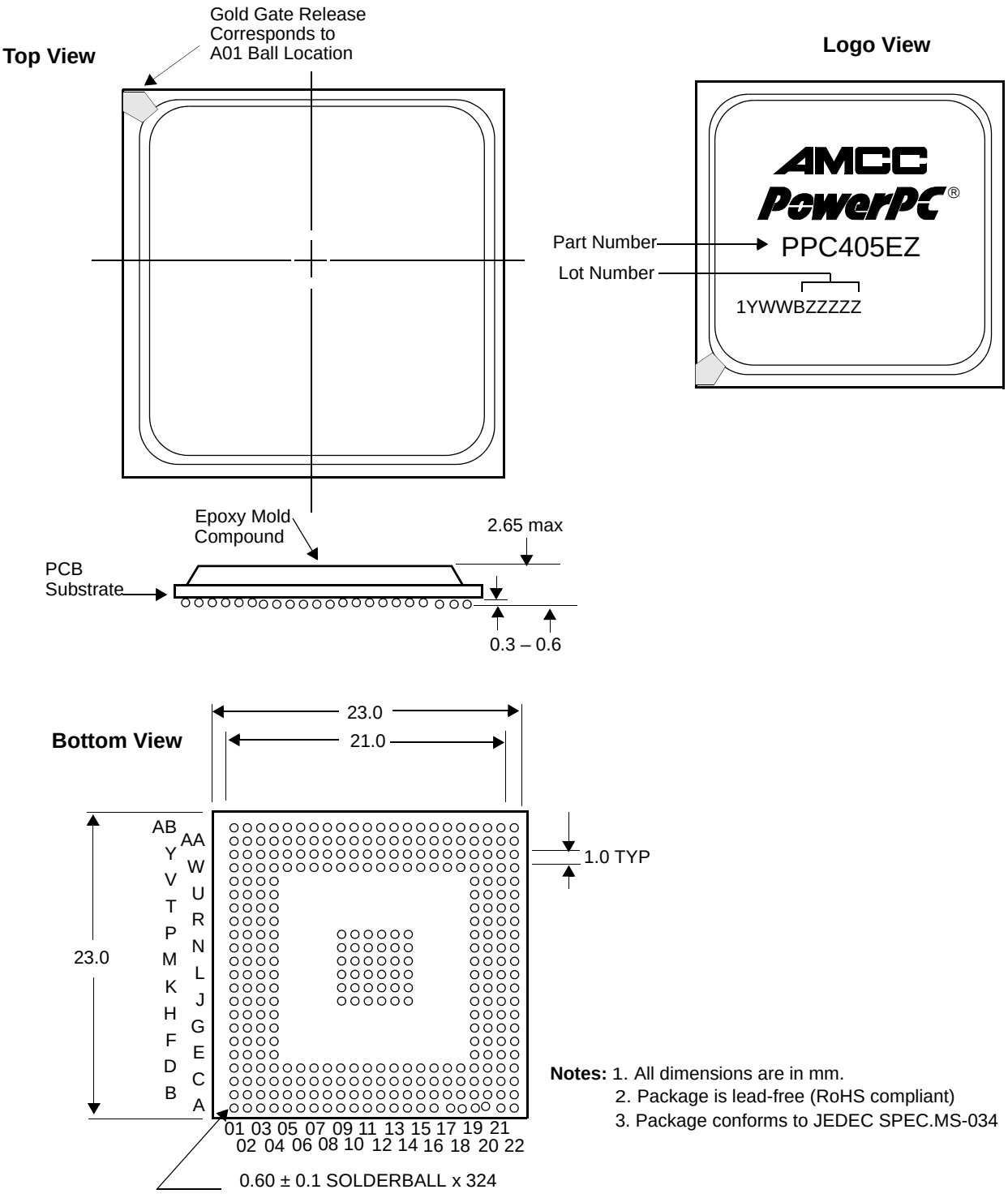
Features include:
- 10-bit resolution at 30 M samples/sec
- Segmented DAC
- Single-ended current outputs (6 mA maximum swing at 3.3 V)
- Monotonicity ensured
- Straight binary input
- Internal bandgap voltage reference
- Power management by means of Sleep Mode
- Integrated functional test logic
- Input trigger from Chameleon Timer supported
- OPB interface with optional DMA support

JTAG

Features include:
- IEEE 1149.1 test access port
- JTAG Boundary Scan Description Language (BSDL)

Refer to **http://www.amcc.com/Embedded/Partners** for a list of AMCC partners supplying probes for use with the JTAG interface.

Figure 2. 23mm, 324-Ball EPBGA Core



Notes: 1. All dimensions are in mm.
2. Package is lead-free (RoHS compliant)
3. Package conforms to JEDEC SPEC.MS-034

Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The Page column indicates the page within the table “Signal Functional Description” on page 35 on which the signals in the indicated interface group begin.

Table 3. Signals Listed Alphabetically (Sheet 1 of 11)

Signal Name	Ball	Interface Group	Page
ADC_AGND	AB07	Power	40
ADC_AV_{DD}	AB08		
ADC_In0	T01	Analog to Digital Converter (ADC)	37
ADC_In1	U01		
ADC_In2	W01		
ADC_In3	Y01		
ADC_In4	AA01		
ADC_In5	AB02		
ADC_In6	AB03		
ADC_In7	AB04		
ADC_InTrig[TS6][GPIO109]	U04		
ADC_VRef	AB06		
BusReq[GPIO007]	D20	External Peripheral	38
CAN0_Rx	C02	Controller Area Network	37
CAN0_Tx	B03		
$\overline{\text{CAN0\_TxE}}$	C01		
CAN1_Rx	C04		
CAN1_Tx	B04		
$\overline{\text{CAN1\_TxE}}$	A03		
$\overline{\text{CRAM\_AdV}}$[GPIO010]	B22	External Peripheral	38
CRAM_Clk[GPIO008]	F19		
DAC_AGND	A07	Power	40
DAC_AV_{DD}	A08		
DAC_CRef	B08	Digital to Analog Converter (DAC)	37
DAC_GRef	B07		
DAC_IOutP	A06		
DAC_IPTrig[TS5][GPIO108]	C08		
DAC_IRRef	B09		
DAC_VRef	B06		
DebugEn	C17	System	49
$\overline{\text{DMAAck}}$[GPIO027]	A19	External Peripheral	38
$\overline{\text{DMAEOT/TC}}$[GPIO026]	A20		
$\overline{\text{DMAReq}}$[GPIO025]	C19		
EMCCOL	U02	Ethernet	35
EMCCRS	J04		
EMCMDC	R03		
EMCMDIO	N03		

Table 3. Signals Listed Alphabetically (Sheet 2 of 11)

Signal Name	Ball	Interface Group	Page
EMCRxClk	M01	Ethernet	35
EMCRxDv	R01		
EMCRxD0	L02		
EMCRxD1	L01		
EMCRxD2	M02		
EMCRxD3	N01		
EMCRxEr	M03		
EMCTxClk	R02	Ethernet	35
EMCTxD0	N02		
EMCTxD1	P02		
EMCTxD2	P03		
EMCTxD3	P04		
EMCTxEn	U03		
EMCTxEr	T02		

Table 3. Signals Listed Alphabetically (Sheet 3 of 11)

Signal Name	Ball	Interface Group	Page
GND	A01	Power	40
GND	A02		
GND	A05		
GND	A09		
GND	A14		
GND	A18		
GND	A22		
GND	B02		
GND	B21		
GND	C03		
GND	C09		
GND	C20		
GND	D04		
GND	D06		
GND	D08		
GND	D09		
GND	D12		
GND	D15		
GND	D19		
GND	E01		
GND	E22		
GND	H04		
GND	H19		
GND	J01		
GND	J09		
GND	J11		
GND	J12		
GND	J14		
GND	J22		
GND	K10		
GND	K11		
GND	K13		
GND	L04		
GND	L09		
GND	L11		
GND	L12		
GND	L13		
GND	L14		

Table 3. Signals Listed Alphabetically (Sheet 4 of 11)

Signal Name	Ball	Interface Group	Page
GND	M09		
GND	M10		
GND	M11		
GND	M12		
GND	M14		
GND	M19		
GND	N10		
GND	N12		
GND	N13		
GND	P01		
GND	P09		
GND	P11		
GND	P12		
GND	P14		
GND	P22		
GND	R04		
GND	R19		
GND	V01		
GND	V22		
GND	W04	Power	40
GND	W06		
GND	W08		
GND	W09		
GND	W11		
GND	W15		
GND	W19		
GND	Y03		
GND	Y06		
GND	Y20		
GND	AA02		
GND	AA04		
GND	AA05		
GND	AA21		
GND	AB01		
GND	AB05		
GND	AB09		
GND	AB14		
GND	AB18		
GND	AB22		

Table 3. Signals Listed Alphabetically (Sheet 5 of 11)

Signal Name	Ball	Interface Group	Page
[GPIO000]PerCS4	G20	System	49
[GPIO001]PerCS5[NFCE1]	F20		
[GPIO002]PerCS6[NFCE2]	F21		
[GPIO003]PerCS7[NFCE3]	E21		
[GPIO004]HoldReq	D22		
[GPIO005]HoldPri	D21		
[GPIO006]HoldAck	C22		
[GPIO007]BusReq	D20		
[GPIO008]CRAM_Clk	F19		
[GPIO009]PerReady	C21		
[GPIO010]CRAM_AdV	B22		
[GPIO011]NFCLE	W03		
[GPIO012]NFData7	AA03		
[GPIO013]NFData6	Y02		
[GPIO014]NFData5	Y04		
[GPIO015]NFData4	Y05		
[GPIO016]NFData3	AA06		
[GPIO017]NFData2	Y07		
[GPIO018]NFData1	AA07		
[GPIO019]NFData0	Y08		
[GPIO020]NFALE	AA08		
[GPIO021]NFCE0	Y09		
[GPIO022]NFRE	AA09		
[GPIO023]NFWE	Y10		
[GPIO024]NFRB	AA10		
[GPIO025]DMAReq	C19		
[GPIO026]DMAEOT/TC	A20		
[GPIO027]DMAAck	A19		
[GPIO028]PWM_OE1[TS1O]	B15		
[GPIO029]PWM_OE2[TS2O]	A15		
[GPIO030]PWM_OE3[TS3]	C13		
[GPIO031]PWM_8	C11		

Table 3. Signals Listed Alphabetically (Sheet 6 of 11)

Signal Name	Ball	Interface Group	Page
[GPIO100]PWM_9	A10	System	49
[GPIO101]PWM_10	B10		
[GPIO102]PWM_11	C10		
[GPIO103]PWM_12	C06		
[GPIO104]PWM_13	C07		
[GPIO105]PWM_14	B05		
[GPIO106]PWM_15	C05		
[GPIO107]PWM_DivClk[IRQ4]	A04		
[GPIO108]DAC_IPTrig[TS5]	C08		
[GPIO109]ADC_InTrig[TS6]	U04		
[GPIO110]$\overline{\text{UART0\_DCD}}$	D02		
[GPIO111]$\overline{\text{UART0\_DSR}}$	D01		
[GPIO112]$\overline{\text{UART0\_CTS}}$	E03		
[GPIO113]$\overline{\text{UART0\_DTR}}$[TmrClk][IEEE_1588TS]	F04		
[GPIO114]$\overline{\text{UART0\_RTS}}$[$\overline{\text{SPI\_SS\_2}}$]	F03		
[GPIO115]$\overline{\text{UART0\_RI}}$[$\overline{\text{SPI\_SS\_3}}$]	E02		
[GPIO116][$\overline{\text{SPI\_SS\_In}}$]$\overline{\text{SPI\_SS1}}$	D14		
[GPIO117]IRQ0[TrcClk]	T03		
[GPIO118]IRQ1[TS1E]	V02		
[GPIO119]IRQ2[TS2E]	V03		
[GPIO120]IRQ3[TS4]	W02		
GPIO121	C14		
$\overline{\text{Halt}}$	C18	System	36
HoldAck[GPIO006]	C22	External Peripheral	38
$\overline{\text{HoldPri}}$[GPIO005]	D21		
$\overline{\text{HoldReq}}$[GPIO004]	D22		
[IEEE_1588TS]$\overline{\text{UART0\_DTR}}$[TmrClk][GPIO113]	F04	IEEE 1588 Network Synchronization	35
IIC0SClk	B16	IIC Peripheral	35
IIC0SData	C15		
IRQ0[TrcClk][GPIO117]	T03	Interrupt	35
IRQ1[TS1E][GPIO118]	V02		
IRQ2[TS2E][GPIO119]	V03		
IRQ3[TS4][GPIO120]	W02		
[IRQ4]PWM_DivClk[GPIO107]	A04		
NFALE[GPIO020]	AA08	NAND Flash	38
$\overline{\text{NFCE0}}$[GPIO021]	Y09	NAND Flash	38
[$\overline{\text{NFCE1}}$]$\overline{\text{PerCS5}}$[GPIO001]	F20		
[$\overline{\text{NFCE2}}$]$\overline{\text{PerCS6}}$[GPIO002]	F21		
[$\overline{\text{NFCE3}}$]$\overline{\text{PerCS7}}$[GPIO003]	E21		
NFCLE[GPIO011]	W03		
NFData0[GPIO019]	Y08	NAND Flash	38
NFData1[GPIO018]	AA07		
NFData2[GPIO017]	Y07		
NFData3[GPIO016]	AA06		
NFData4[GPIO015]	Y05		
NFData5[GPIO014]	Y04		
NFData6[GPIO013]	Y02		
NFData7[GPIO012]	AA03		

Table 3. Signals Listed Alphabetically (Sheet 7 of 11)

Signal Name	Ball	Interface Group	Page
NFRB[GPIO024]	AA10	NAND Flash	38
$\overline{\text{NFRE}}$[GPIO022]	AA09		
$\overline{\text{NFWE}}$[GPIO023]	Y10		
$OV_{DD}1$	D05	Power	40
$OV_{DD}1$	D07		
$OV_{DD}1$	D11		
$OV_{DD}1$	D16		
$OV_{DD}1$	D18		
$OV_{DD}1$	E04		
$OV_{DD}1$	G04		
$OV_{DD}1$	J10		
$OV_{DD}1$	J13		
$OV_{DD}1$	K09		
$OV_{DD}1$	M04		
$OV_{DD}1$	N09		
$OV_{DD}1$	P10		
$OV_{DD}1$	T04		
$OV_{DD}1$	V04		
$OV_{DD}1$	W05		
$OV_{DD}1$	W07		
$OV_{DD}2$	E19	Power	40
$OV_{DD}2$	G19		
$OV_{DD}2$	K14		
$OV_{DD}2$	L19		
$OV_{DD}2$	N14		
$OV_{DD}2$	P13		
$OV_{DD}2$	T19		
$OV_{DD}2$	V19		
$OV_{DD}2$	W12		
$OV_{DD}2$	W16		
$OV_{DD}2$	W18		

Table 3. Signals Listed Alphabetically (Sheet 8 of 11)

Signal Name	Ball	Interface Group	Page
PerAddr04	U19	External Peripheral	38
PerAddr05	V20		
PerAddr06	W21		
PerAddr07	W22		
PerAddr08	U20		
PerAddr09	V21		
PerAddr10	U21		
PerAddr11	U22		
PerAddr12	T20		
PerAddr13	T21		
PerAddr14	T22		
PerAddr15	R20		
PerAddr16	P19		
PerAddr17	R21		
PerAddr18	R22		
PerAddr19	P20		
PerAddr20	P21		
PerAddr21	N20		
PerAddr22	N21		
PerAddr23	N22		
PerAddr24	M20		
PerAddr25	M21		
PerAddr26	M22		
PerAddr27	L22		
PerAddr28	L21		
PerAddr29	L20		
PerAddr30	K22		
PerAddr31	K21		
PerClk	K20	External Peripheral	38
$\overline{\text{PerCS0}}$	H20		
$\overline{\text{PerCS1}}$	G22		
$\overline{\text{PerCS2}}$	G21		
$\overline{\text{PerCS3}}$	F22		
$\overline{\text{PerCS4}}$[GPIO000]	G20		
$\overline{\text{PerCS5}}$[$\overline{\text{NFCE1}}$][GPIO001]	F20		
$\overline{\text{PerCS6}}$[$\overline{\text{NFCE2}}$][GPIO002]	F21		
$\overline{\text{PerCS7}}$[$\overline{\text{NFCE3}}$][GPIO003]	E21		

Table 3. Signals Listed Alphabetically (Sheet 9 of 11)

Signal Name	Ball	Interface Group	Page
PerData00	Y11	External Peripheral	38
PerData01	AA11		
PerData02	AA12		
PerData03	AB13		
PerData04	Y12		
PerData05	AA13		
PerData06	AB15		
PerData07	Y13		
PerData08	AA14		
PerData09	AA15		
PerData10	AB16		
PerData11	Y14		
PerData12	W14		
PerData13	AB17		
PerData14	Y15		
PerData15	AA16		
PerData16	Y16		
PerData17	AA17		
PerData18	AA18		
PerData19	Y17		
PerData20	Y18		
PerData21	AB19		
PerData22	W17		
PerData23	AA19		
PerData24	AB20		
PerData25	Y19		
PerData26	AA20		
PerData27	AB21		
PerData28	Y22		
PerData29	AA22		
PerData30	Y21		
PerData31	W20		
$\overline{\text{PerOE}}$	E20	External Peripheral	38
PerReady[GPIO009]	C21	External Peripheral	38
Per$\overline{\text{RW}}$	J21	External Peripheral	38
$\overline{\text{PerWBE0}}$	J20	External Peripheral	38
$\overline{\text{PerWBE1}}$	H22		
$\overline{\text{PerWBE2}}$	J19		
$\overline{\text{PerWBE3}}$	H21		
PLL_AGND	AB11	Power	40
PLL_AV_{DD}	AB12		
PWM_DivClk[IRQ4][GPIO107]	A04	Chameleon Timer	36
PWM_OE0	A16	Chameleon Timer	36
PWM_OE1[TS1O][GPIO028]	B15		
PWM_OE2[TS2O][GPIO029]	A15		
PWM_OE3[TS3][GPIO030]	C13		
PWM_TBA	B14		

Table 3. Signals Listed Alphabetically (Sheet 10 of 11)

Signal Name	Ball	Interface Group	Page
PWM_1	B13	Chameleon Timer	36
PWM_2	C12		
PWM_3	B12		
PWM_4	A13		
PWM_5	A12		
PWM_6	A11		
PWM_7	B11		
PWM_8[GPIO031]	C11		
PWM_9[GPIO100]	A10		
PWM_10[GPIO101]	B10		
PWM_11[GPIO102]	C10		
PWM_12[GPIO103]	C06		
PWM_13[GPIO104]	C07		
PWM_14[GPIO105]	B05		
PWM_15[GPIO106	C05		
Reserved	B19	Other Pins	40
SPI_ClkOut	B17	Serial Peripheral	38
SPI_DI	D17		
SPI_DO	C16		
$\overline{\text{SPI\_SS0}}$	A17		
$\overline{\text{SPI\_SS1}}$[$\overline{\text{SPI\_SS\_In}}$][GPIO116]	D14		
[$\overline{\text{SPI\_SS2}}$]UART0_RTS[GPIO114]	F03		
[$\overline{\text{SPI\_SS3}}$]$\overline{\text{UART0\_RI}}$[GPIO115]	E02		
[$\overline{\text{SPI\_SS\_In}}$]$\overline{\text{SPI\_SS1}}$[GPIO116]	D14		
SysClk	AB10	System	36
SysErr	B20		
$\overline{\text{SysReset}}$	B18		
TCK	H01	JTAG	35
TDI	L03		
TDO	K03		
TestEn	A21		
TMS	G02	JTAG	35
[TmrClk]UART0_DTR[IEEE1588TS][GPIO113]	F04	System	36
[TrcClk]IRQ0[GPIO117]	T03	Trace	36
$\overline{\text{TRST}}$	G01	JTAG	35
[TS1E]IRQ1[GPIO118]	V02	Trace	36
[TS2E]IRQ2[GPIO119]	V03		
[TS1O]PWM_OE1[GPIO028]	B15		
[TS2O]PWM_OE2[GPIO029]	A15		
[TS3]PWM_OE3[GPIO030]	C13		
[TS4]IRQ3[GPIO120]	W02		
[TS5]DAC_IPTrig[GPIO108]	C08		
[TS6]ADC_InTrig[GPIO109]	U04		

Table 3. Signals Listed Alphabetically (Sheet 11 of 11)

Signal Name	Ball	Interface Group	Page
$\overline{\text{UART0\_CTS}}$[GPIO112]	E03	UART Peripheral	39
$\overline{\text{UART0\_DCD}}$[GPIO110]	D02		
$\overline{\text{UART0\_DSR}}$[GPIO111]	D01		
$\overline{\text{UART0\_DTR}}$[TmrClk][IEEE_1588TS][GPIO113]	F04		
$\overline{\text{UART0\_RI}}$[$\overline{\text{SPI\_SS\_3}}$][GPIO115]	E02		
$\overline{\text{UART0\_RTS}}$[$\overline{\text{SPI\_SS\_2}}$][GPIO114]	F03		
UART0_Rx	B01		
UART0_Tx	D03		
UART1_Rx	F02	UART Peripheral	39
UART1_Tx	F01		
USB_FClk	G03	USB	39
USB1Dev0	K02		
$\overline{\text{USB1Dev0}}$	K01		
USB1Host0	H03		
$\overline{\text{USB1Host0}}$	H02		
USB1Host1	J03		
$\overline{\text{USB1Host1}}$	J02		
V_{DD}	D10	Power	40
V_{DD}	D13		
V_{DD}	K04		
V_{DD}	K12		
V_{DD}	K19		
V_{DD}	L10		
V_{DD}	M13		
V_{DD}	N04		
V_{DD}	N11		
V_{DD}	N19		
V_{DD}	W10		
V_{DD}	W13		

In the following table, only the primary (default) signal name is shown for each ball. Multiplexed or multifunction signals are marked with an asterisk (*). To determine what signals or functions are multiplexed on those balls, look up the primary signal name in “Signals Listed Alphabetically” on page 17.The following table lists the signals by ball assignment.

Table 4. Signals Listed by Ball Assignment (Sheet 1 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	GND	B01	UART0_Rx	C01	$\overline{\text{CAN0\_TxE}}$	D01	$\overline{\text{UART0\_DSR}}$*
A02	GND	B02	GND	C02	CAN0_Rx	D02	$\overline{\text{UART0\_DCD}}$*
A03	$\overline{\text{CAN1\_TxE}}$	B03	CAN0_Tx	C03	GND	D03	UART0_Tx
A04	PWM_DivClk*	B04	CAN1_Tx	C04	CAN1_Rx	D04	GND
A05	GND	B05	PWM_14*	C05	PWM_16*	D05	$OV_{DD}1$
A06	DAC_IOutP	B06	DAC_VRef	C06	PWM_12*	D06	GND
A07	DAC_AGND	B07	DAC_GRef	C07	PWM_13*	D07	$OV_{DD}1$
A08	DAC_AV_{DD}	B08	DAC_CRef	C08	DAC_IPTrig*	D08	GND
A09	GND	B09	DAC_IRRef	C09	GND	D09	GND
A10	PWM_9*	B10	PWM_10*	C10	PWM_11*	D10	VDD
A11	PWM_6	B11	PWM_7	C11	PWM_8*	D11	$OV_{DD}1$
A12	PWM_5	B12	PWM_3	C12	PWM_2	D12	GND
A13	PWM_4	B13	PWM_1	C13	PWM_OE3*	D13	V_{DD}
A14	GND	B14	PWM_TBA	C14	GPIO121	D14	$\overline{\text{SPI\_SS1}}$*
A15	PWM_OE2*	B15	PWM_OE1*	C15	IIC0SData	D15	GND
A16	PWM_OE0	B16	IIC0SClk	C16	SPI_DO	D16	$OV_{DD}1$
A17	$\overline{\text{SPI\_SS0}}$	B17	SPI_ClkOut	C17	DebugEn	D17	SPI_DI
A18	GND	B18	$\overline{\text{SysReset}}$	C18	$\overline{\text{Halt}}$	D18	$OV_{DD}1$
A19	$\overline{\text{DMAAck}}$*	B19	Reserved	C19	$\overline{\text{DMAReq}}$*	D19	GND
A20	$\overline{\text{DMAEOT/TC}}$*	B20	SysErr	C20	GND	D20	BusReq*
A21	TestEn	B21	GND	C21	PerReady*	D21	$\overline{\text{HoldPri}}$*
A22	GND	B22	$\overline{\text{CRAM\_AdV}}$*	C22	HoldAck*	D22	$\overline{\text{HoldReq}}$*

Table 4. Signals Listed by Ball Assignment (Sheet 2 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	GND	F01	UART1_Tx	G01	$\overline{\text{TRST}}$	H01	TCK
E02	$\overline{\text{UART0\_RI}}$*	F02	UART1_Rx	G02	TMS	H02	$\overline{\text{USB1Host0}}$
E03	$\overline{\text{UART0\_CTS}}$*	F03	$\overline{\text{UART0\_RTS}}$*	G03	USB_FClk	H03	USB1Host0
E04	$OV_{DD}1$	F04	$\overline{\text{UART0\_DTR}}$*	G04	$OV_{DD}1$	H04	GND
E05	No ball	F05	No ball	G05	No ball	H05	No ball
E06	No ball	F06	No ball	G06	No ball	H06	No ball
E07	No ball	F07	No ball	G07	No ball	H07	No ball
E08	No ball	F08	No ball	G08	No ball	H08	No ball
E09	No ball	F09	No ball	G09	No ball	H09	No ball
E10	No ball	F10	No ball	G10	No ball	H10	No ball
E11	No ball	F11	No ball	G11	No ball	H11	No ball
E12	No ball	F12	No ball	G12	No ball	H12	No ball
E13	No ball	F13	No ball	G13	No ball	H13	No ball
E14	No ball	F14	No ball	G14	No ball	H14	No ball
E15	No ball	F15	No ball	G15	No ball	H15	No ball
E16	No ball	F16	No ball	G16	No ball	H16	No ball
E17	No ball	F17	No ball	G17	No ball	H17	No ball
E18	No ball	F18	No ball	G18	No ball	H18	No ball
E19	$OV_{DD}2$	F19	CRAM_Clk*	G19	$OV_{DD}2$	H19	GND
E20	$\overline{\text{PerOE}}$	F20	$\overline{\text{PerCS5}}$*	G20	$\overline{\text{PerCS4}}$*	H20	$\overline{\text{PerCS0}}$
E21	$\overline{\text{PerCS7}}$*	F21	$\overline{\text{PerCS6}}$*	G21	$\overline{\text{PerCS2}}$	H21	$\overline{\text{PerWBE3}}$
E22	GND	F22	$\overline{\text{PerCS3}}$	G22	$\overline{\text{PerCS1}}$	H22	$\overline{\text{PerWBE1}}$

Table 4. Signals Listed by Ball Assignment (Sheet 3 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	GND	K01	$\overline{\text{USB1Dev0}}$	L01	EMCRxD1	M01	EMCRxClk
J02	$\overline{\text{USB1Host1}}$	K02	USB1Dev0	L02	EMCRxD0	M02	EMCRxD2
J03	USB1Host1	K03	TDO	L03	TDI	M03	EMCRxEr
J04	EMCCRS	K04	V_{DD}	L04	GND	M04	$OV_{DD}1$
J05	No ball	K05	No ball	L05	No ball	M05	No ball
J06	No ball	K06	No ball	L06	No ball	M06	No ball
J07	No ball	K07	No ball	L07	No ball	M07	No ball
J08	No ball	K08	No ball	L08	No ball	M08	No ball
J09	GND	K09	$OV_{DD}1$	L09	GND	M09	GND
J10	$OV_{DD}1$	K10	GND	L10	V_{DD}	M10	GND
J11	GND	K11	GND	L11	GND	M11	GND
J12	GND	K12	V_{DD}	L12	GND	M12	GND
J13	$OV_{DD}1$	K13	GND	L13	GND	M13	V_{DD}
J14	GND	K14	$OV_{DD}2$	L14	GND	M14	GND
J15	No ball	K15	No ball	L15	No ball	M15	No ball
J16	No ball	K16	No ball	L16	No ball	M16	No ball
J17	No ball	K17	No ball	L17	No ball	M17	No ball
J18	No ball	K18	No ball	L18	No ball	M18	No ball
J19	$\overline{\text{PerWBE2}}$	K19	V_{DD}	L19	$OV_{DD}2$	M19	GND
J20	$\overline{\text{PerWBE0}}$	K20	PerClk	L20	PerAddr29	M20	PerAddr24
J21	Per$\overline{\text{RW}}$	K21	PerAddr31	L21	PerAddr28	M21	PerAddr25
J22	GND	K22	PerAddr30	L22	PerAddr27	M22	PerAddr26

Table 4. Signals Listed by Ball Assignment (Sheet 4 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	EMCRxD3	P01	GND	R01	EMCRxDv	T01	ADC_In0
N02	EMCTxD0	P02	EMCTxD1	R02	EMCTxClk	T02	EMCTxEr
N03	EMCMDIO	P03	EMCTxD2	R03	EMCMDC	T03	IRQ0*
N04	V_{DD}	P04	EMCTxD3	R04	GND	T04	$OV_{DD}1$
N05	No ball	P05	No ball	R05	No ball	T05	No ball
N06	No ball	P06	No ball	R06	No ball	T06	No ball
N07	No ball	P07	No ball	R07	No ball	T07	No ball
N08	No ball	P08	No ball	R08	No ball	T08	No ball
N09	$OV_{DD}1$	P09	GND	R09	No ball	T09	No ball
N10	GND	P10	$OV_{DD}1$	R10	No ball	T10	No ball
N11	V_{DD}	P11	GND	R11	No ball	T11	No ball
N12	GND	P12	GND	R12	No ball	T12	No ball
N13	GND	P13	$OV_{DD}2$	R13	No ball	T13	No ball
N14	$OV_{DD}2$	P14	GND	R14	No ball	T14	No ball
N15	No ball	P15	No ball	R15	No ball	T15	No ball
N16	No ball	P16	No ball	R16	No ball	T16	No ball
N17	No ball	P17	No ball	R17	No ball	T17	No ball
N18	No ball	P18	No ball	R18	No ball	T18	No ball
N19	V_{DD}	P19	PerAddr16	R19	GND	T19	$OV_{DD}2$
N20	PerAddr21	P20	PerAddr19	R20	PerAddr15	T20	PerAddr12
N21	PerAddr22	P21	PerAddr20	R21	PerAddr17	T21	PerAddr13
N22	PerAddr23	P22	GND	R22	PerAddr18	T22	PerAddr14

Table 4. Signals Listed by Ball Assignment (Sheet 5 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	ADC_In1	V01	GND	W01	ADC_In2	Y01	ADC_In3
U02	EMCCOL	V02	IRQ1*	W02	IRQ3*	Y02	NFData6*
U03	EMCTxEn	V03	IRQ2*	W03	NFCLE*	Y03	GND
U04	ADC_InTrig*	V04	$OV_{DD}1$	W04	GND	Y04	NFData5*
U05	No ball	V05	No ball	W05	$OV_{DD}1$	Y05	NFData4*
U06	No ball	V06	No ball	W06	GND	Y06	GND
U07	No ball	V07	No ball	W07	$OV_{DD}1$	Y07	NFData2*
U08	No ball	V08	No ball	W08	GND	Y08	NFData0*
U09	No ball	V09	No ball	W09	GND	Y09	$\overline{\text{NFCE0}}$*
U10	No ball	V10	No ball	W10	V_{DD}	Y10	$\overline{\text{NFWE}}$*
U11	No ball	V11	No ball	W11	GND	Y11	PerData00
U12	No ball	V12	No ball	W12	$OV_{DD}2$	Y12	PerData04
U13	No ball	V13	No ball	W13	V_{DD}	Y13	PerData07
U14	No ball	V14	No ball	W14	PerData12	Y14	PerData11
U15	No ball	V15	No ball	W15	GND	Y15	PerData14
U16	No ball	V16	No ball	W16	$OV_{DD}2$	Y16	PerData16
U17	No ball	V17	No ball	W17	PerData22	Y17	PerData19
U18	No ball	V18	No ball	W18	$OV_{DD}2$	Y18	PerData20
U19	PerAddr04	V19	$OV_{DD}2$	W19	GND	Y19	PerData25
U20	PerAddr08	V20	PerAddr05	W20	PerData31	Y20	GND
U21	PerAddr10	V21	PerAddr09	W21	PerAddr06	Y21	PerData30
U22	PerAddr11	V22	GND	W22	PerAddr07	Y22	PerData28

Table 4. Signals Listed by Ball Assignment (Sheet 6 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	ADC_In4	AB01	GND				
AA02	GND	AB02	ADC_In5				
AA03	NFData7*	AB03	ADC_In6				
AA04	GND	AB04	ADC_In7				
AA05	GND	AB05	GND				
AA06	NFData3*	AB06	ADC_VRef				
AA07	NFData1*	AB07	ADC_AGND				
AA08	NFALE*	AB08	ADC_AV_{DD}				
AA09	$\overline{NFRE}$*	AB09	GND				
AA10	NFRB*	AB10	SysClk				
AA11	PerData01	AB11	PLL_AGND				
AA12	PerData02	AB12	PLL_AV_{DD}				
AA13	PerData05	AB13	PerData03				
AA14	PerData08	AB14	GND				
AA15	PerData09	AB15	PerData06				
AA16	PerData15	AB16	PerData10				
AA17	PerData17	AB17	PerData13				
AA18	PerData18	AB18	GND				
AA19	PerData23	AB19	PerData21				
AA20	PerData26	AB20	PerData24				
AA21	GND	AB21	PerData27				
AA22	PerData29	AB22	GND				

Pin Group List

The following table provides a summary of the number of package pins (balls) associated with each functional interface group.

Table 5. Pin Groups

Group	No. of Pins
Total Signal Pins	**200**
V_{DD}	12
$OV_{DD}1$	17
$OV_{DD}2$	11
GND	77
ADC_AV_{DD}	1
ADC_GND	1
DAC_AV_{DD}	1
DAC_GND	1
PLL_AV_{DD}	1
PLL_GND	1
Reserved	1
Total Pins	**324**

In the table “Signal Functional Description” on page 35, each external signal is listed along with a short description of the signal function. Active-low signals (for example, $\overline{\text{Halt}}$) are marked with an overline. See the preceding table, “Signals Listed Alphabetically” on page 17, for the pin (ball) number to which each signal is assigned.

Multiplexed Pins

Some signals are multiplexed on the same package pin so that the pin can be used for different functions. In most cases, the signal names shown in this table are not accompanied by signal names that may be multiplexed on the same pin. If you need to know what, if any, signals are multiplexed with a particular signal, look up the name in “Signals Listed Alphabetically” on page 17. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

Initialization Strapping

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Initialization” on page 51). Note that the use of these pins for strapping is not considered multiplexing since the strapping function is not programmable.

Pull-Up and Pull-Down Resistors

Pull-up and pull-down resistors are used for strapping during reset and to retain unused or undriven inputs in an appropriate state. The recommended pull-up value of 3kΩ to +3.3V and pull-down value of 1kΩ to GND, applies only to individually terminated signals. To prevent possible damage to the device, I/Os capable of becoming outputs *must never* be tied together and terminated through a common resistor.

If your system-level test methodology permits, input-only signals can be connected together and terminated through either a common resistor or directly to +3.3V or GND. When a resistor is used, its value must ensure that the grouped I/Os reach a valid logic zero or logic one state when accounting for the total input current into the PPC405EZ.

Signal Functional Descriptions

The following table provides a description of the I/O signals on the PPC405EZ.

Table 6. Signal Functional Description (Sheet 1 of 6)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
Ethernet Interface				
EMCCOL	Collision signal from the PHY.	I	3.3V LVTTL	5
EMCCRS	Carrier sense signal from the PHY.	I	3.3V LVTTL	5
EMCMDC	Management data clock to the PHY.	O	3.3V LVTTL	
EMCMDIO	Management data I/O between the Ethernet controller and the PHY.	I/O	3.3V LVTTL	
EMCRxClk	Input receive clock from the PHY.	I	3.3V LVTTL Rcvr	
EMCRxDV	Receive data valid.	I	3.3V LVTTL	5
EMCRxEr	Receive error from the PHY.	I	3.3V LVTTL Rcvr	
EMCRxD0:3	Receive data from the PHY. EMCRxD3 is the msb.	I	3.3V LVTTL	5
EMCTxClk	Input transmit clock from the PHY.	I	3.3V LVTTL	
EMCTxD0:3	Transmit data to the PHY. EMCTxD3 is the msb.	O	3.3V LVTTL	
EMCTxEn	Transmit enable.	O	3.3V LVTTL	
EMCTxEr	Transmit error to the PHY.	O	3.3V LVTTL	
IEEE 1588 Network Synchronization Interface				
IEEE_1588TS	Test signal.	O	3.3V LVTTL	
IIC Peripheral Interface				
IIC0SClk	IIC Serial Clock.	I/O	3.3V IIC	1, 5
IIC0SData	IIC Serial Data.	I/O	3.3V IIC	1, 5
Interrupts Interface				
IRQ0:4	Interrupt requests.	I	3.3V LVTTL	1, 5
JTAG Interface				
TCK	Test clock.	I	3.3V LVTTL Rcvr w/pull-up	5
TDI	Test data in.	I	3.3V LVTTL	5
TDO	Test data out.	O	3.3V LVTTL	
TMS	Test mode select.	I	3.3V LVTTL	5
$\overline{\text{TRST}}$	Test reset. Must be low at power-on to initialize the JTAG controller and for normal operation of the PPC405EZ.	I	3.3V LVTTL Rcvr w/pull-up	5

Table 6. Signal Functional Description (Sheet 2 of 6)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	System input clock.	I	3.3V LVTTL	
SysErr	Machine check exception has occurred.	O	3.3V LVTTL	
$\overline{\text{SysReset}}$	Main system reset. This signal may be driven by the PPC405EZ to cause a board level reset to occur.	I	3.3V LVTTL	
TestEn	Test enable. Reserved for manufacturing LSSD test.	I	3.3V LVTTL	5
DebugEn	Debug enable.	I	3.3V LVTTL	5
$\overline{\text{Halt}}$	External request to stop the processor.	I	3.3V LVTTL	4
TmrClk	Processor timer external input.	I	3.3V LVTTL	
GPIO000:03	General purpose I/O. All of the GPIO signals are multiplexed with other signals. Which signal a pin is connected to depends on the setting of bits in the GPIO registers.	I/O	3.3V LVTTL	
GPIO004:05		I/O	3.3V LVTTL	5
GPIO006:08		I/O	3.3V LVTTL	
GPIO009		I/O	3.3V LVTTL	4
GPIO010:11		I/O	3.3V LVTTL	
GPIO012:19		I/O	3.3V LVTTL	5
GPIO019:27		I/O	3.3V LVTTL	
GPIO028:31 GPIO100:12		I/O	3.3V LVTTL	5
GPIO113:14		I/O	3.3V LVTTL	
GPIO115:21		I/O	3.3V LVTTL	5
Trace Interface				
TrcClk	Trace interface clock. Operates at half the CPU core frequency.	I	3.3V LVTTL	
TS1E TS2E	Even trace execution status.	I	3.3V LVTTL	
TS1O TS2O	Odd trace execution status.	I	3.3V LVTTL	
TS3:6	Trace status.	I	3.3V LVTTL	
Chameleon Timer Interface				
PWM_DivClk	Divided-down clock.	O	3.3V LVTTL	
PWM_OE0	PWM 0 Output enable input.	I	3.3V LVTTL	4
PWM_OE1:3	PWM 1:3 Output enable input.	I	3.3V LVTTL	
PWM_TBA	Time Base A.	I/O	3.3V LVTTL	
PWM_1:15	PWM Interface bus.	I/O	3.3V LVTTL	5

Table 6. Signal Functional Description (Sheet 3 of 6)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
Analog to Digital (ADC) Interface				
ADC_In0:7	Analog inputs. Analog inputs to the ADC should be referenced to ADC_AGND and should not exceed the value of VRef.	I	Analog Wide-Wire receiver	
ADC_InTrig	Input trigger.	I	3.3V LVTTL	
ADC_VRef	Analog input reference voltage. Allowable voltage range is 2V–ADC_AV_{DD}.	I	Analog Wide-Wire receiver	
Digital to Analog (DAC) Interface				
DAC_CRef	Reference voltage for the gate of the DAC current sources. This voltage should be connected to the DAC_AV_{DD} voltage with a 1nF filter capacitor at the signal pin.	I	Analog Wide-Wire driver	
DAC_IOutP	Analog positive output current.	O	Analog Wide-Wire driver	
DAC_IPTrig	Input trigger.	I	3.3V LVTTL	
DAC_IRRef	Analog input reference current.	I	Analog Wide-Wire driver	
DAC_VRef	Analog band gap voltage reference input. Allowable voltage range is 1.15V–1.26V, with a typical value of 1.174V.	I	Analog Wide-Wire driver	
DAC_GRef	Reference voltage for the gate of the cascode device in the DAC current sources. This voltage should be connected to the DAC_AV_{DD} voltage with a 1nF filter capacitor at the signal pin.	I	Analog Wide-Wire driver	
Controller Area Network Interface				
CAN0_Rx	Receive input.	I	3.3V LVTTL Rcvr w/pull-up	5
CAN0_Tx	Transmit output.	O	3.3V LVTTL	
$\overline{\text{CAN0\_TxE}}$	Transmit enable.	O	3.3V LVTTL	
CAN1_Rx	Receive input.	I	3.3V LVTTL	5
CAN1_Tx	Transmit output.	O	3.3V LVTTL	
$\overline{\text{CAN1\_TxE}}$	Transmit enable.	O	3.3V LVTTL	

Table 6. Signal Functional Description (Sheet 4 of 6)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
External Peripheral Interface				
$\overline{\text{CRAM\_AdV}}$	Address valid signal for PSRAM/CRAM support.	O	3.3V LVTTL	
CRAM_Clk	PerClk gated for PSRAM/CRAM support.	O	3.3V LVTTL	
PerAddr04:31	Memory address bus 4:31.	O	3.3V LVTTL	
BusReq	External PLB bus request.	O	3.3V LVTTL	
PerClk	Clock output.	O	3.3V LVTTL	
$\overline{\text{PerCS0:7}}$	Chip selects 0:7.	O	3.3V LVTTL	
PerData00:31	Memory data bus 0:31.	I/O	3.3V LVTTL	5
$\overline{\text{PerOE}}$	Output enable.	O	3.3V LVTTL	
PerReady	Wait for PSRAM/CRAM support.	I	3.3V LVTTL	
PerR$\overline{\text{W}}$	Read/Write.	O	3.3V LVTTL	
$\overline{\text{PerWBE0:3}}$	Write bus enable 0:3.	O	3.3V LVTTL	
$\overline{\text{DMAAck}}$	External DMA peripheral acknowledge.	O	3.3V LVTTL	
$\overline{\text{DMAEOT/TC}}$	External DMA peripheral end-of-transmission/terminal count.	I/O	3.3V LVTTL	5
$\overline{\text{DMAReq}}$	External peripheral DMA request.	I	3.3V LVTTL	5
HoldReq	External request for bus access.	I	3.3V LVTTL	
HoldAck	External request acknowledge.	O	3.3V LVTTL	
HoldPri	External bus request priority.	I	3.3V LVTTL	
NAND Flash Interface				
NFALE	Address latch enable.	O	3.3V LVTTL	
$\overline{\text{NFCE0:3}}$	Cchip selects 0:3.	O	3.3V LVTTL	
NFCLE	Command latch enable.	O	3.3V LVTTL	
NFData0:7	Data bits 0:7	I/O	3.3V LVTTL	
NFRB	Read/Busy. If low, indicates that Read/Erase command is in process. If high, indicates that the command is complete.	I	3.3V LVTTL	
$\overline{\text{NFRE}}$	Read enable.	O	3.3V LVTTL	
$\overline{\text{NFWE}}$	Write enable.	O	3.3V LVTTL	
Serial Peripheral Interface				
SPI_ClkOut	Serial peripheral interface clock.	O	3.3V LVTTL	
SPI_DI	Master and slave input.	I	3.3V LVTTL	5
SPI_DO	Master and slave output.	O	3.3V LVTTL	
$\overline{\text{SPI\_SS0:3}}$	Slave Select 0:3.	O	3.3V LVTTL	
$\overline{\text{SPI\_SS\_In}}$	Slave Select Input for multi-master collision detection.	I	3.3V LVTTL	

Table 6. Signal Functional Description (Sheet 5 of 6)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
UART Peripheral Interface				
$\overline{\text{UART0\_CTS}}$	Clear to send.	I	3.3V LVTTL	
$\overline{\text{UART0\_DCD}}$	Data carrier detect.	I	3.3V LVTTL	
$\overline{\text{UART0\_DSR}}$	Data set ready.	I	3.3V LVTTL	
$\overline{\text{UART0\_DTR}}$	Data terminal ready.	O	3.3V LVTTL	
$\overline{\text{UART0\_RI}}$	Ring indicator.	I	3.3V LVTTL	
$\overline{\text{UART0\_RTS}}$	Request to send.	O	3.3V LVTTL	
UART0_Rx	Receive data.	I	3.3V LVTTL	5
UART0_Tx	Transmit data.	O	3.3V LVTTL	
UART1_Rx	Receive data	I	3.3V LVTTL	5
UART1_Tx	Transmit data	O	3.3V LVTTL	
USB Interface				
USB1FClk	48 MHz clock for USB	I	3.3V LVTTL	
USB1DEV0	Device differential + data signal	I/O	5V tolerant USB Diff	
$\overline{\text{USB1DEV0}}$	Device differential – data signal	I/O	5V tolerant USB Diff	
USB1HOST0	Host 0 differential + data signal	I/O	5V tolerant USB Diff	
$\overline{\text{USB1HOST0}}$	Host 0 differential – data signal	I/O	5V tolerant USB Diff	
USB1HOST1	Host 1 differential + data signal	I/O	5V tolerant USB Diff	
$\overline{\text{USB1HOST1}}$	Host 1 differential – data signal	I/O	5V tolerant USB Diff	

Table 6. Signal Functional Description (Sheet 6 of 6)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 34 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
Power				
V_{DD}	Logic V_{DD} supply.	na	na	na
$OV_{DD}1$	Non-EBC I/O V_{DD} supply.	na	na	na
$OV_{DD}2$	EBC I/O V_{DD} supply.	na	na	na
GND	System ground.	na	na	na
ADC_AV_{DD}	ADC analog V_{DD} supply.	na	Analog Wide-Wire receiver	na
ADC_AGND	ADC analog ground.	na	Analog Wide-Wire receiver	na
DAC_AV_{DD}	DAC analog V_{DD} supply. It is recommended that this voltage be provided by means of a voltage supply and voltage plane separate from the logic voltage.	na	Analog Wide-Wire receiver	na
DAC_AGND	DAC analog ground.	na	Analog Wide-Wire receiver	na
PLL_AV_{DD}	PLL analog V_{DD} supply. See “Absolute Maximum Ratings” on page 41 for filter recommendations.	na	na	na
PLL_AGND	PLL analog ground.	na	na	na
Other Pins				
Reserved	Reserved pins. Do not make voltage, ground, or signal connections to these pins.	na	na	na

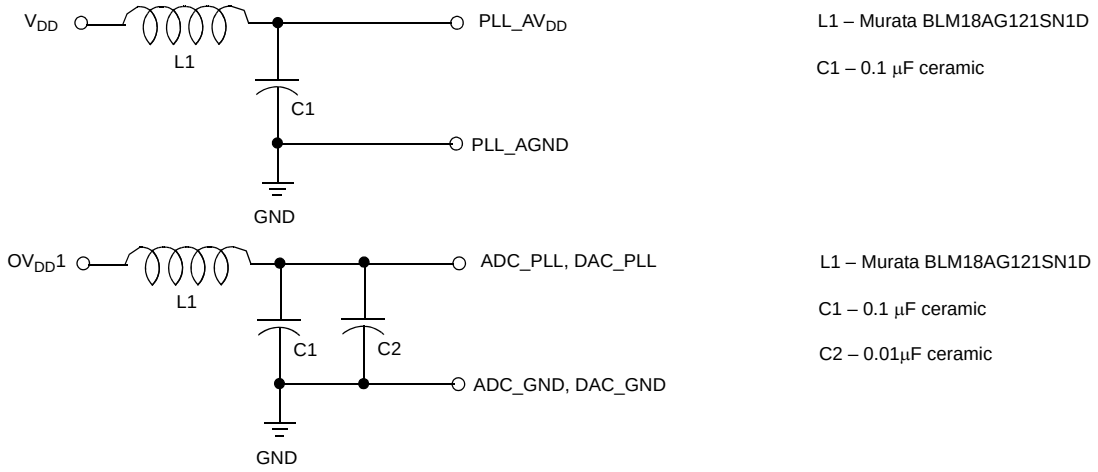
Ratings and Specifications

Table 7. Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specification contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit	Notes
Supply Voltage (Internal Logic)	V_{DD}	0 to +1.6	V	
Non-EBC I/O Supply Voltage	$OV_{DD}1$	0 to +3.6	V	
EBC I/O Supply Voltage	$OV_{DD}2$	0 to +3.6	V	3
PLL Analog Supply Voltage	PLL_AV_{DD}	0 to +1.6	V	
ADC Analog Supply Voltage	ADC_AV_{DD}	0 to +3.465	V	
DAC Analog Supply Voltage	DAC_AV_{DD}	0 to +3.465	V	
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to +3.6	V	
Input Voltage (5.0V LVTTL receivers)	V_{IN}	0 to +5.5	V	
Storage Temperature Range	T_{STG}	-55 to +150	°C	
Case temperature under bias	T_C	-40 to +120	°C	
Junction temperature	T_{JMax}	+125	°C	

1. All voltages are specified with respect to GND.
2. The analog voltages use for the system PLL, the ADC, and the DAC can be derived from V_{DD} and $OV_{DD}1$, but must be filtered as shown below before entering the PPC405EZ. Use a separate filter for each voltage. The maximum value for ADC_PLL and DAC_PLL must be limited to the values shown in this table.
3. $OV_{DD}2$ must be limited to a maximum value of +3.3V if CRAM/PSRAM devices are attached to the EBC interface. This is a limitation imposed by the CRAM/PSRAM devices, not the PPC405EZ.



L1 – Murata BLM18AG121SN1D

C1 – 0.1 μF ceramic

L1 – Murata BLM18AG121SN1D

C1 – 0.1 μF ceramic

C2 – 0.01μF ceramic

Table 8. Package Thermal Specifications

The PPC405EZ is designed to operate within a case temperature range of -40°C to +105°C. Thermal resistance values for the EPBGA packages in a convection environment are as follows:

Parameter	Symbol	Airflow ft/min (m/sec)						Unit
		0 (0)	100 (0.51)	200 (1.02)	300 (1.52)	400 (2.02)	600 (3.03)	
Junction-to-ambient thermal resistance *without* heat sink	θ_{JA}	29.3	24.1	22.9	22.4	22.0	21.6	°C/W
Junction-to-ambient thermal resistance *with* heat sink	θ_{JA}	22.7	14.3	12.3	11.5	11.1	10.7	°C/W
		Resistance Value						
Junction-to-case thermal resistance	θ_{JC}	11.9						°C/W
Junction-to-board thermal resistance	θ_{JB}	16.4						°C/W

Notes:

1. Values in the table are achieved with the following JEDEC standard board: 114.5mm x 101.6mm x 1.6mm, 4 layers.
2. For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
   a. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
   b. $T_A = T_C - P x \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
   c. $T_{CMax} = T_{JMax} - P x \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.
3. Values with a heat sink were achieved with a 38.1mm x 38.1mm x 16.5mm unit, attached to the chip using a 0.1mm thickness of adhesive having a thermal conductivity of 1.3W/mK.

Thermal Management

The following heat sink was used in the above thermal analysis:

Aavid Thermalloy, PN 79985

The heat sink is manufactured by:

Aavid Thermalloy
70 Commercial St.
Concord, NH 03301
USA
Tel: (603)224-9988
URL: **www.aavidthermalloy.com**

Table 9. Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	+1.425	+1.5	+1.575	V	
I/O Supply Voltage (for non-EBC I/O)	$OV_{DD}1$	+3.0	+3.3	+3.6	V	
I/O Supply Voltage (for EBC I/O)	$OV_{DD}2$	+3.0	+3.3	+3.6 (see Note 1)	V	1
PLL Analog Supply Voltage	PLL_AV_{DD}	+1.4	+1.5	+1.6	V	
ADC Analog Supply Voltage	ADC_AV_{DD}	+3.135	+3.3	+3.465	V	
DAC Analog Supply Voltage	DAC_AV_{DD}	+3.135	+3.3	+3.465	V	
I/O Input Low (3.3V LVTTL)	V_{IL}	0		+0.8	V	
I/O Input High (3.3V LVTTL)	V_{IH}	+2.0		+3.6	V	
I/O Output Low (3.3V LVTTL)	V_{OL}	0		+0.4	V	
I/O Output High (3.3V LVTTL)	V_{OH}	+2.4		+3.6	V	
I/O High (USB, 5V tolerant)	V_{OH}	+2.8			V	
I/O Low (USB, 5V tolerant)	V_{OL}			+0.3	V	
I/O Input High (IIC)	V_{IH}	$0.7OV_{DD}$		OV_{DD} + 0.3	V	
I/O Input Low (IIC)	V_{IL}	–0.3		$+0.3OV_{DD}$	V	
I/O Output High (IIC)	V_{IH}				V	
I/O Output Low (IIC)	V_{OL}	0		+0.4	V	
Input Leakage Current (no pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current (with internal pull-down)	I_{IL2}	0		200	µA	
I/O Maximum Allowable Overshoot (3.3V LVTTL)	V_{MAO}			+3.9	V	
I/O Maximum Allowable Undershoot (3.3V LVTTL)	V_{MAU}	–0.6			V	
Case Temperature	T_C	–40		+105	°C	

Notes:
1. When using CRAM or PSRAM memory on the EBC interface, this voltage must be limited to a maximum of +3.3V. This is a limitation imposed by the CRAM/PSRAM devices, not the PPC405EZ.

Table 10. Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
3.3V LVTTL I/O	C_{IN1}	1.9	pF	
USB 5V Tolerant I/O	C_{IN2}	3.2	pF	
IIC I/O	C_{IN3}	5.8	pF	

Table 11. Typical DC Power Supply Requirements

Frequency (MHz)	+1.5V Supply	+3.3V Supply	Total	Unit	Notes
166	0.81	0.24	1.05	W	1
266	0.97	0.25	1.22	W	1
333	1.13	0.29	1.42	W	2
416	1.2	0.28	1.48	W	3

Table 12. DC Power Supply Loads

Parameter	Symbol	Typical	Maximum	Unit	Notes
V_{DD} (+1.5V) active operating current	I_{DD}	425	815	mA	1
OV_{DD} (+3.3V) active operating current	I_{ODD}	60	95	mA	1
AV_{DD} (+1.5V) active operating current	I_{ADD}	20	35	mA	1
ADC_AVDD (3.3V) ADC input current	I_{ADCDD}	7	8	mA	1
DAC_AVDD (3.3V) DAC input current	I_{DACDD}	7	8	mA	1

Notes:

1. Typical and Maximum values are estimates and subject to change.

Test Conditions

Clock timing and switching characteristics are specified in accordance with *minimum* operating conditions shown in the table “Recommended DC Operating Conditions” on page 43. For all signals, AC specifications are characterized at T_C = 85°C with the 50pF test load shown in the figure to the right.

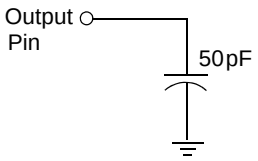
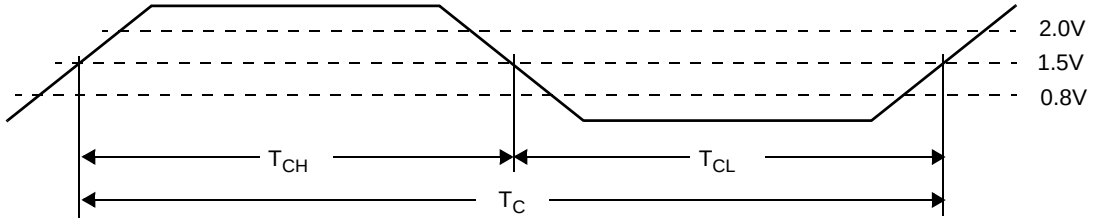


Table 13. System Clocking Specifications

Symbol	Parameter	Min	Max	Units
CPU				
PF_C	Processor clock frequency (must be ≥ SCF_C)	133.33	416	MHz
SysClk Input				
SCF_C	Frequency	33.33	100	MHz
SCT_{CS}	Edge stability (phase jitter, cycle to cycle)	na	± 0.1	ns
SCT_{CH}	Input high time	0.6	na	ns
SCT_{CL}	Input low time	0.6	na	ns
SC_{RT}	Rise time	na	0.4	ns
Note: Input slew rate = 1V/ns				
TrcClk Output				
TCF_C	Clock output frequency		$PF_C/2$	MHz
TCT_{CS}	Clock edge stability (phase jitter, cycle to cycle)		± 0.2	ns
Other Clocks				
$VCOF_C$	VCO frequency	600	1333.33	MHz
$PLBF_C$	PLB frequency	33	166	MHz
$OPBF_C$	OPB frequency	33	83	MHz

Figure 3. Clocking Waveform



Spread Spectrum Clocking

Care must be taken if using a spread spectrum clock generator (SSCG) with the PPC405EZ. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is called tracking skew. The PLL bandwidth and phase angle determine how much tracking skew exists between the SSCG and the PLL for a given frequency deviation and modulation frequency. If using an SSCG with the PPC405EZ the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC405EZ with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation must not exceed –3%, and the modulation frequency must not exceed 40kHz. In some cases, on-board PPC405EZ peripherals impose more stringent requirements (see Note 1).
- Use the peripheral bus clock for logic that is synchronous to the peripheral bus because this clock tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur, assuming that the connected device is running at precise baud rates. If an external serial clock is used, baud rate is unaffected by the modulation.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Caution: The system designer must ensure that any SSCG used with the PPC405EZ meets these requirements and does not adversely affect other aspects of the system.

Table 14. Peripheral Interface I/O Clock Timings

Clock	Min	Max	Units
EMCTxClk frequency	2.5	25	MHz
EMCTxClk high time	35% of nominal	–	ns
EMCTxClk low time	35% of nominal	–	ns
EMCRxClk frequency	2.5	25	MHz
EMCRxClk high time	35% of nominal	–	ns
EMCRxClk low time	35% of nominal	–	ns
TmrClk	na	100	MHz
PerClk	33	83	MHz
TCK	na	20	MHz
USB1FClk (48MHz ± 0.05%)	47.976	48.024	MHz
PWM_TBA	na	83	MHz

Figure 4. Input Setup and Hold Timing Waveform

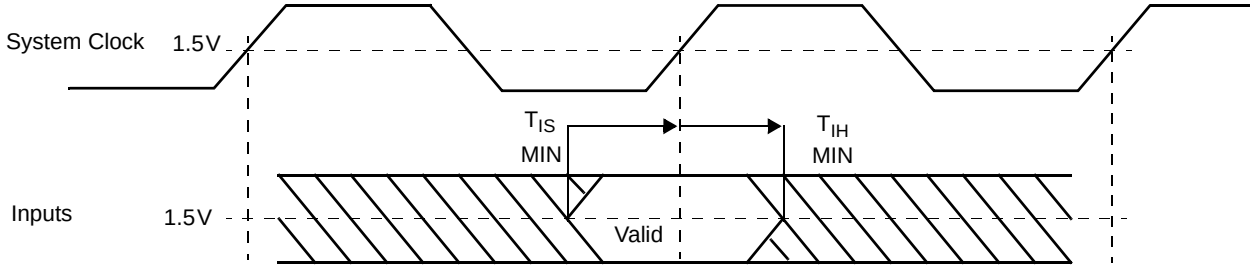


Figure 5. Output Delay and Float Timing Waveform

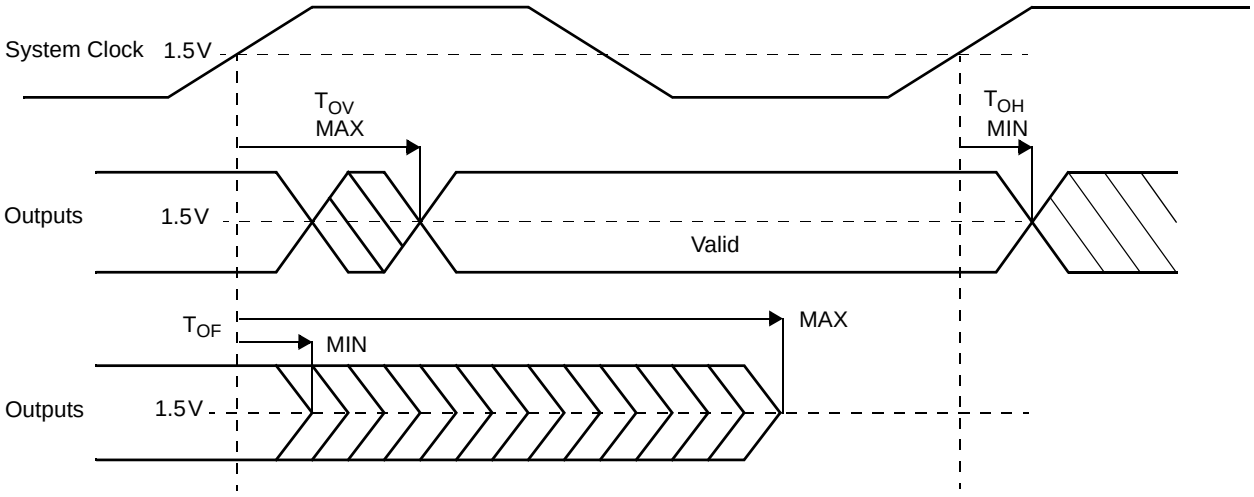


Table 15. I/O Specifications—All CPU Speeds (Sheet 1 of 2)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard. Timing shown is with EMAC noise filter selected.
2. For all interfaces, I/O H is specified at 2.4 V and I/O L is specified at 0.4 V.
3. Maximum skew between IIC output signals is 6ns.
4. Maximum skew between all SPI output signals is 3ns. All SPI inputs signals are latched with less than 4ns of skew between channels.
5. Maximum skew between all PWM output signals is 3.75ns. All PWM input signals are latched with less than 2.5ns of skew between channels.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (min)	I/O L (min)		
Ethernet Interface								
EMCRxD[0:3]	2.5	4			19.1	8.7	EMCRxClk	
EMCTxD[0:3]			20	2	19.1	8.7	EMCTxClk	
EMCRxEr	2.5	4	na	na	na	na	EMCRxClk	
EMCMDIO	na	na	na	na	19.1	8.7		async
EMCRxDv	2.5	4	na	na	na	na	EMCRxClk	
EMCCRS	na	na			19.1	8.7		async
EMCTxEr			20	2	19.1	8.7	EMCTxClk	
EMCTxEn			20	2	19.1	8.7	EMCTxClk	
EMCMDC	na	na	na	na	19.1	8.7		async
EMCCOL	na	na			19.1	8.7		async
Internal Peripheral Interface								
IIC0SClk	na	na	na	na	IIC 2.1	IIC 2.1	na	3
IIC0SData	na	na	na	na	IIC 2.1	IIC 2.1	na	3
$\overline{\text{UART0\_CTS}}$	na	na	na	na	na	na	na	
$\overline{\text{UART0\_RTS}}$	na	na	na	na	19.1	8.7	na	
UART0_Rx	na	na	na	na	na	na	na	
UART0_Tx	na	na	na	na	19.1	8.7	na	
UART1_Rx	na	na	na	na	na	na	na	
UART1_Tx	na	na	na	na	19.1	8.7	na	
USB_FClk					USB 2.1	USB 2.1		
USB1DEV0					USB 2.1	USB 2.1		
$\overline{\text{USB1DEV0}}$					USB 2.1	USB 2.1		
USB1HOST0					USB 2.1	USB 2.1		
$\overline{\text{USB1HOST0}}$					USB 2.1	USB 2.1		
USB1HOST1					USB 2.1	USB 2.1		
$\overline{\text{USB1HOST1}}$					USB 2.1	USB 2.1		
SPI_ClkOut					19.1	8.7		4
SPI_DI			na	na	19.1	8.7		4
SPI_DO	na	na			19.1	8.7		4
$\overline{\text{SPI\_SS0:3}}$					19.1	8.7		
$\overline{\text{SPI\_SS\_In}}$					19.1	8.7		
CAN0_Rx			na	na	na	na		
CAN0_Tx					19.1	8.7		
$\overline{\text{CAN0\_TxE}}$					19.1	8.7		
CAN1_Rx			na	na	na	na		
CAN1_Tx	na	na			19.1	8.7		
$\overline{\text{CAN1\_TxE}}$					19.1	8.7		
ADC_In0:7			na	na	na	na		

Table 15. I/O Specifications—All CPU Speeds (Sheet 2 of 2)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard. Timing shown is with EMAC noise filter selected.
2. For all interfaces, I/O H is specified at 2.4 V and I/O L is specified at 0.4 V.
3. Maximum skew between IIC output signals is 6ns.
4. Maximum skew between all SPI output signals is 3ns. All SPI inputs signals are latched with less than 4ns of skew between channels.
5. Maximum skew between all PWM output signals is 3.75ns. All PWM input signals are latched with less than 2.5ns of skew between channels.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (min)	I/O L (min)		
ADC_InTrig			na	na	na	na		
ADC_VRef			na	na	na	na		
DAC_CRef			na	na	na	na		
DAC_IOutP			na	na	na	na		
DAC_IPTrig					19.1	8.7		
DAC_IRRef			na	na	na	na		
DAC_VRef			na	na	na	na		
DAC_GRef			na	na	na	na		
PWM_DivClk					19.1	8.7		5
PWM_OE[0]					19.1	8.7		5
PWM_OE[1:3]					19.1	8.7		5
PWM_TBA					19.1	8.7		5
PWM_1:15					19.1	8.7		5
IEEE_1588TS					19.1	8.7		
Interrupts Interface								
[IRQ0:4]					19.1	8.7		
JTAG Interface								
TCK	na	na	na	na	na	na		
TDI	22.5	0	na	na	na	na	TCK	
TDO	na	na	25	0	19.1	8.7	TCK	
TMS	22.5	0	na	na	na	na	TCK	
$\overline{\text{TRST}}$	na	na	na	na	na	na	TCK	
System Interface								
GPIO000:31	na	na	na	na	19.1	8.7		
GPIO100:20	na	na	na	na	19.1	8.7		
$\overline{\text{Halt}}$	22.5	0	na	na	na	na	TCK	
SysErr	na	na	15	25.5	19.1	8.7	TCK	
$\overline{\text{SysReset}}$	na	na	na	na	19.1	8.7	async	
$\overline{\text{TestEn}}$	na	na	na	na	na	na	async	
DebugEn	na	na	na	na	na	na		
SysClk	na	na	na	na	na	na		

Table 16. I/O Specifications—416 MHz CPU

Notes:
1. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
2. I/O H is specified at 2.4 V and I/O L is specified at 0.4 V.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
External Peripheral Interface								
PerClk	na	na			19.1	8.7	na	
CRAM_Clk	na	na			19.1	8.7	na	
$\overline{\text{CRAM\_AdV}}$	na	na	7.2	2	19.1	8.7	PerClk/ CRAM_Clk	
PerAddr04:31	na	na	7.35	2.16	19.1	8.7	PerClk/ CRAM_Clk	
BusReq	na	na	7.3	2.1	19.1	8.7	PerClk/ CRAM_Clk	
$\overline{\text{PerCS0:7}}$	na	na	7.3	2.1	19.1	8.7	PerClk/ CRAM_Clk	
PerData00:31	1.6	2.1	7.5	2.1	19.1	8.7	PerClk/ CRAM_Clk	
HoldReq	1.6	2.1	na	na	na	na	PerClk/ CRAM_Clk	
HoldAck	na	na	7.3	2.1	19.1	8.7	PerClk/ CRAM_Clk	
HoldPri	1.6	2.1	na	na	na	na	PerClk/ CRAM_Clk	
$\overline{\text{PerOE}}$	na	na	7.35	2.15	19.1	8.7	PerClk/ CRAM_Clk	
PerReady	1.6	2.1	na	na	na	na	PerClk/ CRAM_Clk	
PerR$\overline{\text{W}}$	na	na	7.35	2.15	19.1	8.7	PerClk/ CRAM_Clk	
$\overline{\text{PerWBE0:3}}$	na	na	7.3	2.15	19.1	8.7	PerClk/ CRAM_Clk	
NFALE			7.1	0.9	19.1	8.7	PerClk/ CRAM_Clk	
$\overline{\text{NFCE0}}$			7.1	0.9	19.1	8.7	PerClk/ CRAM_Clk	
NFCLE			7.1	0.9	19.1	8.7	PerClk/ CRAM_Clk	
NFData0:7	9.2	-0.7	7.1	0.9	19.1	8.7	PerClk/ CRAM_Clk	
NFRB	10	0			19.1	8.7	PerClk/ CRAM_Clk	
$\overline{\text{NFRE}}$			7.1	0.9	19.1	8.7	PerClk/ CRAM_Clk	
$\overline{\text{NFWE}}$			7.1	0.9	19.1	8.7	PerClk/ CRAM_Clk	
$\overline{\text{DMAAck}}$	na	na	7.3	2.1	19.1	8.7		
$\overline{\text{DMAEOT/TC}}$					19.1	8.7		
$\overline{\text{DMAReq}}$	5	0.9	na	na	19.1	8.7		

Initialization

The following describes the method by which initial chip settings are established when a system reset occurs.

Strapping

When the SysReset input is driven low (system reset), the state of certain I/O pins is read in order to enable default initial conditions before PPC405EZ start-up. The actual instant of capture is the nearest system clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. The recommended pull-up is 3kΩ to +3.3V, or 10kΩ to +5V. The recommended pull-down is 1KΩ to GND. These pins are only used for strap functions during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options. The signal names assigned to the pins for normal operation appear below the pin number.

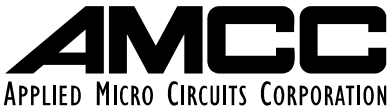
Table 17. Strapping Pin Assignments

		Pin Strapping			
Function	**Option**	**F03** (GPIO114)	**E03** (GPIO112)	**D01** (GPIO111)	**D02** (GPIO110)
Initialize from EBC	8 bits wide	0	0	0	0
	16 bits wide	0	0	0	1
	32 bits wide	0	0	1	0
Initialize from NAND Flash	512 page, 3 addr cycle	0	0	1	1
	512 page, 4 addr cycle	0	1	0	0
	2K page, 4 addr cycle	0	1	0	1
	2K page, 5 addr cycle	0	1	1	0
Initialize from SPI	Slow	0	1	1	1
	Fast	1	0	0	0
Reserved	na	1	0	0	1
Initialize from IIC **Note:** If reading of initialization data from the IIC interface fails, the PPC405EZ defaults to strapping option 0010.	na	1	0	1	0
		1	0	1	1
		1	1	0	0
		1	1	0	1
		1	1	1	0
		1	1	1	1

Revision Log

Date	Version	Contents of Modification
01/13/2006	1.08	Initial distribution for review.
03/09/2006	1.09	Misc. corrections. Correct AMCC address. Add revision log. Change three EBC signals to match previous chips (HoldAck, HoldPri, and HoldReq).
04/10/2006	1.10	Misc. corrections. Add pull-up/pull-down notes. Update clock timings. Correct Bootstrap pin numbers. Correct pin number swaps. Add circuit types to signal descriptions.
04/21/2006	1.11	Reduce recommended logic voltage range by 0.025V. Add 266MHz and 333MHz CPU speeds. Allow 3.3V power supply for ADC and DAC. Add output currents to I/O tables. Correct Recommended Operating Conditions. Remove 5V Tolerant input current curve. Add output current values (based on I/O circuit type) to I/O tables Correct filter circuit component units-of-measure from m to µ.
05/12/2006	1.12	Correct ADC_In6 and ADC_In7 pins assignment. Correct EBC_Dbus24 and EBC_Dbus25 pins assignment. Change signal name NI_DivClk to PWM_DivClk. Add typical DC power requirements.
06/13/2006	1.13	Split OV_{DD} voltage pins into two sets so EBC voltage can be different from other I/O if necessary. Update from engineering review.
07/18/2006	1.14	Timing updates.
08/8/2006	1.15	Chameleon Timer and IEEE 1588 PTP updates. Add package thermal data.
08/30/2006	1.16	Analog voltage filter updates. Part number updates.
09/05/2006	1.17	Remove TE package and references to “industrial” from thermal package data. Remove watermark and change status to Preliminary. Add heat sink data and increase case temperature range to +105°C.
09/18/2006	1.18	Change minimum CPU frequency to 133.33MHz. Add DC power supply current load values.
10/18/2006	1.19	Change pin assignments for the Ethernet Tx and Rx data signals. Alter prefixes and remove extraneous characters from some signal names to make them consistent with the UM and previous chips. There are no functional or pin (ball) number changes. Correct JTAG ID. Remove CAN disable option. Reduce maximum SPI speed. Change power specifications in Description. Add link to AMCC partners supplying probes. Deleted internal clock signal timing table. Added PerClk signal to external peripheral timing table. Restrict ADC and DAC analog voltage filters to $OV_{DD}1$.
02/07/2007	1.20	Typographical Updates

Date	Version	Contents of Modification
02/20/2007	1.21	The $VCOF_c$ minimal value in the System Clock Specification in Table 13: Changed to 600 MHz instead of 66
02/21/2007	1.22	Changes to the UART section and the Ethernet section
02/27/2007	1.23	Added a sentence to the NAND Flash Controller section
03/05/2007	1.24	Change picture on page 16.
04/02/2007	1.25	Added a overline on the signal CRAM_AdV.
04/23/2007	1.26	Changed the PVR value on page 4
08/22/2007	1.27	Added missing information to table 14.



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