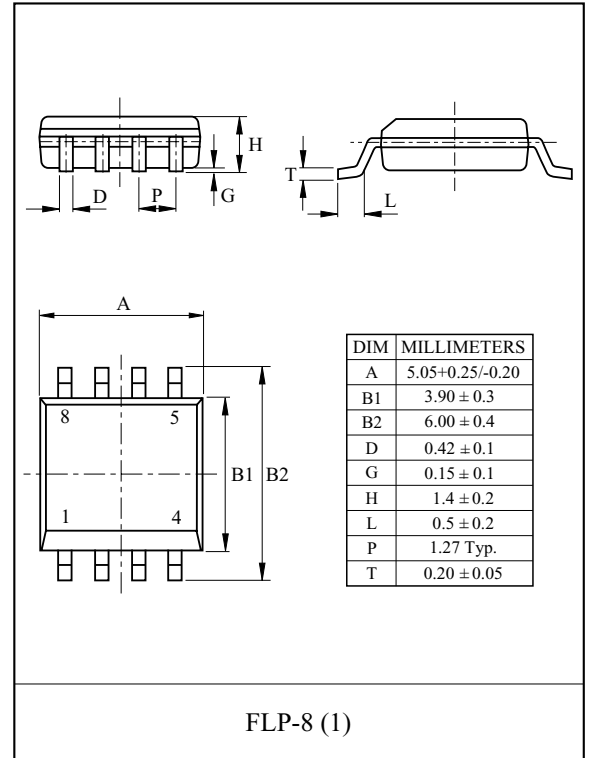


General Description

Switching regulator and DC-DC Converter applications.
It is mainly suitable for power management in PC, portable equipment and battery powered systems.

FEATURES

- N-Channel
 - : $V_{DSS}=30V$, $I_D=7.6A$.
 - : $R_{DS(ON)}=20m\ \Omega$ (Max.) @ $V_{GS}=10V$
 - : $R_{DS(ON)}=40m\ \Omega$ (Max.) @ $V_{GS}=4.5V$
- P-Channel
 - : $V_{DSS}=-30V$, $I_D=-5.3A$.
 - : $R_{DS(ON)}=45m\ \Omega$ (Max.) @ $V_{GS}=-10V$
 - : $R_{DS(ON)}=60m\ \Omega$ (Max.) @ $V_{GS}=-4.5V$
- Super High Dense Cell Design.
- Reliable and rugged.

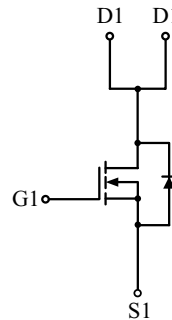
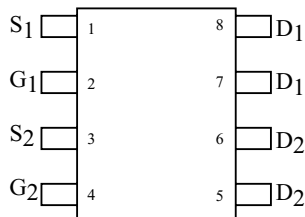


MAXIMUM RATING (Ta=25 °C)

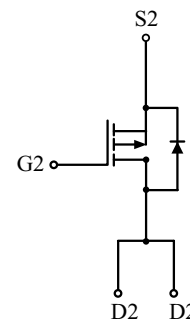
CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		V_{DSS}	30	-30	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Drain Current	DC	I_D^*	7.6	-5.3	A
	Pulsed (note1)	I_{DP}	30	-20	
Source-Drain Diode Current		I_S	1.7	-1.7	A
Drain Power Dissipation		P_D^*	2		W
Maximum Junction Temperature		T_j	150		°C
Storage Temperature Range		T_{stg}	-55 ~ 150		°C
Thermal Resistance, Junction to Ambient		R_{thJA}	62.5		°C/W

* : Surface Mounted on FR4 Board, $t \leq 10$ sec.

PIN CONNECTION (TOP VIEW)



N-Channel MOSFET



P-Channel MOSFET

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ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V,	N-Ch	30	-	-	V
		I _D =-250μA, V _{GS} =0V,	P-Ch	-30	-	-	
Drain Cut-off Current	I _{DSS}	V _{GS} =0V, V _{DS} =24V	N-Ch	-	-	1	μA
		V _{GS} =0V, V _{DS} =-24V	P-Ch	-	-	-1	
Gate Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	N-Ch	-	-	±100	nA
			P-Ch	-	-	±100	
Gate Threshold Voltage	V _{th}	V _{DS} =V _{GS} , I _D =250μA	N-Ch	1.0	1.7	3	V
		V _{DS} =V _{GS} , I _D =-250μA	P-Ch	-1.0	-1.6	-3	
Drain-Source ON Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =7A (Note 1)	N-Ch	-	14	20	m Ω
		V _{GS} =-10V, I _D =-5A (Note 1)	P-Ch	-	35	45	
		V _{GS} =4.5V, I _D =6A (Note 1)	N-Ch	-	24	40	
		V _{GS} =-4.5V, I _D =-4A (Note 1)	P-Ch	-	50	60	
ON State Drain Current	I _{D(ON)}	V _{GS} =10V, V _{DS} =10V (Note 1)	N-Ch	20	-	-	A
		V _{GS} =-10V, V _{DS} =-5V (Note 1)	P-Ch	-20	-	-	
Forward Transconductance	g _{fs}	V _{DS} =10V, I _D =7A (Note 1)	N-Ch	-	10	-	S
		V _{DS} =-5V, I _D =-5A (Note 1)	P-Ch	-	9	-	
Source-Drain Diode Forward Voltage	V _{SD}	I _S =1.7A, V _{GS} =0V (Note 1)	N-Ch	-	0.76	1.2	V
		I _S =-1.7A, V _{GS} =0V (Note 1)	P-Ch	-	-0.74	-1.2	

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CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Dynamic (Note 2)								
Total Gate Charge	Q_g	N-Ch : $V_{DS}=15V, I_D=7A,$ $V_{GS}=10V$ (Fig.1)	N-Ch	-	20.1	-	nC	
			P-Ch	-	13.8	-		
		N-Ch : $V_{DS}=15V, I_D=7A,$ $V_{GS}=4.5V$ (Fig.1)	N-Ch	-	10.5	-		
			P-Ch : $V_{DS}=-15V, I_D=-5A,$ $V_{GS}=-4.5V$ (Fig.3)	P-Ch	-	6.85		-
Gate-Source Charge	Q_{gs}	N-Ch : $V_{DS}=15V, I_D=7A,$ $V_{GS}=10V$ (Fig.1)	N-Ch	-	2.64	-	ns	
Gate-Drain Charge	Q_{gd}	P-Ch : $V_{DS}=-15V, I_D=-5A,$ $V_{GS}=-10V$ (Fig.3)	P-Ch	-	1.52	-		
			N-Ch	-	6.08	-		
P-Ch	-	3.65	-					
Turn-on Delay time	$t_{d(on)}$	N-Ch : $V_{DD}=15V, I_D=1A,$ $V_{GS}=10V, R_G=6\ \Omega$ (Fig.2)	N-Ch	-	8.3	-	ns	
Turn-on Rise time	t_r		P-Ch	-	5.6	-		
			N-Ch	-	27.5	-		
Turn-off Delay time	$t_{d(off)}$		P-Ch : $V_{DD}=-15V, V_{GS}=-10V,$ $R_L=2.7\ \Omega, R_G=3\ \Omega$ (Fig.4)	P-Ch	-	20.5		-
				N-Ch	-	20.8		-
Turn-off Fall time	t_f		N-Ch	-	13.6	-		
			P-Ch	-	8.3	-		
P-Ch	-		7.8	-				
Input Capacitance	C_{iss}	N-Ch : $V_{DS}=15V, V_{GS}=0V, f=1.0MHz$ P-Ch : $V_{DS}=-15V, V_{GS}=0V, f=1.0MHz$	N-Ch	-	1014	-	pF	
Output Capacitance	C_{oss}		P-Ch	-	714	-		
			N-Ch	-	213	-		
			P-Ch	-	161	-		
			N-Ch	-	151	-		
Reverse transfer Capacitance	C_{rss}		P-Ch	-	102	-		

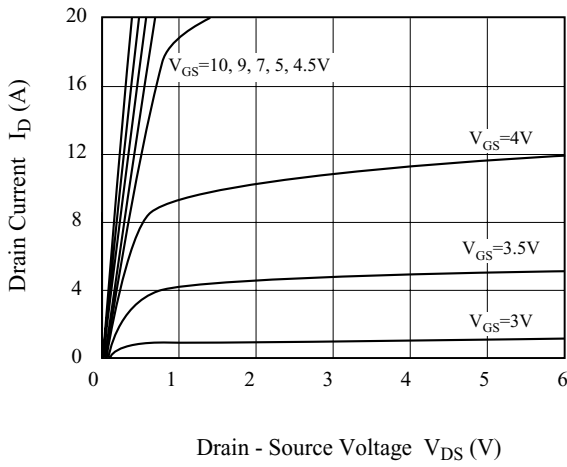
Note 1) Pulse test : Pulse width $\leq 300\ \mu s$, Duty Cycle $\leq 2\%$.

Note 2) Guaranteed by design. Not subject to production testing.

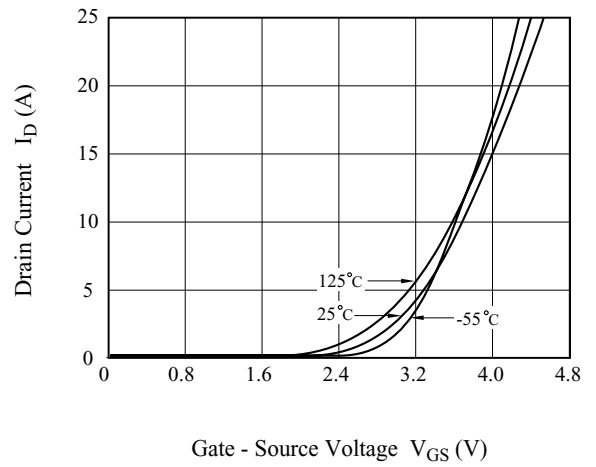
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N-Channel

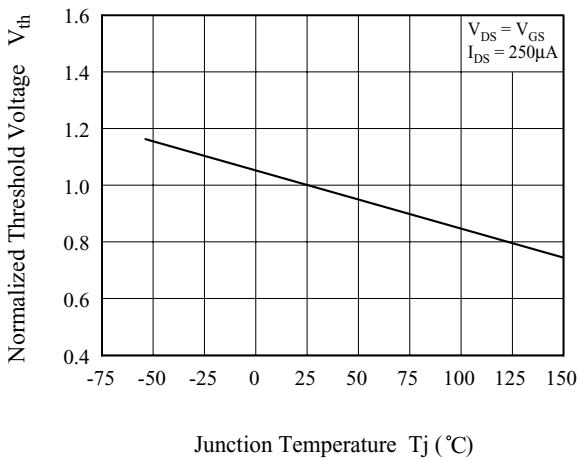
$I_D - V_{DS}$



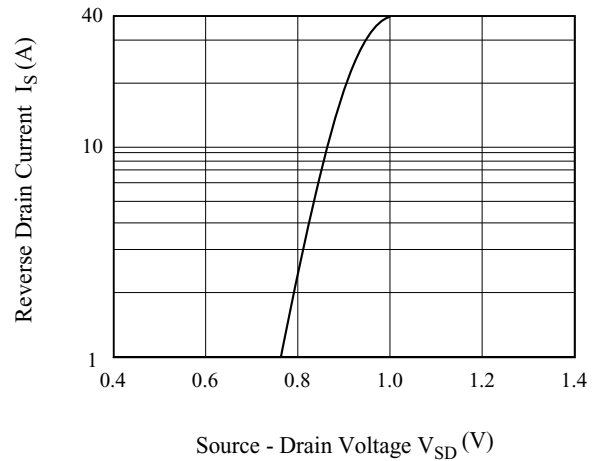
$I_D - V_{GS}$



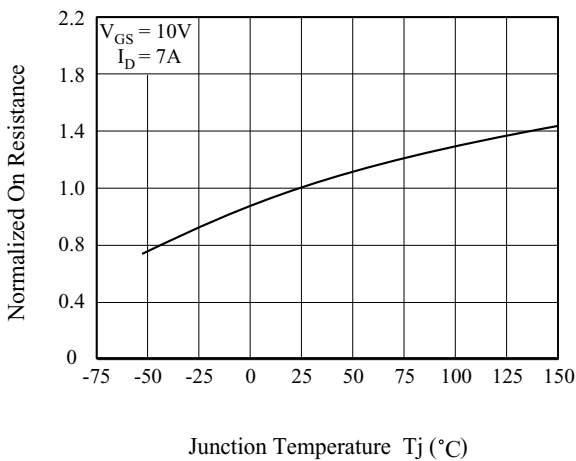
$V_{th} - T_j$



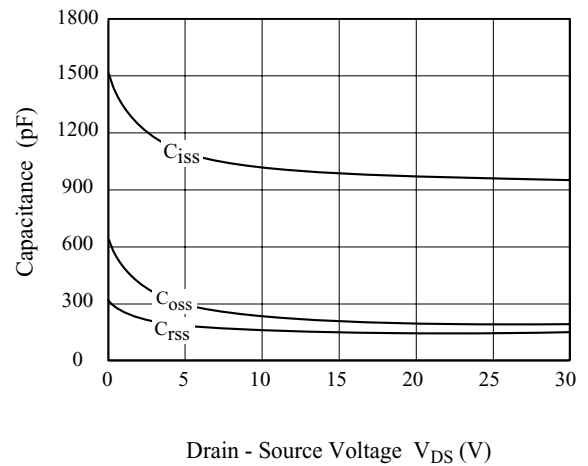
$I_S - V_{SD}$



$R_{DS(ON)} - T_j$

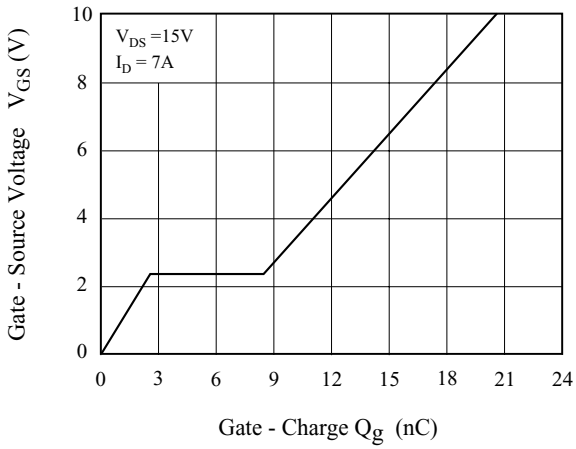


$C - V_{DS}$

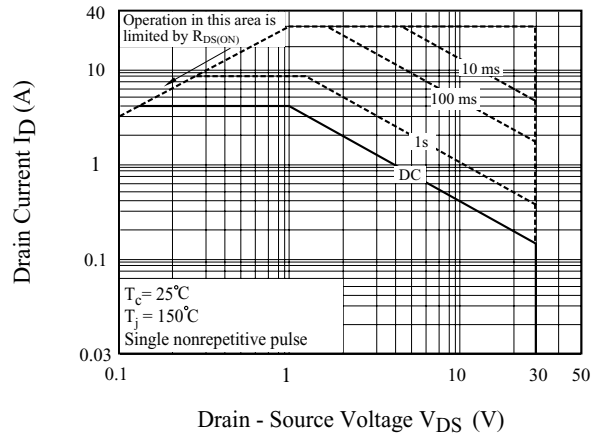


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$Q_g - V_{GS}$

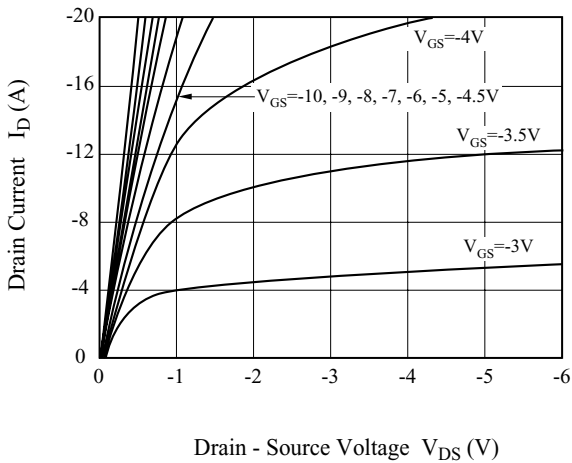


Safe Operation Area

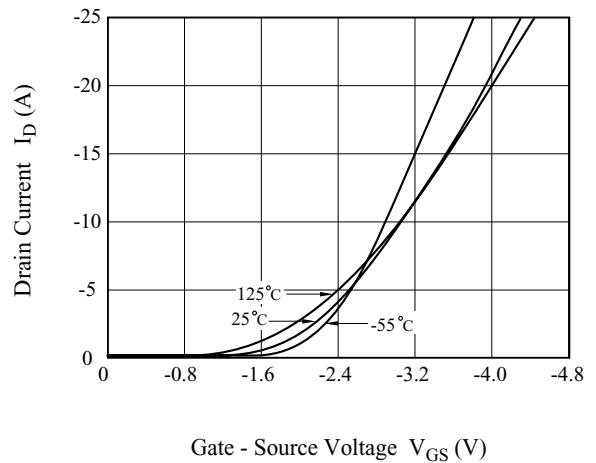


P-Channel

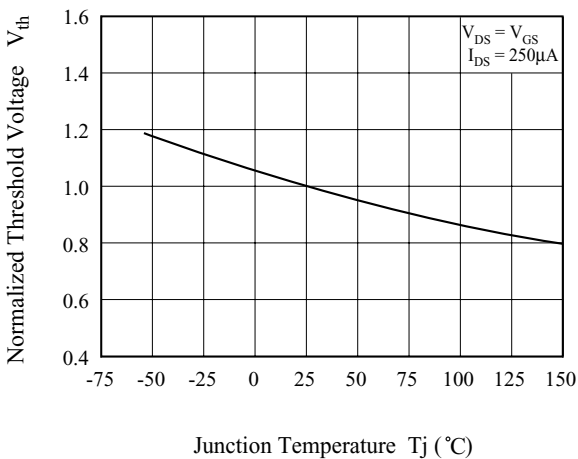
$I_D - V_{DS}$



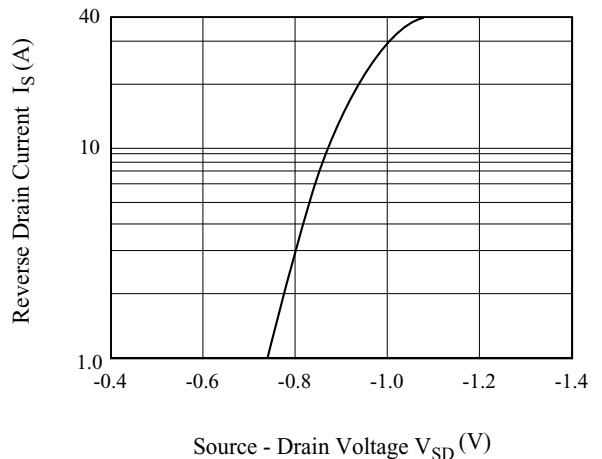
$I_D - V_{GS}$



$V_{th} - T_j$

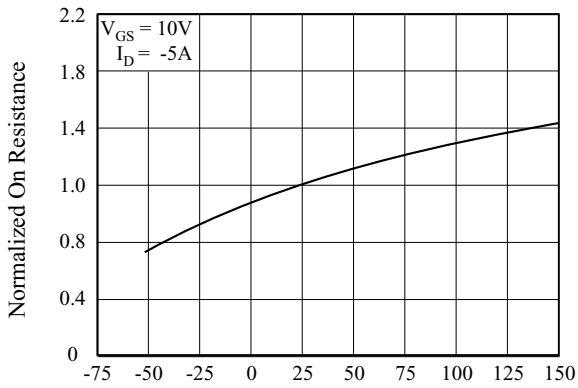


$I_S - V_{SD}$



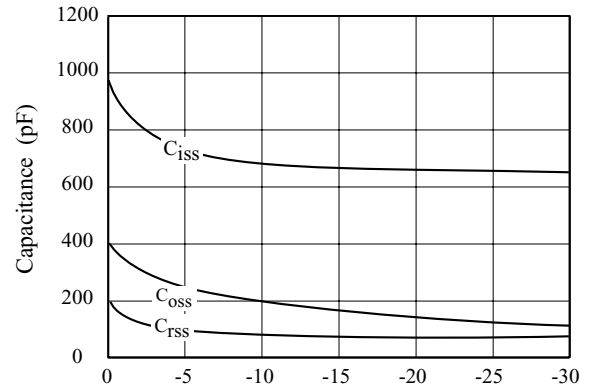
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$R_{DS(ON)} - T_j$



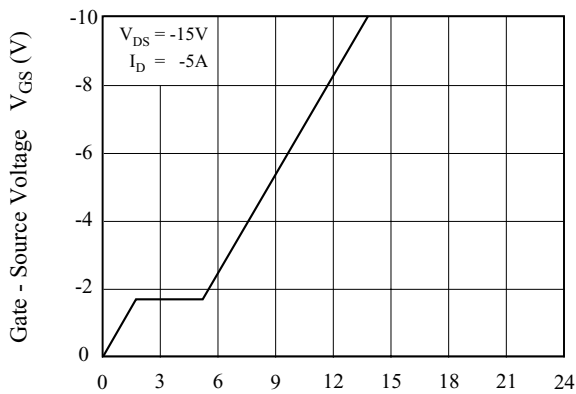
Junction Temperature T_j (°C)

$C - V_{DS}$



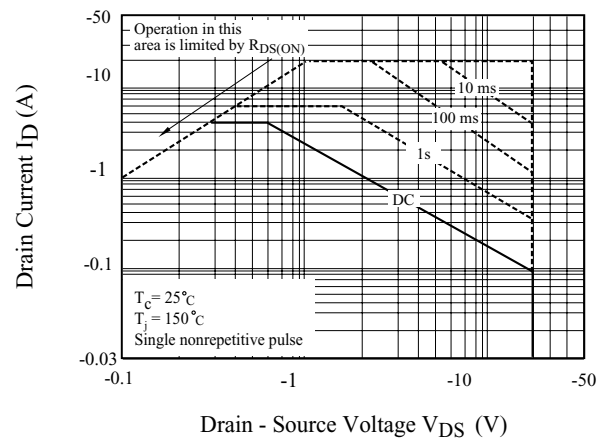
Drain - Source Voltage V_{DS} (V)

$Q_g - V_{GS}$



Gate - Charge Q_g (nC)

Safe Operation Area



Drain - Source Voltage V_{DS} (V)

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N - Channel

Fig.1 Gate Charge

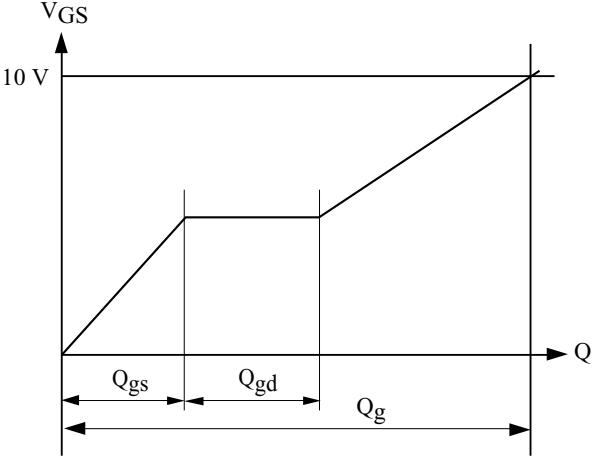
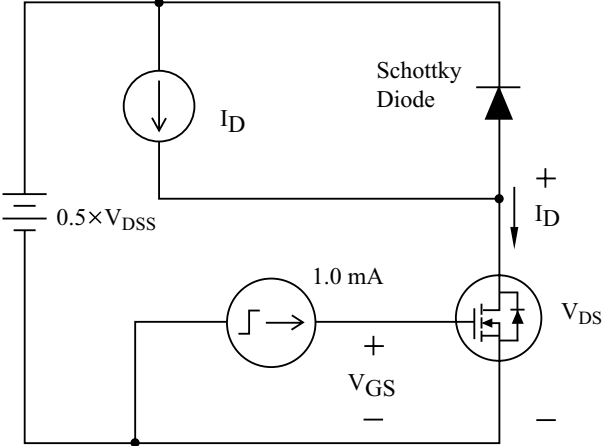
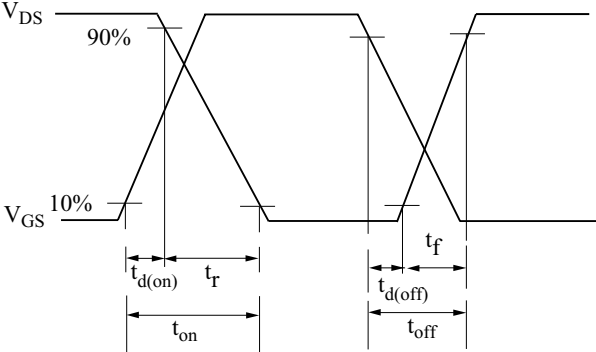
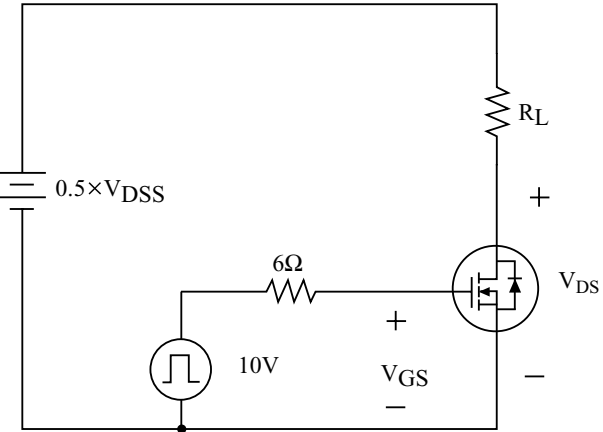


Fig.2 Resistive Load Switching



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P - Channel

Fig.3 Gate Charge

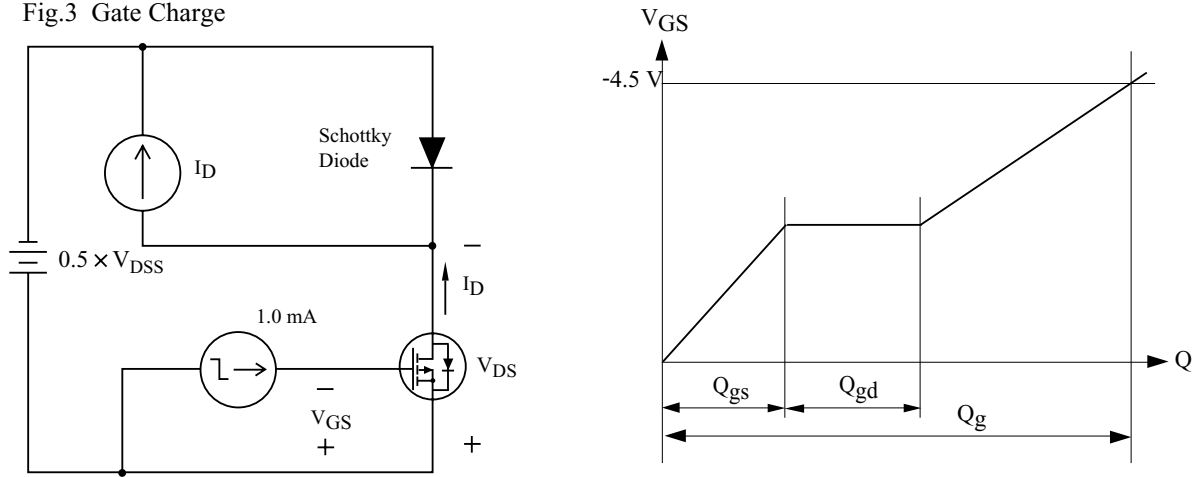


Fig.4 Resistive Load Switching

