M36W0Rx0x0UL4

32- or 64-Mbit (mux I/O, multiple bank, multilevel, burst) flash memory, 16- or 32-Mbit PSRAM, 1.8 V supply MCP

Features

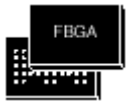
- Multichip package
  - 1 die of 32 Mbit (2 Mbit x 16) or 64 Mbit (4 Mbit x 16) mux I/O multiple bank, multilevel, burst) flash memory
  - 1 die of 16/32 Mbit mux I/O, burst PSRAM
- Supply voltage
  - $V_{DD} = V_{DDQ} = 1.7$ to 1.95 V
  - $V_{PPF} = 9$ V for fast programming
- Electronic signature
  - Manufacturer code: 20h
  - 32 Mbit flash device codes:
    Top - M36W0R5040U4: 8828h
    Bottom - M36W0R5040L4: 8829h
  - 64 Mbit flash device codes:
    Top - M36W0R6040U4 and M36W0R6050U4: 88C0h
    Bottom - M36W0R6040L4 and M36W0R6050L4: 88C1h

Flash memory

- Synchronous/asynchronous read
  - Synchronous burst read mode: 66 MHz
  - Random access: 70 ns
- Synchronous burst read suspend
- Programming time
  - 10 µs by word typical for factory program
  - Double/quadruple word program option
- Memory blocks
  - Multiple bank memory array: 4 Mbit banks
  - Parameter blocks (top or bottom location)
- Dual operations
  - Program erase in 1 bank, read in others
  - No delay between read and write
- Common flash interface (CFI)
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked
  - $\overline{WP}$ for block lock-down
- Security
  - 128 bit user programmable OTP cells
  - 64 bit unique device number
- 100 000 program/erase cycles per block

PSRAM

- Asynchronous modes
  - Random read 70 ns access time
  - Asynchronous write
- Synchronous mode:
  - NOR flash
  - Full synchronous (burst read and write)
- Burst read/write operations
  - 4-, 8- and 16-word
  - Clock frequency: 83 MHz
- Low power consumption
  - Active current: < 20 mA
  - Standby current: 70 µA
- Low power features
  - Partial array self-refresh (PASR)
  - Deep power-down (DPD) mode
  - Automatic temperature-compensated self-Refresh (ATSR)



TFBGA56 (ZS)
8 x 6 mm

TFBGA88 (ZAM)
8 x 10 mm

Table 1. Device summary

M36W0Rx0x0UL4	
M36W0R5040U4	M36W0R5040L4
M36W0R6040U4	M36W0R6040L4
M36W0R6050U4	M36W0R6050L4

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1 Description

The M36W0R5040U4, M36W0R5040L4, M36W0R6040U4, M36W0R6040L4, M36W0R6050U4, and M36W0R6050L4 each combine two memory devices in a multichip package:

- a 32-Mbit or 64-Mbit, multiple bank flash memory, the M58WR0xxKUL
- either:
  - a 16-Mbit pseudo SRAM, the M69KM024A
  - a 32-Mbit pseudo SRAM, the M69KM048A.

Collectively, these four devices are referred to in this document as the M36W0Rx0x0UL4.

The purpose of this document is to describe how the two memory components operate with respect to each other. It must be read in conjunction with the M58WR0xxKUL, and M69KM024A or M69KM048A datasheets, which detail all the specifications required to operate the flash memory and PSRAM components. These datasheets are available from your local Numonyx distributor.

The memory is offered in two stacked packages:

- TFBGA56 (8 x 6 mm, 10 x 6 ball array, 0.5 mm pitch) package
- TFBGA88 (8 x 10 mm, 8 x 10 ball array, 0.8 mm pitch) package

Recommended operating conditions do not allow more than one memory to be active at the same time.

Figure 1. Logic diagram - TFBGA56 package

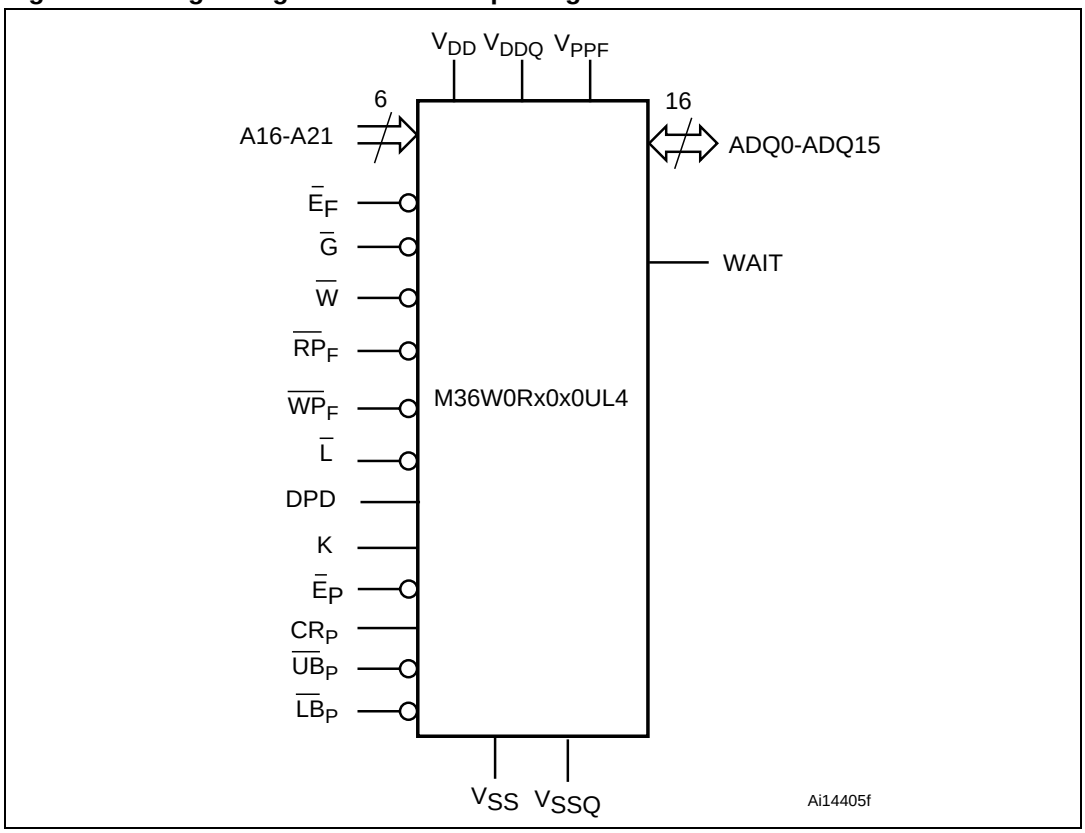


Figure 2. Logic diagram - TFBGA88 package

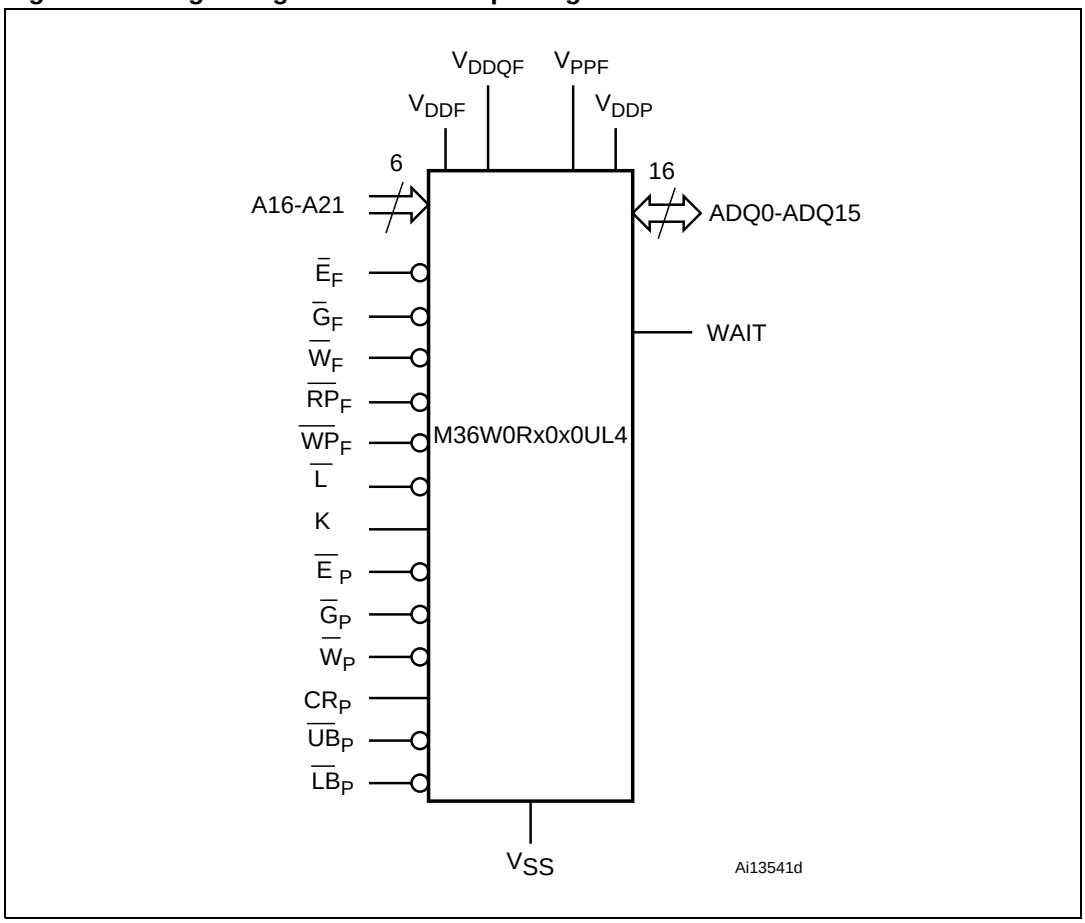


Table 2. Signal names

Name	Function	Direction
Common to both packages		
A16-A21(1)	Address inputs	Inputs
ADQ0-ADQ15	Flash memory and PSRAM common data input/outputs, address inputs or command inputs	Inputs/outputs
$\overline{L}$	Flash memory and PSRAM Latch Enable input	Input
K	Flash memory and PSRAM Burst Clock	Input
WAIT	Flash memory and PSRAM Wait Data in burst mode	Output
$\overline{E}_F$	Flash memory Chip Enable input	Input
$\overline{WP}_F$	Flash memory Write Protect input	Input
$\overline{RP}_F$	Flash memory Reset input	Input
$\overline{E}_P$	PSRAM Chip Enable input	Input
$\overline{UB}_P$	PSRAM Upper Byte Enable input	Input
$\overline{LB}_P$	PSRAM Lower Byte Enable input	Input
CR_P	PSRAM Configuration Register Enable input	Input
V_{PPF}	Flash memory optional supply voltage for fast program and erase	Power supply
V_{SS}	Flash memory and PSRAM shared ground	Ground
V_{SSQ}	Flash memory and PSRAM shared ground.	Ground
NC	Not connected internally	
Only in TFBGA56 package		
DPD	Deep power-down	Input
$\overline{G}$	Flash memory and PSRAM Output Enable input	Input
$\overline{W}$	Flash memory and PSRAM Write Enable input	Input
V_{DD}	Flash memory and PSRAM shared power supply	Power supply
V_{DDQ}	Flash memory and PSRAM shared power supply for I/O buffers	Power supply
Only in TFBGA88 package		
$\overline{G}_F$	Flash memory Output Enable input	Input
$\overline{W}_F$	Flash memory Write Enable input	Input
$\overline{G}_P$	PSRAM Output Enable input	Input
$\overline{W}_P$	PSRAM Write Enable input	Input
V_{DDF}	Flash memory power supply	Power supply
V_{CCP}	PSRAM supply voltage is the core supply voltage.	Power supply

1. In the TFBGA56 package, address inputs A16-A18 in the PSRAM are used in conjunction with ADQ0 to ADQ15 to select the cells in the memory array that are accessed during read and write operations. However, in the TFBGA88 package, it is is address inputs A16-A19.

Figure 3. TFBGA56 package connections (top view through package)

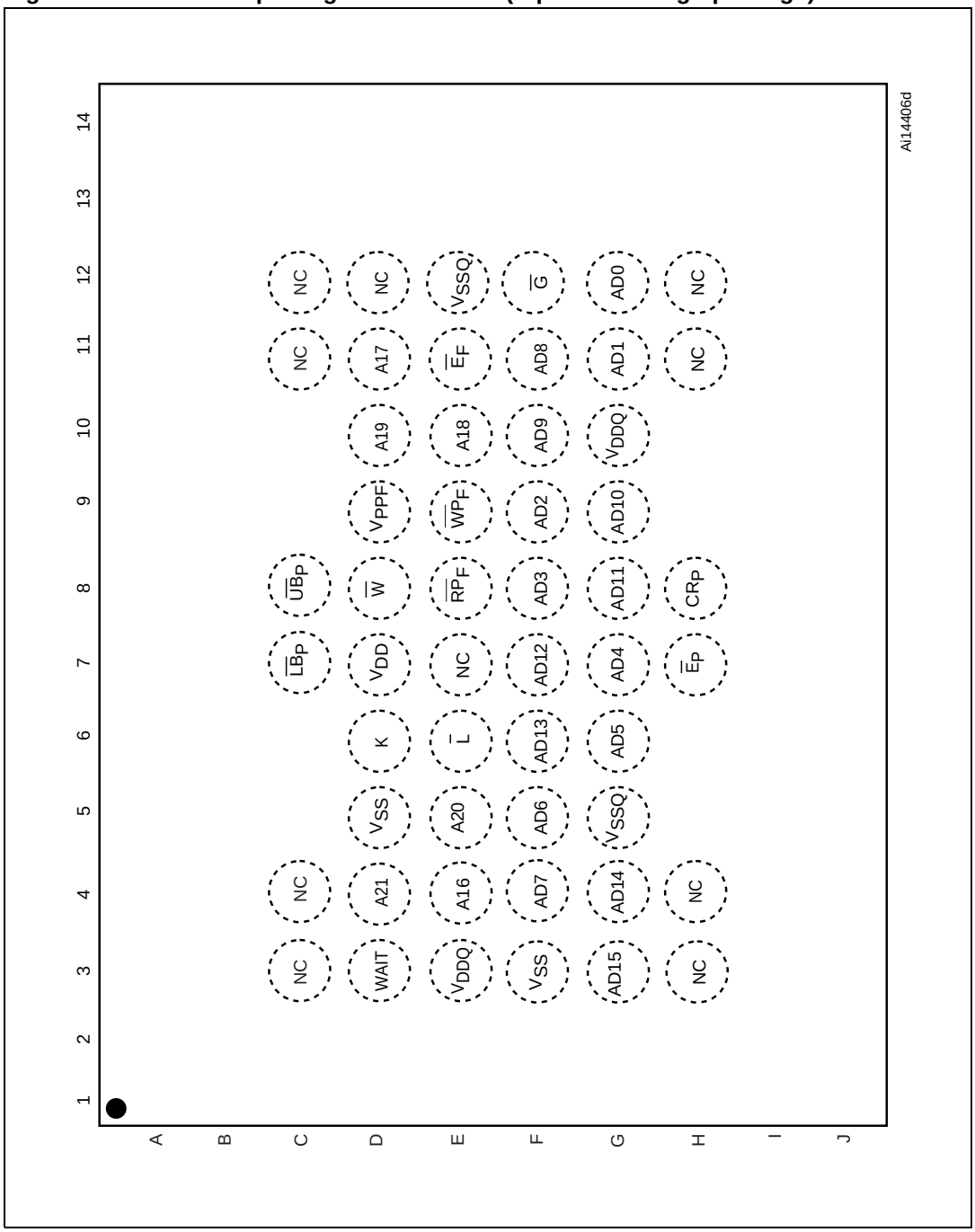
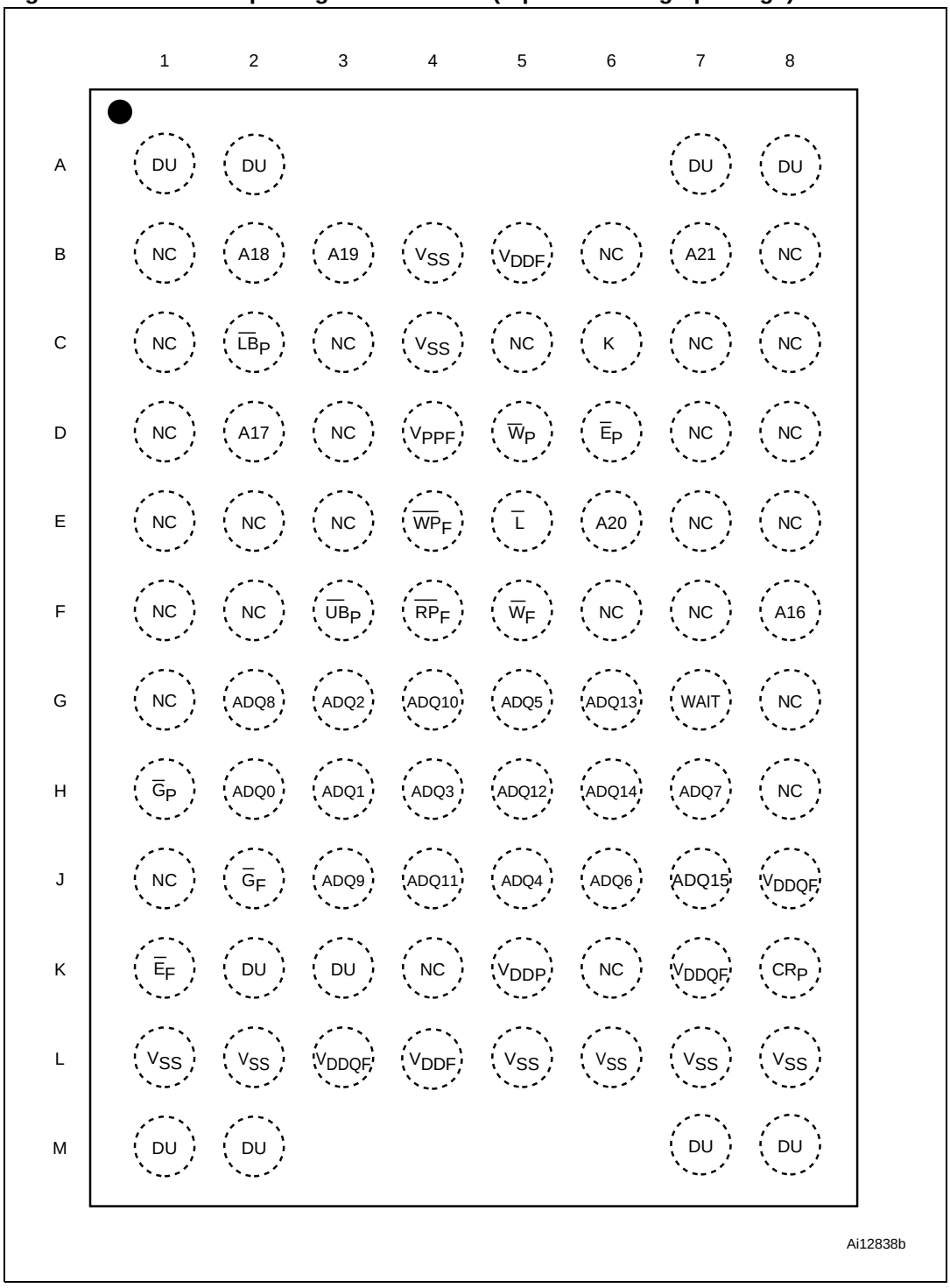


Figure 4. TFBGA88 package connections (top view through package)



2 Signal descriptions

See *Figure 1: Logic diagram - TFBGA56 package* and *Table 2: Signal names* for a brief overview of the signals connected to this device.

There are some signals that are not common to both device packages and are, therefore, explained separately.

2.1 Common signals

The following are the signals that are the same for the TFBGA56 package and the TFBGA88 package.

2.1.1 Data inputs/outputs (ADQ0-ADQ15)

The data I/O output the data stored at the selected address during a bus read operation, or they input a command or the data to be programmed during a bus write operation.

2.1.2 Latch Enable ($\overline{L}$)

The Latch Enable input is common to the flash memory and PSRAM components.

For more details on the Latch Enable signal, please refer to the datasheets of the respective memory components: M69KM024A or M69KM048A for the PSRAM and M58WR0xxKUL for the flash memory.

2.1.3 Clock (K)

The Clock input is common to the flash memory and PSRAM components.

For more details on the Clock signal, please refer to the datasheets of the respective memory components: M69KM024A or M69KM048A for the PSRAM and M58WR0xxKUL for the flash memory.

2.1.4 Wait (WAIT)

The Wait output is common to the flash memory and PSRAM components.

For details on the Wait signal, please refer to the datasheets of the respective memory components:M69KM024A or M69KM048A for the PSRAM and M58WR0xxKUL for the flash memory.

2.1.5 Flash memory Chip Enable ($\overline{E}_F$)

The flash memory Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at $V_{IL}$and Reset is at V_{IH} the device is in active mode. When flash memory Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

It is not allowed to set both $\overline{E}_F$ and $\overline{E}_P$ to V_{IL} at the same time.

2.1.6 Flash memory Write Protect ($\overline{WP}_F$)

Write Protect is an input that provides additional hardware protection for each block. When Write Protect is at V_{IL}, the lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When Write Protect is at V_{IH}, the lock-down is disabled and the locked-down blocks can be locked or unlocked (refer to the M58WR0xxKUL datasheet).

2.1.7 Flash memory Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset supply current I_{DD2}. Refer to the M58WR0xxKUL datasheet for the value of $I_{DD2.}$ After Reset all blocks are in the locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. When the device exits reset mode it enters asynchronous read mode. However, a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3 V logic without any additional circuitry, and can be tie to V_{RPH} (refer to the M58WR0xxKUL datasheet).

2.1.8 PSRAM Chip Enable ($\overline{E}_P$)

Chip Enable, $\overline{E}_P$, activates the PSRAM device when driven Low (asserted). When de-asserted (V_{IH}), the device is disabled and goes automatically into low-power standby mode or deep power-down mode, according to the RCR settings.

It is not allowed to set both $\overline{E}_F$ and $\overline{E}_P$ to V_{IL} at the same time.

2.1.9 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte Enable, $\overline{UB}_P$, gates the data on the upper byte of the address inputs/data inputs/outputs (ADQ8-ADQ15) to or from the upper part of the selected address during a write or read operation.

2.1.10 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$, gates the data on the lower byte of the address inputs/data input/outputs (ADQ0-ADQ7) to or from the lower part of the selected address during a write or read operation.

If both $\overline{LB}_P$ and $\overline{UB}_P$ are disabled (High), the device prevents the data bus from receiving or transmitting data. Although the device seems to be deselected, it remains in an active mode as long as $\overline{E}_P$ remains Low.

2.1.11 PSRAM Configuration Register Enable (CR_P)

When this signal is driven High, V_{IH}, bus read or write operations access either the value of the Refresh Configuration Register (RCR) or the Bus Configuration Register (BCR), according to the value of A19.

2.1.12 V_{PPF} flash memory program supply voltage

V_{PPF} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0 V to V_{DDQ}), V_{PPF} acts as a control input. In this case a voltage lower than V_{PPLK} gives absolute protection against program or erase, while V_{PPF} in the V_{PP1} range enables these functions (see the M58WR0xxKUL datasheet for the relevant values).

V_{PPF} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the program/erase algorithm is completed.

2.1.13 V_{SS} ground

V_{SS} ground is the common flash memory and PSRAM ground. It is the reference for the core supplies and must be connected to the system ground.

2.1.14 V_{SSQ} ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQF}. V_{SSQ} must be connected to V_{SS}

Note: Each device in a system should have V_{DDF}, V_{DDQF} and V_{PP} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 8: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PP} program and erase currents.

2.2 TFBGA56 signals

2.2.1 TFBGA56 address inputs (ADQ0-ADQ15 and A16-A21)

The following address inputs are common to the flash memory and PSRAM components:

- ADQ0-ADQ15, and
- A16-A19 when stacked with a 16-Mbit PSRAM, or
- A16-A20 when stacked with a 32-Mbit PSRAM.

In the flash memory, the address inputs select the cells in the array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the Program/Erase Controller.

In the PSRAM, the address following inputs are used in conjunction with ADQ0 to ADQ15 to select the cells in the memory array that are accessed during read and write operations:

- A16-A19 when stacked with a 16-Mbit PSRAM, or
- A16-A20 when stacked with a 32-Mbit PSRAM.

A21 is an address input for the 64-Mbit flash memory device only.

2.2.2 Deep power-down (DPD)

The deep power-down input puts the device in deep power-down mode. When the device is in standby mode and the Enhanced Configuration Register bit ECR15 is set, asserting the deep power-down input causes the memory to enter deep power-down mode.

When the device is in deep power-down mode, the memory cannot be modified and the data is protected.

The polarity of the DPD pin is determined by ECR14. The deep power-down input is active Low by default.

2.2.3 Output Enable ($\overline{G}$)

The Output Enable input is common to the flash memory and PSRAM components. For details on the Output Enable signal, please refer to the datasheets of the respective memory components: M69KM024A or M69KM048A for the PSRAM and M58WR0xxKUL for the flash memory.

2.2.4 Write Enable ($\overline{W}$)

The Write Enable Input is common to the flash memory and PSRAM components. For details on the Write Enable signal, please refer to the datasheets of the respective memory components: M69KM024A or M69KM048A for the PSRAM and M58WR0xxKUL for the flash memory.

2.2.5 V_{DD} supply voltage

V_{DD} is common to both flash memory and PSRAM components and provides the power supply to the internal core. It is the main power supply for all memory operations (read, program, and erase).

2.2.6 V_{DDQ} supply voltage

V_{DDQ} is common to both flash memory and PSRAM components and provides the power supply to the I/O pins. It enables all outputs to be powered independently of V_{DD}. V_{DDQ} can be tied to V_{DD} or use a separate supply.

2.3 TFBGA88 signals

2.3.1 TFBGA88 address inputs

The following address inputs are common to the flash memory and PSRAM components:

- ADQ0-ADQ15, and
- A16-A19 when stacked with a 16-Mbit PSRAM, or
- A16-A20 when stacked with a 32-Mbit PSRAM.

A21 is an address input for the 64-Mbit flash memory component only.

In the PSRAM, the address following inputs are used in conjunction with ADQ0 to ADQ15 to select the cells in the memory array that are accessed during read and write operations:

- A16-A19 when stacked with a 16-Mbit PSRAM, or
- A16-A20 when stacked with a 32-Mbit PSRAM.

In the flash memory, the address inputs select the cells in the array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the Program/Erase Controller.

2.3.2 Flash memory Output Enable ($\overline{G}_F$)

The Output Enable input controls data outputs during the bus read operation of the flash memory.

2.3.3 Flash memory Write Enable ($\overline{W}_F$)

The Write Enable input controls the bus write operation of the flash memory's command interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable, whichever occurs first.

2.3.4 V_{DDF} flash memory supply voltage

V_{DDF} provides the power supply to the internal core of the flash memory. It is the main power supply for all flash memory operations (read, program, and erase).

2.3.5 V_{CCP} PSRAM supply voltage

The V_{CCP} supply voltage is the core supply voltage.

2.3.6 PSRAM Output Enable ($\overline{G}_P$)

When held Low, V_{IL}, the Output Enable, $\overline{G}_P$, enables the bus read operations of the memory.

2.3.7 PSRAM Write Enable ($\overline{W}_P$)

Write Enable, $\overline{W}_P$, controls the bus write operation of the memory. When asserted (V_{IL}), the device is in write mode and write operations can be performed either to the configuration registers or to the memory array.

3 Functional description

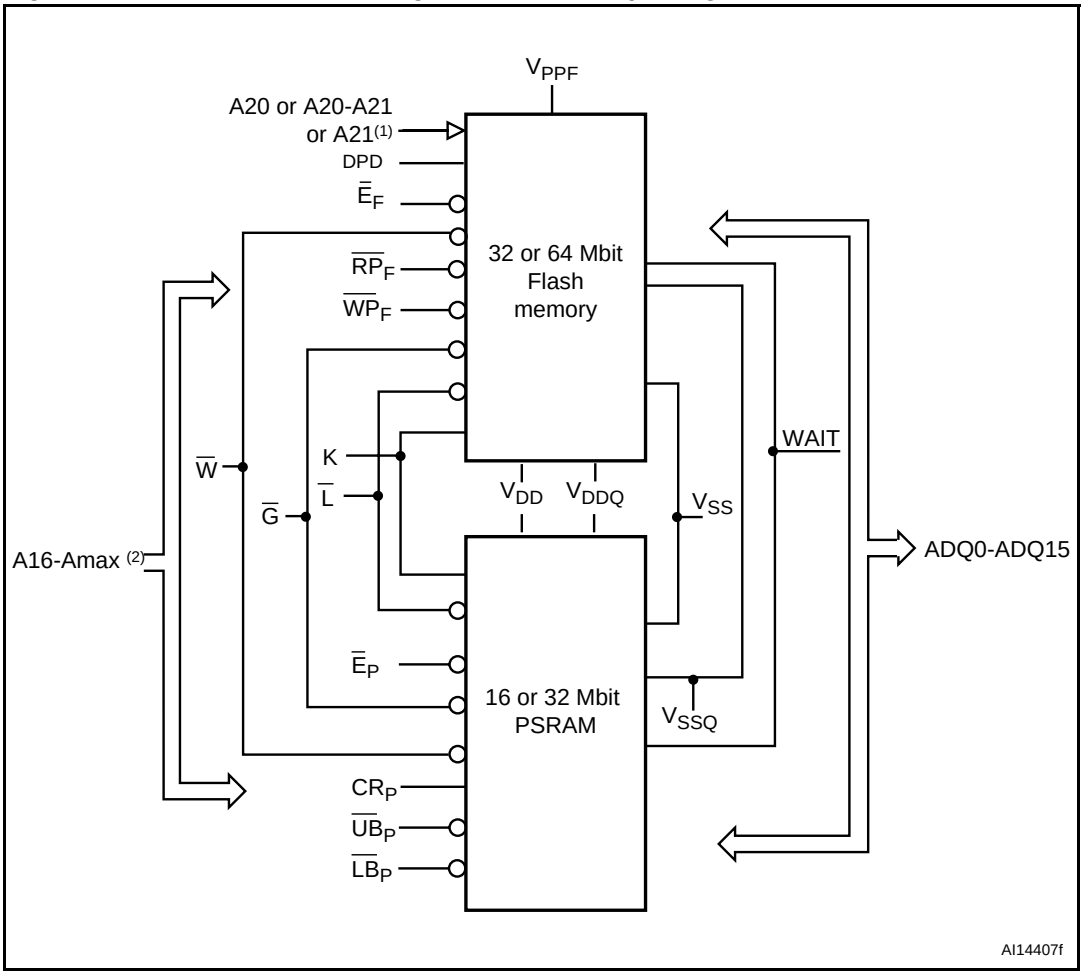
The PSRAM and flash memory components share the same power supplies and the same grounds. They are distinguished by two Chip Enable inputs: $\overline{E}_F$ for the flash memory and $\overline{E}_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time, such as simultaneous read operations on the flash memory and the PSRAM component, which would result in a data bus contention.

Therefore, it is recommended to put the other device in the high impedance state when reading the selected device.

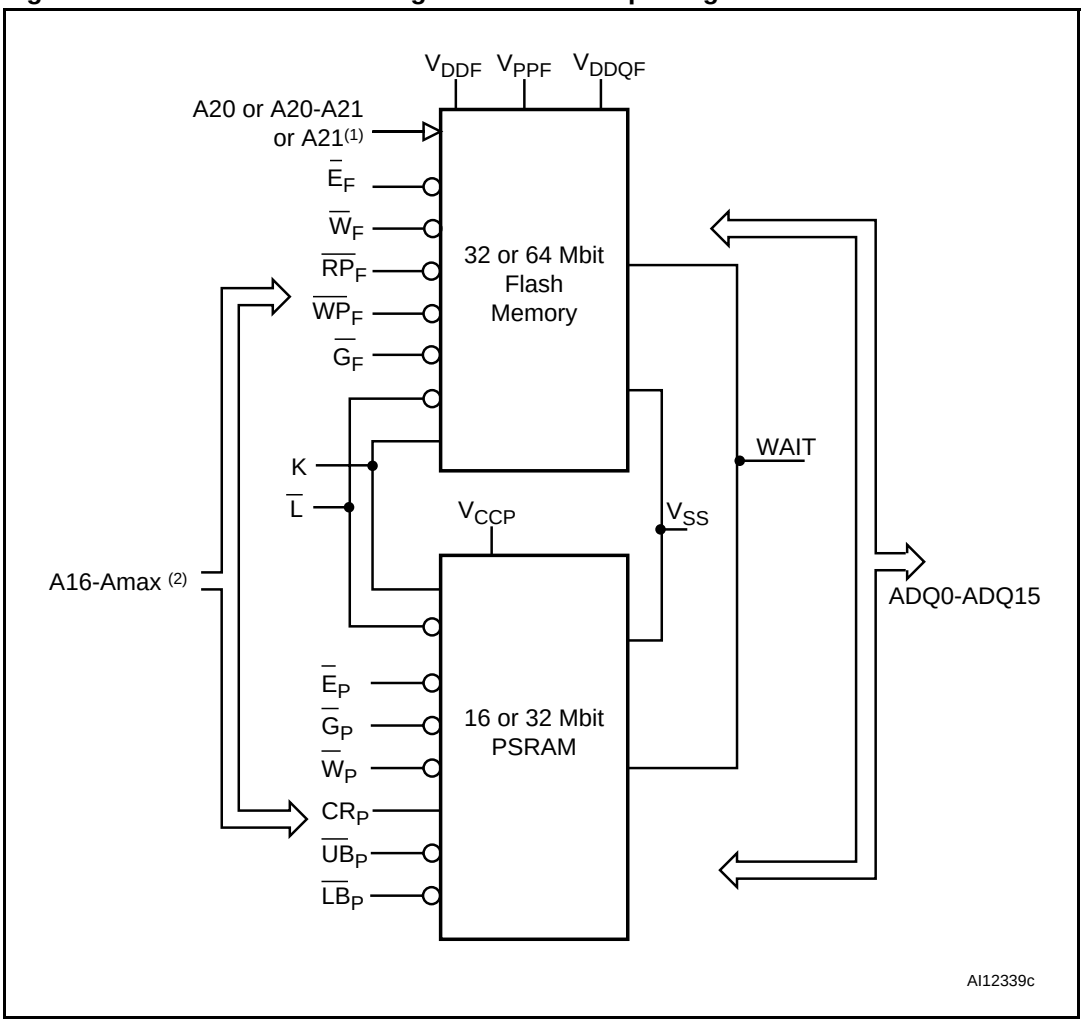
Figure 5 outlines the functional block diagram for the TFBGA56 package, while *Figure 6* outlines the one for TFBGA88 package.

Figure 5. Functional block diagram - TFBGA56 package



1. A20 for the M36W0R5040x4, A20-A21 for the M36W0R6040x4, and A21 for the M36W0R6050x4.
2. Amax is equal to A19 when stacked with a 16-Mbit PSRAM, or A20 when stacked with a 32-Mbit PSRAM.

Figure 6. Functional block diagram - TFBGA88 package



1. A20 for the M36W0R5040x4, A20-A21 for the M36W0R6040x4, and A21 for the M36W0R6050x4.
2. Amax is equal to A19 when stacked with a 16-Mbit PSRAM, or A20 when stacked with a 32-Mbit PSRAM.

Table 3. TFBGA56 package operating modes - standard asynchronous operation

Operation[1][2]		$\overline{E}_F$	$\overline{RP}_F$	WAIT[3]	$\overline{G}$	$\overline{W}$	$\overline{L}$	$\overline{UB}_P$	$\overline{LB}_P$	CR_P	$\overline{E}_P$	ADQ0-ADQ7	ADQ8-ADQ15
Flash memory	Bus read	V_{IL}	V_{IH}		V_{IL}	V_{IH}	V_{IH}	Any PSRAM mode is allowed.				Data output	
	Bus write	V_{IL}	V_{IH}		V_{IH}	V_{IL}	V_{IH}					Data input	
	Address latch	V_{IL}	V_{IH}		V_{IH}	X	V_{IL}					Data output or Hi-Z[4]	
	Output disable	V_{IL}	V_{IH}		V_{IH}	V_{IH}	V_{IH}	Any PSRAM mode is allowed.				Hi-Z	
	Standby	V_{IH}	V_{IH}	Hi-Z	X	X	X					Hi-Z	
	Reset	X	V_{IL}	Hi-Z	X	X	X					Hi-Z	
PSRAM	Word read	The flash memory must be disabled.			V_{IL}	V_{IH}	¯_/¯	V_{IL}	V_{IL}	V_{IL}	V_{IL}	Address in/ data out valid	
	Word write				V_{IH}	V_{IL}		V_{IL}	V_{IL}	V_{IL}		Address in/ data in valid	
	Output disable/no operation	Any flash memory mode is allowed.			V_{IH}	V_{IH}	X	X	X	V_{IL}		High-Z	
	Deep power-down[5]				X	X	X	X	X	X	V_{IH}	High-Z	
	Standby				X	X	X	X	X	X	V_{IH}	High-Z	

1. The Clock signal, K, must remain Low when the PSRAM is operating in asynchronous mode.
2. X = ‘don’t care’
3. In the flash memory the WAIT signal polarity is configured using the Set Configuration Register command.
4. See the M58WR0xxKUL datasheet.
5. The device enters deep power-down mode by driving the Chip Enable signal, $\overline{E}$, from Low to High, with bit 4 of the RCR set to “0”. The device remains in deep power-down mode until $\overline{E}$ goes Low again and is held Low for $t_{ELEH(DP)}$.

Table 4. TFBGA88 package operating modes - standard asynchronous operation(1)

	Operation(2)	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{RP}_F$	WAIT (3)	$\overline{L}_P$	$\overline{E}_P$	$\overline{W}_P$	$\overline{G}_P$	$\overline{UB}_P$	$\overline{LB}_P$	CR_P	A19	A16-A18	ADQ0-ADQ7	ADQ8-ADQ15
Flash memory	Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}		V_{IH}	The PSRAM must be disabled								Data output	
	Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}		V_{IH}									Data input	
	Address latch	V_{IL}	V_{IH}	X	V_{IH}		V_{IL}									Address input	
	Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}		V_{IH}	Any PSRAM mode is allowed								Hi-Z	
	Standby	V_{IH}	X	X	V_{IH}	Hi-Z	X									Hi-Z	
	Reset	X	X	X	V_{IL}	Hi-Z	X									Hi-Z	
PSRAM	Word read						¯_/¯	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	Address in valid		Address in/data out valid	
	Word write								V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Address in valid		Address in/ data in valid	
	Output disable/no operation						X		V_{IH}	X	X	X	V_{IL}	X		High-Z	
	Deep power-down(4)							V_{IH}	X	X	X	X	X	X		High-Z	
	Standby							V_{IH}	X	X	X	X	X	V_{IL}	X	High-Z	

1. X = ‘don’t care’
2. The Clock signal, K, must remain Low in asynchronous operating mode.
3. In the flash memory the WAIT signal polarity is configured using the Set Configuration Register command.
4. The device enters deep power-down mode by driving the Chip Enable signal, $\overline{E}$, from Low to High, with bit 4 of the RCR set to ‘0’. The device remains in deep power-down mode until $\overline{E}$ goes Low again and is held Low for $t_{ELEH(DP)}$.

4 Maximum ratings

Stressing the device above the ratings listed in *Table 5: Absolute maximum ratings* may cause permanent damage to the device. These are only stress ratings and operating the device at these or any other conditions above those indicated in the operating sections of this specification is not suggested. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient operating temperature	–30	85	°C
T_{BIAS}	Temperature under bias	–30	85	°C
T_{STG}	Storage temperature	–55	125	°C
V_{IO}	Input or output voltage	–0.2	2.45	V
V_{DD}, V_{DDQ}	Flash and PSRAM core and input/output supply voltages	–0.2	2.45	V
V_{PPF}	Flash program voltage	–0.2	10	V
I_O	Output short circuit current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 6: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 6. Operating and AC measurement conditions

Parameter	Flash memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DD} supply voltage	1.7	1.95	–	–	V
V_{DDQ} supply voltage	1.7	1.95	–	–	V
V_{PPF} supply voltage (factory environment)	8.5	9.5	–	–	V
V_{PPF} supply voltage (application environment)	–0.4	V_{DDQ} +0.4	–	–	V
Ambient operating temperature	–30	85	–30	85	°C
Load capacitance (C_L)	30		30		pF
Output circuit resistors (R_1, R_2)	16.7		16.7		kΩ
Input rise and fall times		5		2	ns
Input pulse voltages	0 to V_{DDQ}		0 to $V_{DD}/2$		V
Input and output timing ref. voltages	$V_{DDQ}/2$		$V_{DD}/2$		V

Figure 7. AC measurement I/O waveform

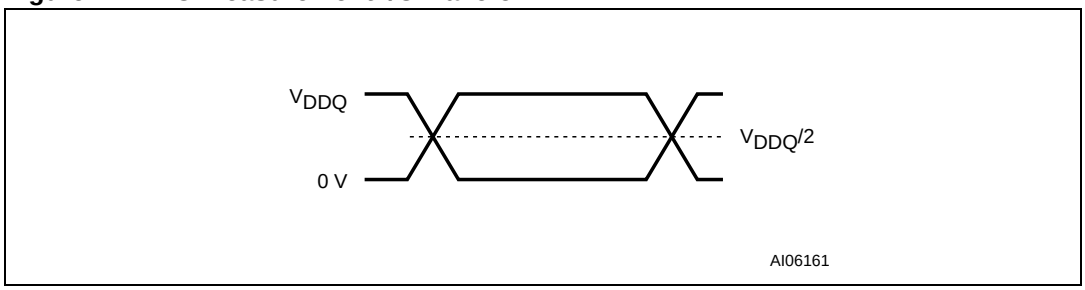


Figure 8. AC measurement load circuit

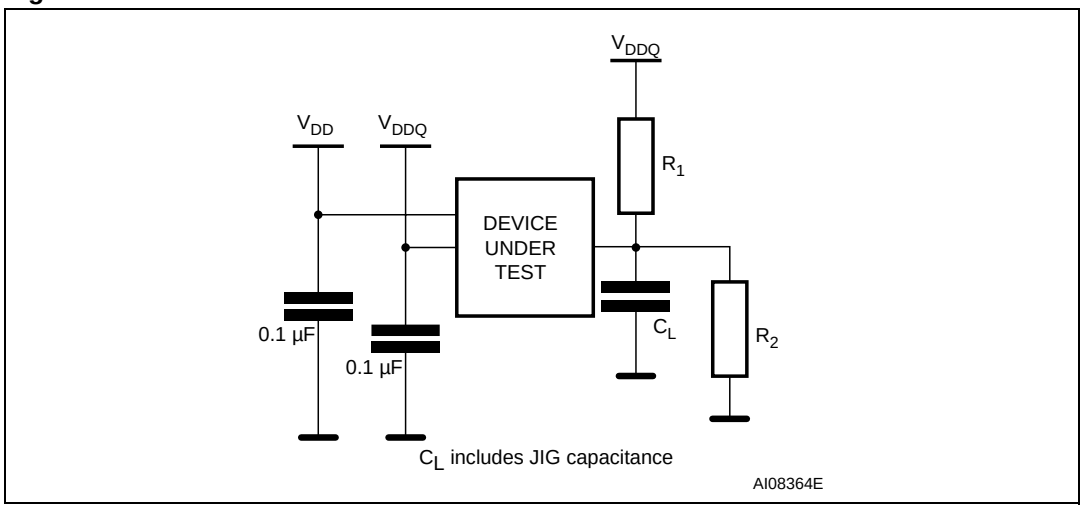


Table 7. Device capacitance

Symbol	Parameter	Test condition	Min	Max(1)	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		14	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		18	pF

1. Sampled only, not 100% tested.

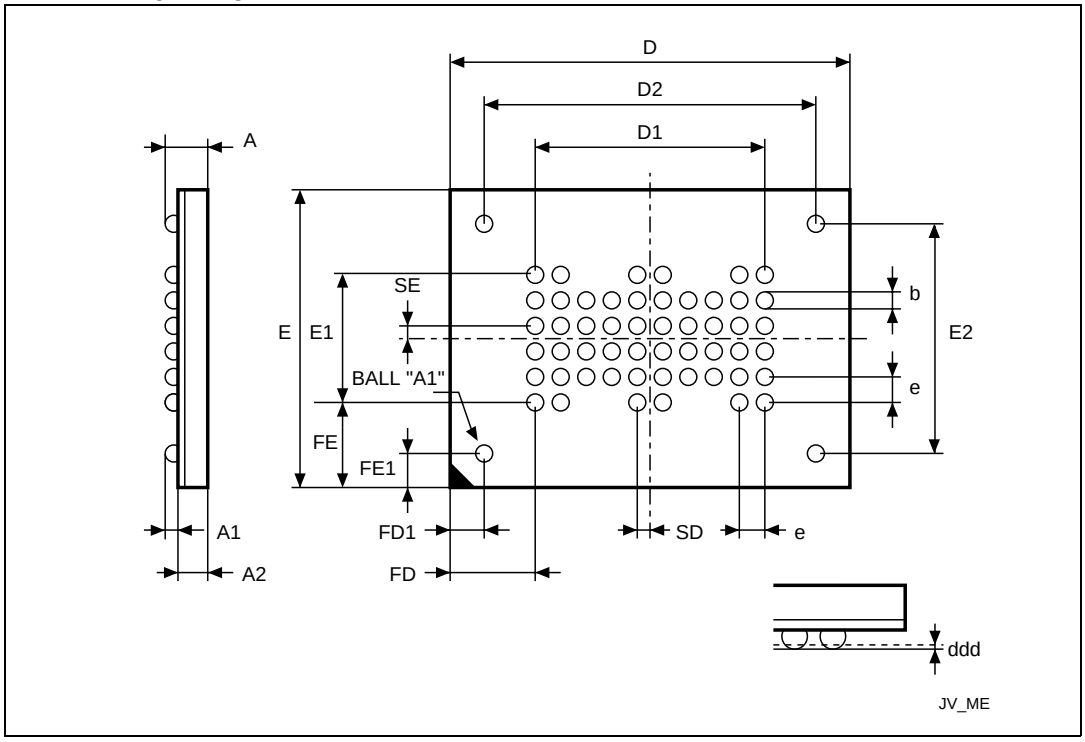
Please refer to the M58WR0xxKUL and the M69KM024A or M69KM048A datasheets for further DC and AC characteristics values and illustrations.

6 Package mechanical

To meet environmental requirements Numonyx offers these devices in ECOPACK® packages, which have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK specifications are available at: *www.numonyx.com*.

Figure 9. TFBGA56 8 × 6 x 1.2 mm, 10 x 6 ball array - 0.5 mm pitch, bottom view package outline

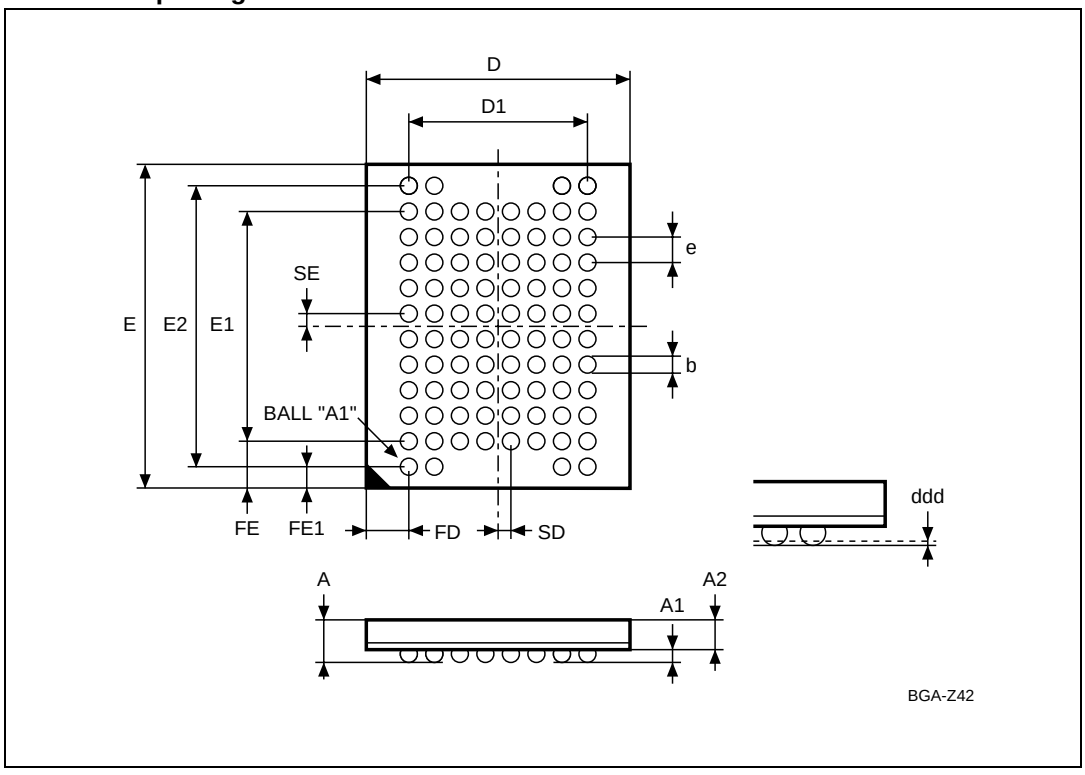


1. Drawing is not to scale.

Table 8. TFBGA56 8 × 6 x 1.2 mm, 10 x 6 ball array - 0.5 mm pitch, package data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.15			0.0006	
A2	0.79			0.031		
b	0.30	0.25	0.35	0.012	0.010	0.014
D	6.00	5.90	6.10	0.236	0.232	0.240
D1	4.50			0.177		
E	4.00	3.90	4.10	0.157	0.154	0.161
E1	2.50			0.098		
e	0.50			0.020		
FD	0.75			0.030		
FE	0.75			0.030		
SD	0.25			0.010		

Figure 10. TFBGA88 8 × 10 mm, 8 × 10 ball array - 0.8 mm pitch, bottom view package outline



1. Drawing is not to scale.

Table 9. Stacked TFBGA88 8 × 10 mm - 8 × 10 active ball array, 0.8 mm pitch, package data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.850			0.0335		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600			0.2205		
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200			0.2835		
E2	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	1.200			0.0472		
FE	1.400			0.0551		
FE1	0.600			0.0236		
SD	0.400			0.0157		
SE	0.400			0.0157		

7 Part numbering

Table 10. Ordering information scheme

Example: M36 W 0 R 5 0 4 0 U 4 ZS F

Device type
M36 = multichip package (flash + RAM)

Flash 1 architecture
W = multiple bank, burst mode

Flash 2 architecture
0 = no die

Operating voltage
R = V_{DD} = V_{DDQ} = 1.7 V to 1.95 V

Flash 1 density
5 = 32 Mbit
6 = 64 Mbit

Flash 2 density
0 = no die

RAM 1 density
4 = 16 Mbit
5 = 32 Mbit

RAM 2 density
0 = no die

Parameter block location
U = top block flash
L = bottom block flash

Product version
4 = 65 nm flash technology and multilevel design, 70 ns speed class; RAM, 70 ns speed mux I/O

Package
ZS = stacked TFBGA56 8 x 6 mm - 10 x 6 active ball array, 0.50 mm pitch
ZAM = stacked TFBGA88 8 × 10 mm - 8 × 10 active ball array, 0.8 mm pitch

Packing option
E = ECOPACK® package, standard packing
F = ECOPACK® package, tape and reel packing

Note: Devices are shipped from the factory with the memory content bits, in valid blocks, erased to "1". For further information on any aspect of this device, please contact your nearest Numonyx sales office.

8 Revision history

Table 11. Document revision history

Date	Revision	Changes
24-Oct-2007	1	Initial release.
30-Oct-2007	2	Modified the device codes on page 1.
26-Mar-2008	3	Added the M36W0R5040U4 and M36W0R5040L4 root part numbers and all their associated data throughout this document. Applied Numonxy branding.
29-Apr-2008	4	Replaced the M69KM048AB with M69KM048A everywhere in the document. Corrected the product version in *Table 10: Ordering information scheme*.
20-May-2008	5	Changed the maximum flash frequency from 86 MHz to 66 MHz on page 1.
17-Jul-2008	6	Changed the ambient operating temperature from -25 to -30 in *Table 5: Absolute maximum ratings* and *Table 6: Operating and AC measurement conditions*.

Please Read Carefully: