

NSB1706DMW5T1

Dual Bias Resistor Transistor

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSB1706DMW5T1, two BRT devices are housed in the SC-88A package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch/3000 Unit Tape and Reel

MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB0}	50	Vdc
Collector-Emitter Voltage	V_{CE0}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

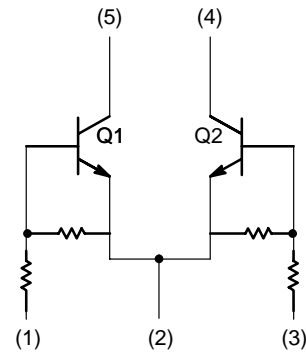
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	187 (Note 1.) 256 (Note 2.) 1.5 (Note 1.) 2.0 (Note 2.)	mW mW/ $^\circ\text{C}$
Thermal Resistance - Junction-to-Ambient	$R_{\theta JA}$	670 (Note 1.) 490 (Note 2.)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	250 (Note 1.) 385 (Note 2.) 2.0 (Note 1.) 3.0 (Note 2.)	mW mW/ $^\circ\text{C}$
Thermal Resistance - Junction-to-Ambient	$R_{\theta JA}$	493 (Note 1.) 325 (Note 2.)	$^\circ\text{C}/\text{W}$
Thermal Resistance - Junction-to-Lead	$R_{\theta JL}$	188 (Note 1.) 208 (Note 2.)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	- 55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad



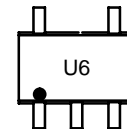
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SC-88A
CASE 419A

MARKING DIAGRAM



U6 = Device Marking

NSB1706DMW5T1

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	-	-	100	nA _{dc}
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	-	-	500	nA _{dc}
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	-	-	0.18	mA _{dc}
Collector-Base Breakdown Voltage ($I_C = 10\ \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	-	-	V _{dc}
Collector-Emitter Breakdown Voltage (Note 2) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	-	-	V _{dc}

ON CHARACTERISTICS (Note 2)

DC Current Gain ($V_{CE} = 10\text{ V}$, $I_C = 5.0\text{ mA}$)	MUN5233DW1T1	h_{FE}	80	200	-	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 1\text{ mA}$)	MUN5233DW1T1	$V_{CE(sat)}$	-	-	0.25	V _{dc}
Output Voltage (on) ($V_{CC} = 5.0\text{ V}$, $V_B = 2.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	MUN5233DW1T1	V_{OL}	-	-	0.2	V _{dc}
Output Voltage (off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.25\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	MUN5233DW1T1	V_{OH}	4.9	-	-	V _{dc}
Input Resistor	MUN5233DW1T1	R1	3.3	4.7	6.1	k Ω
Resistor Ratio MUN5233DW1T1		R1/R2	0.055	0.1	0.185	

1. New resistor combinations. Updated curves to follow in subsequent data sheets.
2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

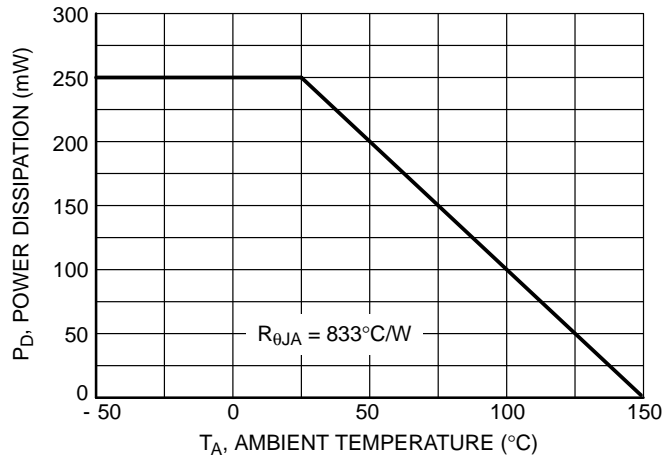
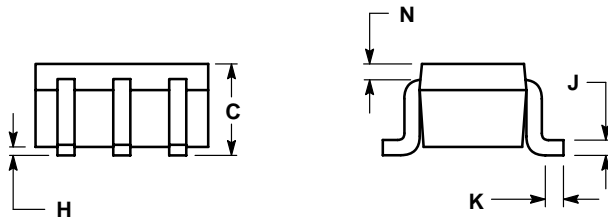
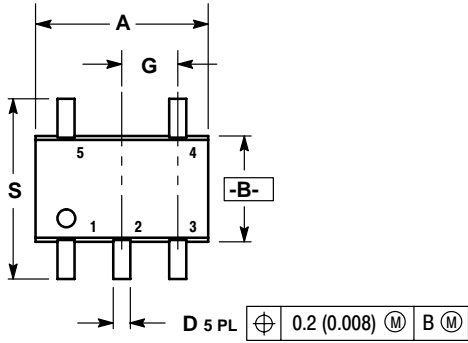


Figure 1. Derating Curve

NSB1706DMW5T1

PACKAGE DIMENSIONS

SC-88A
CASE 419A-02
ISSUE F




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

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